

## Six Output Differential Buffer for PCIe Gen3

9DB633

### Recommended Application:

6 output PCIe Gen3 zero-delay/fanout buffer

### General Description:

The 9DB633 zero-delay buffer supports PCIe Gen3 requirements, while being backwards compatible to PCIe Gen2 and Gen1. The 9DB633 is driven by a differential SRC output pair from an IDT 932S421 or 932SQ420 or equivalent main clock generator. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking. An SMBus interface allows control of the PLL bandwidth and bypass options, while 2 clock request (OE#) pins make the 9DB633 suitable for Express Card applications.

### Key Specifications:

- Cycle-to-cycle jitter < 50 ps
- Output-to-output skew < 50 ps
- PCIe Gen3 phase jitter < 1.0ps RMS

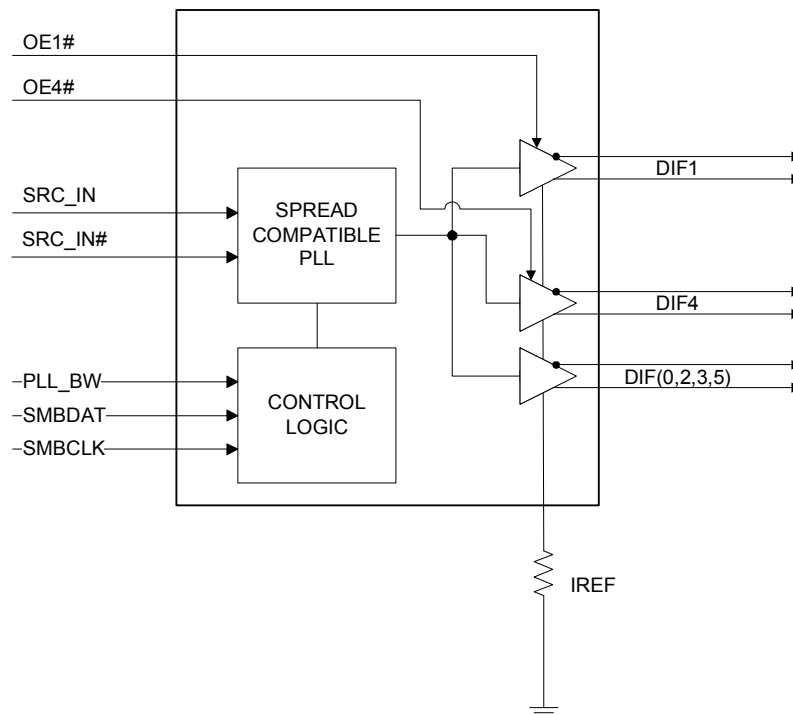
### Features/Benefits:

- OE# pins/Suitable for Express Card applications
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled

### Output Features:

- 6 - 0.7V current mode differential HCSL output pairs

### Block Diagram



Pin Configuration

PLL_BW	1	<b>9DB633</b>	28	VDDA
SRC_IN	2		27	GNDA
SRC_IN#	3		26	IREF
vOE1#	4		25	vOE4#
DIF_0	5		24	DIF_5
DIF_0#	6		23	DIF_5#
VDD	7		22	VDD
GND	8		21	GND
DIF_1	9		20	DIF_4
DIF_1#	10		19	DIF_4#
DIF_2	11		18	DIF_3
DIF_2#	12		17	DIF_3#
VDD	13		16	VDD
SMBDAT	14		15	SMBCLK

**Note:** Pins preceded by 'v' have internal 120K ohm pull down resistors

Power Distribution Table

Pin Number		Description
VDD	GND	
7, 13, 16, 22	8,21	Differential Outputs
13	8	SMBus
N/A	27	IREF
28	27	Analog VDD & GND for PLL core

## Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	PLL_BW	IN	3.3V input for selecting PLL Band Width 0 = low, 1= high
2	SRC_IN	IN	0.7 V Differential SRC TRUE input
3	SRC_IN#	IN	0.7 V Differential SRC COMPLEMENTARY input
4	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
5	DIF_0	OUT	0.7V differential true clock output
6	DIF_0#	OUT	0.7V differential Complementary clock output
7	VDD	PWR	Power supply, nominal 3.3V
8	GND	IN	Ground pin.
9	DIF_1	OUT	0.7V differential true clock output
10	DIF_1#	OUT	0.7V differential Complementary clock output
11	DIF_2	OUT	0.7V differential true clock output
12	DIF_2#	OUT	0.7V differential Complementary clock output
13	VDD	PWR	Power supply, nominal 3.3V
14	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
15	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
16	VDD	PWR	Power supply, nominal 3.3V
17	DIF_3#	OUT	0.7V differential Complementary clock output
18	DIF_3	OUT	0.7V differential true clock output
19	DIF_4#	OUT	0.7V differential Complementary clock output
20	DIF_4	OUT	0.7V differential true clock output
21	GND	PWR	Ground pin.
22	VDD	PWR	Power supply, nominal 3.3V
23	DIF_5#	OUT	0.7V differential Complementary clock output
24	DIF_5	OUT	0.7V differential true clock output
25	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
26	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

**Note:**

Pins preceded by ' v ' have internal 120K ohm pull down resistors

## Electrical Characteristics - Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDDA				4.6	V	1,2
3.3V Logic Supply Voltage	VDD				4.6	V	1,2
Input Low Voltage	V <sub>IL</sub>		GND-0.5			V	1
Input High Voltage	V <sub>IH</sub>	Except for SMBus interface			V <sub>DD</sub> +0.5V	V	1
Input High Voltage	V <sub>IHSMB</sub>	SMBus clock and data pins			5.5V	V	1
Storage Temperature	T <sub>s</sub>		-65		150	°C	1
Junction Temperature	T <sub>j</sub>				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Operation under these conditions is neither implied nor guaranteed.

## Electrical Characteristics - Input/Supply/Common Parameters

T<sub>A</sub> = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T <sub>COM</sub>	Commercial range	0		70	°C	1
	T <sub>IND</sub>	Industrial range	-40		85	°C	1
Input High Voltage	V <sub>IH</sub>	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>IL</sub>	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I <sub>IN</sub>	Single-ended inputs, V <sub>IN</sub> = GND, V <sub>IN</sub> = VDD	-5		5	uA	1
	I <sub>INP</sub>	Single-ended inputs V <sub>IN</sub> = 0 V; Inputs with internal pull-up resistors V <sub>IN</sub> = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F <sub>ibyp</sub>	V <sub>DD</sub> = 3.3 V, Bypass mode	10		110	MHz	2
	F <sub>ipll</sub>	V <sub>DD</sub> = 3.3 V, 100MHz PLL mode	33	100.00	110	MHz	2
Pin Inductance	L <sub>pin</sub>				7	nH	1
Capacitance	C <sub>IN</sub>	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C <sub>INDIF_IN</sub>	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C <sub>OUT</sub>	Output pin capacitance			6	pF	1
Clk Stabilization	T <sub>STAB</sub>	From V <sub>DD</sub> Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1.8	ms	1,2
Input SS Modulation Frequency	f <sub>MODIN</sub>	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	t <sub>LATOE#</sub>	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	cycles	1,3
Tdrive_PD#	t <sub>DRVPD</sub>	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t <sub>F</sub>	Fall time of control inputs			5	ns	1,2
Trise	t <sub>R</sub>	Rise time of control inputs			5	ns	1,2
SMBus Input Low Voltage	V <sub>ILSMB</sub>				0.8	V	1
SMBus Input High Voltage	V <sub>IHSMB</sub>		2.1		V <sub>DDSMB</sub>	V	1
SMBus Output Low Voltage	V <sub>OLSMB</sub>	@ I <sub>PULLUP</sub>			0.4	V	1
SMBus Sink Current	I <sub>PULLUP</sub>	@ V <sub>OL</sub>	4			mA	1
Nominal Bus Voltage	V <sub>DDSMB</sub>	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t <sub>RSMB</sub>	(Max V <sub>IL</sub> - 0.15) to (Min V <sub>IH</sub> + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t <sub>FSMB</sub>	(Min V <sub>IH</sub> + 0.15) to (Max V <sub>IL</sub> - 0.15)			300	ns	1
SMBus Operating Frequency	f <sub>MAXSMB</sub>	Maximum SMBus operating frequency			100	kHz	1,5

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>Control input must be monotonic from 20% to 80% of input swing.

<sup>3</sup>Time from deassertion until outputs are >200 mV

<sup>4</sup>DIF\_IN input

<sup>5</sup>The differential input clock must be running for the SMBus to be active

### Electrical Characteristics - DIF\_IN Clock Input Parameters

$T_{AMB}=T_{COM}$  or  $T_{IND}$  unless otherwise indicated, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	$V_{CROSS}$	Cross Over Voltage	150	375	900	mV	1
Input Swing - DIF_IN	$V_{SWING}$	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	1		8	V/ns	1,2
Input Leakage Current	$I_{IN}$	$V_{IN} = V_{DD}, V_{IN} = GND$	-5		5	uA	
Input Duty Cycle	$d_{in}$	Measurement from differential waveform	45		55	%	1
Input Jitter - Cycle to Cycle	$J_{DIFn}$	Differential Measurement	0		125	ps	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup> Slew rate measured through +/-75mV window centered around differential zero

### Electrical Characteristics - DIF 0.7V Current Mode Differential Outputs

$T_A = T_{COM}$  or  $T_{IND}$ ; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	0.6	2.5	4	V/ns	1, 2, 3
Slew rate matching	$\Delta Trf$	Slew rate matching, Scope averaging on		9.5	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	740	850	mV	1
Voltage Low	VLow		-150	8	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		760	1150	mV	1
Min Voltage	Vmin		-300	-3			1
Vswing	Vswing	Scope averaging off	300	1506		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	378	550	mV	1, 5
Crossing Voltage (var)	$\Delta V_{cross}$	Scope averaging off		54	140	mV	1, 6

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.  $I_{REF} = VDD/(3xR_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32mA$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7V @ Z_O=50\Omega$  (100 $\Omega$  differential impedance).

<sup>2</sup> Measured from differential waveform

<sup>3</sup> Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

<sup>4</sup> Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

<sup>5</sup> Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

<sup>6</sup> The total variation of all Vcross measurements in any particular system. Note that this is a subset of V\_cross\_min/max (V\_cross absolute) allowed. The intent is to limit Vcross induced modulation by setting V\_cross\_delta to be smaller than V\_cross absolute.

### Electrical Characteristics - Current Consumption

$T_A = T_{COM}$  or  $T_{IND}$ ; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	$I_{DD3.3OP}$	All outputs active @100MHz, $C_L = Full$ load;		134	150	mA	1
Powerdown Current	$I_{DD3.3PD}$	All diff pairs driven			N/A	mA	1
	$I_{DD3.3PDZ}$	All differential pairs tri-stated			N/A	mA	1

<sup>1</sup> Guaranteed by design and characterization, not 100% tested in production.

### Electrical Characteristics - Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode	2	2.3	4	MHz	1
		-3dB point in Low BW Mode	0.4	0.5	1	MHz	1
PLL Jitter Peaking	t <sub>JPEAK</sub>	Peak Pass band Gain		1	2	dB	1
Duty Cycle	t <sub>DC</sub>	Measured differentially, PLL Mode	45	48	55	%	1
Duty Cycle Distortion	t <sub>DCD</sub>	Measured differentially, Bypass Mode @100MHz	-2	1	2	%	1,4
Skew, Input to Output	t <sub>pdBYP</sub>	Bypass Mode, V <sub>T</sub> = 50%	2500	3660	4500	ps	1
	t <sub>pdPLL</sub>	Hi BW PLL Mode V <sub>T</sub> = 50%	-250	0	250	ps	1
Skew, Output to Output	t <sub>sk3</sub>	V <sub>T</sub> = 50%		15	50	ps	1
Jitter, Cycle to cycle	t <sub>jcy-cyc</sub>	PLL mode		40	50	ps	1,3
		Additive Jitter in Bypass Mode		10	50	ps	1,3

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>I<sub>REF</sub> = V<sub>DD</sub>/(3xR<sub>R</sub>). For R<sub>R</sub> = 475Ω (1%), I<sub>REF</sub> = 2.32mA. I<sub>OH</sub> = 6 x I<sub>REF</sub> and V<sub>OH</sub> = 0.7V @ Z<sub>O</sub>=50Ω.

<sup>3</sup>Measured from differential waveform

<sup>4</sup>Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

### Electrical Characteristics - PCIe Phase Jitter Parameters

TA = T<sub>COM</sub> or T<sub>IND</sub>; Supply Voltage VDD = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Phase Jitter, PLL Mode	t <sub>jphPCIeG1</sub>	PCIe Gen 1		32	86	ps (p-p)	1,2,3
	t <sub>jphPCIeG2</sub>	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.1	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.3	3.1	ps (rms)	1,2
	t <sub>jphPCIeG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	1	ps (rms)	1,2,4
Additive Phase Jitter, Bypass Mode	t <sub>jphPCIeG1</sub>	PCIe Gen 1		2	5	ps (p-p)	1,2,3
	t <sub>jphPCIeG2</sub>	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.2	0.3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.8	1	ps (rms)	1,2
	t <sub>jphPCIeG3</sub>	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.1	0.2	ps (rms)	1,2,4

<sup>1</sup>Applies to all outputs.

<sup>2</sup>See <http://www.pcisig.com> for complete specs

<sup>3</sup>Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

<sup>4</sup>Subject to final ratification by PCI SIG.

SRC Reference Clock			
Common Recommendations for Differential Routing	Dimension or Value	Unit	Figure
L1 length, route as non-coupled 50ohm trace	0.5 max	inch	1
L2 length, route as non-coupled 50ohm trace	0.2 max	inch	1
L3 length, route as non-coupled 50ohm trace	0.2 max	inch	1
$R_s$	33	ohm	1
$R_t$	49.9	ohm	1

Down Device Differential Routing			
L4 length, route as coupled microstrip 100ohm differential trace	2 min to 16 max	inch	1
L4 length, route as coupled stripline 100ohm differential trace	1.8 min to 14.4 max	inch	1

Differential Routing to PCI Express Connector			
L4 length, route as coupled microstrip 100ohm differential trace	0.25 to 14 max	inch	2
L4 length, route as coupled stripline 100ohm differential trace	0.225 min to 12.6 max	inch	2

Figure 1: Down Device Routing

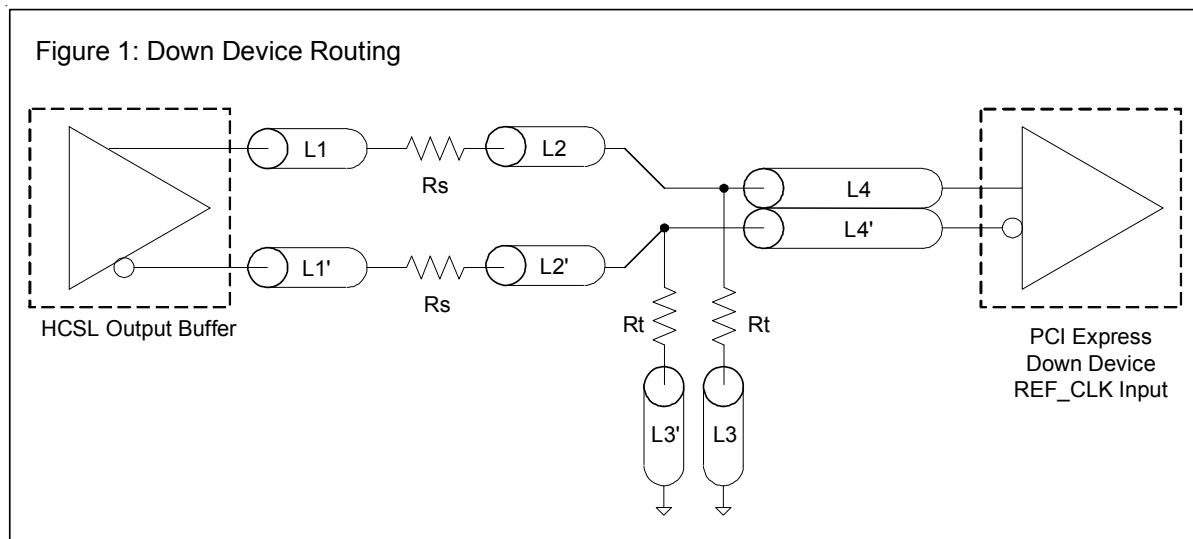
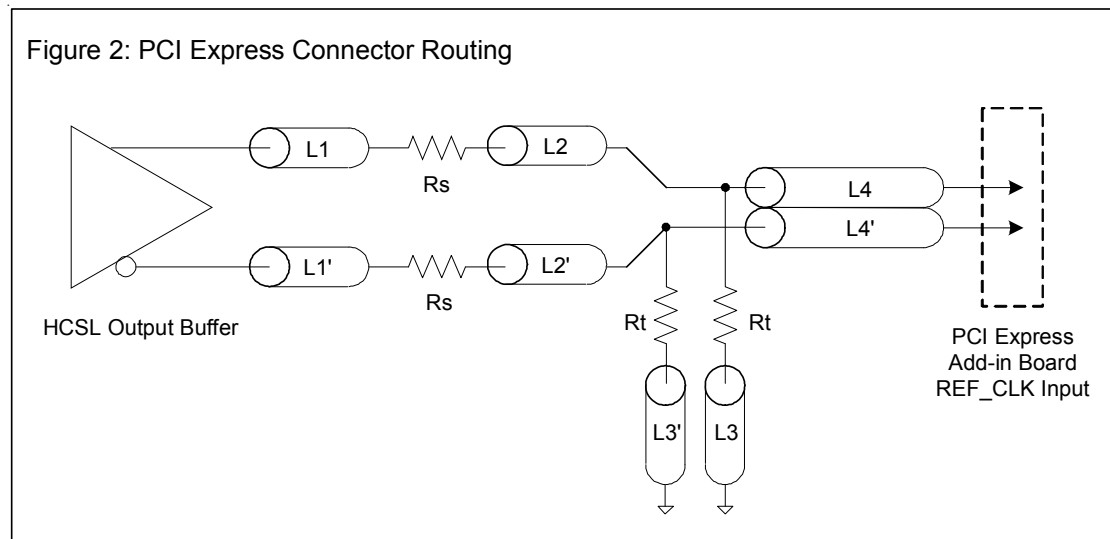


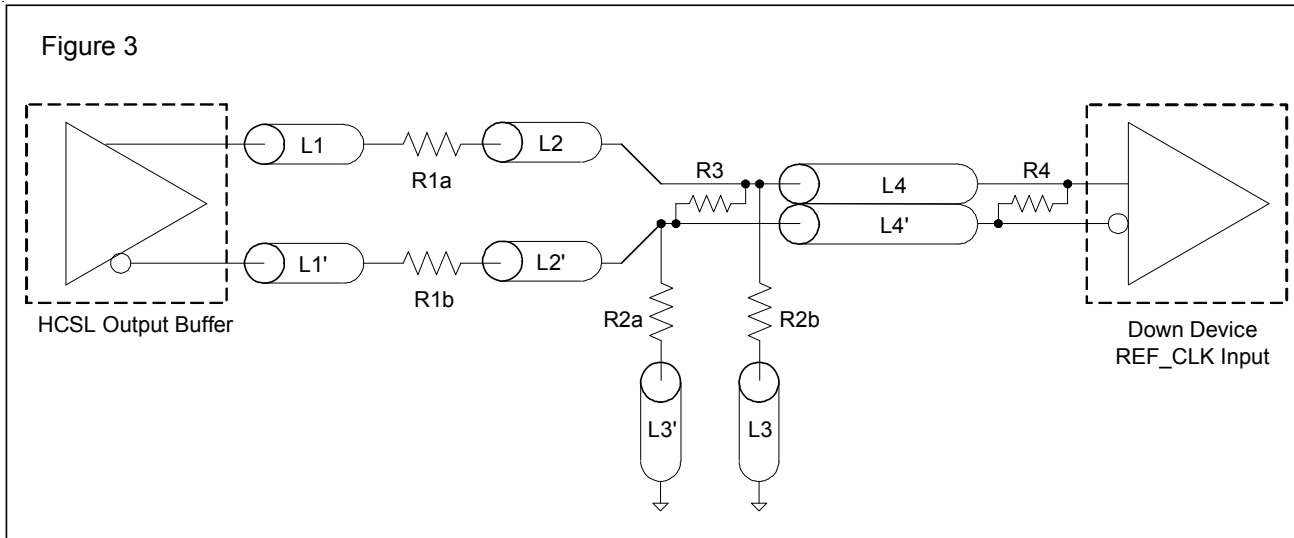
Figure 2: PCI Express Connector Routing



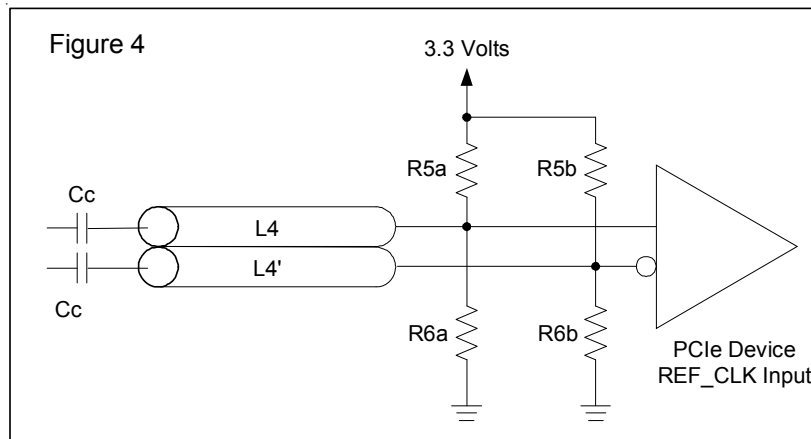
Alternative Termination for LVDS and other Common Differential Signals (figure 3)							
V <sub>diff</sub>	V <sub>p-p</sub>	V <sub>cm</sub>	R1	R2	R3	R4	Note
0.45v	0.22v	1.08	33	150	100	100	
0.58	0.28	0.6	33	78.7	137	100	
0.80	0.40	0.6	33	78.7	none	100	ICS874003i-02 input compatible
0.60	0.3	1.2	33	174	140	100	Standard LVDS

R1a = R1b = R1

R2a = R2b = R2



Cable Connected AC Coupled Application (figure 4)		
Component	Value	Note
R5a, R5b	8.2K 5%	
R6a, R6b	1K 5%	
Cc	0.1 $\mu$ F	
V <sub>cm</sub>	0.350 volts	





## General SMBus serial interface information for the 9DB633

### How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address  $D4_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) sends the data byte count = X
- ICS clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N + X - 1**  
(see Note 2)
- ICS clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

### How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address  $D4_{(H)}$
- ICS clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- ICS clock will **acknowledge**
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address  $D5_{(H)}$
- ICS clock will **acknowledge**
- ICS clock will send the data byte count = X
- ICS clock sends **Byte N + X - 1**
- ICS clock sends **Byte 0 through byte X (if  $X_{(H)}$  was written to byte 8).**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D4_{(H)}$		
WR	WRite	
Beginning Byte = N		ACK
Data Byte Count = X		ACK
Beginning Byte N		ACK
	X Byte	○
		○
		○
		○
Byte N + X - 1		ACK
P	stoP bit	

Index Block Read Operation		
Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address $D4_{(H)}$		
WR	WRite	
Beginning Byte = N		ACK
Data Byte Count = X		ACK
RT	Repeat starT	
Slave Address $D5_{(H)}$		
RD	ReaD	
Beginning Byte = N		ACK
Data Byte Count = X		ACK
ACK		
ACK		Beginning Byte N
	X Byte	○
		○
		○
		○
Byte N + X - 1		
N	Not acknowledge	
P	stoP bit	

SMBusTable: Device Control Register, READ/WRITE ADDRESS (D5/D4)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	SW_EN	Enables SMBus Control of bits (1:0)	RW	PLL controlled by SMBus registers	PLL controlled by device pins	1
Bit 6	-	RESERVED		RW	-	-	X
Bit 5	-	RESERVED		RW	-	-	X
Bit 4	-	RESERVED		RW	-	-	X
Bit 3	-	RESERVED		RW	-	-	X
Bit 2	-	RESERVED		RW	-	-	X
Bit 1	-	PLL BW #adjust	Selects PLL Bandwidth	RW	Low BW	High BW	1
Bit 0	-	PLL Enable	Bypasses PLL for board test	RW	PLL bypassed (fan out mode)	PLL enabled (ZDB mode)	1

SMBusTable: Output Enable Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RESERVED		RW	-	-	X
Bit 6	-	RESERVED		RW	-	-	X
Bit 5	24,23	PCIEX5	Output Control	RW	Disable	Enable	1
Bit 4	-	RESERVED		RW	-	-	X
Bit 3	18,17	PCIEX3	Output Control	RW	Disable	Enable	1
Bit 2	11,12	PCIEX2	Output Control	RW	Disable	Enable	1
Bit 1	-	RESERVED		RW	-	-	X
Bit 0	5,6	PCIEX0	Output Control	RW	Disable	Enable	1

SMBusTable: Function Select Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RESERVED		RW	-	-	X
Bit 6	-	RESERVED		RW	-	-	X
Bit 5	-	RESERVED		RW	-	-	X
Bit 4	-	RESERVED		RW	-	-	X
Bit 3	-	RESERVED		RW	-	-	X
Bit 2	-	RESERVED		RW	-	-	X
Bit 1	-	RESERVED		RW	-	-	X
Bit 0	-	RESERVED		RW	-	-	X

SMBusTable: Vendor &amp; Revision ID Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

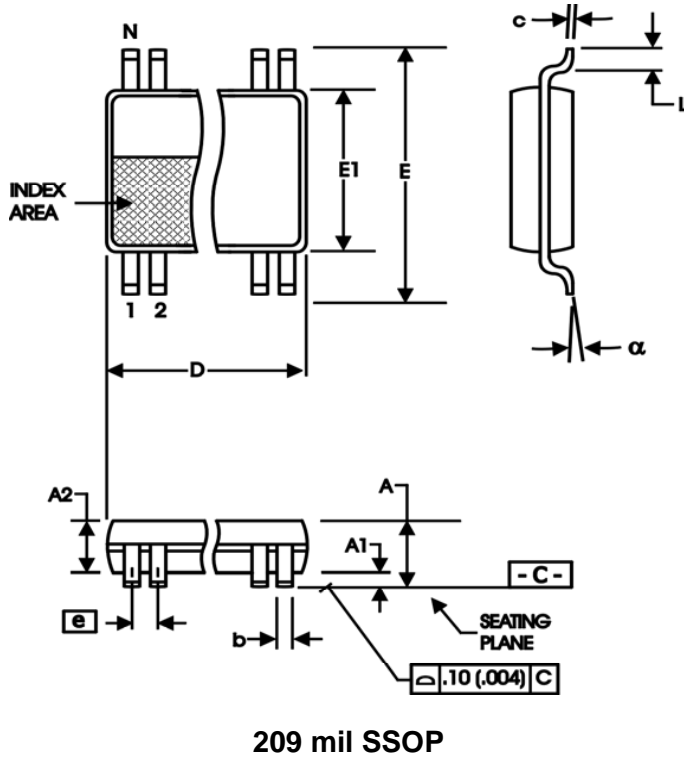
**SMBusTable: DEVICE ID**

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID = 06 Hex		R	-	-	0
Bit 6	-			R	-	-	0
Bit 5	-			R	-	-	0
Bit 4	-			R	-	-	0
Bit 3	-			R	-	-	0
Bit 2	-			R	-	-	1
Bit 1	-			R	-	-	1
Bit 0	-			R	-	-	0

**SMBusTable: Byte Count Register**

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	0

## 28-pin SSOP Package Drawing and Dimensions



209 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

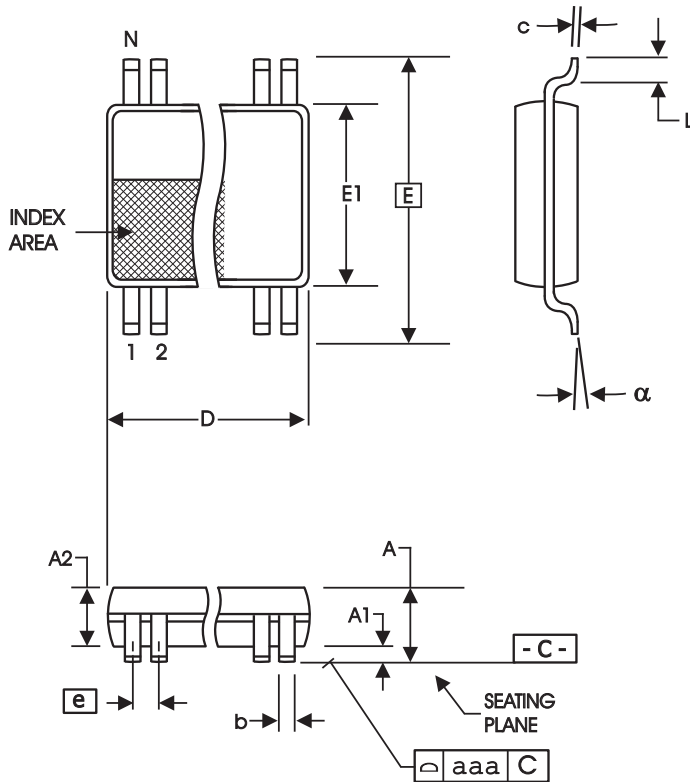
VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

10-0033

## 28-pin TSSOP Package Drawing and Dimensions



4.40 mm. Body, 0.65 mm. Pitch TSSOP  
(173 mil) (25.6 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
$\alpha$	0°	8°	0°	8°
aaa	--	0.10	--	.004

### VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

## Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DB633AFLF	Tubes	28-pin SSOP	0 to +70°C
9DB633AFLFT	Tape and Reel	28-pin SSOP	0 to +70°C
9DB633AFILF	Tubes	28-pin SSOP	-40 to +85°C
9DB633AFILFT	Tape and Reel	28-pin SSOP	-40 to +85°C
9DB633AGLF	Tubes	28-pin TSSOP	0 to +70°C
9DB633AGLFT	Tape and Reel	28-pin TSSOP	0 to +70°C
9DB633AGILF	Tubes	28-pin TSSOP	-40 to +85°C
9DB633AGILFT	Tape and Reel	28-pin TSSOP	-40 to +85°C

"LF" after the package code are the Pb-Free configuration and are RoHS compliant.

"A" is the device revision designator (will not correlate to the datasheet revision).

**Revision History**

Rev.	Originator	Issue Date	Description	Page #
A	RDW	6/30/2010	Released to final	
B	RDW	7/12/2010	Changed "PWD" to "Default" in SMBus Register descriptions	10,11
C	RDW	4/20/2011	Changed pull down indicator from '*' to 'v'.	
D	RDW	10/22/2013	Corrected typo for 28SSOP T&R orderable part number; "I" and "L" were swapped.	13
E	RDW	2/19/2014	Corrected typo for Read/Write address from D4/D5 to D5/D4 respectively	9,10
F	RDW	10/20/2016	Updated input clock electrical table to latest format. No change to form, fit or function of the device	5

---

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.