Description

The 9DBL0243 / 9DBL0253 devices are 3.3V members of IDT's Full-Featured PCIe clock family. They support PCIe Gen1–4 Common Clock (CC) architectures and also support NVLINK applications. The 9DBL0243 / 9DBL0253 parts have a Loss of Signal (LOS) indicator to support fault-tolerant, high-reliability systems.

Typical Applications

- PCIe Gen1–4 and NVLINK clock distribution for Riser Cards
- Storage and Networking
- JBOD
- Communications
- Access Points

Output Features

- Loss Of Signal (LOS) open drain output
- 2 1–200 MHz Low-Power (LP) HCSL DIF pairs
  - 9DBL0243 default Zout = 100Ω
  - 9DBL0253 default Zout = 85Ω
- Easy AC-coupling to other logic families; see IDT application note AN-891.

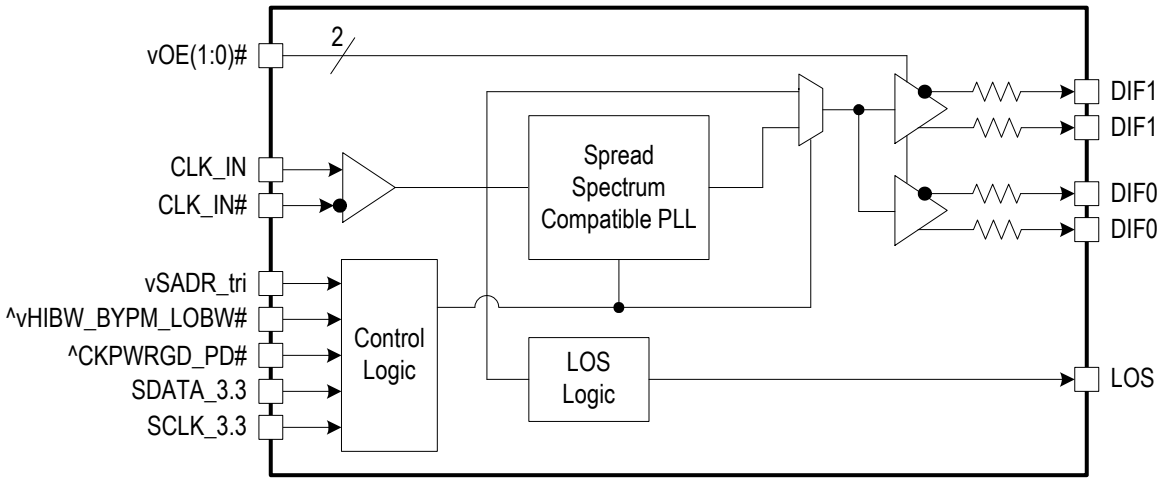
Key Specifications

- PCIe Gen1–4 CC compliant in ZDB or fanout buffer mode
- Supports NVLINK at 156.25MHz in ZDB or fanout buffer mode
- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- Bypass Mode additive phase jitter is 0ps typical rms for PCIe
- Bypass Mode additive phase jitter 160fs rms typical at 156.25M (1.5MHz to 10MHz)

Features

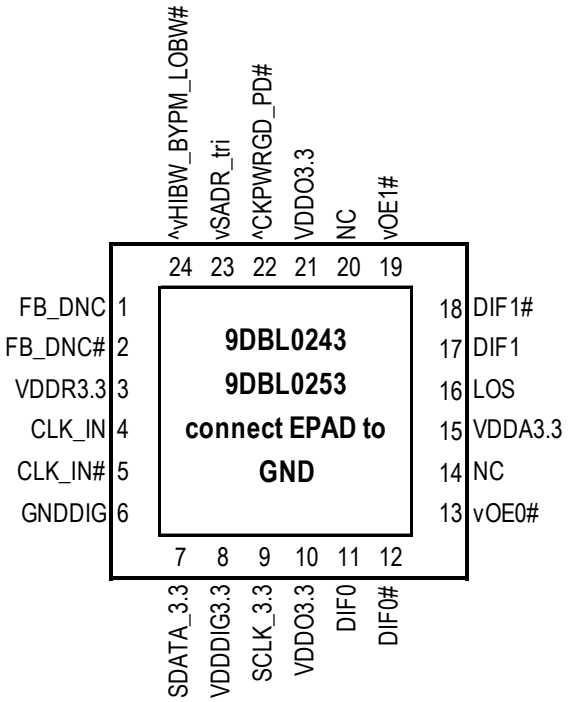
- LOS indicator signals loss of input clock; adds fault tolerance, eases system diagnostics
- Direct connection to 100Ω (0243) or 85Ω (0253) transmission lines; saves 8 resistors compared to standard PCIe devices
- 100mW typical power consumption in PLL mode; eliminates thermal concerns
- OE# pin for each DIF output; supports DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- Spread spectrum tolerant; allows reduction of EMI
- Outputs blocked until PLL is locked; clean system start-up
- Pin/SMBus selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- 3 selectable SMBus addresses; multiple devices can easily share an SMBus segment
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull-up/downs
  - slew rate for each output
  - differential output amplitude
  - output impedance for each output
- Contact IDT for quick-turn customization of SMBus defaults; allows exact optimization to customer requirements.
- 4 × 4 mm 24-VFQFPN; minimal board space

Block Diagram



Pin Assignments

Figure 1. Pin Assignments for 4 x 4 mm 24-VFQFPN Package – Top View



24-pin VFQFPN, 4x4 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor

^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
2	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
3	VDDR3.3	Power	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately, nominally 3.3V.
4	CLK_IN	Input	True input for differential reference clock.
5	CLK_IN#	Input	Complementary input for differential reference clock.
6	GNDDIG	Ground	Ground pin for digital circuitry.
7	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
8	VDDDIG3.3	Power	3.3V digital power (dirty power).
9	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.
10	VDDO3.3	Power	Power supply for outputs, nominally 3.3V.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
11	DIF0	Output	Differential true clock output.
12	DIF0#	Output	Differential complementary clock output.
13	vOE0#	Input	Active low input for enabling output 0. This pin has an internal 120kΩpull-down. 1 = disable outputs, 0 = enable outputs.
14	NC	—	No connection.
15	VDDA3.3	Power	3.3V power for the PLL core.
16	LOS	Open Drain Output	Output indicating loss of input signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. The polarity of this pin is programmable. Consult the SMBus registers for details.
17	DIF1	Output	Differential true clock output.
18	DIF1#	Output	Differential complementary clock output.
19	vOE1#	Input	Active low input for enabling output 1. This pin has an internal 120kΩ pull-down. 1 = disable outputs, 0 = enable outputs.
20	NC	—	No connection.
21	VDDO3.3	Power	Power supply for outputs, nominally 3.3V.
22	^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kΩ pull-up resistor.
23	vSADR_tri	Latched In	Tri-level latch to select SMBus Address. It has an internal 120kΩ pull down resistor. See SMBus Address Selection Table.
24	^vHIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to $V_{DD}/2$ (Bypass Mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for details.
25	EPAD	Ground	Connect EPAD to ground.

Note: “DNC” indicates do not connect to anything.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9DBL0243 / 9DBL0253 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx				4.6	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD Protection	ESD prot	Human Body Model	2500			V	1
Supply Voltage	VDDx				4.6	V	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Thermal Characteristics

Table 3. Thermal Characteristics

Symbol	Parameter	Package	Typical Values	Units	Notes
θ_{JC}	Junction to case	NLG24	62	°C/W	1
θ_{Jb}	Junction to base		5.4	°C/W	1
θ_{JA0}	Junction to air, still air		50	°C/W	1
θ_{JA1}	Junction to air, 1 m/s air flow		43	°C/W	1
θ_{JA3}	Junction to air, 3 m/s air flow		39	°C/W	1
θ_{JA5}	Junction to air, 5 m/s air flow		38	°C/W	1

[1] EPAD soldered to board.

Electrical Characteristics

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 4. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	at I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	at V_{OL}	4			mA	

Table 4. SMBus Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V)			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency			500	kHz	2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] The device must be powered up for the SMBus to function.

[3] The differential input clock must be running for the SMBus to be active.

Table 5. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix)	0.75 V_{DDx}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 V_{DDx}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DDx}	-5		5	µA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	µA	
Input Frequency	F_{IN}	Bypass mode	1		200	MHz	2
		PLL mode	90	100.00	160	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
CLK_IN Loss of Signal Detect Time	t_{LOS}			4.2	6	ms	1
CLK_IN Loss of Signal Release Time	t_{LOSREL}			0.12	0.5	ms	1
Clk Stabilization	t_{STAB}				1.8	ms	1,2

Table 5. Input/Supply/Common Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular Modulation)	30	31.5	33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable frequency for non-PCIe applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	µs	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

Table 6. Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Cross over voltage	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform	45		55	%	1
Input Jitter –Cycle to Cycle	J_{DIFIn}	Differential measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 7. DIF Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	dV/dt	Scope averaging on, fast setting	2.0	2.8	4	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	1.3	2.0	2.9	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Slew rate matching		6	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	754	850	mV	7
Voltage Low	V_{LOW}		-150	-3	150		7
Maximum Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		797	1150	mV	7
Minimum Voltage	Vmin		-300	-39			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	384	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		16	140	mV	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±50mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Table 8. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDA}	V_{DDA}, PLL Mode at 100MHz		7	10	mA	
	I_{DDDIG}	$V_{DDDIG,}$ PLL Mode at 100MHz		3.3	5	mA	
	I_{DDO+R}	V_{DDO} + V_{DDR}, PLL Mode, all outputs at 100MHz		20	26	mA	
Power Down Current	I_{DDRPD}	V_{DDA}, CKPWRGD_PD# = 0		0.6	1.0	mA	1
	$I_{DDDIGPD}$	V_{DDDIG}, CKPWRGD_PD# = 0		3.0	4.3	mA	1
	I_{DDAOPD}	V_{DDO} + V_{DDR}, CKPWRGD_PD# = 0		0.9	1.4	mA	1

[1] Input clock stopped.

Table 9. Output Duty Cycle, Jitter, Skew and PLL Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
PLL Bandwidth	BW	-3dB point in High BW Mode (100MHz)	2	3.3	4	MHz	1,5
		-3dB point in Low BW Mode (100MHz)	1	1.5	2	MHz	1,5
PLL Jitter Peaking	t_{JPEAK}	Peak pass band gain (100MHz)		0.8	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode	-1	0.0	1	%	1,3
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2500	3440	4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-100	8	100	ps	1,4
Skew, Output to Output	t_{sk3}	Mean value at 100MHz, VT = 50%		17	50	ps	1,4
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	PLL Mode		15	50	ps	1,2
		Additive Jitter in Bypass Mode		0.1	1	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

[4] All outputs at default slew rate.

[5] The minimum/typical/maximum values of each BW setting track each other, i.e., Low BW maximum will never occur with High BW minimum.

Table 10. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		23	33	86	ps (p-p)	1,2,3, 5
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0.6	1.0	3	ps (rms)	1,2,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		1.7	2.4	3.1	ps (rms)	1,2,5
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.4	0.50	1	ps (rms)	1,2,5
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.4	0.50	0.5	ps (rms)	1,2,5
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		0.05	0.10	N/A	ps (p-p)	1,2,5
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0.05	0.10		ps (rms)	1,2,4, 5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–5MHz, CDR = 5MHz)		0.05	0.10		ps (rms)	1,2,4, 5
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.05	0.10		ps (rms)	1,2,4, 5
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz)		0.05	0.10		ps (rms)	1,2,4, 5

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev 4.0 version 0.7 draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1–12.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2 + b^2 = c^2*] where a is rms input jitter and c is rms total jitter.

[5] Driven by 9FGL0841 or equivalent.

Table 11. Unfiltered Phase Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Additive Phase Jitter, Fanout Mode	$t_{jph156M}$	156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade roll-off > 10MHz		159		fs (rms)	1,2,3
	$t_{jph156M12k-20}$	156.25MHz, 12kHz to 20MHz, -20dB/decade rollover <12kHz, -40db/decade roll-off > 20MHz		363		fs (rms)	1,2,3

[1] Applies to all outputs when driven by Wenzel clock source.

[2] Driven by Rhode & Schwartz SMA100.

[3] For RMS values additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2].

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OE bit	OEx# Pin	DIFx/DIFx#		PLL
				True Output	Complementary Output	
0	X	X	x	Low[1]	Low[1]	Off
1	Running	1	0	Running	Running	On[3]
1	Running	1	1	Disabled[1]	Disabled[1]	On[3]
1	Running	0	x	Disabled[1]	Disabled[1]	On[3]

[1] The output state is set by B11[1:0] (Low/Low default).

[2] Input polarities defined as default values for xx43/xx53 devices.

[3] If Bypass Mode is selected, the PLL will be off and outputs will be running.

PLL Operating Mode Table

HIBW_BYPM_LOBW#	Mode	Byte1 [7:6] Readback	Byte1 [4:3] Readback
0	PLL Low BW	00	00
M	Bypass	01	01
1	PLL High BW	11	11

Power Connections

Pin Number		Description
V_{DD}	GND	
3	25	Input receiver analog
8	6	Digital power
10, 21	25	DIF outputs
15	25	PLL analog

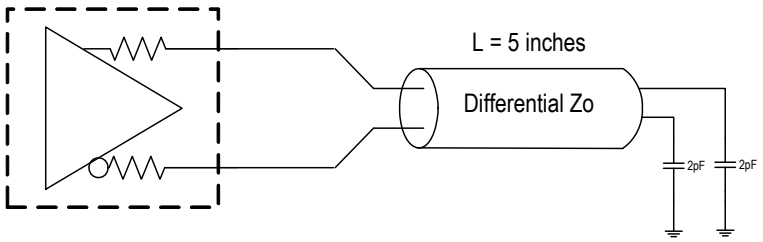
SMBus Addressing Table

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Note: If not using CKPWRGD (CKPWRGD tied to VDD3.3), all 3.3V V_{DD} need to transition from 2.1V to 3.135V in < 300µsec.

Test Loads

Low-Power Push-Pull HCSL Output Test Load
(integrated terminations)



Terminations

Device	DIF Zo (Ω)	Rs (Ω)
9DBL0243	100	None needed
9DBL0253	100	7.5
9DBL0243	85	N/A
9DBL0253	85	None needed

Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

General SMBus Serial Interface Information for 9DBL0243 / 9DBL0253

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus address is latched on SADR pin. Default values are for the xx43and xx53. Contact IDT for quick-turn customization.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	DIF OE1	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 3	Reserved					0
Bit 2	DIF OE0	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 1	Reserved					0
Bit 0	Reserved					0

[1] A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default).

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0	R			Latch
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW[1]	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW[1]			0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.60V	01 = 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

[1] B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: Output Disable Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					1
Bit 4	SLEWRATESEL DIF1	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 3	Reserved					1
Bit 2	SLEWRATESEL DIF0	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 1	Reserved					1
Bit 0	Reserved					1

SMBus Table: Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	Slow Setting	Fast Setting	1

Byte 4 is Reserved.

SMBus Table: Reserved Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Vendor & Revision ID Register

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device ID7	Device ID	RW	9DBL0243/0253 = 52 9DBL0443/0453 = 54 9DBL0643/0653 = 56 9DBL0843/0853 = 58		0
Bit 6	Device ID6		RW			1
Bit 5	Device ID5		RW			0
Bit 4	Device ID4		RW			1
Bit 3	Device ID3		RW			X
Bit 2	Device ID2		RW			X
Bit 1	Device ID1		RW			X
Bit 0	Device ID0		RW			X

SMBus Table: Device ID

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved.

SMBus Table: Byte Count Register

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Byte Count Register

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	FB_imp[1]	Differential Zout (ohms)	RW	00 = 33	10 = 100	see Note
Bit 6	FB_imp[0]		RW	01 = 85	11 = Reserved	
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

Note: xx43 = 10, xx53 = 01.

SMBus Table: Byte Count Register

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					x
Bit 6	Reserved					x
Bit 5	DIF0_imp[1]	Differential Zout (ohms)	RW	00 = 33	10 = 100	see Note
Bit 4	DIF0_imp[0]		RW	01 = 85	11 = Reserved	
Bit 3	Reserved					x
Bit 2	Reserved					x
Bit 1	Reserved					x
Bit 0	Reserved					x

Note: xx43 = 10, xx53 = 01.

SMBus Table: Byte Count Register

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					x
Bit 6	Reserved					x
Bit 5	Reserved					x
Bit 4	Reserved					x
Bit 3	Reserved					x
Bit 2	Reserved					x
Bit 1	DIF1_imp[1]	Differential Zout (ohms)	RW	00 = 33	10 = 100	see Note
Bit 0	DIF1_imp[0]		RW	01 = 85	11 = Reserved	

Note: xx43 = 10, xx53 = 01.

SMBus Table: Byte Count Register

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					x
Bit 6	Reserved					x
Bit 5	OE0_pu/pd[1]	OE0 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 4	OE0_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	1
Bit 3	Reserved					x
Bit 2	Reserved					x
Bit 1	Reserved					x
Bit 0	Reserved					x

SMBus Table: Byte Count Register

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					x
Bit 6	Reserved					x
Bit 5	Reserved					x
Bit 4	Reserved					x
Bit 3	Reserved					x
Bit 2	Reserved					x
Bit 1	OE1_pu/pd[1]	OE1 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 0	OE1_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	1

Note: These values are for xx43 and xx53.

SMBus Table: Byte Count Register

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	0

Note: These values are for xx43 and xx53.

Byte 17 is Reserved.

SMBus Table: Byte Count Register

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					x
Bit 6	Reserved					x
Bit 5	Reserved					x
Bit 4	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	Reserved					x
Bit 2	OE0_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	Reserved					x
Bit 0	Reserved					x

SMBus Table: Byte Count Register

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	LOS Polarity	Determines LOS polarity	RW	Low when input clock absent	High when input clock absent	1
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Note: These values are for 0243 and 0253.

Package Drawings

Figure 2. 4 × 4 × 0.5 mm 24-VFQFPN – page 1

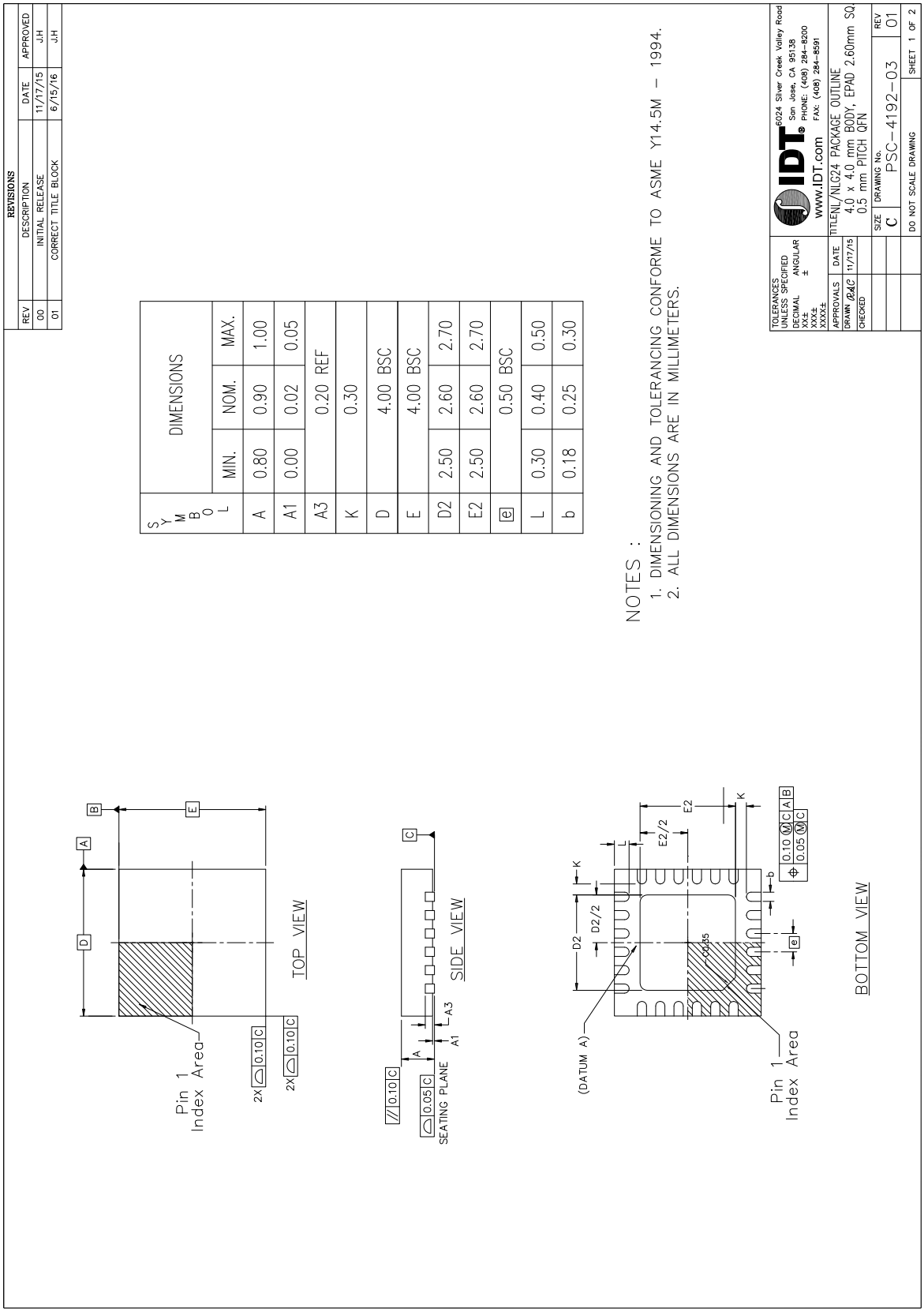
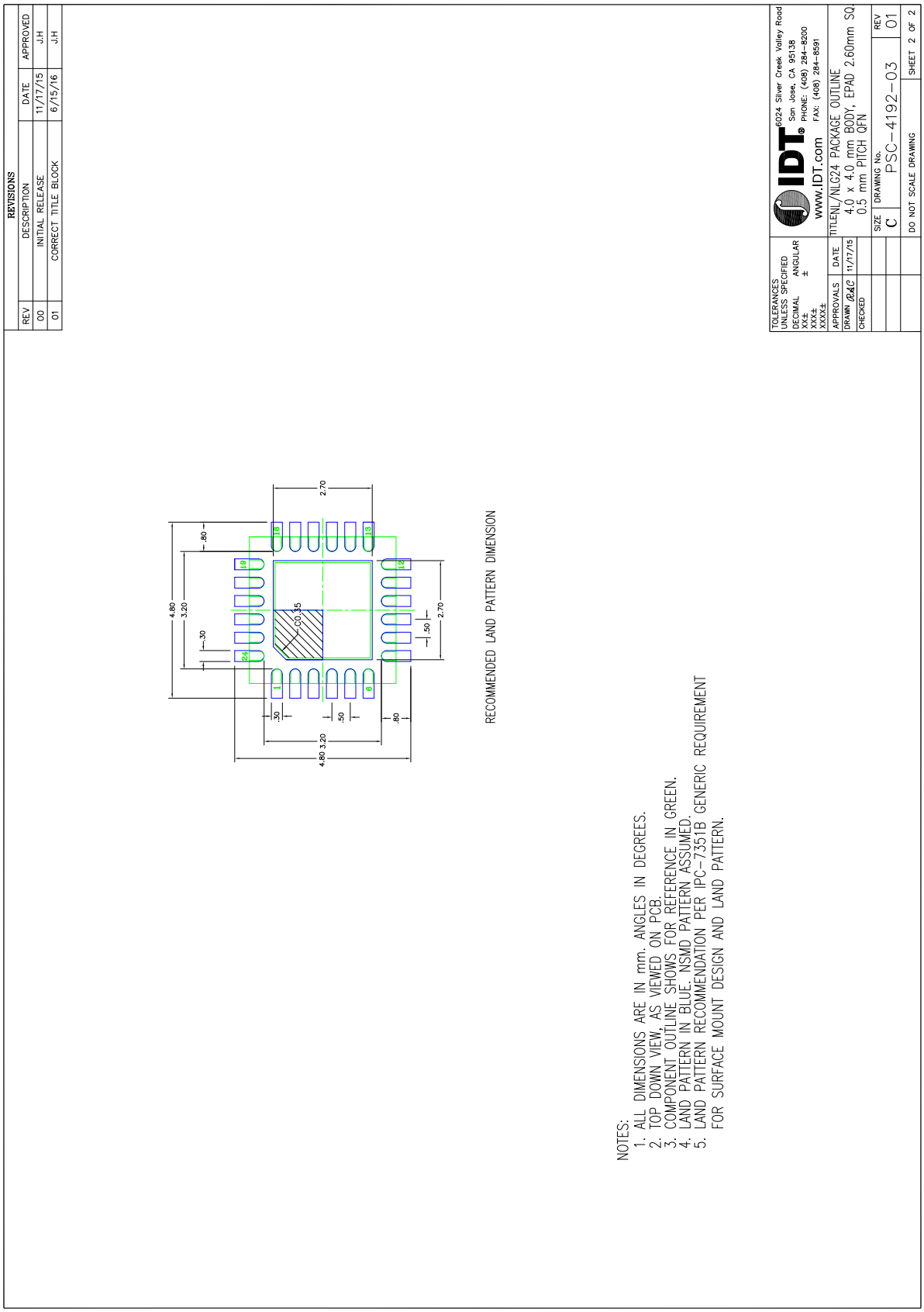
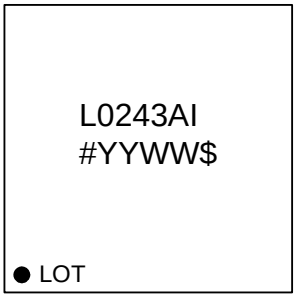


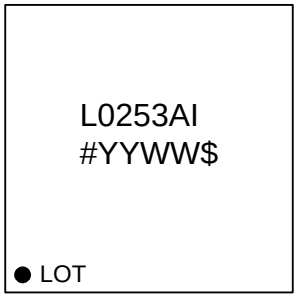
Figure 3. 4 × 4 × 0.5 mm 24-VFQFPN – page 2



Marking Diagrams



1. Line 1: truncated part number
2. “#” denotes stepping number.
3. “YYWW” denotes the last two digits of the year and week the part was assembled.
4. “$” denotes mark code.
5. “LOT” denotes lot number.



Ordering Information

Orderable Part Number	Notes	Package	Carrier Type	Temperature
9DBL0243ANLGI	100Ω	4 × 4 × 0.5 mm 24-VFQFPN	Tubes	-40° to +85°C
9DBL0243ANLGI8		4 × 4 × 0.5 mm 24-VFQFPN	Tape and Reel	-40° to +85°C
9DBL0253ANLGI	85Ω	4 × 4 × 0.5 mm 24-VFQFPN	Tubes	-40° to +85°C
9DBL0253ANLGI8		4 × 4 × 0.5 mm 24-VFQFPN	Tape and Reel	-40° to +85°C

“G” designates PB-free configuration, RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Revision Date	Description of Change
March 15, 2017	▪ Minor update to all electrical tables for consistency; no material changes to specifications. ▪ Rearranged order of content and reformatted tables. ▪ Block diagram redrawn. ▪ Updated package outline drawings to the latest revision (01).
February 1, 2017	▪ Corrected Byte 16[3:2]. These bits are reserved with '00' default.
January, 25, 2017	▪ Updated ohm symbols and output references in Bytes [11:13], stylistic change only.
December 22, 2016	▪ Initial final release ▪ Extensive updates for consistency and clarity throughout the data sheet ▪ Update Electrical Tables with characterization data ▪ Added marking diagrams.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138 USA
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support