4-output 3.3V PCIe Zero-delay Buffer

9DBL04

DATASHEET

Description

The 9DBL04 devices are 3.3V members of IDT's Full-Featured PCIe family. The 9DBL04 supports PCIe Gen1-4 Common Clocked (CC) and PCIe Separate Reference Independent Spread (SRIS) systems. It offers a choice of integrated output terminations providing direct connection to 85Ω or 100Ω transmission lines. The 9DBL04P2 can be factory programmed with a user-defined power up default SMBus configuration.

Recommended Application

PCIe Gen1-4 clock distribution for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

Output Features

- 4 – 1-200 MHz Low-Power (LP) HCSL DIF pairs
  - 9DBL0442 default ZOUT = 100Ω
  - 9DBL0452 default ZOUT = 85Ω
  - 9DBL04P2 factory programmable defaults
- Easy AC-coupling to other logic families, see IDT application note AN-891

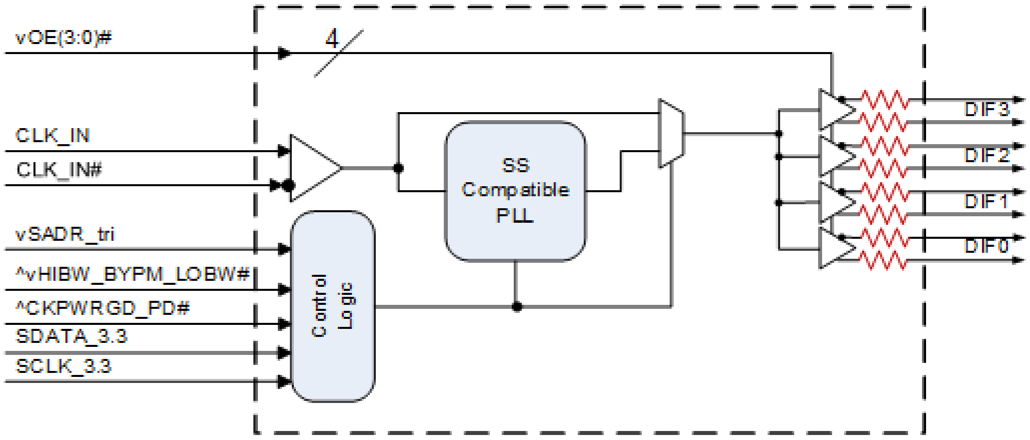
Key Specifications

- PCIe Gen1-2-3-4 CC compliant in ZDB mode
- PCIe Gen2 SRIS compliant in ZDB mode
- Supports PCIe Gen2-3 SRIS in fan-out mode
- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew < 50ps
- Bypass mode *additive* phase jitter is 0 ps typical rms for PCIe
- Bypass mode additive phase jitter 160fs rms typ. @ 156.25M (1.5M to 10M)

Features/Benefits

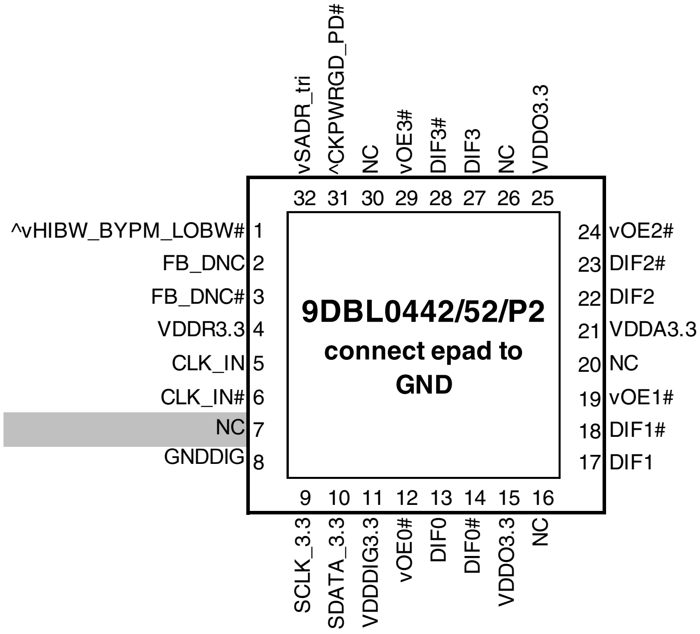
- Direct connection to 100Ω (xx42) or 85Ω (xx52) transmission lines; saves 16 resistors compared to standard PCIe devices
- 132mW typical power consumption in PLL mode; eliminates thermal concerns
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - differential output amplitude
  - output impedance for each output
  - 50, 100, 125MHz operating frequency
- Customer defined SMBus power up default can be programmed into P2 device; allows exact optimization to customer requirements
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- Pin/SMBus selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- Outputs blocked until PLL is locked; clean system start-up
- Device contains default configuration; SMBus interface not required for device operation
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Space saving 32-pin 5x5mm VFQFPN; minimal board space

Block Diagram



Note: Resistors default to internal on xx42/xx52 devices. P2 devices have programmable default impedances on an output-by-output basis.

Pin Configuration



32-pin VFQFPN, 5x5 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor

^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OE bit	OEx# Pin	DIFx/DIFx#		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low[1]	Low[1]	Off
1	Running	1	0	Running	Running	On[3]
1	Running	1	1	Disabled[1]	Disabled[1]	On[3]
1	Running	0	X	Disabled[1]	Disabled[1]	On[3]

1. The output state is set by B11[1:0] (Low/Low default)
2. Input polarities defined as default values for xx42/xx52 devices.
3. If Bypass mode is selected, the PLL will be off, and outputs will be running.

Power Connections

Pin Number		Description
VDD	GND	
4	33	Input receiver analog
11	8	Digital Power
15,25	33	DIF outputs
21	33	PLL Analog

PLL Operating Mode

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

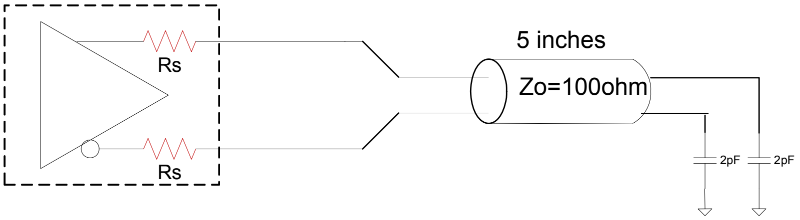
Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	^vHIBW_BYPM_LOB	LATCHED IN	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for Details.
2	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
3	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	VDDR3.3	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	CLK_IN	IN	True Input for differential reference clock.
6	CLK_IN#	IN	Complementary Input for differential reference clock.
7	NC	N/A	No Connection.
8	GNDDIG	GND	Ground pin for digital circuitry
9	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
10	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
11	VDDDIG3.3	PWR	3.3V digital power (dirty power)
12	vOE0#	IN	Active low input for enabling output 0. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
15	VDDO3.3	PWR	Power supply for outputs,nominal 3.3V.
16	NC	N/A	No Connection.
17	DIF1	OUT	Differential true clock output
18	DIF1#	OUT	Differential Complementary clock output
19	vOE1#	IN	Active low input for enabling output 1. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
20	NC	N/A	No Connection.
21	VDDA3.3	PWR	3.3V power for the PLL core.
22	DIF2	OUT	Differential true clock output
23	DIF2#	OUT	Differential Complementary clock output
24	vOE2#	IN	Active low input for enabling output 2. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
25	VDDO3.3	PWR	Power supply for outputs,nominal 3.3V.
26	NC	N/A	No Connection.
27	DIF3	OUT	Differential true clock output
28	DIF3#	OUT	Differential Complementary clock output
29	vOE3#	IN	Active low input for enabling output 3. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
30	NC	N/A	No Connection.
31	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kohm pull-up resistor.
32	vSADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. It has an internal 120kohm pull down resistor. See SMBus Address Selection Table.
33	epad	GND	connect epad to ground.

NOTE: DNC indicates Do Not Connect anything to this pin.

Test Loads

Low-Power Differential Output Test Load



Note: The device can drive transmission line lengths greater than those specified by the PCIe SIG

Terminations

Device	Zo (Ω)	Rs (Ω)
9DBL0442	100	None needed
9DBL0452	100	7.5
9DBL04P2	100	Prog.
9DBL0442	85	N/A
9DBL0452	85	None needed
9DBL04P2	85	Prog.

Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See “AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs” for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBL04. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx				4.6	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2500			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency			500	kHz	2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2.] The device must be powered up for the SMBus to function.

[3.] The differential input clock must be running for the SMBus to be active

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix)	0.75 V_{DDx}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 V_{DDx}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	F_{IN}	Bypass mode	1		200	MHz	2
		100MHz PLL mode	60	100.00	140	MHz	2
		50MHz PLL mode	30	50.00	65	MHz	2
		125MHz PLL mode	75	125.00	175	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30		33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	2	2.8	4	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	1.2	1.9	3.1	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching		7	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	768	850	mV	7
Voltage Low	V_{LOW}		-150	-11	150		7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		811	1150	mV	7
Min Voltage	Vmin		-300	-49			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	357	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		14	140	mV	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDA}	VDDA, PLL Mode @100MHz		7	10	mA	
	I_{DDDIG}	VDDDIG, PLL Mode @100MHz		3.4	5	mA	
	I_{DDO+R}	VDDO+VDDR, PLL Mode, All outputs @100MHz		30.0	37	mA	
Powerdown Current	I_{DDRPD}	VDDA, CKPWRGD_PD# = 0		0.6	1.0	mA	1
	$I_{DDDIGPD}$	VDDDIG, CKPWRGD_PD# = 0		3.1	4.3	mA	1
	I_{DDAOPD}	VDDO+VDDR, CKPWRGD_PD# = 0		0.9	1.3	mA	1

[1] Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
PLL Bandwidth	BW	-3dB point in High BW Mode (100MHz)	2	3.3	4	MHz	1,5
		-3dB point in Low BW Mode (100MHz)	1	1.5	2	MHz	1,5
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain (100MHz)		0.8	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode	-1	0.0	1	%	1,3
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2500	3406	4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-100	8	100	ps	1,4
Skew, Output to Output	t_{sk3}	V_T = 50%		21	55	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	PLL mode		15	50	ps	1,2
		Additive Jitter in Bypass Mode		0.1	1	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1		23	32	86	ps (p-p)	1,2,3,5
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.6	0.8	3	ps (rms)	1,2,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		1.7	2.1	3.1	ps (rms)	1,2,5
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.4	0.48	1	ps (rms)	1,2,5
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.4	0.48	0.5	ps (rms)	1,2,5
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen 1		0.0	0.01	n/a	ps (p-p)	1,2,5
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.0	0.01		ps (rms)	1,2,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.0	0.01		ps (rms)	1,2,4,5
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.01		ps (rms)	1,2,4,5
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.01		ps (rms)	1,2,4,5

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

[5] Driven by 9FGL0841 or equivalent

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures[5]

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		1.2	1.5	2	ps (rms)	1,2
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)	n/a			0.5	ps (rms)	1,2,6
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen 2 (PLL BW of 16MHz , CDR = 5MHz)		0.0	0.01	n/a	ps (rms)	1,2,4
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.0	0.01		ps (rms)	1,2,4,6

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev3.1a. These filters are different than Common Clock filters. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values, additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

[5] As of PCIe Base Specification Rev4.0 draft 0.7, SRIS is not currently defined for Gen1 or Gen4.

[6] This device does not support PCIe Gen3 SRIS in PLL mode. It supports PCIe Gen3 SRIS in bypass mode.

Electrical Characteristics–Unfiltered Phase Jitter Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter, Fanout Mode	$t_{jph156M}$	156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		159		N/A	fs (rms)	1,2,3
	$t_{jph156M12k\text{-}20}$	156.25MHz, 12kHz to 20MHz, -20dB/decade rollover <12kHz, -40db/decade rolloff > 20MHz		363		N/A	fs (rms)	1,2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Driven by Rohde&Schartz SMA100

[3] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus Address is Latched on SADR pin. Unless otherwise indicated, default values are for the xx42 and xx52. P2 devices are fully factory programmable.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved			See B11[1:0]		0
Bit 6	DIF OE3	Output Enable	RW		Pin Control	1
Bit 5	Reserved					0
Bit 4	DIF OE2	Output Enable	RW		Pin Control	1
Bit 3	DIF OE1	Output Enable	RW		Pin Control	1
Bit 2	Reserved					0
Bit 1	DIF OE0	Output Enable	RW		Pin Control	1
Bit 0	Reserved					0

1. A low on these bits will overide the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	**R**	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0	**R**			Latch
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW[1]	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW[1]			0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01= 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	SLEWRATESEL DIF3	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 5	Reserved					1
Bit 4	SLEWRATESEL DIF2	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF1	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 2	Reserved					1
Bit 1	SLEWRATESEL DIF0	Slew rate selection	RW	Slow Setting	Fast Setting	1
Bit 0	Reserved					1

Note: See "Low-Power HCSL Outputs" table for slew rates.

SMBus Table: Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	FREQ_SEL_EN	Enable SW selection of frequency	RW	SW frequency change disabled	SW frequency change enabled	0
Bit 4	FSEL1	Freq. Select Bit 1	RW[1]	00 = 100M, 10 = 125M 01 = 50M, 11= Reserved		0
Bit 3	FSEL0	Freq. Select Bit 0	RW[1]			0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	Slow Setting	Fast Setting	1

1. B3[5] must be set to a 1 for these bits to have any effect on the part.

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	B rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			1
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	RW	00 = FGx, 01 = DBx ZDB/FOB, 10 = DMx, 11= DBx FOB		0
Bit 6	Device Type0		RW			1
Bit 5	Device ID5	Device ID	RW	000110binary or 04 hex		0
Bit 4	Device ID4		RW			0
Bit 3	Device ID3		RW			0
Bit 2	Device ID2		RW			1
Bit 1	Device ID1		RW			0
Bit 0	Device ID0		RW			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved

SMBus Table: PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Stop State and Impedance Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	FB_imp[1]	FB Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	FB_imp[0]	FB Zout	RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

Note: xx42 = 10, xx52 = 01, P2 = factory programmable.

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF1_imp[1]	DIF3 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	see Note
Bit 6	DIF1_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 5	Reserved					
Bit 4	Reserved					
Bit 3	DIF0_imp[1]	DIF1 Zout	RW	00=33Ω DIF Zout	10=100Ω DIF Zout	
Bit 2	DIF1_imp[0]		RW	01=85Ω DIF Zout	11 = Reserved	
Bit 1	Reserved					
Bit 0	Reserved					

Note: xx42 = 10, xx52 = 01, P2 = factory programmable.

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					see Note
Bit 6	Reserved					
Bit 5	DIF3_imp[1]	DIF6 Zout	RW	00=33ς DIF Zout	10=100ς DIF Zout	
Bit 4	DIF3_imp[0]	DIF6 Zout	RW	01=85ς DIF Zout	11 = Reserved	
Bit 3	Reserved					
Bit 2	Reserved					
Bit 1	DIF2_imp[1]	DIF4 Zout	RW	00=33ς DIF Zout	10=100ς DIF Zout	
Bit 0	DIF2_imp[0]	DIF4 Zout	RW	01=85ς DIF Zout	11 = Reserved	

Note: xx42 = 10, xx52 = 01, P2 = factory programmable.

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE1_pu/pd[1]	OE3 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 6	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	Reserved					0
Bit 4	Reserved					1
Bit 3	OE0_pu/pd[1]	OE1 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 2	OE0_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	Reserved					0
Bit 0	Reserved					1

Note: xx42 = 10, xx52 = 01, P2 = factory programmable.

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					1
Bit 5	OE3_pu/pd[1]	OE6 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 4	OE3_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	OE2_pu/pd[1]	OE4 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 0	OE2_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	HIBW_BYPM_LOBWpu/pd[1]	HIBW_BYPM_LOBW Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	1
Bit 2	HIBW_BYPM_LOBWpu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	0

Note: xx42 = 10, xx52 = 01, P2 = factory programmable.

Bytes 17 is Reserved

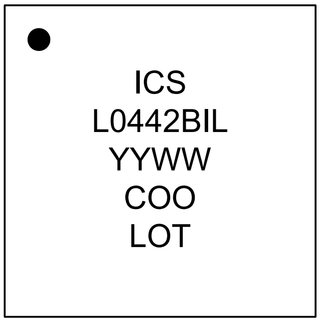
SMBus Table: Polarity Control

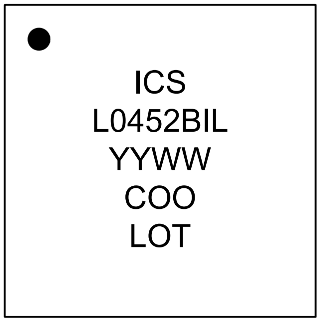
Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	OE3_polarity	Sets OE6 polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	Reserved					0
Bit 4	OE2_polarity	Sets OE4 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE1_polarity	Sets OE3 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	Reserved					0
Bit 1	OE0_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 0	Reserved					0

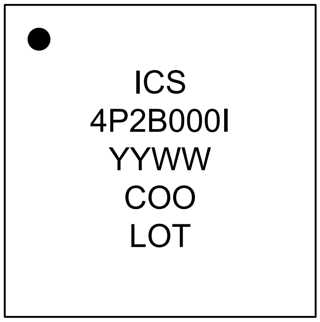
SMBus Table: Polarity Control

Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Marking Diagrams







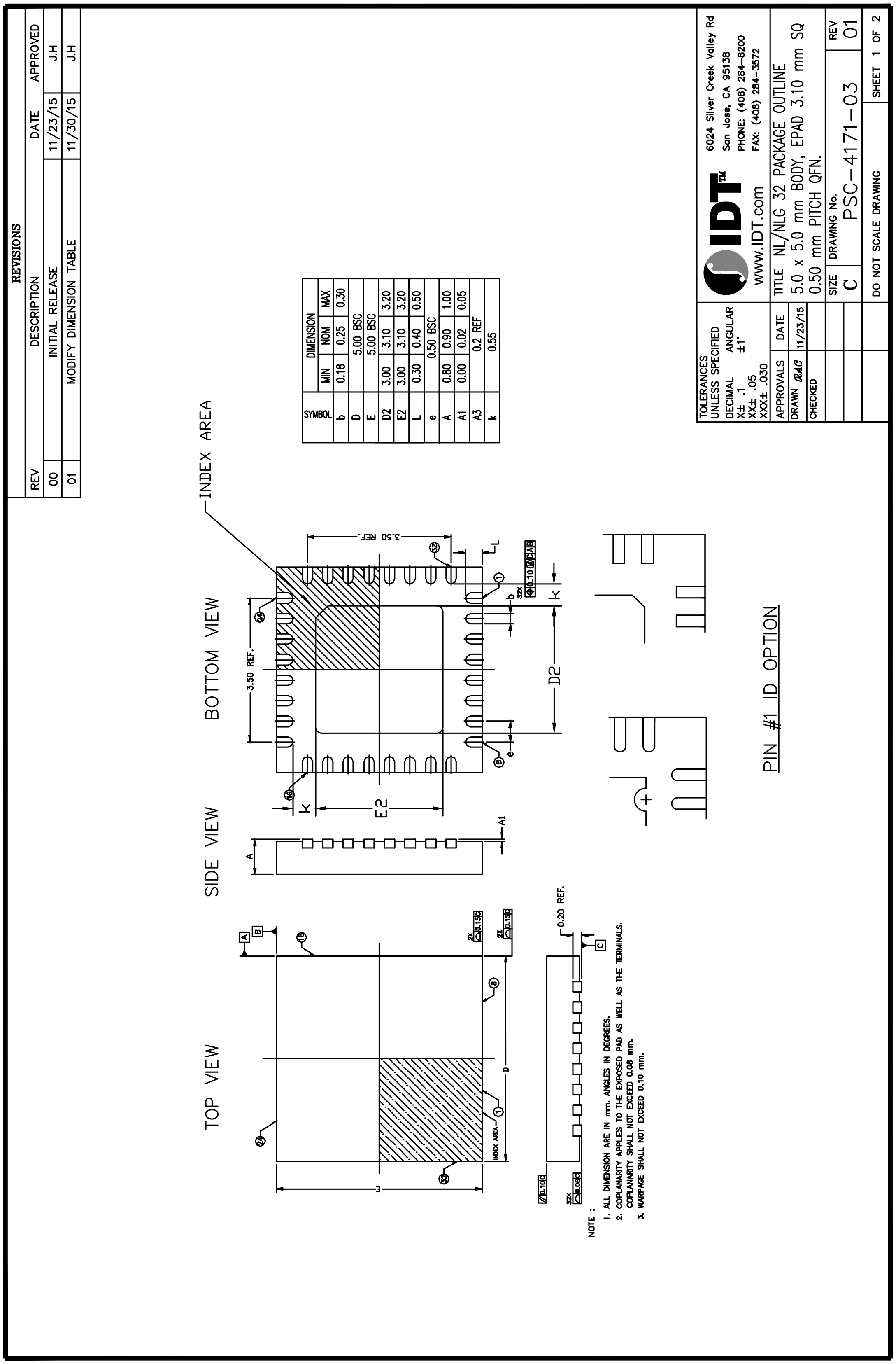
Notes:
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “I” denotes industrial temperature range device.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG32	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1] ePad soldered to board

Package Outline and Dimensions (NLG32)



REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/23/15	J.H
01	MODIFY DIMENSION TABLE	11/30/15	J.H

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	3.00	3.10	3.20
E2	3.00	3.10	3.20
L	0.30	0.40	0.50
e		0.50 BSC	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k		0.55	

NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS	DATE
DRAWN RAC	11/23/15
CHECKED	

IDT™
www.IDT.com
6024 Silver Creek Valley Rd
San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY, EPAD 3.10 mm SQ
0.50 mm PITCH QFN.

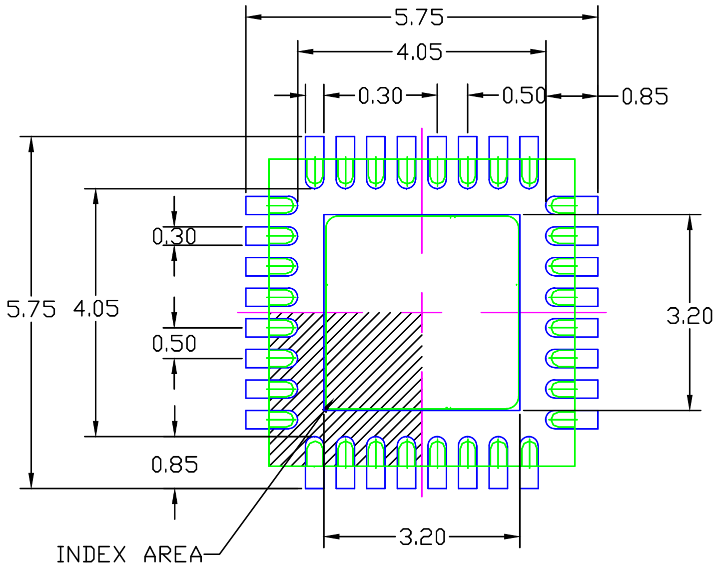
SIZE	DRAWING No.	REV
C	PSC-4171-03	01

DO NOT SCALE DRAWING
SHEET 1 OF 2

Package Outline and Dimensions (NLG32), cont.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/23/15	J.H
01	MODIFY DIMENSION TABLE	11/30/15	J.H



RECOMMENDED LAND PATTERN.

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

APPROVALS	DATE
DRAWN ℘𝒳℘	12/20/06
CHECKED	

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San Jose, CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572

TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY, EPAD 3.10 mm SQ
0.50 mm PITCH QFN.

SIZE	DRAWING No.	REV
C	PSC-4171-03	01

DO NOT SCALE DRAWING SHEET 2 OF 2

Ordering Information

Part / Order Number	Notes	Shipping Packaging	Package	Temperature
9DBL0442BKILF	100Ω	Trays	32-pin VFQFPN	-40 to +85° C
9DBL0442BKILFT		Tape and Reel	32-pin VFQFPN	-40 to +85° C
9DBL0452BKILF	85Ω	Trays	32-pin VFQFPN	-40 to +85° C
9DBL0452BKILFT		Tape and Reel	32-pin VFQFPN	-40 to +85° C
9DBL04P2BxxxKILF	Factory configurable. Contact IDT for addtional information.	Trays	32-pin VFQFPN	-40 to +85° C
9DBL04P2BxxxKILFT		Tape and Reel	32-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
"B" is the device revision designator (will not correlate with the datasheet revision).
"xxx" is a unique factory assigned number to identify a particular default configuration.

Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	5/31/2016	1. Add PCIe G1-4 Common Clock and PCIe SRIS to electrical tables 2. Update Electrical Tables to final 3. Changed '1' value in Byte 0 to indicate "Pin Control" 4. Stylistic update to block diagram 5. Minor updates to SMBus registers 0 and 1 for Readability 6. Front page text update for family consistency. 7. Removed '000' code from ordering information, updated table. 8. Minor corrections to Byte 1 [1:0] and Byte 11 [1:0]	Various
B	RDW	6/14/2016	1. Electrical Table and SMBus Updates/Corrections 2. Release to final.	Various
C	RDW	6/21/2016	1. Updated ESD from 2000V to 2500V	5
D	RDW	11/11/2016	1. Corrected pin 32 to indicate an internal pull down resistor, not a pull up resistor.	2, 3

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