General Description

The 9DBL08x3 devices are 3.3V members of IDT's Full-Featured PCIe clock family. They support PCIe Gen1-4 Common Clock (CC) architectures and also support NVLINK applications. The 9DBL08x3 parts have a Loss of Signal (LOS) indicator to support fault-tolerant, high reliability systems.

Recommended Application

PCIe Gen1-4 and NVLINK clock distribution for Riser Cards, Storage, Networking, JBOD, Communications, Access Points

Output Features

- Loss Of Signal (LOS) open drain output
- 8 – 1-200 MHz Low-Power (LP) HCSL DIF pairs
  - 9DBL0843 default Zout = 100Ω
  - 9DBL0853 default Zout = 85Ω
- Easy AC-coupling to other logic families, see IDT application note AN-891.

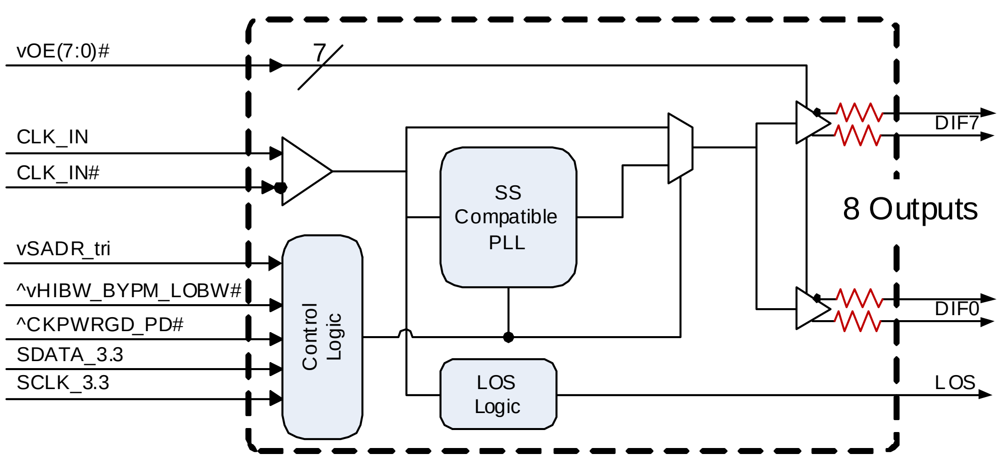
Key Specifications

- PCIe Gen1-4 CC compliant in ZDB or fanout buffer mode
- Supports NVLINK at 156.25M in ZDB or fanout buffer mode
- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew < 50ps
- Bypass mode additive phase jitter is 0 ps typical rms for PCIe
- Bypass mode additive phase jitter 160fs rms typ. @ 156.25M (1.5M to 10M)

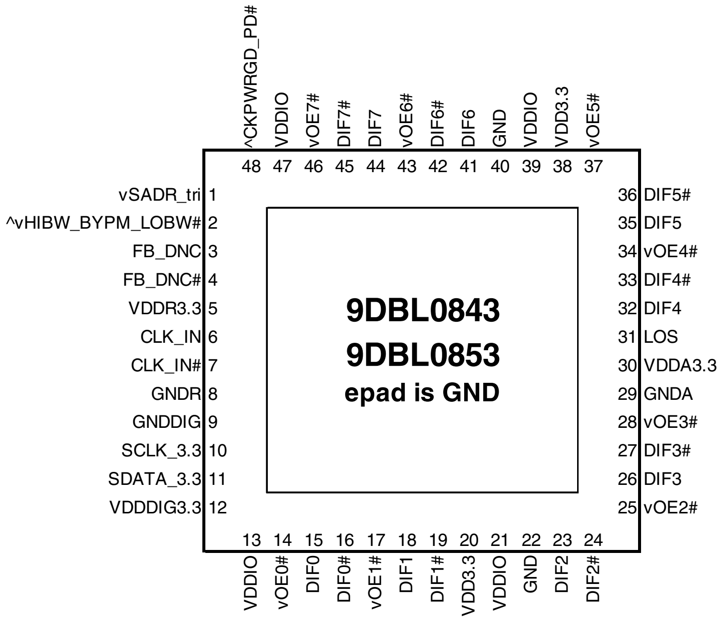
Features/Benefits

- LOS indicator signals loss of input clock; adds fault tolerance, eases system diagnostics
- Direct connection to 100Ω (xx43) or 85Ω (xx53) transmission lines; saves 32 resistors compared to standard PCIe devices
- 205mW typical power consumption (PLL mode@3.3V); eliminates thermal concerns
- VDDIO allows >33% power savings at optional 1.05V; maximum power savings
- OE# pin for each DIF output; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- Outputs blocked until PLL is locked; clean system start-up
- Pin/SMBus selectable PLL bandwidth and PLL Bypass; minimize phase jitter for each application
- Device contains default configuration; SMBus interface not required for device operation
- 3 selectable SMBus addresses; multiple devices can easily share an SMBus segment
- SMBus-selectable features allows optimization to customer requirements:
  - control input polarity
  - control input pull up/downs
  - slew rate for each output
  - differential output amplitude
  - output impedance for each output
- Contact IDT for quick-turn customization of SMBus defaults; allows exact optimization to customer requirements
- Space saving 48-pin 6 × 6mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



48-pin VFQFPN, 6x6 mm, 0.4mm pitch

^v prefix indicates internal 120KOhm pull up *AND pull* down resistor (biased to VDD/2)
v prefix indicates internal 120KOhm pull down resistor
^ prefix indicates internal 120KOhm pull up resistor

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx		PLL
				True O/P	Comp. O/P	
0	X	X	X	Low[1]	Low[1]	Off
1	Running	1	0	Running	Running	On[3]
1	Running	1	1	Disabled[1]	Disabled[1]	On[3]
1	Running	0	X	Disabled[1]	Disabled[1]	On[3]

1. The output state is set by B11[1:0] (Low/Low default)
2. Input polarities defined as default values for xx43/xx53 devices.
3. If Bypass mode is selected, the PLL will be off, and outputs will be running.

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Note: If not using CKPWRGD (CKPWRGD tied to VDD3.3), all 3.3V VDD need to transition from 2.1V to 3.135V in <300usec.

PLL Operating Mode Table

HiBW_BypM_LoBW#	MODE	Byte1 [7:6] Readback	Byte1 [4:3] Control
0	PLL Lo BW	00	00
M	Bypass	01	01
1	PLL Hi BW	11	11

Power Connections

Pin Number			Description
VDD	VDDIO	GND	
5		8	Input receiver analog
12		9	Digital Power
20, 38	13, 21, 39, 47	22, 29, 40, 49	DIF outputs
30		29	PLL Analog

Pin Descriptions

PIN #	Pin Name	Type	Description
1	vSADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. See SMBus Address Selection Table.
2	^vHIBW_BYPM_LOBW#	LATCHED IN	Tri-level input to select High BW, Bypass or Low BW mode. This pin is biased to VDD/2 (Bypass mode) with internal pull up/pull down resistors. See PLL Operating Mode Table for Details.
3	FB_DNC	DNC	True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
4	FB_DNC#	DNC	Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin.
5	VDDR3.3	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
6	CLK_IN	IN	True Input for differential reference clock.
7	CLK_IN#	IN	Complementary Input for differential reference clock.
8	GNDR	GND	Analog Ground pin for the differential input (receiver)
9	GNDDIG	GND	Ground pin for digital circuitry
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	VDDDIG3.3	PWR	3.3V digital power (dirty power)
13	VDDIO	PWR	Power supply for differential outputs
14	vOE0#	IN	Active low input for enabling output 0. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
15	DIF0	OUT	Differential true clock output
16	DIF0#	OUT	Differential Complementary clock output
17	vOE1#	IN	Active low input for enabling output 1. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	VDD3.3	PWR	Power supply, nominal 3.3V
21	VDDIO	PWR	Power supply for differential outputs
22	GND	GND	Ground pin.
23	DIF2	OUT	Differential true clock output
24	DIF2#	OUT	Differential Complementary clock output
25	vOE2#	IN	Active low input for enabling output 2. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
26	DIF3	OUT	Differential true clock output
27	DIF3#	OUT	Differential Complementary clock output
28	vOE3#	IN	Active low input for enabling output 3. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
29	GNDA	GND	Ground pin for the PLL core.
30	VDDA3.3	PWR	3.3V power for the PLL core.
31	LOS	OPEN DRAIN OUT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. The pin is normally pulled low and goes high when the input clock is not present.
32	DIF4	OUT	Differential true clock output
33	DIF4#	OUT	Differential Complementary clock output
34	vOE4#	IN	Active low input for enabling output 4. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
35	DIF5	OUT	Differential true clock output

Pin Descriptions (cont.)

PIN #	Pin Name	Type	Description
36	DIF5#	OUT	Differential Complementary clock output
37	vOE5#	IN	Active low input for enabling output 5. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
38	VDD3.3	PWR	Power supply, nominal 3.3V
39	VDDIO	PWR	Power supply for differential outputs
40	GND	GND	Ground pin.
41	DIF6	OUT	Differential true clock output
42	DIF6#	OUT	Differential Complementary clock output
43	vOE6#	IN	Active low input for enabling output 6. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
44	DIF7	OUT	Differential true clock output
45	DIF7#	OUT	Differential Complementary clock output
46	vOE7#	IN	Active low input for enabling output 7. This pin has an internal 120kohm pull-down. 1 =disable outputs, 0 = enable outputs
47	VDDIO	PWR	Power supply for differential outputs
48	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal 120kohm pull-up resistor.
49	EPAD	GND	Connect to Ground.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBL08x3. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx				4.6	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2500			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	V_{IN} = V_{DD} , V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–SMBus Parameters

TA = $T_{AMB;}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency			500	kHz	2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2.] The device must be powered up for the SMBus to function.

[3.] The differential input clock must be running for the SMBus to be active

Electrical Characteristics–Input/Supply/Common Output Parameters - Normal Operating Conditions

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	VDDx	Supply voltage for core and analog	3.135	3.3	3.465	V	
Output Supply Voltage	VDDIO	Supply voltage for Low Power HCSL Outputs	0.95	1.05-3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix)	0.75 V_{DDx}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 V_{DDx}	0.5 V_{DDx}	0.6 V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 V_{DDx}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-50		50	uA	
Input Frequency	F_{IN}	Bypass mode	1		200	MHz	2
		PLL mode	90	100.00	160	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1
	C_{OUT}	Output pin capacitance			6	pF	1
CLK_IN Loss of Signal Detect Time	t_{LOS}			4.2	6	ms	1
CLK_IN Loss of Signal Release Time	t_{LOSREL}			0.12	0.5	ms	1
Clk Stabilization	t_{STAB}				1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30	31.5	33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1	2	3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]Control input must be monotonic from 20% to 80% of input swing.

[3]Time from deassertion until outputs are >200 mV

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew rate	dV/dt	Scope averaging on, fast setting	2	2.9	4	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	1.2	2.0	3.1	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching		7	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	777	850	mV	7
Voltage Low	V_{LOW}		-150	-8	150		7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		818	1150	mV	7
Min Voltage	Vmin		-300	-52			7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	385	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		15	140	mV	1,6

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = T_{AMB}, Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDA}	VDDA, PLL Mode, @100MHz		7	10	mA	
	I_{DD}	VDDx, All outputs active @100MHz		20	30	mA	
	I_{DDIO}	VDDIO, All outputs active @100MHz		35	40	mA	
Powerdown Current	I_{DDAPD}	VDDA, CKPWRGD_PD#=0		0.6	1	mA	1
	I_{DDPD}	VDDx, CKPWRGD_PD#=0		3.9	8	mA	1
	I_{DDIOPD}	VDDIO, CKPWRGD_PD#=0		0.04	0.10	mA	1

[1] Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
PLL Bandwidth	BW	-3dB point in High BW Mode (100MHz)	2	3.3	4	MHz	1,5
		-3dB point in Low BW Mode (100MHz)	1	1.5	2	MHz	1,5
PLL Jitter Peaking	t_{JPEAK}	Peak Pass band Gain (100MHz)		0.8	2	dB	1
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode	-1	0.0	1	%	1,3
Skew, Input to Output	t_{pdBYP}	Bypass Mode, V_T = 50%	2500	3440	4500	ps	1
	t_{pdPLL}	PLL Mode V_T = 50%	-100	8	100	ps	1,4
Skew, Output to Output	t_{sk3}	Mean value @100MHz, VT = 50%		29	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		15	50	ps	1,2
		Additive Jitter in Bypass Mode		0.1	1	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

Electrical Characteristics–Unfiltered Phase Jitter Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Additive Phase Jitter, Fanout Mode	$t_{jph156M}$	156.25MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		159		fs (rms)	1,2,3
	$t_{jph156M12k-20}$	156.25MHz, 12kHz to 20MHz, -20dB/decade rollover <12kHz, -40db/decade rolloff > 20MHz		363		fs (rms)	1,2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] DRiven by Rohde&Schartz SMA100

[3] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

Electrical Characteristics–Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limit	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		23	33	86	ps (p-p)	1,2,3,5
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.6	1.0	3	ps (rms)	1,2,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		1.7	2.4	3.1	ps (rms)	1,2,5
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.4	0.50	1	ps (rms)	1,2,5
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.4	0.50	0.5	ps (rms)	1,2,5
Additive Phase Jitter, Bypass mode	$t_{jphPCIeG1-CC}$	PCIe Gen 1		0.09	0.10	n/a	ps (p-p)	1,2,5
	$t_{jphPCIeG2-CC}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.05	0.10		ps (rms)	1,2,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5-16MHz or 8-5MHz, CDR = 5MHz)		0.05	0.10		ps (rms)	1,2,4,5
	$t_{jphPCIeG3-CC}$	PCIe Gen 3 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.05	0.10		ps (rms)	1,2,4,5
	$t_{jphPCIeG4-CC}$	PCIe Gen 4 (PLL BW of 2-4MHz or 2-5MHz, CDR = 10MHz)		0.05	0.10		ps (rms)	1,2,4,5

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.

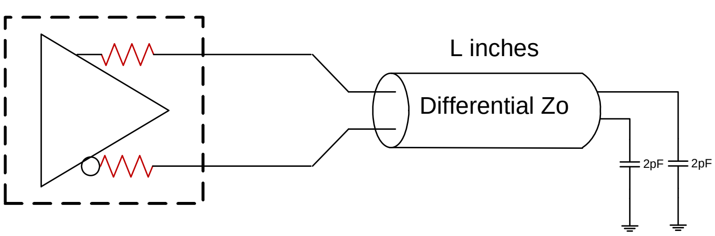
[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS values additive jitter is calculated by solving the following equation for b [*a^2+b^2=c^2*] where a is rms input jitter and c is rms total jitter.

[5] Driven by 9FGL0841 or equivalent

Test Loads

Low-Power push-pull HCSL Output test load
(integrated terminations)



L = 5 inches

Terminations

Device	Zo (Ω)	Rs (Ω)
9DBL0843	100	None needed
9DBL0853	100	7.5
9DBL0843	85	N/A
9DBL0853	85	None needed

Alternate Terminations

The 9DBL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Thermal Characteristics

Parameter	Symbol	Conditions	Package	Typical Value	Units	Notes
Thermal Resistance	θ_{JC}	Junction to Case	NDG48	33	°C/W	1
	θ_{Jb}	Junction to Base		2.1	°C/W	1
	$\theta_{JA0\theta}$	Junction to Air, still air		37	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		30	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		27	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		26	°C/W	1

[1]ePad soldered to board

General SMBus Serial Interface Information for 9DBL08x3

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) sends the byte count = X
- IDT clock will acknowledge
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will acknowledge each byte one at a time
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

NOTE: SMBus Address is Latched on SADR pin. Unless otherwise indicated, default values are for the 0x43, and 0x53. Contact Factory for Quick-turn Customization.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will acknowledge
- Controller (host) sends the beginning byte location = N
- IDT clock will acknowledge
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will acknowledge
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE7	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 6	DIF OE6	Output Enable	RW		Pin Control	1
Bit 5	DIF OE5	Output Enable	RW		Pin Control	1
Bit 4	DIF OE4	Output Enable	RW		Pin Control	1
Bit 3	DIF OE3	Output Enable	RW		Pin Control	1
Bit 2	DIF OE2	Output Enable	RW		Pin Control	1
Bit 1	DIF OE1	Output Enable	RW		Pin Control	1
Bit 0	DIF OE0	Output Enable	RW		Pin Control	1

1. A low on these bits will overide the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	PLLMODERB1	PLL Mode Readback Bit 1	R	See PLL Operating Mode Table		Latch
Bit 6	PLLMODERB0	PLL Mode Readback Bit 0	R			Latch
Bit 5	PLLMODE_SWCNTRL	Enable SW control of PLL Mode	RW	Values in B1[7:6] set PLL Mode	Values in B1[4:3] set PLL Mode	0
Bit 4	PLLMODE1	PLL Mode Control Bit 1	RW[1]	See PLL Operating Mode Table		0
Bit 3	PLLMODE0	PLL Mode Control Bit 0	RW[1]			0
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01= 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF7	Adjust Slew Rate of DIF7	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF6	Adjust Slew Rate of DIF6	RW	Slow Setting	Fast Setting	1
Bit 5	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	Slow Setting	Fast Setting	1
Bit 4	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	Slow Setting	Fast Setting	1
Bit 1	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1

Note: See "Low-Power HCSL Outputs" table for slew rates.

SMBus Table: Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL FB	Adjust Slew Rate of FB	RW	Slow Setting	Fast Setting	1

Byte 4 is Reserved

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	A rev = 0000		0
Bit 6	RID2		R			0
Bit 5	RID1		R			0
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	DeviceID7	Device ID	RW	9DBL0243/0253 = 52 9DBL0443/0453 = 54 9DBL0643/0653 = 56 9DBL0843/0853 = 58		0
Bit 6	Device ID6		RW			1
Bit 5	Device ID5		RW			0
Bit 4	Device ID4		RW			1
Bit 3	Device ID3		RW			X
Bit 2	Device ID2		RW			X
Bit 1	Device ID1		RW			X
Bit 0	Device ID0		RW			X

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved

SMBus Table: PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Power-Down (PD) Restore	Restore Default Config. In PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	Reserved					0
Bit 0	Reserved					0

SMBus Table: Impedance Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	FB_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 6	FB_imp[0]		RW	01=85	11 = Reserved	
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

Note: xx43 = 10, xx53 = 01

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF3_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 6	DIF3_imp[0]		RW	01=85	11 = Reserved	
Bit 5	DIF2_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 4	DIF2_imp[0]		RW	01=85	11 = Reserved	
Bit 3	DIF1_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 2	DIF1_imp[0]		RW	01=85	11 = Reserved	
Bit 1	DIF0_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 0	DIF0_imp[0]		RW	01=85	11 = Reserved	

Note: xx43 = 10, xx53 = 01

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	DIF7_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 6	DIF7_imp[0]		RW	01=85	11 = Reserved	
Bit 5	DIF6_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 4	DIF6_imp[0]		RW	01=85	11 = Reserved	
Bit 3	DIF5_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 2	DIF5_imp[0]		RW	01=85	11 = Reserved	
Bit 1	DIF4_imp[1]	Differential Zout (ohms)	RW	00=33	10=100	see Note
Bit 0	DIF4_imp[0]		RW	01=85	11 = Reserved	

Note: xx43 = 10, xx53 = 01

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE3_pu/pd[1]	OE3 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 6	OE3_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE2_pu/pd[1]	OE2 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 4	OE2_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	OE1_pu/pd[1]	OE1 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 2	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	OE0_pu/pd[1]	OE0 Pull-up(PuP)/ Pull-down(Pdwn) control	RW	00=None	10=Pup	0
Bit 0	OE0_pu/pd[0]		RW	01=Pdwn	11 = Pup+Pdwn	1

Note: These values are for xx43 and xx53.

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	OE7_pu/pd[1]	OE7 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 6	OE7_pu/pd0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 5	OE6_pu/pd[1]	OE6 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 4	OE6_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 3	OE5_pu/pd[1]	OE5 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 2	OE5_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1
Bit 1	OE4_pu/pd[1]	OE4 Pull-up(PuP)/	RW	00=None	10=Pup	0
Bit 0	OE4_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	1

Note: These values are for xx43 and xx53.

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up(PuP)/	RW	00=None	10=Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]	Pull-down(Pdwn) control	RW	01=Pdwn	11 = Pup+Pdwn	0

Note: These values are for xx43 and xx53.

Bytes 17 is Reserved and and reads back 0h00.

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	OE7_polarity	Sets OE7 polarity	RW	Enabled when Low	Enabled when High	0
Bit 6	OE6_polarity	Sets OE6 polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	OE5_polarity	Sets OE5 polarity	RW	Enabled when Low	Enabled when High	0
Bit 4	OE4_polarity	Sets OE4 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE3_polarity	Sets OE3 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	OE2_polarity	Sets OE2 polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 0	OE0_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0

Note: These values are for xx43, and xx53.

SMBus Table: Polarity Control

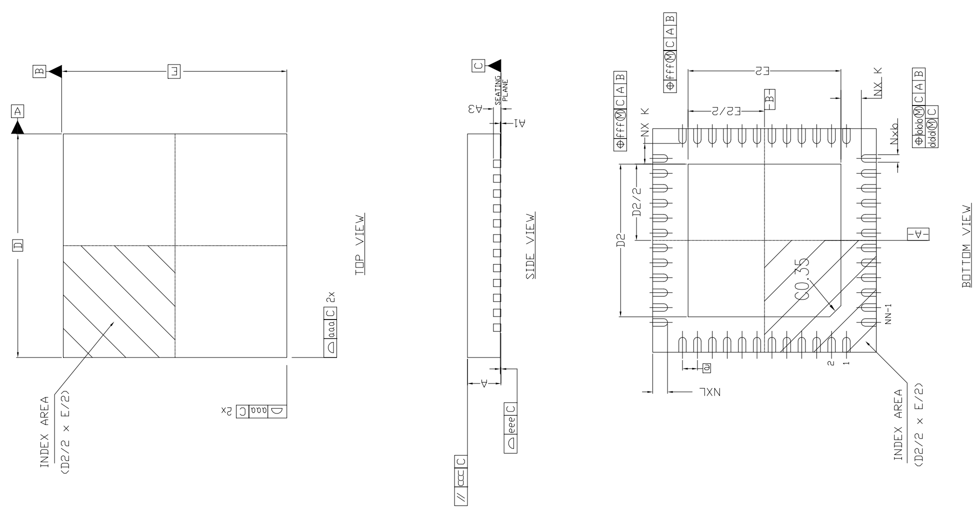
Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					0
Bit 1	LOS Polarity	Determines LOS polarity	RW	Low when input clock is absent	Hi when input clock is absent	1
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power Down when Low	Power Down when High	0

Note: These values are for xx43, and xx53.

Package Outline and Dimensions (NDG48)

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	5/18/16	JH



SYMBOL	MIN	NOM	MAX
D2	3.95	4.10	4.20
E2	3.95	4.10	4.20
L	0.30	0.40	0.50
K		0.55 REF	
D		6.00 BSC	
E		6.00 BSC	
e		0.40 BSC	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3	---	0.20 REF	---
N		48	
ND		12	
NE		12	
b	0.15	0.20	0.25
TOLERANCE of FORM & POSITION			
aaa		0.10	
bbb		0.07	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

TOLERANCES UNLESS SPECIFIED
DECIMAL X± XX± XXX±
ANGULAR ±1°

APPROVALS: DRAWN — DATE 01/11/08; CHECKED

IDT™ www.IDT.com
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TITLE ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY, EPAD 4.10mm SQ
0.40 mm PITCH VFQFN

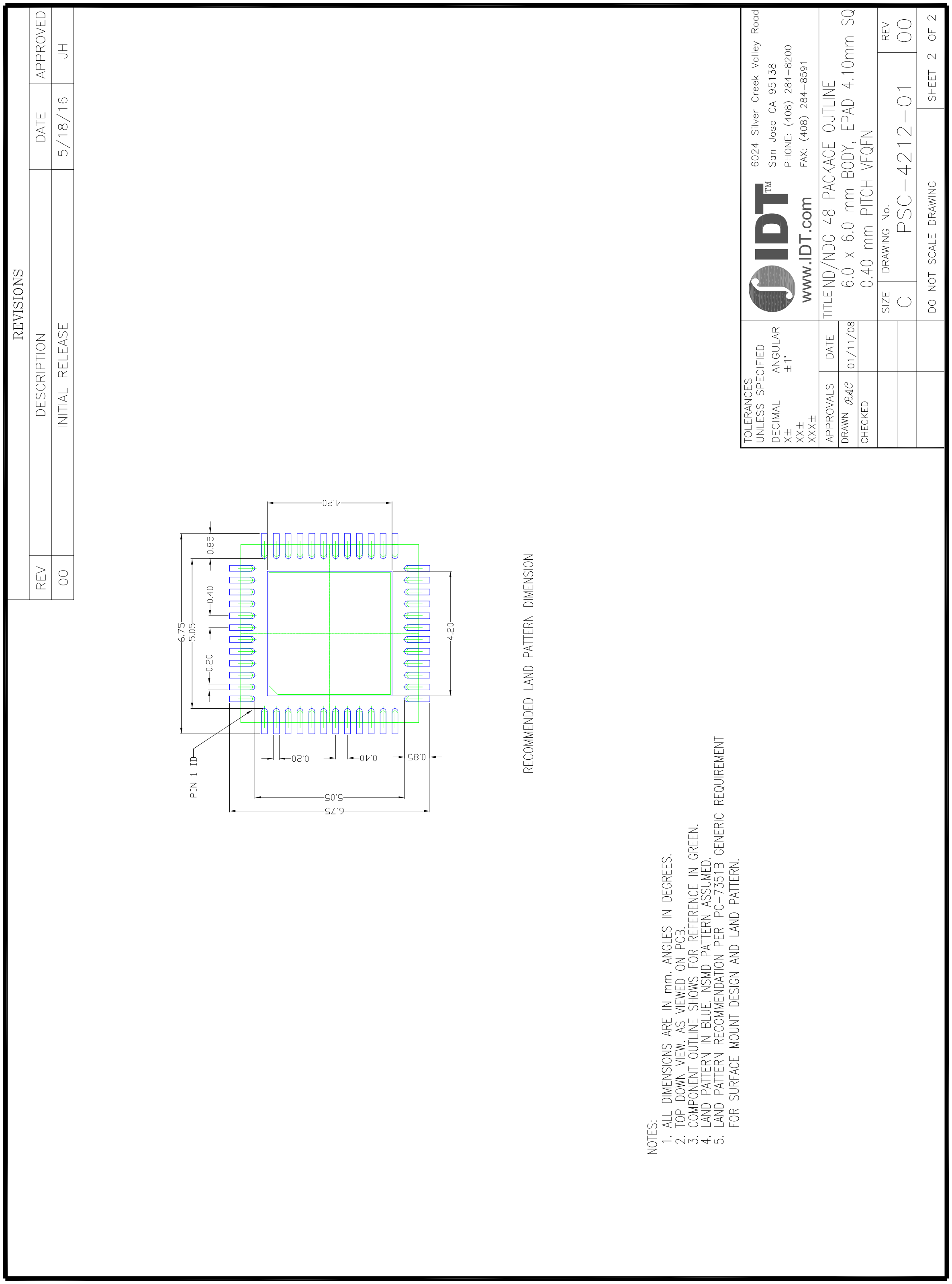
SIZE: C — DRAWING No.: PSC-4212-01 — REV: 00

DO NOT SCALE DRAWING — SHEET 1 OF 2

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

Package Outline and Dimensions (NDG48), cont.



Ordering Information

Part / Order Number	Notes	Shipping Packaging	Package	Temperature
9DBL0843ANDGI	100Ω	Trays	6 × 6 × 0.4 mm 48-VFQFPN	-40 to +85° C
9DBL0843ANDGI8		Tape and Reel	6 × 6 × 0.4 mm 48-VFQFPN	-40 to +85° C
9DBL0853ANDGI	85Ω	Trays	6 × 6 × 0.4 mm 48-VFQFPN	-40 to +85° C
9DBL0853ANDGI8		Tape and Reel	6 × 6 × 0.4 mm 48-VFQFPN	-40 to +85° C

"G" designates PB-free configuration, RoHS compliant.
"A" is the device revision designator (will not correlate with the datasheet revision).

Marking Diagrams

1. "G" denotes RoHS compliant package.
2. "YYWW" denotes the last two digits of the year and week the part was assembled.
3. "$" denotes the mark code.
4. "LOT" denotes the lot number.

Revision History

Revision Date	Description of Change
February 1, 2017	▪ Corrected Byte 16[3:2]. These bits are reserved with '00' default. ▪ Corrected Byte 19[1]. This bit determines the LOS polarity.
January 25, 2017	▪ Corrected ohm symbols and output references in Bytes [11:13], stylistic update only.
December 21, 2016	▪ Extensive updates for consistency and clarity throughout the data sheet. ▪ Update Electrical Tables with characterization data. ▪ Move to final.
August 26, 2016	▪ Initial release

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