5-output 1.8V HCSL Fanout Buffer

9DBV0531

DATASHEET

Description

The 9DBV0531 is a member of IDT's Full-Featured PCIe family. The device has 5 output enables for clock management, and 3 selectable SMBus addresses.

Recommended Application

PCIe Gen1-3 clock distribution in Storage, Networking, Computing, Consumer

Output Features

- 5 - 1-200MHz Low-Power (LP) HCSL DIF pairs
- Easy AC-coupling to other logic families, see IDT application note AN-891

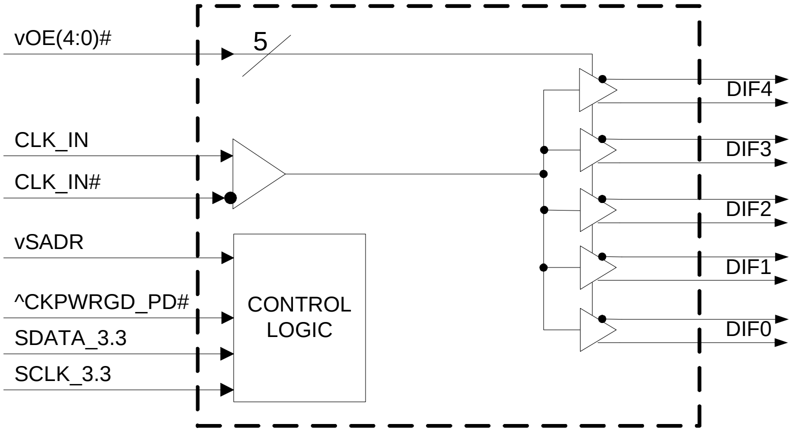
Key Specifications

- *Additive* cycle-to-cycle jitter <5ps
- Output-to-output skew < 50ps
- *Additive* phase jitter is <100fs rms for PCIe Gen3
- *Additive* phase jitter <300fs rms (12kHz-20MHz @125MHz)

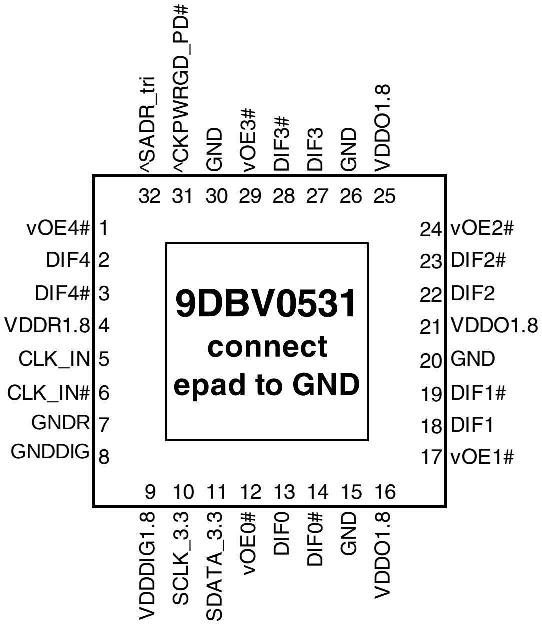
Features/Benefits

- LP-HCSL outputs; save 10 resistors and 17mm^2 compared to standard HCSL
- 50mW typical power consumption; eliminates thermal concerns
- OE# pin for each output; support DIF power management
- HCSL differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- SMBus-selectable features allow optimization to customer requirements
  - Slew rate for each output; allows tuning for various line lengths
  - Differential output amplitude; allows tuning for various application environments
- 1MHz to 200MHz operating frequency
- 3.3V tolerant SMBus interface works with legacy controllers
- Selectable SMBus addresses; multiple devices can easily share an SMBus segment
- Device contains default configuration; SMBus interface not required for device operation
- Space saving 32-pin 5x5mm VFQFPN; minimal board space

Block Diagram



Pin Configuration



32-pin VFQFPN, 5x5 mm, 0.5mm pitch

^ prefix indicates internal 120KOhm pull up resistor

^v prefix indicates internal 120KOhm pull up AND pull down resistor (biased to VDD/2)

v prefix indicates internal 120KOhm pull down resistor

SMBus Address Selection Table

	SADR	Address	+ Read/Write bit
State of SADR on first application of CKPWRGD_PD#	0	1101011	x
	M	1101100	x
	1	1101101	x

Power Management Table

CKPWRGD_PD#	CLK_IN	SMBus OEx bit	OEx# Pin	DIFx	
				True O/P	Comp. O/P
0	X	X	X	Low	Low
1	Running	0	X	Low	Low
1	Running	1	0	Running	Running
1	Running	1	1	Low	Low

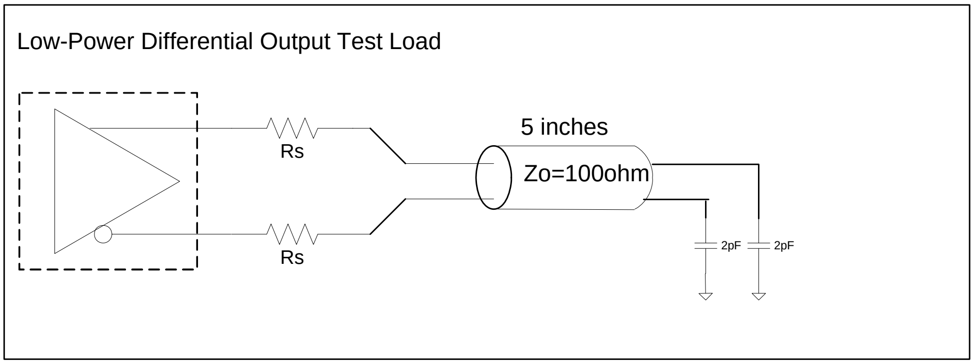
Power Connections

Pin Number		Description
VDD	GND	
4	7	Input receiver analog
9	8	Digital Power
16, 25	15,20,26,30	DIF outputs
21	20	Analog

Pin Descriptions

Pin#	Pin Name	Type	Pin Description
1	vOE4#	IN	Active low input for enabling DIF pair 4. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
2	DIF4	OUT	Differential true clock output
3	DIF4#	OUT	Differential Complementary clock output
4	VDDR1.8	PWR	1.8V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately.
5	CLK_IN	IN	True Input for differential reference clock.
6	CLK_IN#	IN	Complementary Input for differential reference clock.
7	GNDR	GND	Analog Ground pin for the differential input (receiver)
8	GNDDIG	GND	Ground pin for digital circuitry
9	VDDDIG1.8	PWR	1.8V digital power (dirty power)
10	SCLK_3.3	IN	Clock pin of SMBus circuitry, 3.3V tolerant.
11	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
12	vOE0#	IN	Active low input for enabling DIF pair 0. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
13	DIF0	OUT	Differential true clock output
14	DIF0#	OUT	Differential Complementary clock output
15	GND	GND	Ground pin.
16	VDDO1.8	PWR	Power supply for outputs, nominally 1.8V.
17	vOE1#	IN	Active low input for enabling DIF pair 1. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
18	DIF1	OUT	Differential true clock output
19	DIF1#	OUT	Differential Complementary clock output
20	GND	GND	Ground pin.
21	VDDO1.8	PWR	Power supply for outputs, nominally 1.8V.
22	DIF2	OUT	Differential true clock output
23	DIF2#	OUT	Differential Complementary clock output
24	vOE2#	IN	Active low input for enabling DIF pair 2. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
25	VDDO1.8	PWR	Power supply for outputs, nominally 1.8V.
26	GND	GND	Ground pin.
27	DIF3	OUT	Differential true clock output
28	DIF3#	OUT	Differential Complementary clock output
29	vOE3#	IN	Active low input for enabling DIF pair 3. This pin has an internal pull-down. 1 =disable outputs, 0 = enable outputs
30	GND	GND	Ground pin.
31	^CKPWRGD_PD#	IN	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
32	^SADR_tri	LATCHED IN	Tri-level latch to select SMBus Address. It has an internal 120Kohm pull down resistor. See SMBus Address Selection Table.
33	ePAD	GND	Connect epad to ground.

Test Loads



Alternate Differential Output Terminations

Rs	Zo	Units
33	100	Ohms
27	85	

Alternate Terminations

The 9DBV0531 can easily drive LVPECL, LVDS, and CML logic. See “AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs” for details.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBV0531. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Applies to all VDD pins	-0.5		2.5	V	1,2
Input Voltage	V_{IN}		-0.5		V_{DD}+0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins			3.3	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.5V.

Electrical Characteristics–Clock Input Parameters

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	40		60	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	VDDx	Supply voltage for core and analog	1.7	1.8	1.9	V	
Ambient Operating Temperature	T_{COM}	Commmercial range	0	25	70	°C	1
	T_{IND}	Industrial range	-40	25	85	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus	0.75 V_{DD}		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Single-ended tri-level inputs ('_tri' suffix)	0.4 V_{DD}		0.6 V_{DD}	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus	-0.3		0.25 V_{DD}	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	
Input Frequency	F_{in}		1		200	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,6
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock		0.6	1	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable Frequency for PCIe Applications (Triangular Modulation)	30	31.500	33	kHz	
Input SS Modulation Frequency non-PCIe	f_{MODIN}	Allowable Frequency for non-PCIe Applications (Triangular Modulation)	0		66	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	1		3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion		10.000	300	us	1,3
Tfall	t_F	Fall time of single-ended control inputs			5	ns	2
Trise	t_R	Rise time of single-ended control inputs			5	ns	2
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V, see note 4 for V_{DDSMB} < 3.3V			0.8	V	4
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V, see note 5 for V_{DDSMB} < 3.3V	2.1		3.3	V	5
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	
Nominal Bus Voltage	V_{DDSMB}	Bus Voltage	1.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			400	kHz	7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

[4] For V_{DDSMB} < 3.3V, V_{ILSMB} <= $0.35V_{DDSMB}$

[5] For V_{DDSMB} < 3.3V, V_{IHSMB} >= $0.65V_{DDSMB}$

[6] DIF_IN input

[7] The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	dV/dt	Scope averaging on, fast setting	2.3	3.4	4.3	V/ns	1,2,3
	dV/dt	Scope averaging on, slow setting	1.4	2.2	3.1	V/ns	1,2,3
Slew rate matching	ΔdV/dt	Slew rate matching, Scope averaging on		5	20	%	1,2,4
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	774	850	mV	7
Voltage Low	V_{LOW}		-150	0	150		7
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		813	1150	mV	7
Min Voltage	Vmin		-300	-55			7
Vswing	Vswing	Scope averaging off	300	1548		mV	1,2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	250	404	550	mV	1,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		12	140	mV	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Electrical Characteristics–Current Consumption

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Supply Current	I_{DDR}	VDDR @100MHz		2	3	mA	
	I_{DDDIG}	VDDIG, All outputs @100MHz		0.2	0.5	mA	
	I_{DDO}	VDD1.8, All outputs @100MHz		23	27	mA	
Powerdown Current	I_{DDRPD}	VDDR, CKPWRGD_PD# = 0		0.001	0.1	mA	2
	$I_{DDDIGPD}$	VDDDIG, CKPWRGD_PD# = 0		0.17	0.3	mA	2
	I_{DDOPD}	VDD1.8, CKPWRGD_PD# = 0		0.4	0.8	mA	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Duty Cycle Distortion	t_{DCD}	Measured differentially, @100MHz	-1	-0.1	0.5	%	1,3
Skew, Input to Output	t_{pdBYP}	V_T = 50%	1800	2342	3000	ps	1
Skew, Output to Output	t_{sk3}	V_T = 50%		37	50	ps	1,4
Jitter, Cycle to cycle	$t_{jcyc\text{-}cyc}$	*Additive* Jitter		0.1	5	ps	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Electrical Characteristics–Phase Jitter Parameters

TA = T_{COM} or T_{IND}; Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	INDUSTRY LIMIT	UNITS	Notes
Additive Phase Jitter	$t_{jphPCIeG1}$	PCIe Gen 1		0.1	5	N/A	ps (p-p)	1,2,3,5
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.4	N/A	ps (rms)	1,2,3,4,5
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.01	0.4	N/A	ps (rms)	1,2,3,4
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.00	0.1	N/A	ps (rms)	1,2,3,4
	$t_{jphSGMIIM0}$	125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		165	200	N/A	fs (rms)	1,6
	$t_{jphSGMIIM1}$	125MHz, 12kHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz		251	300	N/A	fs (rms)	1,6

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

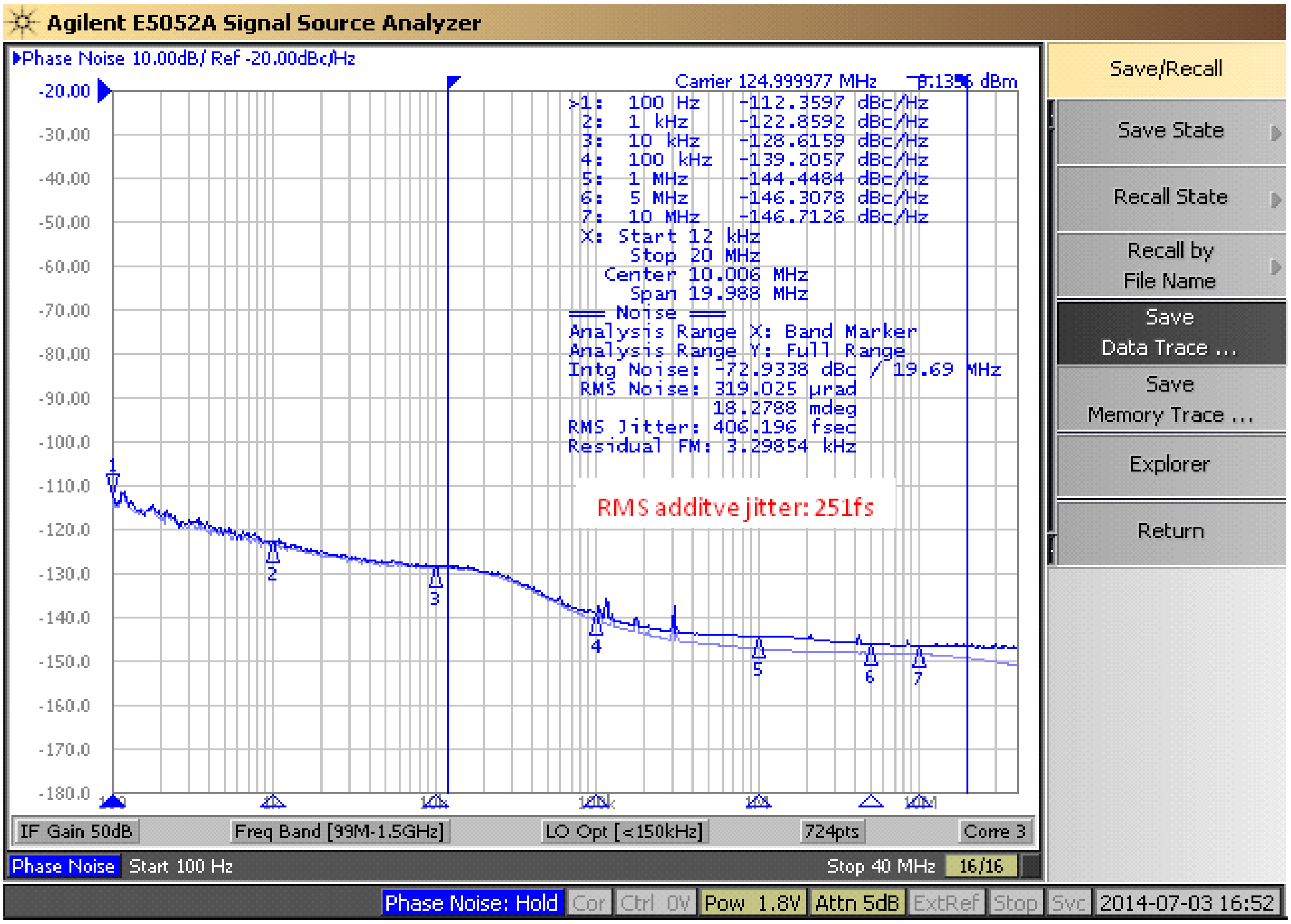
[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

[5] Driven by 9FGV0831 or equivalent

[6] Rohde&Schwarz SMA100

Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



```
Carrier 124.999977 MHz   -[illegible].13[illegible]6 dBm
>1:  100 Hz    -112.3597 dBc/Hz
 2:  1 kHz     -122.8592 dBc/Hz
 3:  10 kHz    -128.6159 dBc/Hz
 4:  100 kHz   -139.2057 dBc/Hz
 5:  1 MHz     -144.4484 dBc/Hz
 6:  5 MHz     -146.3078 dBc/Hz
 7:  10 MHz    -146.7126 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Full Range
Intg Noise: -72.9338 dBc / 19.69 MHz
 RMS Noise: 319.025 µrad
            18.2788 mdeg
RMS Jitter: 406.196 fsec
Residual FM: 3.29854 kHz
```

RMS additve jitter: 251fs

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: SMBus Address is Latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation

Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register [1]

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	DIF OE3	Output Enable	RW	Low/Low	OE# pin control	1
Bit 5	DIF OE2	Output Enable	RW	Low/Low	OE# pin control	1
Bit 4	Reserved					1
Bit 3	DIF OE1	Output Enable	RW	Low/Low	OE# pin control	1
Bit 2	Reserved					1
Bit 1	DIF OE0	Output Enable	RW	Low/Low	OE# pin control	1
Bit 0	Reserved					1

1. A low on these bits will overide the OE# pin and force the differential output Low/Low

SMBus Table: PLL Operating Mode and Output Amplitude Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					1
Bit 5	DIF OE4	Output Enable	RW	Low/Low	OE# pin control	1
Bit 4	Reserved					0
Bit 3	Reserved					1
Bit 2	Reserved					1
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.7V	1
Bit 0	AMPLITUDE 0		RW	10= 0.8V	11 = 0.9V	0

1. A low on the DIF OE bit will overide the OE# pin and force the differential output Low/Low

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	SLEWRATESEL DIF3	Slew Rate Selection	RW	Slow setting	Fast setting	1
Bit 5	SLEWRATESEL DIF2	Slew Rate Selection	RW	Slow setting	Fast setting	1
Bit 4	Reserved					1
Bit 3	SLEWRATESEL DIF1	Slew Rate Selection	RW	Slow setting	Fast setting	1
Bit 2	Reserved					1
Bit 1	SLEWRATESEL DIF0	Slew Rate Selection	RW	Slow setting	Fast setting	1
Bit 0	Reserved					1

SMBus Table: DIF Slew Rate Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					1
Bit 6	Reserved					1
Bit 5	Reserved					0
Bit 4	Reserved					0
Bit 3	Reserved					0
Bit 2	Reserved					1
Bit 1	Reserved					1
Bit 0	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow setting	Fast setting	1

Byte 4 is Reserved and reads back 'hFF

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	**R**	A rev = 0000		0
Bit 6	RID2		**R**			0
Bit 5	RID1		**R**			0
Bit 4	RID0		**R**			0
Bit 3	VID3	VENDOR ID	**R**	0001 = IDT		0
Bit 2	VID2		**R**			0
Bit 1	VID1		**R**			0
Bit 0	VID0		**R**			1

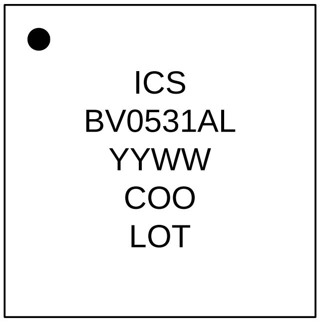
SMBus Table: Device Type/Device ID

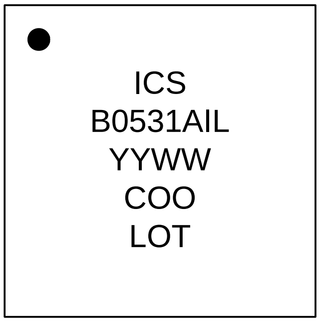
Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	**R**	00 = FGV, 01 = DBV, 10 = DMV, 11= DBV fanout only		1
Bit 6	Device Type0		**R**			1
Bit 5	Device ID5	Device ID	**R**	000101 binary or 05 hex		0
Bit 4	Device ID4		**R**			0
Bit 3	Device ID3		**R**			0
Bit 2	Device ID2		**R**			1
Bit 1	Device ID1		**R**			0
Bit 0	Device ID0		**R**			1

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					0
Bit 6	Reserved					0
Bit 5	Reserved					0
Bit 4	BC4	Byte Count Programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Marking Diagrams





Notes:

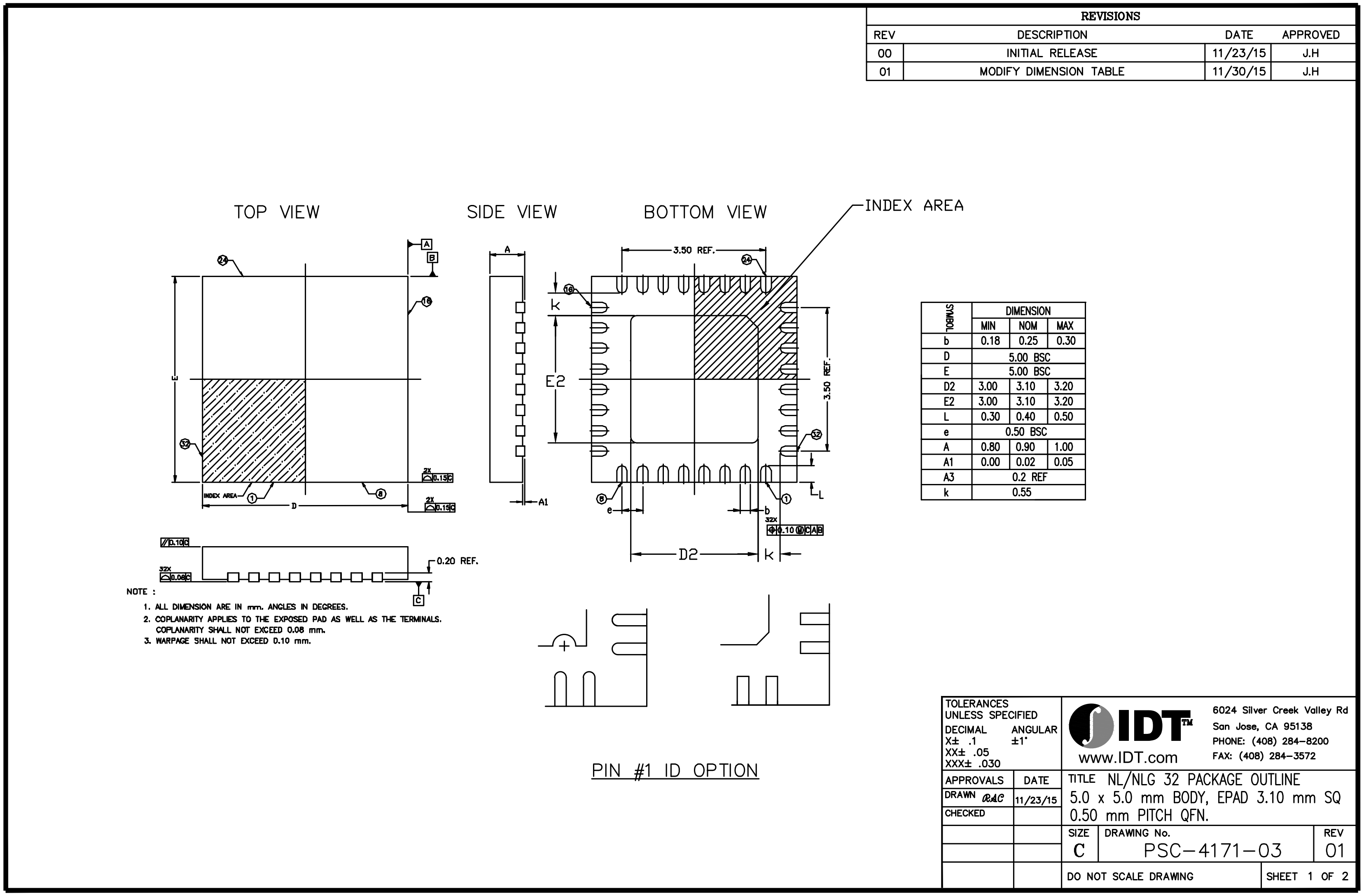
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.

Thermal Characteristics

PARAMETER	SYMBOL	CONDITIONS	PKG	TYP VALUE	UNITS	NOTES
Thermal Resistance	θ_{JC}	Junction to Case	NLG32	42	°C/W	1
	θ_{Jb}	Junction to Base		2.4	°C/W	1
	θ_{JA0}	Junction to Air, still air		39	°C/W	1
	θ_{JA1}	Junction to Air, 1 m/s air flow		33	°C/W	1
	θ_{JA3}	Junction to Air, 3 m/s air flow		28	°C/W	1
	θ_{JA5}	Junction to Air, 5 m/s air flow		27	°C/W	1

[1] ePad soldered to board

Package Outline and Dimensions (NLG32)



REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/23/15	J.H
01	MODIFY DIMENSION TABLE	11/30/15	J.H

SYMBOL	DIMENSION		
	MIN	NOM	MAX
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
D2	3.00	3.10	3.20
E2	3.00	3.10	3.20
L	0.30	0.40	0.50
e		0.50 BSC	
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.2 REF	
k		0.55	

NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

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APPROVALS		DATE
DRAWN	RAC	11/23/15
CHECKED		

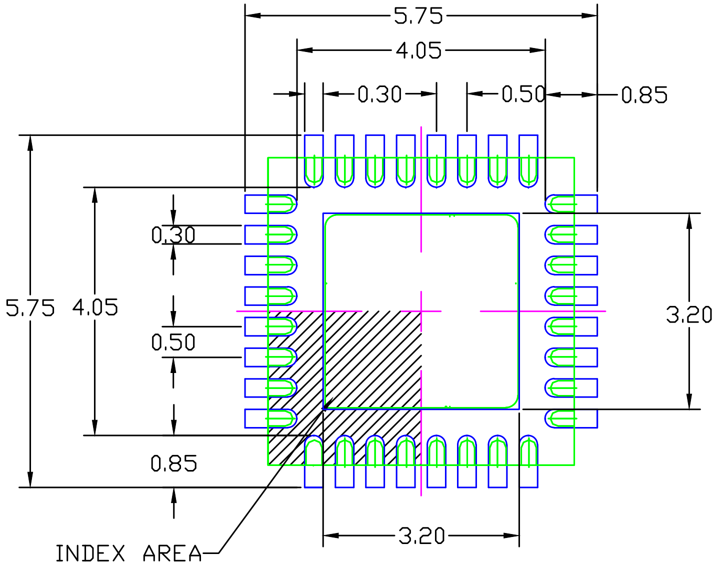
TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY, EPAD 3.10 mm SQ
0.50 mm PITCH QFN.

SIZE	DRAWING No.	REV
C	PSC-4171-03	01

DO NOT SCALE DRAWING
SHEET 1 OF 2

Package Outline and Dimensions (NLG32), cont.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	11/23/15	J.H
01	MODIFY DIMENSION TABLE	11/30/15	J.H



RECOMMENDED LAND PATTERN.

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
X± .1 ±1°
XX± .05
XXX± .030

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APPROVALS	DATE
DRAWN PSCP	12/20/06
CHECKED	

TITLE NL/NLG 32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY, EPAD 3.10 mm SQ
0.50 mm PITCH QFN.

SIZE	DRAWING No.	REV
C	PSC-4171-03	01

DO NOT SCALE DRAWING
SHEET 2 OF 2

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9DBV0531AKLF	Trays	32-pin VFQFPN	0 to +70° C
9DBV0531AKLFT	Tape and Reel	32-pin VFQFPN	0 to +70° C
9DBV0531AKILF	Trays	32-pin VFQFPN	-40 to +85° C
9DBV0531AKILFT	Tape and Reel	32-pin VFQFPN	-40 to +85° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.
“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Initiator	Issue Date	Description	Page #
A	RDW	7/28/2014	1. Updated front page text 2. Updated block diagram 3. Updated electrical tables 4. Updated test loads diagrams. 5. Updated Smbus byte 2, 3 and 6 labeling. Functionality did not change. 6. Move to final.	Various
B	RDW	8/27/2014	1. Updated min Vhigh on DIF outputs from 630mV to 660mV, correcting a typo.	7
C	RDW	8/28/2014	1. Corrected Supply Voltage in Absolute Maximim Ratings. 2. Lowered additive phase jitter specs.	Various
D	RDW	3/28/2016	1. Revised front page text extensively. 2. Added note about Spread Spectrum Compatibility to the features. 3. Change pin names of VDDA1.8 and GNDA to VDDO1.8 and GND, to clarify that this part does not have a PLL. Updated Power Connections table. This is a document change only. There is no silicon change. 4. Corrected OE4# to indicate an internal pull down, not a pull up. 5. Added epad nomenclature to DS 6. Updated package drawing to lastest version - no package change. 7. Replaced LVDS termination info with reference to AN-891 8. Update current consumption table to remove references to VDDA1.8 9. Added "RMS additive phase jitter: 251fs" to phase noise plot 10. Updated "Clock Input Parameters" table for consistency - no silicon change. 11. Updated "Output Duty Cycle, Jitter, Skew and PLL Characteristics" and "Phase Jitter" tables to remove references to bypass mode.	1-5,7,9 14
E	RDW	5/23/2016	Updated POD drawings with the latest from Doc Control	14,15

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