Description

The 9FGL0641 / 9FGL0651 devices are 3.3V members of IDT's 3.3V Full-Featured PCIe family. The devices have 6 output enables for clock management and support 2 different spread spectrum levels in addition to spread off. The 9FGL0641 / 9FGL0651 supports PCIe Gen1–4 Common Clocked architectures (CC), PCIe Separate Reference no-Spread (SRnS) and Separate Reference Independent Spread (SRIS) clocking architectures.

Typical Applications

- Servers/High-Performance Computing/Accelerators
- Storage
- Embedded Systems/Industrial Control

Output Features

- Six 100MHz Low-Power HCSL (LP-HCSL) DIF pairs:
  - 9FGL0641 default Zo = 100Ω
  - 9FGL0651 default Zo = 85Ω
- One 3.3V LVCMOS REF output with Wake-On-LAN (WOL) support
- See AN-891 for easy AC-coupling to other logic families

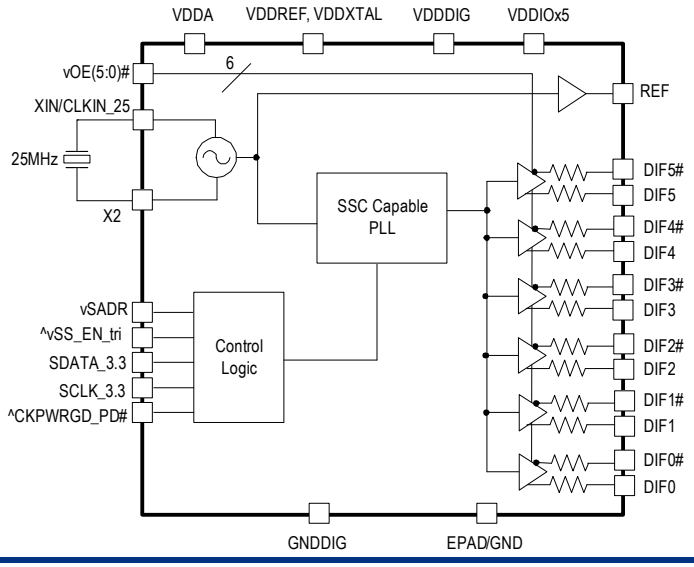
Key Specifications

- PCIe Gen1–4 CC compliant; Gen2–3 SRIS compliant
- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 50ps
- DIF 12kHz–20MHz phase jitter is < 2ps rms when SSC is off
- REF phase jitter is < 150fs rms; SSC off
- ±100ppm frequency accuracy on all clocks

Features

- Direct connection to loads saves 24 resistors compared to standard PCIe devices
- 188mW typical power consumption at 3.3V
- V_{DDIO} rail allows 30% power savings at optional 1.05V
- SMBus-selectable features allows optimization to customer requirements:
  - Control input polarity
  - Control input pull-up/pull-down
  - Slew rate for each output
  - Differential output amplitude
  - 33Ω, 85Ω or 100Ω output impedance for each output
- Devices contain default configuration; SMBus not required
- Contact factory for customized versions
- 25MHz input frequency
- OE# pins; support DIF power management
- Pin-selectable SRnS, CC 0% and CC/SRIS -0.5% spread
- SMBus-selectable CC/SRIS -0.25% spread
- Clean switching between the CC/SRIS spread settings
- DIF outputs blocked until PLL is locked; clean system start-up
- 2 selectable SMBus addresses
- Space saving 5 × 5 mm 40-VFQFPN package

Block Diagram



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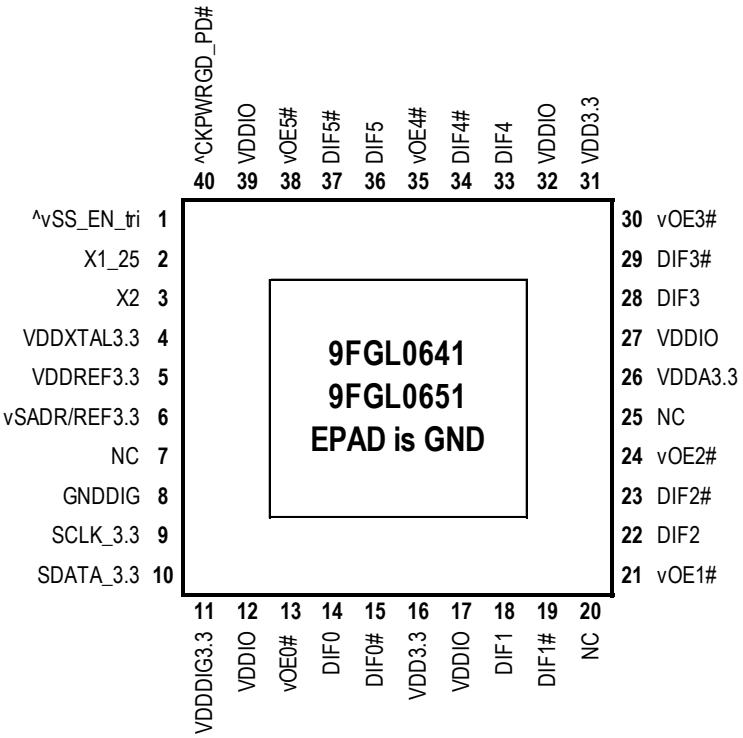
Pin Assignment

Figure 1. Pin Assignments for 5 × 5 mm 40-VFQFPN Package – Top View



40-VFQFPN, 5 x 5 mm, 0.4mm pitch

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

^v prefix indicates internal 120kOhm pull-up and pull-down resistors

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	^vSS_EN_tri	Latched In	Latched select input to select spread spectrum amount at initial power up. See Spread Selection table.
2	X1_25	Input	Crystal input. Nominally 25.00MHz.
3	X2	Output	Crystal output.
4	VDDXTAL3.3	Power	Power supply for XTAL. Nominally 3.3V.
5	VDDREF3.3	Power	V_{DD} for REF output. Nominally 3.3V.
6	vSADR/REF3.3	Latched I/O	Latch to select SMBus address; 3.3V LVCMOS copy of X1/REFIN pin.
7	NC	—	No Connection.
8	GNDDIG	GND	Ground pin for digital circuitry.
9	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
10	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
11	VDDDIG3.3	Power	3.3V digital power (dirty power).
12	VDDIO	Power	Power supply for differential outputs.
13	vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
14	DIF0	Output	Differential true clock output.
15	DIF0#	Output	Differential complementary clock output.
16	VDD3.3	Power	Power supply. Nominally 3.3V.
17	VDDIO	Power	Power supply for differential outputs.
18	DIF1	Output	Differential true clock output.
19	DIF1#	Output	Differential complementary clock output.
20	NC	—	No Connection.
21	vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
22	DIF2	Output	Differential true clock output.
23	DIF2#	Output	Differential complementary clock output.
24	vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
25	NC	—	No Connection.
26	VDDA3.3	Power	3.3V power for the PLL core.
27	VDDIO	Power	Power supply for differential outputs.
28	DIF3	Output	Differential true clock output.
29	DIF3#	Output	Differential complementary clock output.
30	vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
31	VDD3.3	Power	Power supply. Nominally 3.3V.
32	VDDIO	Power	Power supply for differential outputs.
33	DIF4	Output	Differential true clock output.
34	DIF4#	Output	Differential complementary clock output.
35	vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
36	DIF5	Output	Differential true clock output.
37	DIF5#	Output	Differential Complementary clock output.
38	vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
39	VDDIO	Power	Power supply for differential outputs.
40	^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
41	EPAD	GND	Connect to ground.

Table 2. Spread Selection

^vSS_EN_tri Pin	B1[4:3]	Spread%	Note
0	00	0	PCIe SRNS mode.
—	01	-0.25	PCIe Common Clock or SRIS mode.
M (V_{DD}/2)	10	0	PCIe Common Clock or SRIS mode.
1	11	-0.50	PCIe Common Clock or SRIS mode.

If SRnS mode is desired, power up with ^vSS_EN_tri = '0'. Do not attempt to switch to the other modes via SMBus control in Byte 1. If Common Clock (CC) or SRIS mode is desired, power up with ^vSS_EN_tri at either 'M' or '1'. The desired spread spectrum amount can then be selected via Byte 1 without a requiring a system reset. Once 'M' or '1' is latched at power up, do not attempt to enter SRNS mode or a system reset will be required.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGL0641 / 9FGL0651 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Units	Notes
3.3V Supply Voltage	V_{DDxx}	Applies to V_{DD}, V_{DDA} and V_{DDIO}, if present.	-0.5	4.6	V	1,2
Input Voltage	V_{IN}		-0.5	V_{DD} + 0.5	V	1,3
Input High Voltage, SMBus	V_{IHSMB}	SMBus clock and data pins.		3.9	V	1
Storage Temperature	Ts		-65	150	°C	1
Junction Temperature	Tj			125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500		V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 4.6V.

Thermal Characteristics

Table 4. Thermal Characteristics

Symbol	Parameter	Package	Typical Values	Units	Notes
θ_{JC}	Junction to case.	NDG40	42	°C/W	1
θ_{Jb}	Junction to base.		2.4	°C/W	1
θ_{JA0}	Junction to air, still air.		39	°C/W	1
θ_{JA1}	Junction to air, 1 m/s air flow.		33	°C/W	1
θ_{JA3}	Junction to air, 3 m/s air flow.		28	°C/W	1
θ_{JA5}	Junction to air, 5 m/s air flow.		27	°C/W	1

[1] EPAD soldered to board.

Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 5. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V.			0.8	V	
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V.	2.1		3.6	V	
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	
SCLK/SDATA Rise Time	t_{RSMB}	(Max. V_{IL} - 0.15V) to (Min. V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min. V_{IH} + 0.15V) to (Max. V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{SMB}	SMBus operating frequency.			500	kHz	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] The device must be powered up for the SMBus to function.

Table 6. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDxxx}	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V	
IO Supply Voltage	V_{DDIO}	Supply voltage for differential low power outputs.	0.9975	1.05–3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus.	0.75 × V_{DDx}		V_{DDx} + 0.3	V	
Input Low Voltage	V_{IL}		-0.3		0.25 × V_{DDx}	V	
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix).	0.75 × V_{DDx}		V_{DDx} + 0.3	V	
Input Mid Voltage	V_{IMtri}		0.4 × V_{DDx}	0.5 x V_{DDx}	0.6 × V_{DDx}	V	
Input Low Voltage	V_{ILtri}		-0.3		0.25 × V_{DDx}	V	6
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-50		50	µA	
Input Frequency	F_{IN}	XTAL or X1 input.		25		MHz	4
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{OUT}	Output pin capacitance.			6	pF	1
CLK Stabilization	t_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.		0.3	1.8	ms	1,2
SS Modulation Frequency	f_{MOD}	Triangular modulation.	30	31.6	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1	2	3	clocks	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion.		28	300	µs	1,3
Fall Time	t_F	Fall time of single-ended control inputs.			5	ns	1,2
Rise Time	t_R	Rise time of single-ended control inputs.			5	ns	1,2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] Contact the factory for other frequencies.

Table 7. DIF Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	Trf	Scope averaging on, fast setting.	2	2.7	4	V/ns	2,3
		Scope averaging, slow setting.	1	1.9	3	V/ns	2,3
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	250	409	550	mV	1,4,5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		14	140	mV	1,4,9
Avg. Clock Period Accuracy	T_{PERIOD_AVG}		-100	0.0	+2600	ppm	2,10,13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread spectrum modulation.	9.9491	10.0	10.1011	ns	2,6
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$			16	50	ps	2
Voltage High	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	761	850	mV	1
Voltage Low	V_{LOW}		-150	-7	150	mV	1
Absolute Maximum Voltage	V_{MIN}	Measurement on single-ended signal using absolute value (scope averaging off).		819	1150	mV	1,7,15
Absolute Minimum Voltage	V_{MAX}		-300	-46			1,8,15
Duty Cycle	t_{DC}		45	49	55	%	2
Slew Rate Matching	ΔTrf	Single-ended measurement.		6	20	%	1,14
Skew, Output to Output	t_{sk3}	Averaging on, V_T = 50%.		12	50	ps	2

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 8.6.2 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors C_L. Single-ended probes must be used for measurements requiring single ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2pF.

[12] PCIe Gen1–4 specify ±300ppm frequency tolerances. The 9FGL0xxx devices already meet the tighter ±100ppm frequency tolerances proposed for PCIe Gen5 and required by most servers.

[13] “ppm” refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default SMBus amplitude settings.

Table 8. DIF LP-HCSL Output Unfiltered Phase Jitter Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Phase Jitter, 12kHz–20MHz	$t_{jph12k20M}$	100MHz outputs with REF output enabled, SSC off.		1.9	2	ps (rms)

Table 9. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDAOP}	V_{DDA}, all outputs active at 100MHz.		14	17	mA	
	I_{DDOP}	All other V_{DD}, except V_{DDA} and V_{DDIO}, all outputs active at100MHz.		16	20	mA	
	I_{DDIOOP}	V_{DDIO}, all outputs active at100MHz.		27	32	mA	
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	V_{DDA}, DIF outputs off, REF output running.		0.9	1.1	mA	1
	I_{DDPD}	All other V_{DD}, except V_{DDA} and V_{DDIO}, DIF outputs off, REF output running.		6.0	7.6	mA	1
	I_{DDIOOP}	V_{DDIO}, DIF outputs off, REF output running.		0.04	0.05	mA	1
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	V_{DDA}, all outputs off.		0.9	1.1	mA	
	I_{DDPD}	All other V_{DD}, except V_{DDA} and V_{DDIO}, all outputs off.		1.8	2.2	mA	
	I_{DDIOOP}	V_{DDIO}, all outputs off.		0.04	0.08	mA	

[1] This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 10. Filtered Phase Jitter Parameters - PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter	$t_{jphPCIeG1-CC}$	PCIe Gen1.		17	29	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.4	0.58	3	ps (rms)	1,2
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		1.1	1.58	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.3	0.36	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.3	0.36	0.5	ps (rms)	1,2

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev 4.0 version 1.0. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

Table 11. Filtered Phase Jitter Parameters - PCIe Separate Reference Independent Spread (SRIS) Architectures [3]

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	Phase Jitter – 0.25% spread	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.7	0.73	2	ps (rms)	1,2
		PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.4	0.42	0.7	ps (rms)	1,2
	Phase Jitter – 0.5% spread	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.7	0.73	2	ps (rms)	1,2
		PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.6	0.63	0.7	ps (rms)	1,2

[1] Applies to all outputs.

[2] Based on PCIe Base Specification Rev3.1a. These filters are different than Common Clocked filters. See http://www.pcisig.com for latest specifications.

[3] Per PCIe Base Specification Rev4.0 version 1.0, SRIS is not currently defined for Gen1 or Gen4.

Table 12. REF Output

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Long Accuracy	ppm	See Tperiod min-max values.		0		ppm	1,2
Clock Period	T_{period}	REF output.		40		ns	2
High Output Voltage	V_{HIGH}	I_{OH} = -2mA.	0.8 × V_{DDREF}			V	
Low Output Voltage	V_{LOW}	I_{OL} = 2mA.			0.2 × V_{DDREF}	V	
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 1F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}.	0.5	0.9	1.5	V/ns	1
	t_{rf1}	Byte 3 = 5F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}.	1.0	1.5	2.5	V/ns	1,3
	t_{rf1}	Byte 3 = 9F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}.	1.5	2.1	3.1	V/ns	1
	t_{rf1}	Byte 3 = DF, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}.	2.0	2.7	3.8	V/ns	1
Duty Cycle	d_{t1X}	V_T = V_{DD}/2 V.	45	49.7	55	%	1,4
Duty Cycle Distortion	d_{tcd}	V_T = V_{DD}/2 V.	-1	0	0	%	1,5
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	V_T = V_{DD}/2 V.		35	125	ps	1,4
Noise Floor	t_{jdBc1k}	1kHz offset.		-145	-135	dBc	1,4
	$t_{jdBc10k}$	10kHz offset to Nyquist.		-150	-140	dBc	1,4
Jitter, Phase	t_{jphREF}	12kHz to 5MHz, DIF SSC off.		0.13	0.3	ps (rms)	1,4

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.

[3] Default SMBus value.

[4] When driven by a crystal.

[5] When driven by an external oscillator via the X1 pin, X2 should be floating.

Power Management

Table 13. Power Management [3]

CKPWRGD_PD#	SMBus OE bit	OEx# Pin	DIF		REF
			True O/P	Comp. O/P	
0	X	X	Low [1]	Low [1]	Hi-Z [2]
1	1	0	Running	Running	Running
1	1	1	Disabled [1]	Disabled [1]	Running
1	0	X	Disabled [1]	Disabled [1]	Disabled [4]

[1] The output state is set by B11[1:0] (Low/Low default).

[2] REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5] = 1, in which case REF is running.

[3] Input polarities defined at default values for 9FGL0641/0651.

[4] See SMBus description for Byte 3, bit 4.

Table 14. SMBus Address Selection

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

Table 15. Power Connections

Pin Number			Description
V_{DD}	V_{DDIO}	GND	
4		41	XTAL OSC.
5		41	REF power.
11		8	Digital (dirty) power.
	12, 17, 27, 32, 39	41	DIF outputs.
26		41	PLL analog.

Test Loads

Figure 2. Single-ended Output Test Load

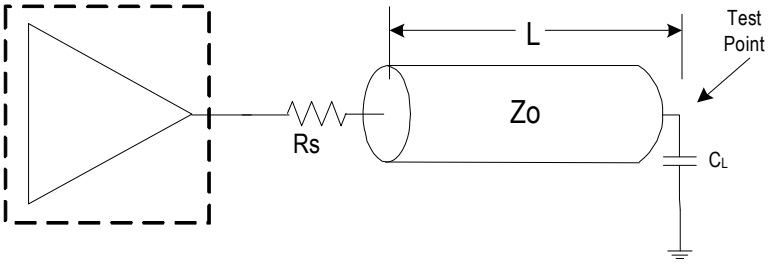


Figure 3. Low-Power HCSL Output Test Load (standard PCIe source-terminated test load)

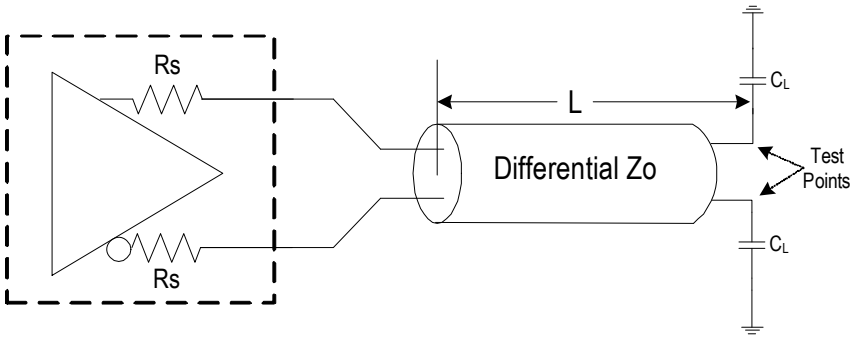


Figure 4. Test Setup for PCIe Jitter Measurements

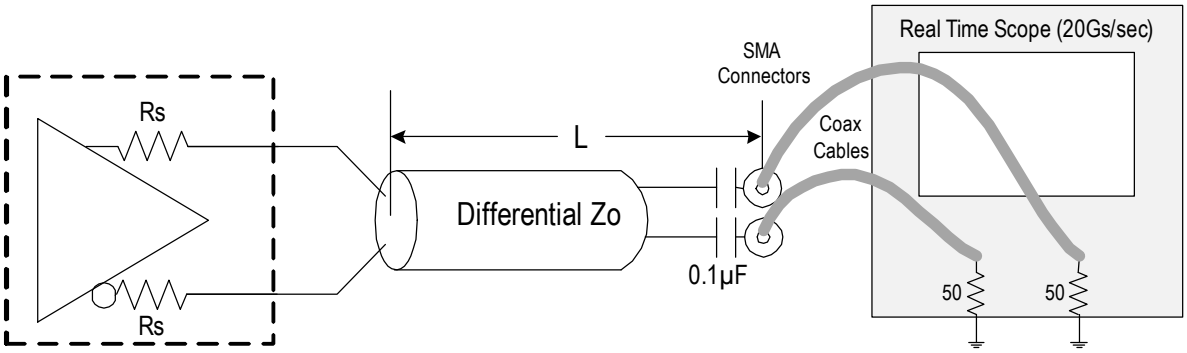


Table 16. Terminations

Device	L (inches)	Zo (Ω)	Rs (Ω)	REF C_L (pF)	DIF C_L (pF)
9FGL0641	5	100	None needed	4.7	2
9FGL0651	5	100	7.5		
9FGL0641	5	85	N/A		
9FGL0651	5	85	None needed		

Alternate Terminations

The 9FGL family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for details.

Crystal Characteristics

Table 17. Recommended Crystal Characteristics

Parameter	Value	Units
Frequency	25MHz	MHz
Resonance Mode	Fundamental	—
Frequency Tolerance @ 25°C	±20	ppm maximum
Frequency Stability, reference at 25°C over operating temperature range	±20	ppm maximum
Temperature Range (industrial)	-40 to +85	°C
Temperature Range (commercial)	0 to +70	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: Unless otherwise indicated, default values are for the 0641, and 0651. Read/Write Address is latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: Output Enable Register

Byte 0	Name	Control Function	Type	0	1	Default
Bit 7	DIF OE5	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 6	DIF OE4	Output Enable	RW		Pin Control	1
Bit 5	Reserved					X
Bit 4	DIF OE3	Output Enable	RW	See B11[1:0]	Pin Control	1
Bit 3	DIF OE2	Output Enable	RW		Pin Control	1
Bit 2	DIF OE1	Output Enable	RW		Pin Control	1
Bit 1	Reserved					X
Bit 0	DIF OE0	Output Enable	RW	See B11[1:0]	Pin Control	1

[1] A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default).

SMBus Table: Spread Spectrum and V_{HIGH} Control Register

Byte 1	Name	Control Function	Type	0	1	Default
Bit 7	SSENRB1	SS Enable Readback Bit1	R	See Spread Selection table.		Latch
Bit 6	SSENRB1	SS Enable Readback Bit0	R			Latch
Bit 5	SSEN_SWCNTRL	Enable SW control of SS	RW	SS controlled by latch (B1[7:6]).	Values in B1[4:3] control SS amount.	0
Bit 4	SSENSW1	SS Enable Software Ctl Bit1	RW[1]	See Spread Selection table.		0
Bit 3	SSENSW0	SS Enable Software Ctl Bit0	RW[1]			0
Bit 2	Reserved					X
Bit 1	AMPLITUDE 1	Controls Output Amplitude	RW	00 = 0.6V	01 = 0.68V	1
Bit 0	AMPLITUDE 0		RW	10 = 0.75V	11 = 0.85V	0

[1] See notes on Spread Selection table. B1[5] must be set to a 1 in order to use B1[4:3].

SMBus Table: DIF Slew Rate Control Register

Byte 2	Name	Control Function	Type	0	1	Default
Bit 7	SLEWRATESEL DIF5	Adjust Slew Rate of DIF5	RW	Slow Setting	Fast Setting	1
Bit 6	SLEWRATESEL DIF4	Adjust Slew Rate of DIF4	RW	Slow Setting	Fast Setting	1
Bit 5	Reserved					X
Bit 4	SLEWRATESEL DIF3	Adjust Slew Rate of DIF3	RW	Slow Setting	Fast Setting	1
Bit 3	SLEWRATESEL DIF2	Adjust Slew Rate of DIF2	RW	Slow Setting	Fast Setting	1
Bit 2	SLEWRATESEL DIF1	Adjust Slew Rate of DIF1	RW	Slow Setting	Fast Setting	1
Bit 1	Reserved					X
Bit 0	SLEWRATESEL DIF0	Adjust Slew Rate of DIF0	RW	Slow Setting	Fast Setting	1

Note: See DIF Low-Power HCSL Outputs table for slew rates.

SMBus Table: Nominal V_{HIGH} Amplitude Control / REF Control Register

Byte 3	Name	Control Function	Type	0	1	Default
Bit 7	REF	Slew Rate Control	RW	00 = Slowest	01 = Slow	0
Bit 6			RW	10 = Fast	11 = Faster	1
Bit 5	REF Power Down Function	Wake-on-Lan Enable for REF	RW	REF disabled in Power Down	REF runs in Power Down	0
Bit 4	REF OE	REF Output Enable	RW	Disabled [1]	Enabled	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

[1] The disabled state depends on Byte11[1:0]. '00' = Low, '01' = Hi-Z, '10' = Low, '11' = High.

Byte 4 is Reserved.

SMBus Table: Revision and Vendor ID Register

Byte 5	Name	Control Function	Type	0	1	Default
Bit 7	RID3	Revision ID	R	C rev = 0010		0
Bit 6	RID2		R			0
Bit 5	RID1		R			1
Bit 4	RID0		R			0
Bit 3	VID3	VENDOR ID	R	0001 = IDT		0
Bit 2	VID2		R			0
Bit 1	VID1		R			0
Bit 0	VID0		R			1

SMBus Table: Device Type/Device ID

Byte 6	Name	Control Function	Type	0	1	Default
Bit 7	Device Type1	Device Type	R	00 = FGx, 01 = DBx, 10 = DMx, 11 = DBx w/oPLL		0
Bit 6	Device Type0		R			0
Bit 5	Device ID5	Device ID	R	000100 binary or 06 hex		0
Bit 4	Device ID4		R			0
Bit 3	Device ID3		R			0
Bit 2	Device ID2		R			1
Bit 1	Device ID1		R			1
Bit 0	Device ID0		R			0

SMBus Table: Byte Count Register

Byte 7	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	BC4	Byte count programming	RW	Writing to this register will configure how many bytes will be read back, default is = 8 bytes.		0
Bit 3	BC3		RW			1
Bit 2	BC2		RW			0
Bit 1	BC1		RW			0
Bit 0	BC0		RW			0

Bytes 8 and 9 are Reserved.

SMBus Table: PLL MN Enable, PD_Restore

Byte 10	Name	Control Function	Type	0	1	Default
Bit 7	PLL M/N En [1]	M/N Programming Enable	RW	M/N Prog. Disabled	M/N Prog. Enabled	0
Bit 6	Power-Down (PD) Restore	Restore Default Config in PD	RW	Clear Config in PD	Keep Config in PD	1
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	Reserved					X

[1] This bit is a '1' on 9FGL0xP1 devices.

SMBus Table: Stop State Control

Byte 11	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	STP[1]	True/Complement DIF Output Disable State	RW	00 = Low/Low	10 = High/Low	0
Bit 0	STP[0]		RW	01 = HiZ/HiZ	11 = Low/High	0

SMBus Table: Impedance Control

Byte 12	Name	Control Function	Type	0	1	Default
Bit 7	DIF2_imp[1]	DIF2 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	See Note
Bit 6	DIF2_imp[0]	DIF2 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	
Bit 5	DIF1_imp[1]	DIF1 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	
Bit 4	DIF1_imp[0]	DIF1 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	DIF0_imp[1]	DIF0 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	See Note
Bit 0	DIF0_imp[0]	DIF0 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	

SMBus Table: Impedance Control

Byte 13	Name	Control Function	Type	0	1	Default
Bit 7	DIF5_imp[1]	DIF5 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	See Note
Bit 6	DIF5_imp[0]	DIF5 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	
Bit 5	DIF4_imp[1]	DIF4 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	
Bit 4	DIF4_imp[0]	DIF4 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	DIF3_imp[1]	DIF3 Zout	RW	00 = 33Ω DIF Zout	10 = 100Ω DIF Zout	See Note
Bit 0	DIF3_imp[0]	DIF3 Zout	RW	01 = 85Ω DIF Zout	11 = Reserved	

SMBus Table: Pull-up Pull-down Control

Byte 14	Name	Control Function	Type	0	1	Default
Bit 7	OE2_pu/pd[1]	OE2 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 6	OE2_pu/pd[0]		RW	01=Pdwn	11 = Pup + Pdwn	1
Bit 5	OE1_pu/pd[1]	OE1 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 4	OE1_pu/pd[0]		RW	01=Pdwn	11 = Pup + Pdwn	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	OE0_pu/pd[1]	OE0 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 0	OE0_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 15	Name	Control Function	Type	0	1	Default
Bit 7	OE5_pu/pd[1]	OE5 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 6	OE5_pu/pd[0]		RW	01=Pdwn	11 = Pup + Pdwn	1
Bit 5	OE4_pu/pd[1]	OE4 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 4	OE4_pu/pd[0]		RW	01=Pdwn	11 = Pup + Pdwn	1
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	OE3_pu/pd[1]	OE3 Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	0
Bit 0	OE3_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	1

SMBus Table: Pull-up Pull-down Control

Byte 16	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	CKPWRGD_PD_pu/pd[1]	CKPWRGD_PD Pull-up (PuP)/ Pull-down (Pdwn) control	RW	00 = None	10 = Pup	1
Bit 0	CKPWRGD_PD_pu/pd[0]		RW	01 = Pdwn	11 = Pup + Pdwn	0

Byte 17 is Reserved.

SMBus Table: Polarity Control

Byte 18	Name	Control Function	Type	0	1	Default
Bit 7	OE5_polarity	Sets OE5 polarity	RW	Enabled when Low	Enabled when High	0
Bit 6	OE4_polarity	Sets OE4 polarity	RW	Enabled when Low	Enabled when High	0
Bit 5	Reserved					X
Bit 4	OE3_polarity	Sets OE3 polarity	RW	Enabled when Low	Enabled when High	0
Bit 3	OE2_polarity	Sets OE2 polarity	RW	Enabled when Low	Enabled when High	0
Bit 2	OE1_polarity	Sets OE1 polarity	RW	Enabled when Low	Enabled when High	0
Bit 1	Reserved					X
Bit 0	OE1_polarity	Sets OE0 polarity	RW	Enabled when Low	Enabled when High	0

SMBus Table: Polarity Control

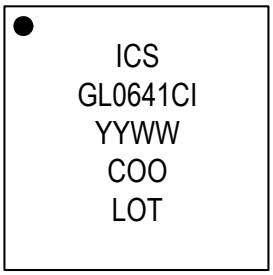
Byte 19	Name	Control Function	Type	0	1	Default
Bit 7	Reserved					X
Bit 6	Reserved					X
Bit 5	Reserved					X
Bit 4	Reserved					X
Bit 3	Reserved					X
Bit 2	Reserved					X
Bit 1	Reserved					X
Bit 0	CKPWRGD_PD	Determines CKPWRGD_PD polarity	RW	Power-down when Low	Power-down when High	0

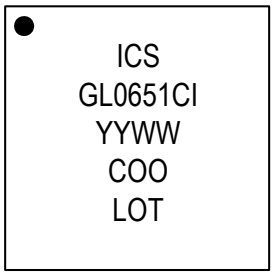
Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/ndndg40-package-outline-50-x-50-mm-bodyepad-350mm-sq-040-mm-pitch-qfn

Marking Diagrams





1. Lines 1 and 2: truncated part number.
2. “I” denotes industrial temperature range.
3. “YYWW” is the last two digits of the year and the week the part was assembled.
4. “COO” denotes country of origin.
5. “LOT” denotes sequential lot number.

Ordering Information

Table 18. Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature	Output Impedance
9FGL0641CKILF	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Trays	-40° to +85°C	100Ω
9FGL0641CKILFT	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Reel	-40° to +85°C	
9FGL0651CKILF	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Trays	-40° to +85°C	85Ω
9FGL0651CKILFT	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Reel	-40° to +85°C	

“LF” denotes Pb-free configuration, RoHS compliant.
“C” is the device revision designator (will not correlate with the datasheet revision)

Revision History

Revision Date	Description of Change
September 18, 2018	▪ Updated Output to Output Skew typical value. ▪ Updated Phase Jitter, -0.5% Spread typical and maximum values.
September 4, 2018	Initial release.

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