9FGS9093

Clock Generator for P9 Systems

The 9FGS9093 is a simple, cost-effective, very high-performance clock generator supporting P9 and Open Power systems. It provides four low-jitter, 133 1/3MHz LP-HCSL outputs with or without spread spectrum.

Applications

- 1, 2, 3, and 4 socket P9 and Open Power systems

Key Specifications

- DIF cycle-to-cycle jitter < 50ps
- DIF output-to-output skew < 100ps
- OUT[3:0] phase jitter: 313ps rms (12kHz–20MHz) with SSC off
- OUT[3:0] phase jitter is PCIe Gen1–3 with SSC on/off
- REF phase jitter: 190fs rms

Features

- 3.3V power supply; easy power supply hookup
- OE[B:A] pins allow different power states
- 85Ω output impedance; eliminates up to 16 resistors and eases board routing
- Configuration selected via strapping pins or I^2C; I^2C interface not required for device control
- 350mW power consumption at 3.3V; reduces thermal concerns
- I^2C address is 0b1101011x, where x is the write/read bit
- 4 × 4 mm 24-VFQFPN; minimal board space

Output Features

- Four Low-Power HCSL (LP-HCSL) spread spectrum capable outputs at 133 1/3MHz
- Two 3.3V LVCMOS REF outputs at 33 1/3MHz

Block Diagram

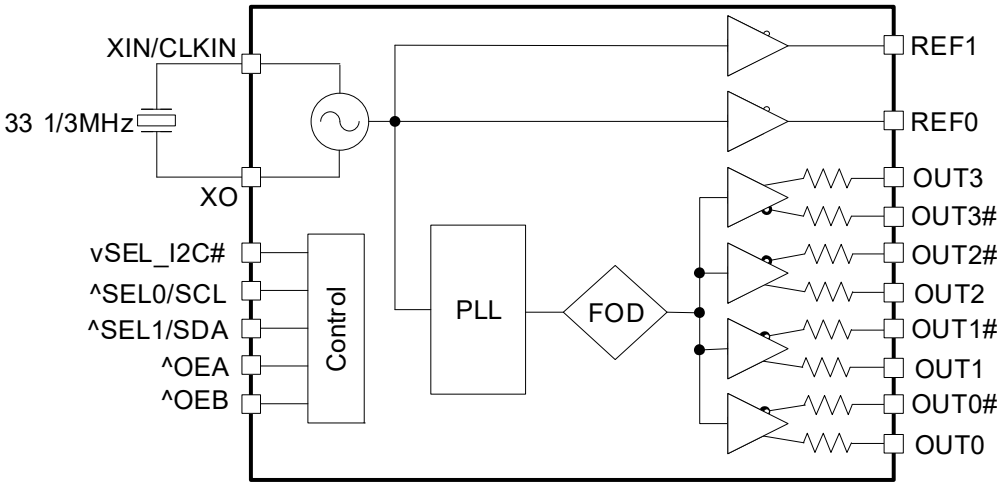


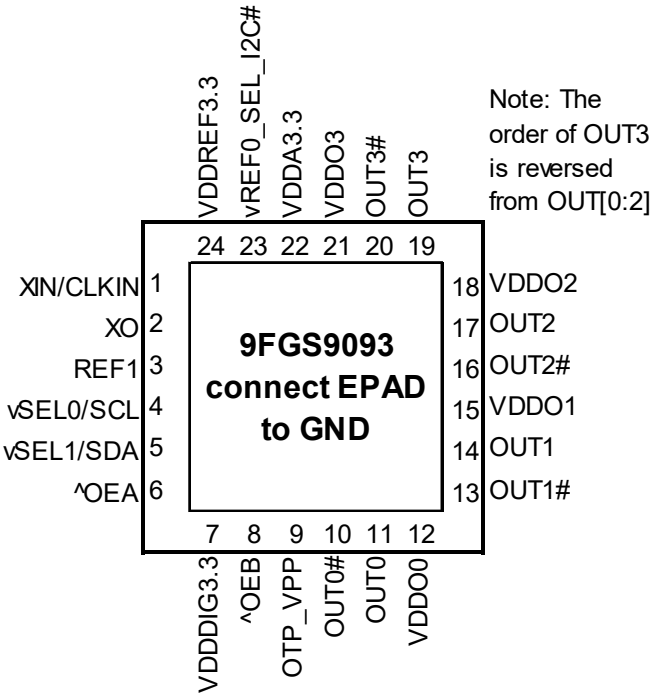
Table 1. OE Mapping

OE[B:A]	OUT0	OUT1	OUT2	OUT3	REF0	REF1
00	Running	Low/Low	Low/Low	Low/Low	Running	Running
01	Running	Running	Low/Low	Low/Low	Running	Running
10	Running	Running	Running	Low/Low	Running	Running
11	Running	Running	Running	Running	Running	Running

Contents

1. Pin Information

1.1 Pin Assignments



4 x 4 mm 24-VFQFPN, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

1.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	XIN/CLKIN	Input	Crystal input or reference clock input.
2	XO	Output	Crystal output.
3	REF1	Output	LVCMOS reference output.
4	vSEL0/SCL	Input	Select pin for internal frequency configurations/I^{2}C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
5	vSEL1/SDA	I/O	Select pin for internal frequency configurations/I^{2}C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-down.
6	^OEA	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
7	VDDDIG3.3	Power	3.3V digital power (dirty power).
8	^OEB	Input	Active high input for enabling outputs. This pin has an internal pull-up resistor. 0 = disable outputs, 1 = enable outputs.
9	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V_{DDD}.
10	OUT0#	Output	Complementary output clock 0.
11	OUT0	Output	Output clock 0.

Pin Number	Pin Name	Type	Description
12	VDDO0	Power	Power supply for output 0.
13	OUT1#	Output	Complementary output clock 1.
14	OUT1	Output	Output clock 1.
15	VDDO1	Power	Power supply for output 1.
16	OUT2#	Output	Complementary output clock 2.
17	OUT2	Output	Output clock 2.
18	VDDO2	Power	Power supply for output 2.
19	OUT3	Output	Output clock 3.
20	OUT3#	Output	Complementary output clock 3.
21	VDDO3	Power	Power supply for output 3.
22	VDDA3.3	Power	3.3V power for the PLL core.
23	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as a LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1, 0 = SCL/SDA.
24	VDDREF3.3	Power	Power supply for REF output, nominally 3.3V.
25	EPAD	GND	Connect to ground.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.465V
Storage Temperature, T_{STG}	-65°C to 150°C
Junction Temperature	125°C
XIN/REF Input	0V to 1.2V voltage swing
Other Inputs	-0.5V to V_{DDD}
LVCMOS Outputs	-0.5V to V_{DDO} + 0.5V
I/O (SDA) Output	10mA

2.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2000	V

2.3 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DDOX}	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	3.135	3.3	3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply if available.	3.135	3.3	3.465	V
T_A	Operating temperature, ambient.	-40		85	°C
C_{LOAD_OUT}	Maximum load capacitance (33.33MHz XTAL).			8	pF
F_{IN}	External reference crystal.		33 1/3		MHz
t_{PU}	Power up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05		5	ms

2.4 Thermal Specifications

Symbol	Parameter	Value	Unit
θ_{JC}	Junction to case.	61.7	°C/W
θ_{Jb}	Junction to base.	5.4	°C/W
θ_{JA0}	Junction to air, still air.	50.1	°C/W
θ_{JA1}	Junction to air, 1 m/s air flow.	43.1	°C/W
θ_{JA3}	Junction to air, 3 m/s air flow.	40.7	°C/W
θ_{JA5}	Junction to air, 5 m/s air flow.	37.7	°C/W

2.5 Electrical Specifications

V_{DDX} = 3.3V ±5%, T_A = -40°C to +85°C unless stated otherwise. T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Table 2. Input Capacitance, LVCMOS Output Impedance, and Internal Pull-down Resistance

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Capacitance (OEA, OEB, SEL1/SDA, SEL0/SCL, REF0_SEL_I2C#)	C_{IN}	-	3	7	pF
Pull-up or Pull-down Resistor (OEA, OEB, SEL1/SDA, SEL0/SCL, REF0_SEL_I2C#)	R_{PD} R_{PU}	100	-	300	kΩ
LVCMOS Output Driver Impedance (V_{DDO} = 1.8V, 2.5V, 3.3V)	R_{OUT}	-	17	-	Ω
Programmable Capacitance at XIN/CLKIN and XO (X1 in parallel with X2)	XIN/CLKIN, XO	-	8	-	pF

Table 3. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Core Supply Current [1]	I_{DDCORE}	133.333MHz on all outputs, 33.33MHz REFCLK, SSC on.	-	29	35	mA
Output Buffer Supply Current	I_{DDO}	LP-HCSL, 133.333MHz, total V_{DDO} current, SSC on. [2]	-	51	61	mA
		REF, 33.33MHz, V_{DDREF}. [2][3]	-	7	8	mA
		OE[B:A] = 00, SSC on. [2]	-	22	26	mA

1. $I_{DDCORE} = I_{DDA} + I_{DDD}$.
2. See Test Loads.
3. Both REF active, includes XO current.

Table 4. DC Electrical Characteristics for Single-ended Inputs and Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Output High Voltage	V_{OH}	I_{OH} = -15mA.	2.4	3.1	V_{DDO}	V
Output Low Voltage	V_{OL}	I_{OL} = 15mA.		0.22	0.4	V
Output Leakage Current (OUT[3:0])	I_{OZDD}	Tri-state outputs, V_{DDO} = 3.465V.	-5		5	µA
Output Leakage Current (REF[1:0])	I_{OZDD}	Tri-state outputs, V_{DDREF} = 3.465V.	-5		5	µA
Input High Voltage	V_{IH}	Single-ended inputs – OE[B:A], SEL1/SDA, SEL0/SCL.	0.7 x V_{DDDIG}		V_{DDDIG} + 0.3	V
Input Low Voltage	V_{IL}	Single-ended inputs – OE[B:A], SEL1/SDA, SEL0/SCL.	GND - 0.3		0.8	V
Input High Voltage	V_{IH}	Single-ended input REF0_SEL_I2C#.	2		V_{DDREF} + 0.3	V
Input Low Voltage	V_{IL}		GND - 0.3		0.4	V
Input High Voltage	V_{IHxin}	Single-ended input – XIN/CLKIN.	0.8		1.2	V
Input Low Voltage	V_{ILxin}		GND - 0.3		0.4	V
Input Rise/Fall Time	t_R/t_F	OE[B:A], SEL1/SDA, SEL0/SCL.			300	ns

Table 5. OUTx Differential Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate [1][2][3]	dV/dt	Scope averaging on.	2	2.65	4	V/ns
Slew Rate Matching [1][2][3]	ΔdV/dt	Scope averaging on.	-	7	20	%
Voltage High [4][5]	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	780	850	mV
Voltage Low [4]	V_{LOW}		-150	20	150	mV
Maximum Voltage	$V_{MAXIMUM}$	Measurement on single-ended signal using absolute value (scope averaging off).	-	803	1150	mV
Minimum Voltage	$V_{MINIMUM}$		-300	-54	-	mV
Crossing Voltage Value [1][4][6]	V_{CROSS}	Scope averaging off.	250	447	550	mV
Crossing Voltage Variation [1][7]	ΔV_{CROSS}	Scope averaging off.	-	16	140	mV

1. Confirmed by design and characterization. Not 100% tested in production.
2. Measured from differential waveform.
3. Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a ±150mV window around differential 0V.
4. Measured from single-ended waveform.
5. Measured with scope averaging off, using statistics function. Variation is difference between minimum and maximum.
6. V_{CROSS} defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
7. The total variation of all Vcross measurements in any particular system. Note that this is a subset of V_{CROSS} minimum/maximum (V_{CROSS} absolute) allowed. The intent is to limit Vcross induced modulation by setting ΔV_{CROSS} to be smaller than V_{CROSS} absolute.

Table 6. AC Timing Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input Frequency	f_{IN}	Input frequency (XIN/CLKIN).	-	33 1/3	-	MHz
Output Frequency	f_{OUT}	REF clock (LVCMOS).	-	33 1/3	-	MHz
		OUTx clock (LP-HCSL).	-	133 1/3	-	MHz
Input Duty Cycle	t2	Duty cycle. [1]	45	50	55	%
Output Duty Cycle	t3	OUT[3:0], outputs.[1]	45	50.3	55	%
		REF[1:0], outputs. [1]	45	49.7	55	%
Slew Rate	t5	LVCMOS REF output (20% to 80% of V_{DDREF}) V_{DDREF} = 3.3V. [1]	2.5	3.4	4.5	V/ns
Cycle-to-Cycle Jitter	t6	OUT[3:0] across all frequency configurations. [1]	-	23	55	ps
		REF[1:0] across all frequency configurations. [1]	-	20	30	ps
Output-to-Output Skew	t7	OUT[3:0]. [1]	-	36	55	ps
Lock Time	t8	PLL lock time from power-up. [2][3]	-	4.5	10	ms

1. Confirmed by design and characterization. Not 100% tested in production.
2. Includes loading the configuration bits from EPROM to PLL registers. It does not include EPROM program minimum/write time.
3. Actual PLL lock time depends on the loop configuration.

Table 7. Phase Jitter Specifications – OUT[3:0]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
GbE Random Jitter (12kHz–20MHz) [1]	JGbE	OUT[3:0] SSC OFF. See Table 10 for Configurations.	-	313	375	fs (rms)

1. Confirmed by design and characterization.

Table 8. Phase Jitter Specifications – REF[1:0]

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Noise Floor [1]	t_{jdBc1k}	1kHz offset.	-	-138	-130	dBc
Noise Floor [1]	$t_{jdBc10k}$	10kHz offset to Nyquist.	-	-152	-145	dBc
Jitter, Phase [1]	t_{jphREF}	12kHz to 5MHz.	-	190	275	fs (rms)

1. Confirmed by design and characterization.

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limits	Unit
Phase Jitter Peak-to-Peak	$t_{jphPCIeG1-CC}$	PCIe Gen1. [1][2][3][4]	-	19	36	86	ps (p-p)
Phase Jitter RMS	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz <f <1.5MHz (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). [1][2][3][4]	-	0.45	1.0	3	ps (rms)
Phase Jitter RMS		PCIe Gen2 High Band 1.5MHz <f <Nyquist (50MHz) (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). [1][2][3][4]	-	1.6	3.1	3.1	ps (rms)
Phase Jitter RMS	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz). [1][2][3][4]	-	0.4	0.7	1	ps (rms)

1. Applies to all differential outputs, guaranteed by design and characterization.
2. Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.
3. Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.
4. Jitter is from the PCIe jitter filter combination that produces the highest jitter and includes spread spectrum where applicable.

Table 10. Test Frequencies for Jitter Measurements

CFG [1:0] (SEL[1:0])	XTAL In/ REF Out	OUT0	OUT1	OUT2	OUT3	Unit
00	33 1/3	133 1/3 SSC on at -0.5%				MHz
01	33 1/3	133 1/3 SSC Off				

Table 11. Spread Spectrum Generation Specifications

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Mod. Frequency	f_{MOD}	See Table 10 for configurations using spread spectrum.	30	31.465	33	kHz
Spread Percent – Down Spread	Spread%			-0.496	-0.5	%

3. Test Loads

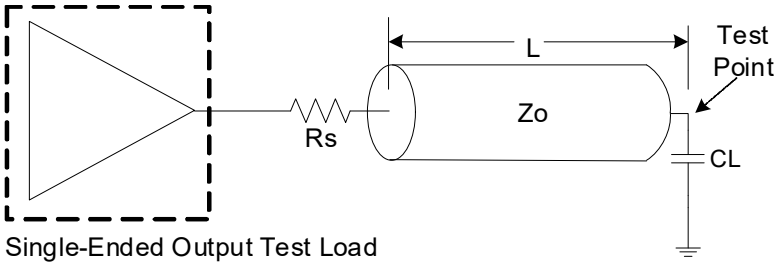


Figure 1. Single-Ended Output Test Load

Table 12. Parameters for Single-Ended Output Test Load

Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
33	50	12	4.7

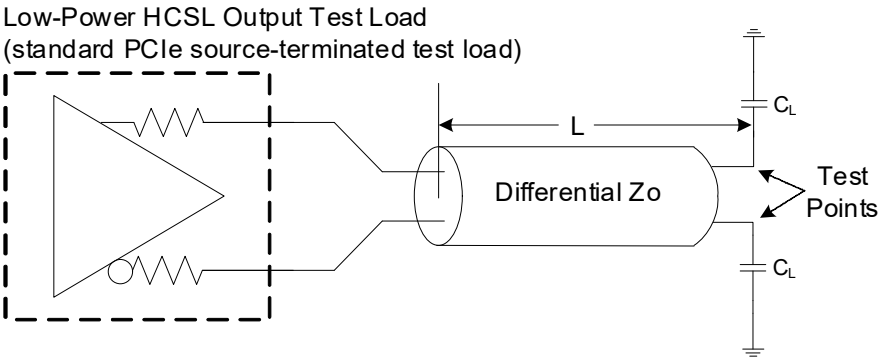


Figure 2. Low-Power HCSL Output Test Load

Table 13. Parameters for Low-Power HCSL Output Test Load

Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
Internal	85	12	2
7.5	100	12	2

4. I²C Bus Characteristics

Table 14. I²C Bus DC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Input High Level	V_{IH}	-	0.7 x V_{DDDIG}	-	-	V
Input Low Level	V_{IL}	-	-	-	0.3 x V_{DDDIG}	V
Hysteresis of Inputs	V_{HYS}	-	0.05 x V_{DDDIG}	0.16 x V_{DDDIG}		V
Input Leakage Current	I_{IN}	-	-1	7.4	30	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA.	-	-	0.4	V

Table 15. I²C Bus AC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Serial Clock Frequency (SCL)	F_{SCLK}	-	10		400	kHz
Bus Free Time between STOP and START	t_{BUF}	-	1.3	0.06	-	µs
Setup Time, START	$t_{SU:START}$	-	0.6	0.02	-	µs
Hold Time, START	$t_{HD:START}$	-	0.6	0.03	-	µs
Setup Time, Data Input (SDA)	$t_{SU:DATA}$	-	0.1	0.01	-	µs
Hold Time, Data Input (SDA)	$t_{HD:DATA}$	-	0	-0.06	-	µs
Output Data Valid from Clock	t_{OVD}	-	-	0.40	0.9	µs
Capacitive Load for Each Bus Line	C_B	-	-	-	400	pF
Rise Time, Data and Clock (SDA, SCL)	t_R	-	20 + 0.1 x C_B	-	300	ns
Fall Time, Data and Clock (SDA, SCL)	t_F	-	20 + 0.1 x C_B	-	300	ns
High Time, Clock (SCL)	t_{HIGH}	-	0.6	-	-	µs
Low Time, Clock (SCL)	t_{LOW}	-	1.3	-	-	µs
Setup Time, STOP	$t_{SU:STOP}$	-	0.6	-	-	µs

Note: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

5. Crystal Characteristics

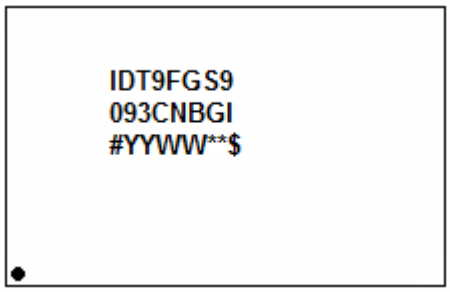
Table 16. Recommended Crystal Characteristics

Parameter	Value	Unit
Frequency	33 1/3	MHz
Resonance Mode	Fundamental	-
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, REF at 25°C Over Operating Temperature Range	±20	ppm maximum
Temperature Range (commercial)	0 to 70	°C
Temperature Range (industrial)	-40 to 85	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

6. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagram



- Lines 1 and 2: part number
  - "G" denotes RoHS compliant package.
  - "I" denotes industrial temperature range.
- Line 3:
  - "#" denotes stepping number.
  - "YWW" denotes the last digit of the year and work week the part was assembled.
  - "**" denotes the lot sequence number.
  - "$" denotes mark code.

8. Ordering Information

Part Number	Package Description	Carrier Type	Temperature Range
9FGS9093CNBGI	4 × 4 mm, 0.50mm pitch 24-VFQFPN	Tray	-40 to +85°C
9FGS9093CNBGI8		Tape & Reel	

"G" indicates Pb-free configuration, RoHS compliant.

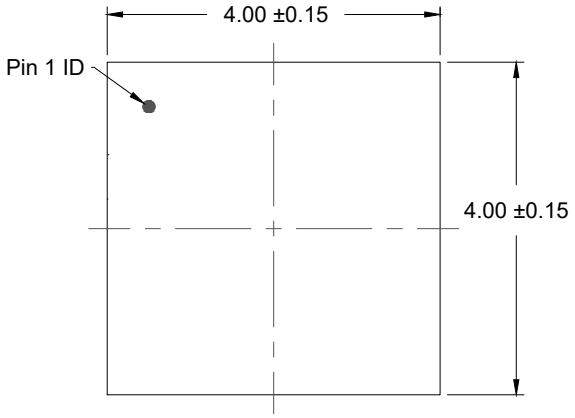
"C" is the device revision designator (will not correlate with the datasheet revision).

9. Revision History

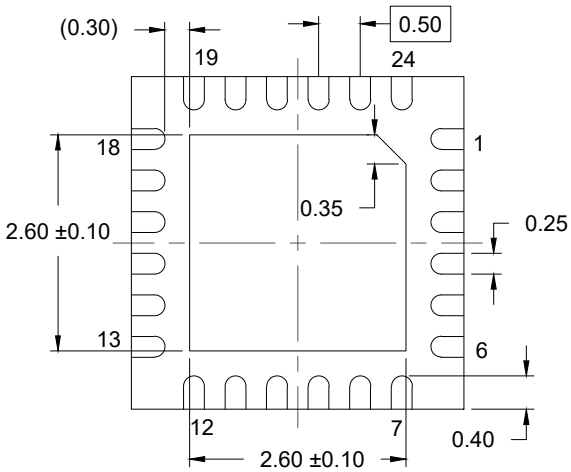
Revision	Date	Description
1.04	Mar 29, 2022	▪ Updated Ordering Information part number from 9FGS9093**A**NBGI/8 to 9FGS9093**C**NBGI/8. ▪ Updated pins 4 and 5 in Pin Descriptions to reflect a pull-down resistor. ▪ Updated Pin Assignments drawing to reflect pins 4 and 5 have a pull-down resistor. ▪ Updated Marking Diagram. ▪ Reformatted datasheet to the latest template.
1.03	Oct 9, 2020	Reformatted to Renesas.
1.02	Jan31, 2018	▪ Updated drive level parameter in Crystal Characteristics table. ▪ Updated Package Outline Drawings text and added hyperlink to document.
1.01	Jun 14, 2017	▪ Updated Current Consumption LP-HCSL values to 51mA typical and 61mA maximum. ▪ Changed packaging carrier type from "Tubes" to "Tray".
1.00	Apr 5, 2017	Initial release.

Package Outline Drawing

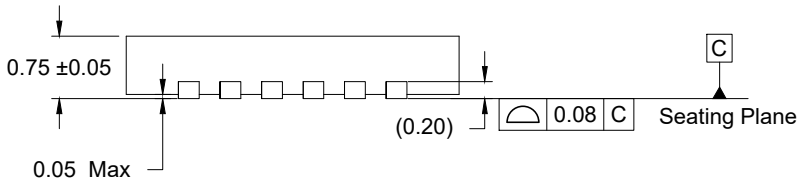
Package Code:NBG24P2
24-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.50 mm Pitch
PSC-4313-02, Revision: 03, Date Created: Jul 20, 2023



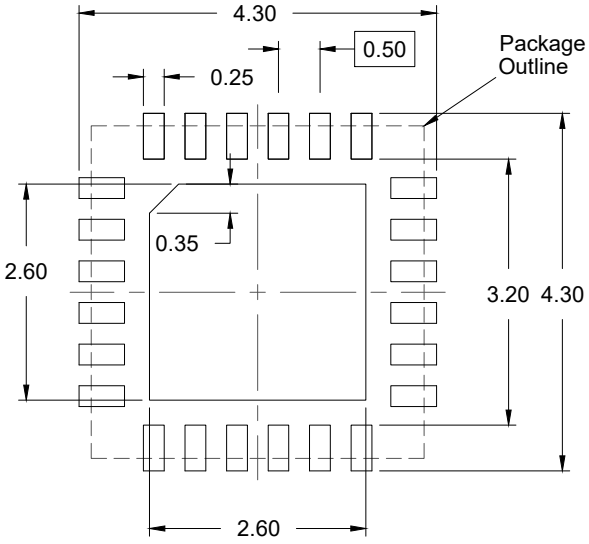
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use o any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.