Low Phase-Noise, Low-Power Programmable PhiClock™ Generator

9FGV1005C
Datasheet

Description

The 9FGV1005C is a member of the Renesas PhiClock™ programmable clock generator family. The 9FGV1005C provides two copies of a single non-spread spectrum output frequency and one copy of the crystal reference input. Two select pins allow for hardware selection of the desired configuration, or two I^2C bits allow easy software selection of the desired configuration. The user may configure any one of the four OTP configurations as the default when operating in I^2C mode. Four unique I^2C addresses are available, allowing easy I^2C access to multiple components.

Typical Applications

- HPC
- Storage
- 10G/25G Ethernet
- Fiber Optic Modules
- SSDs
- NVLink

Output Features

- 1 integer output frequency per configuration
- 2 programmable output pairs plus 1 LVCMOS REF output
- 1MHz–325MHz LVDS or LP-HCSL outputs
- 1MHz–200MHz LVCMOS outputs

Features

- 1.8V–3.3V operation
- Individual 1.8V–3.3V V_{DDO} for each programmable output pair
- Supports HCSL, LVDS and LVCMOS I/O standards
- Supports LVPECL and CML logic with easy AC coupling – see application note AN-891 for alternate terminations
- HCSL utilizes Renesas' LP-HCSL technology for improved performance, lower power and higher integration:
  - Programmable output impedance of 85Ω or 100Ω
- On-board OTP supports up to 4 complete configurations
- Configuration selected via strapping pins or I^2C
- < 100mW at 1.8V, < 200mW at 3.3V (LP-HCSL outputs running at 100MHz)
- 4 programmable I^2C addresses: D0/D1, D2/D3, D4/D5, D6/D7 read/write
- Supported by Renesas Timing Commander™ software
- 3 × 3 mm 16-LGA with integrated crystal option (9FGV1005CQ)

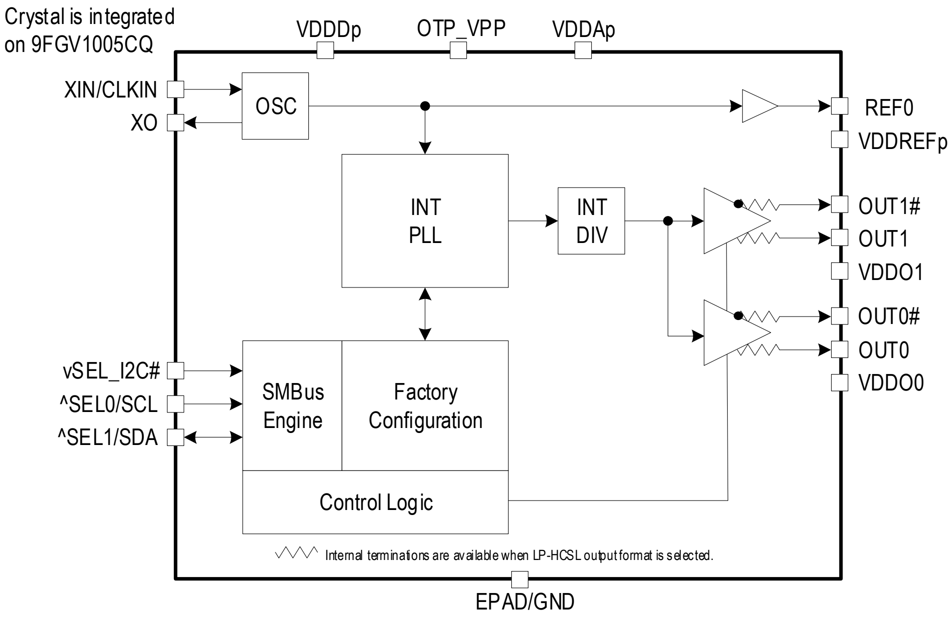
Key Specifications

- 259fs rms typical phase jitter outputs at 156.25MHz (12kHz–20MHz)
- PCIe Gen1–5 compliant

PCIe Clocking Architectures

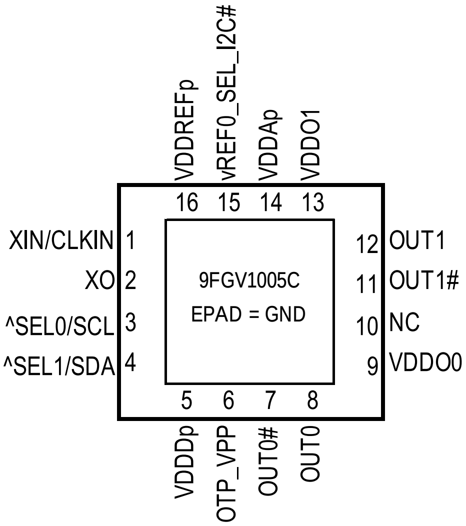
- Common Clocked (CC)
- Independent Reference without spread spectrum (SRnS)

Block Diagram

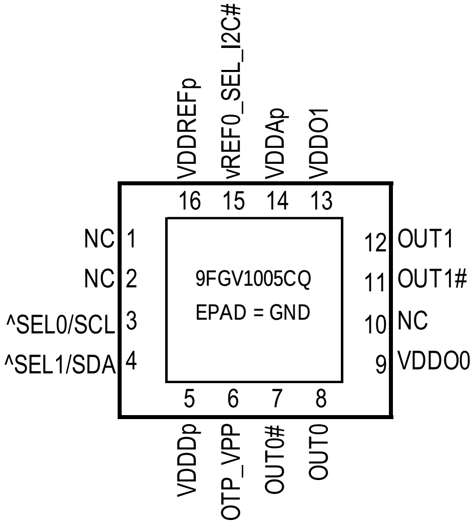


Pin Assignments

Figure 1. Pin Assignments for 3 × 3 mm 16-LGA Package – Top View



16-LGA 3 x 3 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor



16-LGA 3 x 3 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1 [a]	XIN/CLKIN	Input	Crystal input or reference clock input.
2 [a]	XO	Output	Crystal output.
3	^SEL0/SCL	Input	Select pin for internal frequency configurations/I^2C clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-up.
4	^SEL1/SDA	I/O	Select pin for internal frequency configurations/I^2C data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-up.
5	V_{DDDp}	Power	Digital power. 1.8V to 3.3V. V_{DDAp} and V_{DDDp} should be connected to the same power supply.
6	OTP_VPP	Power	Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as V_{DDD}.
7	OUT0#	Output	Complementary output clock 0.
8	OUT0	Output	Output clock 0.
9	V_{DDO0}	Power	Power supply for output 0.
10	NC	—	No connect.
11	OUT1#	Output	Complementary output clock 1.
12	OUT1	Output	Output clock 1.
13	V_{DDO1}	Power	Power supply for output 1.
14	V_{DDAp}	Power	Power supply for analog circuits. V_{DDAp} and V_{DDDp} should be connected to the same power supply. Programmable for nominal voltages of 1.8V, 2.5V or 3.3V.
15	vREF0_SEL_I2C#	Latched I/O	Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the I^2C pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down. 1 = SEL0/SEL1. 0 = SCL/SDA.
16	V_{DDREFp}	Power	Power supply for REF outputs and the internal XO. Nominal voltages are 1.8V, 2.5V or 3.3V.
17	EPAD	GND	Connect to ground.

Note: Unused outputs can be programmed off and left floating. V_{DDREF} and V_{DDO0} have to be connected.

[a] These pins are 'No Connect' on 9FGV1005Q integrated quartz versions and should have no stubs. See *Pin Assignments* diagram for 9FGV1005Q.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1005C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage, V_{DDA}, V_{DDD}, V_{DDO}	3.465V
Storage Temperature, T_{STG}	-65°C to 150°C
ESD Human Body Model	2000V
Junction Temperature	125°C
Inputs	
XIN/CLKIN	0V to 1.2V voltage swing
Other Inputs	-0.5V to V_{DDD}
Outputs	
Outputs, V_{DDO} (LVCMOS)	-0.5V to V_{DDO} + 0.5V
Outputs, IO (SDA)	10mA

Thermal Characteristics

Table 3. Thermal Characteristics [1]

Parameter	Symbol	Conditions	Package	Typical Values	Units	Notes
Thermal Resistance (devices with external crystal)	θ_{JC}	Junction to case.	LTG16	66	°C/W	1
	θ_{Jb}	Junction to base.		5.1	°C/W	1
	θ_{JA0}	Junction to air, still air.		63	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		56	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		51	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		49	°C/W	1
Thermal Resistance Q-series (devices with internal crystal)	θ_{JC}	Junction to case.	LTG16	82.1	°C/W	1
	θ_{Jb}	Junction to base.		42.3	°C/W	1
	θ_{JA0}	Junction to air, still air.		93.6	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		87.1	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		83.3	°C/W	1

[1] EPAD soldered to board.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DDOx}	Power supply voltage for supporting 1.8V outputs.	1.71	1.8	1.89	V
	Power supply voltage for supporting 2.5V outputs.	2.375	2.5	2.625	V
	Power supply voltage for supporting 3.3V outputs.	3.135	3.3	3.465	V
V_{DDD}	Power supply voltage for core logic functions.	1.71		3.465	V
V_{DDA}	Analog power supply voltage. Use filtered analog power supply if available.	1.71		3.465	V
T_A	Operating temperature, ambient.	-40		85	°C
C_L	Maximum load capacitance (3.3V LVCMOS only).			15	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic).	0.05		5	ms

Electrical Characteristics

V_{DDx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Table 5. Common Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Frequency	f_{IN}	Crystal input frequency.	8		50	MHz	1
		CLKIN input frequency.	1		240	MHz	5
Output Frequency	f_{OUT}	Differential clock output.	1		325	MHz	
		Single-ended clock output.	1		200	MHz	
VCO Frequency	f_{VCO}	VCO operating frequency range.	2400	2500	2600	MHz	
Loop Bandwidth	f_{BW}	Input frequency = 25MHz.	0.06		0.9	MHz	
Input High Voltage	V_{IH}	SEL[1:0].	0.7 x V_{DDD}		V_{DDD} + 0.3	V	
Input Low Voltage	V_{IL}	SEL[1:0].	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	REF/SEL_I2C#.	0.65 x V_{DDREF}		V_{DDREF} + 0.3	V	
Input Low Voltage	V_{IL}	REF/SEL_I2C#.	-0.3		0.4	V	
Input High Voltage	V_{IH}	XIN/CLKIN.	0.8		1.2	V	
Input Low Voltage	V_{IL}	XIN/CLKIN.	-0.3		0.4	V	
Input Rise/Fall Time	T_R/T_F	SEL1/SDA, SEL0/SCL.			300	ns	
Input Capacitance	C_{IN}	SEL[1:0].		3	7	pF	
Internal Pull-up Resistor	R_{UP}	SEL[1:0] at 25°C.	200	237	300	kΩ	
Internal Pull-down Resistor	R_{DOWN}	REF/SEL_I2C#.	200	237	300	kΩ	
Programmable Capacitance at XIN and XO (XIN in parallel with XO)	C_L	XIN/CLKIN, XO.	0		8	pF	

Table 5. Common Electrical Characteristics (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Duty Cycle	t2	CLKIN, measured at $V_{DDREF}/2$.	40	50	60	%	
Output Duty Cycle	t3	LVCMOS, f_{OUT} > 156.25MHz.	40	50	60	%	
		LVCMOS, $f_{OUT} \leq$ 156.25MHz.	45	50	55	%	
		LVDS, LP-HCSL outputs.	45	50.2	55	%	
Clock Jitter	t6	Cycle-to-cycle jitter (peak-to-peak), See "Test Frequencies for Jitter Measurements in Common Electrical Characteristics" for configurations.		30	50	ps	4
		Reference clock RMS phase jitter (12kHz to 5MHz integration range). See "Test Frequencies for Jitter Measurements in Common Electrical Characteristics" for configurations.		284		fs rms	4
		OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See "Test Frequencies for Jitter Measurements in Common Electrical Characteristics" for configurations.		259		fs rms	4
Output Skew	t7	Skew between the same frequencies, with outputs using the same driver format.		37	50	ps	
Lock Time	t8a	PLL outputs valid from VDDs reaching 1.5V		5	10	ms	2,3
	t8b	REF outputs valid from VDDs reaching 1.5V		5	11	ms	2,3

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to registers.

[3] Actual PLL lock time depends on the loop configuration.

[4] Actual jitter is configuration dependent. These values are representative of what the device can achieve.

[5] Input doubler off. Maximum input frequency with input doubler on is 160MHz.

Table 6. Test Frequencies for Jitter Measurements in Common Electrical Characteristics Table

V_{DDx} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Device	XIN/CLKIN	OUT0	OUT1	Unit	Notes
9FGV1005C	50	156.25		MHz	1,3
9FGV1005CQ5	50	100		MHz	2,3

[1] This configuration used for 12kHz–20MHz phase jitter measurement.

[2] This configuration used for PCIe filtered phase jitter measurements.

[3] Outputs configured as LP-HCSL or LVDS with REF output off, unless noted.

Table 7. LVCMOS Output Electrical Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Slew Rate	S_R	3.3V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	2.5	3.7	4.6	V/ns
		2.5V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	1.5	2.4	4.6	
		1.8V ±5%, 20% to 80% of V_{DDO} (output load = 4.7pF).	0.8	1.7	3.5	
Output High Voltage	V_{OH}	I_{OH} = -15mA at 3.3V.	0.8 x V_{DDO}		V_{DDO}	V
		I_{OH} = -12mA at 2.5V.				
		I_{OH} = -8mA at 1.8V.				
Output Low Voltage	V_{OL}	I_{OL} = 15mA at 3.3V.		0.22	0.4	V
		I_{OL} = 12mA at 2.5V.				
		I_{OL} = 8mA at 1.8V.				
Output Leakage Current (OUT[0:1])	I_{OZDD}	Programmable outputs, tri-state, V_{DDO} = 3.465V.		0	5	µA
Output Leakage Current (REF)	I_{OZDD}	REF outputs, tri-state, V_{DDO} = 3.465V.		0	5	µA
CMOS Output Driver Impedance	R_{OUT}	T_A = 25°C.		17		Ω

Table 8. LVDS Output Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Units
Differential Output Voltage for the TRUE Binary State	V_{OT} (+)	247	328	454	mV
Differential Output Voltage for the FALSE Binary State	V_{OT} (-)	-454	-332	-247	mV
Change in V_{OT} between Complementary Output States	ΔV_{OT}			50	mV
Output Common Mode Voltage (Offset Voltage) at 3.3V +5% and 2.5V +5%	V_{OS}	1.125	1.19	1.55	V
Output Common Mode Voltage (Offset Voltage) at 1.8V +5%	V_{OS}	0.8	0.86	0.95	V
Change in V_{OS} between Complementary Output States	ΔV_{OS}		0	50	mV
Outputs Short Circuit Current, V_{OUT}+ or V_{OUT}- = 0V or V_{DD}	I_{OS}		6	12	mA
Differential Outputs Short Circuit Current, V_{OUT}+ = V_{OUT}-	I_{OSD}		3	12	mA
Rise Times Tested at 20% – 80%	T_R		257	400	ps
Fall Times Tested at 80% – 20%	T_F		287	400	ps

Table 9. Low-Power (LP) Push-Pull HCSL Differential Outputs

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	$T_{R/F}$	Scope averaging on.	1	2.5	4	V/ns	2,3,16
Slew Rate Matching	$\Delta T_{R/F}$			9	20	%	1,14,16
Crossing Voltage (abs)	V_{CROSS}	Scope averaging off.	250	424	550	mV	1,4,5,16
Crossing Voltage (var)	ΔV_{CROSS}	Scope averaging off.		16	140	mV	1,4,9,16
Average Clock Period Accuracy	T_{PERIOD_AVG}	Outputs set to 100MHz for PCIe applications.	-100	0	+2600	ppm	2,10,12, 13
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread modulation.	9.949	10	10.101	ns	2,6
Absolute Maximum Voltage	V_{MAX}	Includes 300mV of overshoot (Vovs).	660	808	1150	mV	1,7,15
Absolute Minimum Voltage	V_{MIN}	Includes -300mV of undershoot (Vuds).	-300	-54	150	mV	1,8,15

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defined as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.

[10] Refer to Section 8.6 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2pF.

[12] PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. The PhiClock devices already meet the tighter ±100ppm frequency tolerances proposed for PCIe Gen5 and required by most servers.

[13] "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1 ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100 ppm =10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100 ppm applies to systems that do not employ spread spectrum clocking, or that use common clock source. For systems employing spread spectrum clocking, there is an additional 2,500 ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600 ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default amplitude settings.

[16] Guaranteed by design and characterization.

Table 10. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
PCIe Phase Jitter	$t_{jphPCIeG1\text{-}CC}$	PCIe Gen1.		11	18	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2\text{-}CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz).		0.1	0.14	3	ps (rms)	1,2
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz).		1.1	1.6	3.1	ps (rms)	1,2
	$t_{jphPCIeG3\text{-}CC}$	PCIe Gen3 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz).		0.27	0.37	1	ps (rms)	1,2
	$t_{jphPCIeG4\text{-}CC}$	PCIe Gen4 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz).		0.27	0.37	0.5	ps (rms)	1,2

Table 11. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

T_{AMB} = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
PCIe Phase Jitter	$t_{jphPCIeG2\text{-}SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		1.1	1.34	2	ps (rms)	1,4,5
	$t_{jphPCIeG3\text{-}SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz).		0.28	0.39	0.7	ps (rms)	1,4,5

Notes for *Filtered Phase Jitter Parameters* tables:

[1] Applies to all differential outputs at 100MHz, guaranteed by design and characterization.

[2] Based on PCIe Base Specification Rev4.0 version 0.7draft. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

[5] According to the PCIe Base Specification Rev4.0 version 0.7 draft, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

Table 12. Current Consumption

V_{DDO} = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, T_A = -40°C to +85°C unless stated otherwise.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
V_{DDREF} Supply Current	I_{DDREF}	50MHz REFCLK.		5	8	mA	
Core Supply Current	I_{DDCORE}	2500MHz VCO, 50MHz REFCLK.		24	31	mA	3
Output Buffer Supply Current (V_{DDO1})	$I_{DDO}x$	LVDS, 325MHz.		22	28	mA	2
		LP-HCSL, 100MHz.		17	24	mA	2
		LVCMOS, 50MHz.		15	20	mA	1,2
		LVCMOS, 200MHz.		25	40	mA	1,2
Output Buffer Supply Current (V_{DDO0})		LVDS, 325MHz.		8	12	mA	2
		LP-HCSL, 100MHz		6	10	mA	2
		LVCMOS, 50MHz.		4	7	mA	1,2
		LVCMOS, 200MHz.		13	26	mA	1,2
Total Power Down Current	I_{DDPD}	Programmable outputs in HCSL mode, B37[6,0] = 0.		7	10	mA	2
		Programmable outputs in LVDS mode, B37[6,0] = 0.		16	21	mA	2
		Programmable outputs in LVCMOS1 mode, B37[6,0] = 0.		5	7	mA	2

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE} = I_{DDA} + I_{DDD}$.

I^2C Bus Characteristics

Table 13. I^2C Bus DC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Input High Level	V_{IH}		0.7 x V_{DDD}			V
Input Low Level	V_{IL}				0.3 x V_{DDD}	V
Hysteresis of Inputs	V_{HYS}		0.05 x V_{DDD}			V
Input Leakage Current	I_{IN}		-1		30	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA.			0.4	V

Table 14. I^2C Bus AC Characteristics

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Serial Clock Frequency (SCL)	F_{SCLK}		10		400	kHz
Bus free time between STOP and START	t_{BUF}		1.3			µs
Setup Time, START	$t_{SU:START}$		0.6			µs
Hold Time, START	$t_{HD:START}$		0.6			µs
Setup Time, Data Input (SDA)	$t_{SU:DATA}$		0.1			µs
Hold Time, Data Input (SDA) 1	$t_{HD:DATA}$		0			µs
Output Data Valid from Clock	t_{OVD}				0.9	µs
Capacitive Load for Each Bus Line	C_B				400	pF
Rise Time, Data and Clock (SDA, SCL)	t_R		20 + 0.1 x C_B		300	ns
Fall Time, Data and Clock (SDA, SCL)	t_F		20 + 0.1 x C_B		300	ns
High Time, Clock (SCL)	t_{HIGH}		0.6			µs
Low Time, Clock (SCL)	t_{LOW}		1.3			µs
Setup Time, STOP	$t_{SU:STOP}$		0.6			µs

Note: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Crystal Characteristics

Table 15. Recommended Crystal Characteristics

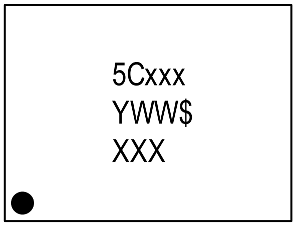
Parameter	Value	Units
Frequency	8–50	MHz
Resonance Mode	Fundamental	—
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, REF at 25°C Over Operating Temperature Range	±20	ppm maximum
Temperature Range (commercial)	0–70	°C
Temperature Range (industrial)	-40–85	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/us/en/document/psc/16-lga-package-outline-drawing-30-x-30-x-110-mm-body-05mm-pitch-ltg16p1

Marking Diagrams



- Line 1: truncated part number
- “YWW” denotes the last digits of the year and week the part was assembled.
- “$” denotes mark code.
- “XXX” denotes lot number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature	Description
9FGV1005CnnnLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	External Crystal
9FGV1005CnnnLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Reel	-40 to +85°C	External Crystal
9FGV1005CQ5aaLTGI	3 × 3 mm, 0.5mm pitch 16-LGA	Tray	-40 to +85°C	Internal 50MHz Crystal
9FGV1005CQ5aaLTGI8	3 × 3 mm, 0.5mm pitch 16-LGA	Reel	-40 to +85°C	Internal 50MHz Crystal

“G” indicates RoHS 6.6 compliance.

“nnn” are decimal digits indicating a specific configuration.

“aa” are alphanumeric digits indicating a specific configuration.

“Q5” indicates 50MHz internal crystal.

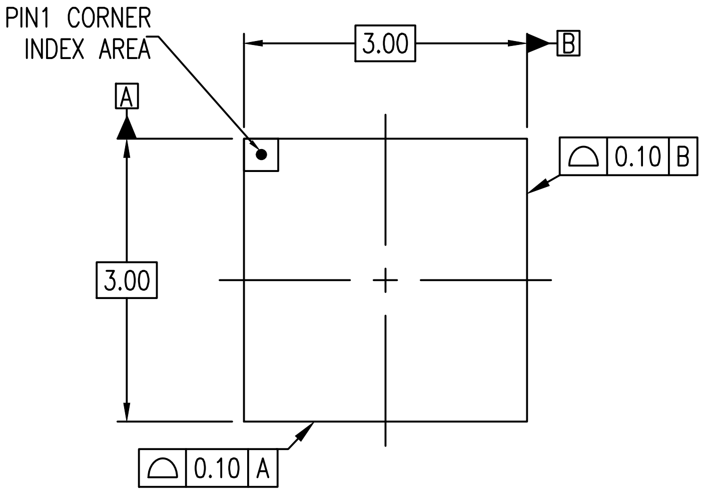
Revision History

Revision Date	Description of Change
February 14, 2020	▪ Updated Lock Time in Common Electri9cal Characteristics table. ▪ Moved datasheet to Final.
January 22, 2020	▪ Updated marking diagram. ▪ Updated datasheet to latest template.
December 20, 2019	Initial release.

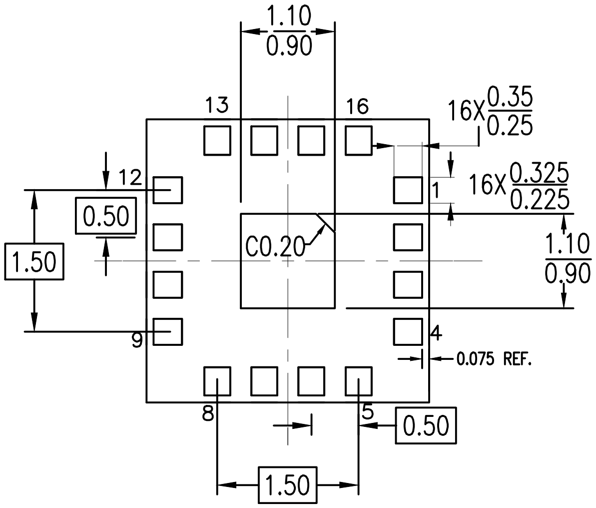
16-LGA Package Outline Drawing

3.0 x 3.0 x 1.10 mm Body, 0.5mm Pitch

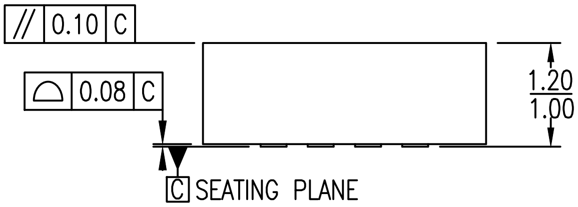
LTG16P1, PSC-4651-01, Rev 02, Page 1



TOP VIEW



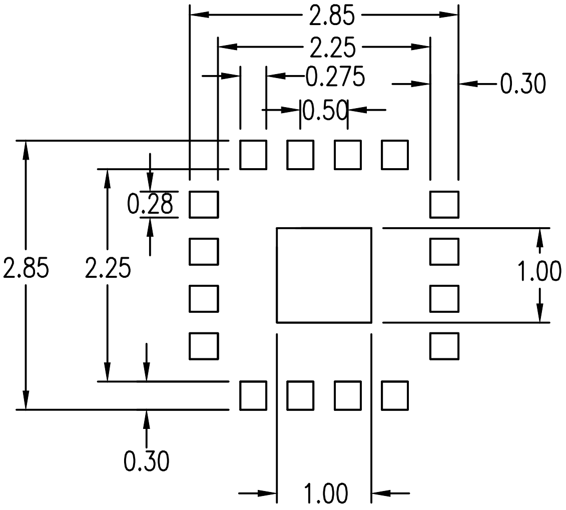
BOTTOM VIEW



SIDE VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC–7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History

Date Created	Rev No.	Description
Nov 6, 2017	Rev 02	Modify Solder Mask & Epad Chamfer
Sept 29, 2017	Rev 01	Modify Land Pattern

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