## Description

The 9FGV1006B is a member of IDT's PhiClock™ programmable clock generator family. The 9FGV1006B provides two copies of a single integer, fractional or spread spectrum output frequency and one copy of the crystal reference input. Two select pins allow for hardware selection of the desired configuration, or two I$^2$C bits allow easy software selection of the desired configuration. The user may configure any one of the four OTP configurations as the default when operating in I$^2$C mode. Four unique I$^2$C addresses are available, allowing easy I$^2$C access to multiple components.

## Typical Applications

- HPC
- Storage
- 10G/25G/100G Ethernet
- Fiber Optic Modules
- eSSDs
- NVLink

## Output Features

- 2 programmable output pairs plus 1 LVCMOS REF output
- 1 integer, fractional or spread spectrum output frequency per configuration
- 10MHz–325MHz LVDS or LP-HCSL outputs
- 10MHz–200MHz LVCMOS outputs

## Features

- 1.8V to 3.3V power supplies
- Individual 1.8V to 3.3V V$_{DDO}$ for each output pair
- Supports HCSL, LVDS and LVCMOS I/O standards
- Supports LVPECL and CML logic with easy AC coupling – see application note AN-891 for alternate terminations
- HCSL utilizes IDT's LP-HCSL technology for improved performance, lower power and higher integration:
  - Programmable output impedance of 85Ω or 100Ω
- On-board OTP supports up to 4 complete configurations
- Configuration selected via strapping pins or I$^2$C
- Internal crystal load capacitors
- < 100mW at 1.8V with LP-HCSL outputs at 100MHz (LP-HCSL)
- 4 programmable I$^2$C addresses: D0, D2, D4, D6
- Supported by IDT Timing Commander™ software and Web Configuration tool
- 3 × 3 mm 16-LGA with integrated crystal option (9FGV1006BQ)
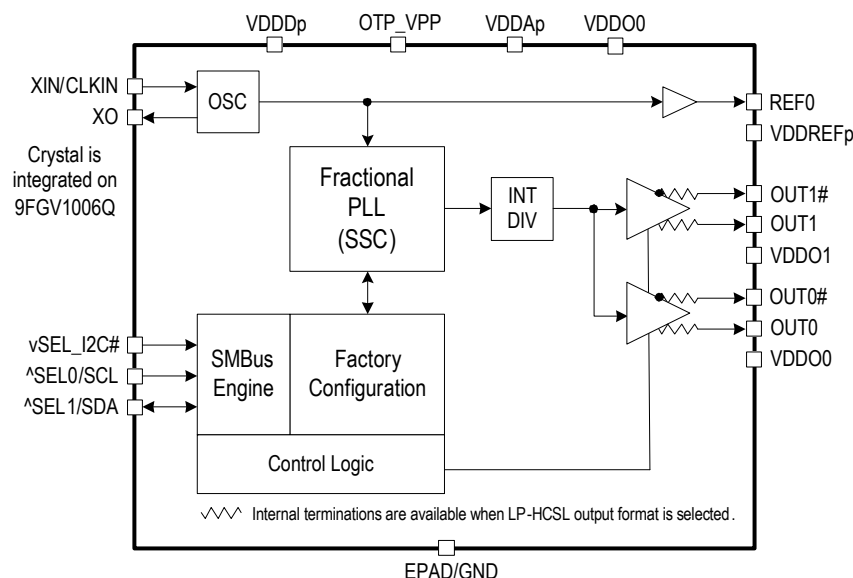- Programmable spread spectrum modulation frequency and amount

## Key Specifications

- 276fs rms typical phase jitter at 156.25MHz (12kHz–20MHz)
- < 0.2ps rms PCIe Gen4 Common Clocked jitter at 100MHz

## PCIe Clocking Architectures

- PCIe Gen1–4 Common Clocked (CC)
- Independent Reference without spread spectrum (SRnS)
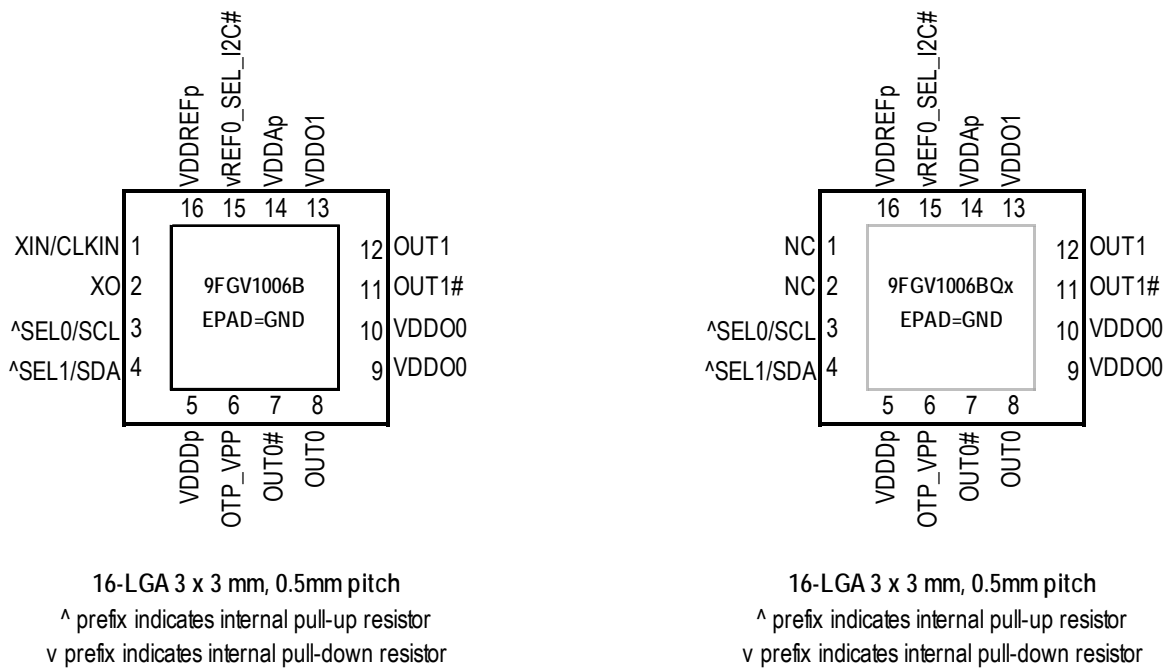- Independent Reference with spread spectrum (SRIS)

## Block Diagram

# Contents

# Pin Assignments

**Figure 1. Pin Assignments for 3 x 3 mm 16-LGA Package – Top View**



16-LGA 3 x 3 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

16-LGA 3 x 3 mm, 0.5mm pitch
^ prefix indicates internal pull-up resistor
v prefix indicates internal pull-down resistor

# Pin Descriptions

Note: Unused outputs can be programmed off and left floating. Output supplies $V_{DDREF}$ and $V_{DDO1}$ have to be connected. This means that if only one output is to be used, it must be OUT1. If OUT0 is used, both pins 9 and 10 must be connected. They may share the same power filter.

**Table 1. Pin Descriptions**

| Number | Name | Type | Description |
|---|---|---|---|
| 1[a] | XIN/CLKIN | Input | Crystal input or reference clock input. |
| 2[a] | XO | Output | Crystal output. |
| 3 | ^SEL0/SCL | Input | Select pin for internal frequency configurations/I$^2$C Clock pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-up. |
| 4 | ^SEL1/SDA | I/O | Select pin for internal frequency configurations/I$^2$C Data pin. Function is determined by state of SEL_I2C# upon power-up. This pin has an internal pull-up. |
| 5 | VDDDp | Power | Digital power. 1.8V to 3.3V. VDDAp and VDDDp should be connected to the same power supply. |
| 6 | OTP_VPP | Power | Voltage for programming OTP. During normal operation, this pin should be connected to the same power rail as $V_{DDD}$. |
| 7 | OUT0# | Output | Complementary output clock 0. |
| 8 | OUT0 | Output | Output clock 0. |
| 9 | VDDO0 | Power | Power supply for output 0. |
| 10 | VDDO0 | Power | Power supply for output 0. |
| 11 | OUT1# | Output | Complementary output clock 1. |

## Table 1. Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|--------|------|------|-------------|
| 12 | OUT1 | Output | Output clock 1. |
| 13 | VDDO1 | Power | Power supply for output 1. |
| 14 | VDDAp | Power | Power supply for analog circuits. VDDAp and VDDDp should be connected to the same power supply. Programmable for nominal voltages of 1.8V, 2.5V or 3.3V. |
| 15 | vREF0_SEL_I2C# | Latched I/O | Latched input/LVCMOS output. At power-up, the state of this pin is latched to select the state of the $I^2C$ pins. After power-up, the pin acts as an LVCMOS reference output. This pin has an internal pull-down.<br>1 = SEL0/SEL1.<br>0 = SCL/SDA. |
| 16 | VDDREFp | Power | Power supply for REF0 and REF1 and the internal XO. Programmable to 1.8V, 2.5V or 3.3V. |
| 17 | EPAD | GND | Connect to ground. |

[a] These pins are 'No Connect' on 9FGV1006BQ integrated quartz version.

# Phase Noise Plot

**Figure 2.  9FGV1006B Phase Noise Plot[1], 3.3V, 25°C.**
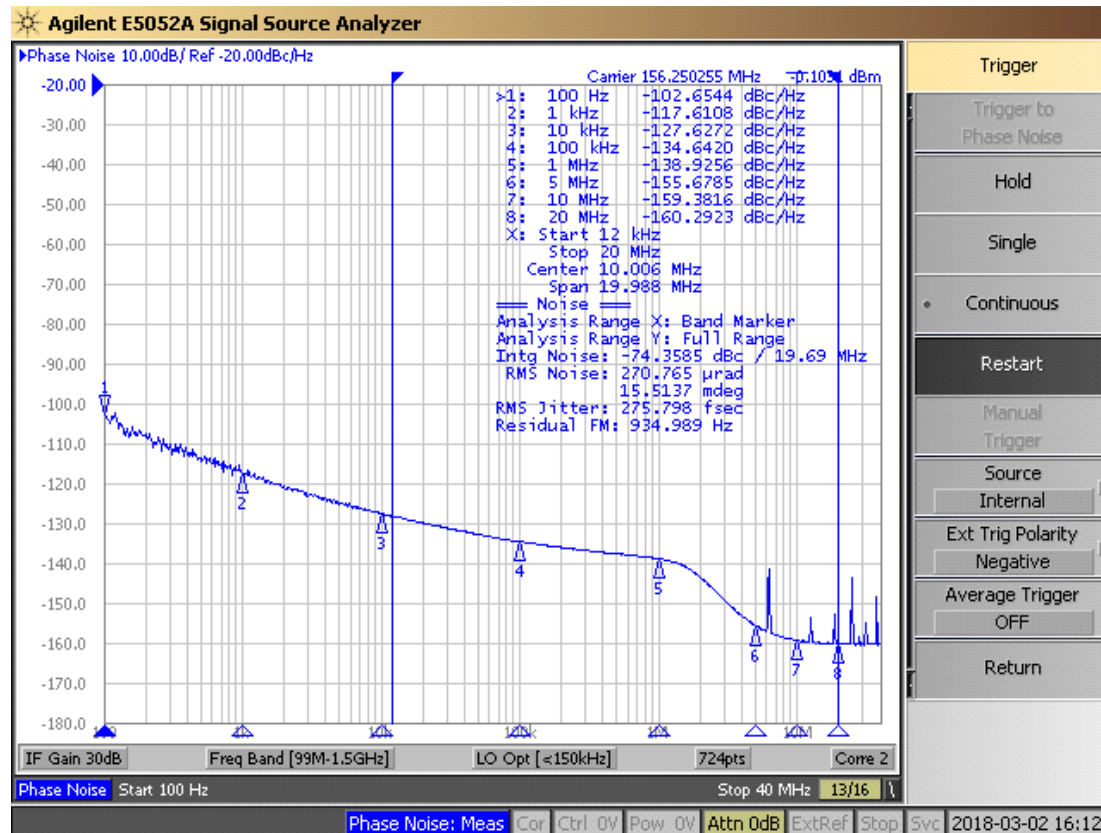


[1] See Test Frequencies for Jitter Measurements table for details.

# Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9FGV1006B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 2.  Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Supply Voltage, $V_{DDA}$, $V_{DDD}$, $V_{DDO}$ | 3.9V |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |
| ESD Human Body Model | 2000V |
| Junction Temperature | 125°C |
| Inputs | |
| XIN/CLKIN | 0V to 1.2V voltage swing |
| Other Inputs | -0.5V to $V_{DDD}$ |
| Outputs | |
| Outputs, $V_{DDO}$ (LVCMOS) | -0.5V to $V_{DDO}$ + 0.5V |
| Outputs, IO (SDA) | 10mA |

# Thermal Characteristics

**Table 3.  Thermal Characteristics**

| Parameter | Symbol | Conditions | Package | Typical Values | Units | Notes |
|---|---|---|---|---|---|---|
| Thermal Resistance (devices with external crystal) | $\theta_{JC}$ | Junction to case. | LTG16 | 66 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to base. | | 5.1 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to air, still air. | | 63 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. | | 56 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. | | 51 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. | | 49 | °C/W | 1 |
| Thermal Resistance Q-series (devices with internal crystal) | $\theta_{JC}$ | Junction to case. | LTG16 | 82.1 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to base. | | 42.3 | °C/W | 1 |
| | $\theta_{JA0}$ | Junction to air, still air. | | 93.6 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. | | 87.1 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. | | 83.3 | °C/W | 1 |

[1] EPAD soldered to board.

# Recommended Operating Conditions

## Table 4. Recommended Operating Conditions

| Symbol | Parameter | Minimum | Typical | Maximum | Units |
|--------|-----------|---------|---------|---------|-------|
| $V_{DDO}x$ | Power supply voltage for supporting 1.8V outputs. | 1.71 | 1.8 | 1.89 | V |
| | Power supply voltage for supporting 2.5V outputs. | 2.375 | 2.5 | 2.625 | V |
| | Power supply voltage for supporting 3.3V outputs. | 3.135 | 3.3 | 3.465 | V |
| $V_{DDD}$ | Power supply voltage for core logic functions. | 1.71 | | 3.465 | V |
| $V_{DDA}$ | Analog power supply voltage. Use filtered analog power supply if available. | 1.71 | | 3.465 | V |
| $T_A$ | Operating temperature, ambient. | -40 | | 85 | °C |
| $C_L$ | Maximum load capacitance (3.3V LVCMOS only). | | | 15 | pF |
| $t_{PU}$ | Power-up time for all $V_{DD}$s to reach minimum specified voltage (power ramps must be monotonic). | 0.05 | | 5 | ms |

# Electrical Characteristics

$V_{DDx}$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, $T_A$ = -40°C to +85°C unless stated otherwise.

## Table 5. Common Electrical Characteristics

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|-----------|--------|------------|---------|---------|---------|-------|-------|
| Input Frequency | $f_{IN}$ | Crystal input frequency. | 8 | | 50 | MHz | 1 |
| | | CLKIN input frequency. | 1 | | 240 | MHz | 5 |
| Output Frequency | $f_{OUT}$ | Differential clock output (LVDS/LP-HCSL). | 10 | | 325 | MHz | |
| | | Single-ended clock output (LVCMOS). | 10 | | 200 | MHz | |
| VCO Frequency | $f_{VCO}$ | VCO operating frequency range. | 2400 | 2500 | 2600 | MHz | |
| Loop Bandwidth | $f_{BW}$ | Input frequency = 25MHz. | 0.06 | | 0.9 | MHz | |
| Input High Voltage | $V_{IH}$ | SEL[1:0]. | $0.7 \times V_{DDD}$ | | $V_{DDD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | SEL[1:0]. | GND - 0.3 | | 0.8 | V | |
| Input High Voltage | $V_{IH}$ | REF/SEL_I2C#. | $0.65 \times V_{DDREF}$ | | $V_{DDREF}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | REF/SEL_I2C#. | -0.3 | | 0.4 | V | |
| Input High Voltage | $V_{IH}$ | XIN/CLKIN. | 0.8 | | 1.2 | V | |
| Input Low Voltage | $V_{IL}$ | XIN/CLKIN. | -0.3 | | 0.4 | V | |
| Input Rise/Fall Time | $T_R/T_F$ | OEA#, OEB# | | | 10 | ns | |
| Input Capacitance | $C_{IN}$ | SEL[1:0]. | | 3 | 7 | pF | |
| Internal Pull-up Resistor | $R_{UP}$ | SEL[1:0] at 25°C. | 200 | 237 | 300 | kΩ | |
| Internal Pull-down Resistor | $R_{DOWN}$ | SEL_I2C#. | 200 | 237 | 300 | kΩ | |

## Table 5.  Common Electrical Characteristics (Cont.)

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Programmable Capacitance at XIN and XO (XIN in parallel with XO) | $C_L$ | XIN/CLKIN, XO. | 0 | | 8 | pF | |
| Input Duty Cycle | t2 | CLKIN, measured at $V_{DDREF}/2$. | 40 | 50 | 60 | % | |
| Output Duty Cycle | t3 | LVCMOS, $f_{OUT}$ > 156.25MHz. | 40 | 50 | 60 | % | |
| | | LVCMOS, $f_{OUT} \leq$ 156.25MHz. | 45 | 50 | 55 | % | |
| | | LVDS, LP-HCSL outputs. | 45 | 50.2 | 55 | % | |
| Clock Jitter | t6 | Cycle-to-cycle jitter (Peak-to-Peak), See Test Frequencies for Jitter Measurements for configurations. | | 24 | | ps | 4 |
| | | Reference clock RMS phase jitter (12kHz to 20MHz integration range). See Test Frequencies for Jitter Measurements for configurations. | | 245 | | fs rms | 4 |
| | | OUTx RMS phase jitter(12kHz to 20MHz integration range) differential output. See Test Frequencies for Jitter Measurements for configurations. | | 276 | | fs rms | 4 |
| Output Skew | t7 | Skew between the same frequencies, with outputs using the same driver format. | | 38 | 60 | ps | |
| Lock Time | t8 | PLL lock time from $V_{DD}$s reaching 1.5V. | | 5 | 10 | ms | 2,3 |

[1] Practical lower frequency is determined by loop filter settings.

[2] Includes loading the configuration bits from OTP to registers.

[3] Actual PLL lock time depends on the loop configuration.

[4] Actual jitter is configuration dependent. These values are representative of what the device can achieve.

[5] Input doubler off. Maximum input frequency with input doubler on is 160MHz.

## Table 6.  Test Frequencies for Jitter Measurements

| Device | XIN/CLKIN | OUT0 | OUT1 | Unit | Notes |
|---|---|---|---|---|---|
| 9FGV1006B | 50 | 156.25 | | MHZ | 3,4 |
| 9FGV1006BQ5 | 50 | 100 | | MHZ | 1,2,3 |

[1] This configuration is used for 12kHz–20MHz REF phase jitter measurement, SSC off.

[2] This configuration is used for PCIe filtered phase jitter measurements with SSC on and off.

[3] Outputs configured as LP-HCSL or LVDS with REF output off, unless noted.

[4] This configuration is used for 12kHz–20MHz OUT phase jitter measurement. REF off, SSC off.

## Table 7.  LVCMOS Output Electrical Characteristics

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Slew Rate | $S_R$ | 3.3V ±5%, 20% to 80% of $V_{DDO}$ (output load = 4.7pF). | 2.6 | 3.7 | 4.7 | V/ns | |
| | | 2.5V ±5%, 20% to 80% of $V_{DDO}$ (output load = 4.7pF). | 1.5 | 2.4 | 4.7 | | |
| | | 1.8V ±5%, 20% to 80% of $V_{DDO}$ (output load = 4.7pF). | 0.8 | 1.7 | 3.2 | | |
| Output High Voltage | $V_{OH}$ | $I_{OH}$ = -15mA at 3.3V. | 0.8 x $V_{DDO}$ | | $V_{DDO}$ | V | |
| | | $I_{OH}$ = -12mA at 2.5V. | | | | | |
| | | $I_{OH}$ = -8mA at 1.8V. | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 15mA at 3.3V. | | 0.22 | 0.4 | V | |
| | | $I_{OL}$ = 12mA at 2.5V. | | | | | |
| | | $I_{OL}$ = 8mA at 1.8V. | | | | | |
| Output Leakage Current | $I_{OZDD}$ | Outputs, tri-stated, $V_{DDO}$, $V_{DDREF}$ = 3.465V. | | 0 | 5 | µA | |
| CMOS Output Driver Impedance | $R_{OUT}$ | $T_A$ = 25°C. | | 17 | | Ω | |

## Table 8.  LVDS Output Electrical Characteristics

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Differential Output Voltage for the TRUE Binary State | $V_{OT}$ (+) | 247 | 328 | 454 | mV | |
| Differential Output Voltage for the FALSE Binary State | $V_{OT}$ (-) | -454 | -332 | -247 | mV | |
| Change in $V_{OT}$ between Complementary Output States | $\Delta V_{OT}$ | | | 50 | mV | |
| Output Common Mode Voltage (Offset Voltage) at 3.3V +5% & 2.5V +5% | $V_{OS}$ | 1.125 | 1.19 | 1.55 | V | |
| Output Common Mode Voltage (Offset Voltage) at 1.8V +5% | $V_{OS}$ | 0.8 | 0.86 | 0.95 | V | |
| Change in $V_{OS}$ between Complementary Output States | $\Delta V_{OS}$ | | 0 | 50 | mV | |
| Outputs Short Circuit Current, $V_{OUT}$+ or $V_{OUT}$- = 0V or $V_{DD}$ | $I_{OS}$ | | 6 | 12 | mA | |
| Differential Outputs Short Circuit Current, $V_{OUT}$+ = $V_{OUT}$- | $I_{OSD}$ | | 3 | 12 | mA | |
| Rise Times Tested at 20%–80% | $T_R$ | | 257 | 375 | ps | |
| Fall Times Tested at 80%–20% | $T_F$ | | 287 | 375 | ps | |

## Table 9. Low-Power (LP) Push-Pull HCSL Differential Outputs

$V_{DDO}$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, $T_A$ = -40°C to +85°C unless stated otherwise.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| Slew Rate | $T_{R/F}$ | Scope averaging on. | 1.25 | 2.5 | 4 | V/ns | 2,3,16 |
| Slew Rate Matching | $\Delta T_{R/F}$ | | | 9 | 20 | % | 1,14,16 |
| Crossing Voltage (abs) | $V_{CROSS}$ | Scope averaging off. | 250 | 424 | 550 | mV | 1,4,5,16 |
| Crossing Voltage (var) | $\Delta V_{CROSS}$ | Scope averaging off. | | 16 | 140 | mV | 1,4,9,16 |
| Average Clock Period Accuracy | $T_{PERIOD\_AVG}$ | Outputs set to 100MHz for PCIe applications. | -100 | 0 | +2600 | | 2,10,12,13 |
| Absolute Period | $T_{PERIOD\_ABS}$ | Includes jitter and spread modulation. | 9.949 | 10 | 10.101 | | 2,6 |
| Voltage High | $V_{HIGH}$ | | 660 | 785 | 850 | mV | 1 |
| Voltage Low | $V_{LOW}$ | | -150 | 13 | 150 | mV | 1 |
| Absolute Maximum Voltage | $V_{MAX}$ | | | 808 | 1150 | mV | 1,7,15 |
| Absolute Minimum Voltage | $V_{MIN}$ | | -300 | -54 | | mV | 1,8,15 |

[1] Measured from single-ended waveform.

[2] Measured from differential waveform.

[3] Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.

[4] Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.

[5] Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

[6] Defined as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.

[7] Defined as the maximum instantaneous voltage including overshoot.

[8] Defined as the minimum instantaneous voltage including undershoot.

[9] Defined as the total variation of all crossing voltages of rising REFCLK+ and falling REFCLK-. This is the maximum allowed variance in $V_{CROSS}$ for any particular system.

[10] Refer to Section 8.6 of the PCI Express Base Specification, Revision 4.0 for information regarding PPM considerations.

[11] System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load $C_L$ = 2pF.

[12] PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. The PhiClock devices already meet the tighter ±100ppm frequency tolerances proposed for PCIe Gen5 and required by most servers.

[13] "ppm" refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum Clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.

[14] Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The rise edge rate of REFCLK+ should be compared to the fall edge rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

[15] At default amplitude settings.

[16] Guaranteed by design and characterization.

## Table 10.  Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

$T_{AMB}$ = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Specification Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| PCIe Phase Jitter | $t_{jphPCIeG1-CC}$ | PCIe Gen1. | | 13 | 26 | 86 | ps (p-p) | 1,2,3 |
| | $t_{jphPCIeG2-CC}$ | PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). | | 0.16 | 0.40 | 3 | ps (rms) | 1,2 |
| | | PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz, 8–16MHz, CDR = 5MHz). | | 0.02 | 0.58 | 3.1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG3-CC}$ | PCIe Gen3 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz). | | 0.02 | 0.20 | 1 | ps (rms) | 1,2 |
| | $t_{jphPCIeG4-CC}$ | PCIe Gen4 (PLL BW of 2–4MHz, 2–5MHz, CDR = 10MHz). | | 0.02 | 0.20 | 0.5 | ps (rms) | 1,2 |

## Table 11.  Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

$T_{AMB}$ = over the specified operating range. Supply Voltages per normal operation conditions; see Test Loads for loading conditions.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Industry Limits | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| PCIe Phase Jitter -0.25% SSC | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz). | | 0.06 | 0.45 | 2 | ps (rms) | 1,2,4,5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.27 | 0.34 | 0.7 | ps (rms) | 1,2,4,5 |
| PCIe Phase Jitter -0.5% SSC | $t_{jphPCIeG2-SRIS}$ | PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz). | | 0.05 | 0.45 | 2 | ps (rms) | 1,2,4,5 |
| | $t_{jphPCIeG3-SRIS}$ | PCIe Gen3 (PLL BW of 2–4MHz, CDR = 10MHz). | | 0.50 | 0.55 | 0.7 | ps (rms) | 1,2,4,5 |

Notes for PCIe Filtered Phase Jitter Tables:

[1] Applies to all differential outputs, guaranteed by design and characterization. Equipment noise removed from results. See PCI Express® Measurement Techniques for Gen5 and Beyond White Paper for details.

[2] Based on PCIe Base Specification Rev4.0 version 1.0. See http://www.pcisig.com for latest specifications.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of $1^{-12}$.

[4] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures.

[5] According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. The PCIe Base Specification Rev5.0 is expected to resolve this.

## Table 12.  Current Consumption

$V_{DDO}$ = 3.3V ±5%, 2.5V ±5%, 1.8V ±5%, $T_A$ = -40°C to +85°C unless stated otherwise.

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DDREF}$ Supply Current | $I_{DDREF}$ | 50MHz REFCLK. | | 3 | 7 | mA | |
| Core Supply Current | $I_{DDCORE}$ | 2400MHz VCO. | | 37 | 48 | mA | 3 |
| Output Buffer Supply Current ($V_{DDO1}$) | $I_{DDOx}$ | LVDS, 350MHz. | | 19 | 24 | mA | 2 |
| | | LP-HCSL, 100MHz. | | 16 | 20 | mA | 2 |
| | | LVCMOS, 50MHz. | | 14 | 19 | mA | 1,2 |
| | | LVCMOS, 200MHz. | | 22 | 34 | mA | 1,2 |
| Output Buffer Supply Current ($V_{DDO0}$ – the total for pins 9 and 10) | | LVDS, 350MHz. | | 7 | 11 | mA | 2 |
| | | LP-HCSL, 100MHz. | | 8 | 10 | mA | 2 |
| | | LVCMOS, 50MHz. | | 8 | 13 | mA | 1,2 |
| | | LVCMOS, 200MHz. | | 8 | 14 | mA | 1,2 |
| Total Power Down Current | $I_{DDPD}$ | Programmable outputs in HCSL mode, B37[0] = 0. | | 19 | 25 | mA | 2,4 |
| | | Programmable outputs in LVDS mode, B37[0] = 0. | | 25 | 34 | mA | 2,4 |
| | | Programmable outputs in LVCMOS1 mode, B37[0] = 0. | | 16 | 22 | mA | 2,4 |
| | | Programmable outputs in HCSL mode, B37[6,0] = 0. | | 10 | 17 | mA | 2,4 |
| | | Programmable outputs in LVDS mode, B37[6,0] = 0. | | 15 | 24 | mA | 2,4 |
| | | Programmable outputs in LVCMOS1 mode, B37[6,0] = 0. | | 7 | 12 | mA | 2,4 |

[1] Single CMOS driver active for each output pair.

[2] See Test Loads for details.

[3] $I_{DDCORE}$ = $I_{DDA}$ + $I_{DDD}$ + $I_{DDAO}$.

[4] Full power-down is accomplished by writing Byte 37[0] first, followed by writing Byte 37[6]. Power-up is the reverse of this sequence.

## Table 13.  Spread Spectrum Generation Specifications

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Output Frequency | $f_{OUT}$ | Output frequency range of spread spectrum outputs. | 10 | | 312.5 | MHz |
| Mod Frequency | $f_{MODPCIe}$ | PCIe Compliant -0.5% spread modulation. | 30 | 31.5 | 33 | kHz |
| Mod Frequency | $f_{MOD}$ | Modulation frequency. | 30 | 31.5 | 63 | kHz |
| Spread% | SSC% | Amount of spread value (programmable) – down spread. | -0.1 | -0.5 | -3.0 | % |
| | | Amount of spread value (programmable) – center spread. | ±0.05 | | ±1.5 | |

# I²C Bus Characteristics

**Table 14. I²C Bus DC Characteristics**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Input High Level | $V_{IH}$ | — | $0.7 \times V_{DDD}$ | | | V |
| Input Low Level | $V_{IL}$ | — | | | $0.3 \times V_{DDD}$ | V |
| Hysteresis of Inputs | $V_{HYS}$ | — | $0.05 \times V_{DDD}$ | | | V |
| Input Leakage Current | $I_{IN}$ | — | -1 | | 30 | µA |
| Output Low Voltage | $V_{OL}$ | $I_{OL}$ = 3mA. | | | 0.4 | V |

**Table 15. I²C Bus AC Characteristics**

| Parameter | Symbol | Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| Serial Clock Frequency (SCL) | $F_{SCLK}$ | — | 10 | | 400 | kHz |
| Bus free time between STOP and START | $t_{BUF}$ | — | 1.3 | | | µs |
| Setup Time, START | $t_{SU:START}$ | — | 0.6 | | | µs |
| Hold Time, START | $t_{HD:START}$ | — | 0.6 | | | µs |
| Setup Time, Data Input (SDA) | $t_{SU:DATA}$ | — | 0.1 | | | µs |
| Hold Time, Data Input (SDA) 1 | $t_{HD:DATA}$ | — | 0 | | | µs |
| Output Data Valid from Clock | $t_{OVD}$ | — | | | 0.9 | µs |
| Capacitive Load for Each Bus Line | $C_B$ | — | | | 400 | pF |
| Rise Time, Data and Clock (SDA, SCL) | $t_R$ | — | $20 + 0.1 \times C_B$ | | 300 | ns |
| Fall Time, Data and Clock (SDA, SCL) | $t_F$ | — | $20 + 0.1 \times C_B$ | | 300 | ns |
| HIGH Time, Clock (SCL) | $t_{HIGH}$ | — | 0.6 | | | µs |
| LOW Time, Clock (SCL) | $t_{LOW}$ | — | 1.3 | | | µs |
| Setup Time, STOP | $t_{SU:STOP}$ | — | 0.6 | | | µs |

Note: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

# Test Loads

**Figure 3.  LVCMOS AC/DC Test Load**
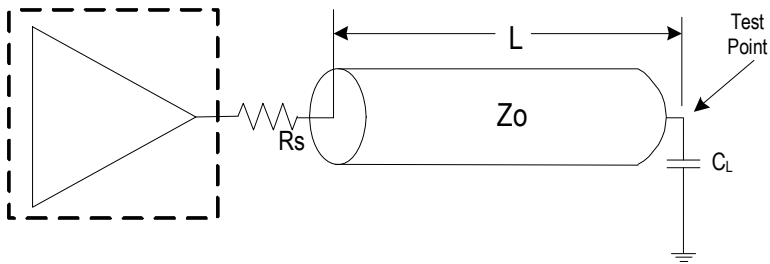


| Rs | Zo | L | $C_L$ |
|----|----|----|----|
| 33Ω | 50Ω | 5 inches | 4.7pF |

**Figure 4.  LP-HCSL AC/DC Test Load**
(Standard PCIe source-terminated test load)
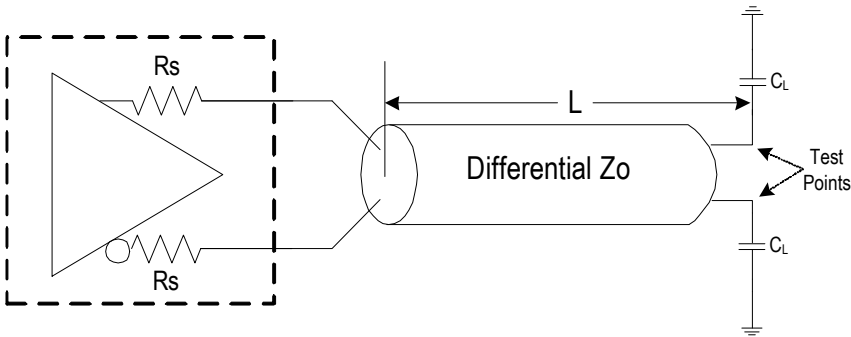


| Rs | Zo | L | $C_L$ |
|----|----|----|----|
| Internal | 100Ω | 5 inches | 2pF |

**Figure 5.  LVDS AC/DC Test Load**
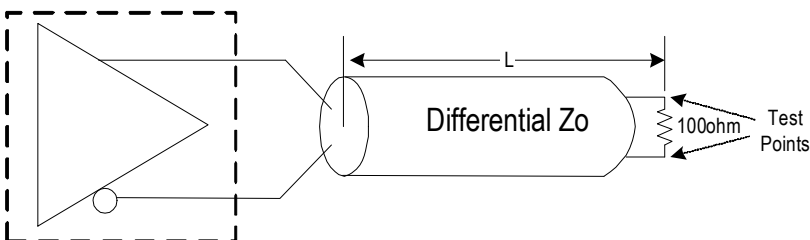


| Rs | Zo | L | $C_L$ |
|----|----|----|----|
| N/A | 100Ω | 5 inches | N/A |

**Figure 6. PCIe Jitter Test Load[1]**
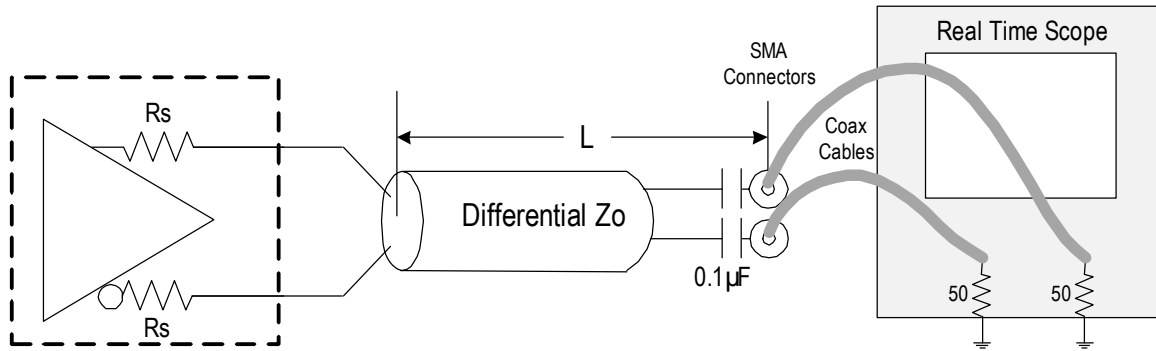


[1] This test setup is used to obtain clock period files for PCIe phase jitter calculations.

| Rs | Zo | L | $C_L$ |
|---|---|---|---|
| Internal | 100Ω | 5 inches | N/A |

# Crystal Characteristics

**Table 16. Recommended Crystal Characteristics**

| Parameter | Value | Units |
|---|---|---|
| Frequency | 8–50 | MHz |
| Resonance Mode | Fundamental | – |
| Frequency Tolerance at 25°C | ±20 | ppm maximum |
| Frequency Stability, REF at 25°C Over Operating Temperature Range | ±20 | ppm maximum |
| Temperature Range (commercial) | 0–70 | °C |
| Temperature Range (industrial) | -40–85 | °C |
| Equivalent Series Resistance (ESR) | 50 | Ω maximum |
| Shunt Capacitance ($C_O$) | 7 | pF maximum |
| Load Capacitance ($C_L$) | 8 | pF maximum |
| Drive Level | 0.1 | mW maximum |
| Aging Per Year | ±5 | ppm maximum |

# Package Outline Drawings

The package outline drawings are appended at the end of this document and are also accessible from the link below. The package information is the most current data available and is subject to change without notice or revision of this document.

www.idt.com/document/psc/16-lga-package-outline-drawing-30-x-30-x-110-mm-body-05mm-pitch-ltg16p1

# Marking Diagrams

```
6B00I
YWW$
XXX
●
```

```
6Q500
YWW$
XXX
●
```
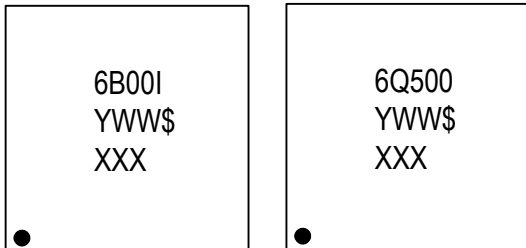
1. Line 1: truncated part number

2. "YWW" denotes the last digits of the year and week the part was assembled.

3. "$" denotes mark code.

4. "XXX" denotes the last three characters of the lot number.

# Ordering Information

| Orderable Part Number | Package | Carrier Type | Temperature | Crystal |
|---|---|---|---|---|
| 9FGV1006BnnnLTGI | 3 × 3 mm, 0.5mm pitch 16-LGA | Tray | -40 to +85°C | External |
| 9FGV1006BnnnLTGI8 | 3 × 3 mm, 0.5mm pitch 16-LGA | Reel | -40 to +85°C | External |
| 9FGV1006BQ5aaLTGI | 3 × 3 mm, 0.5mm pitch 16-LGA | Tray | -40 to +85°C | 50MHz Internal |
| 9FGV1006BQ5aaLTGI8 | 3 × 3 mm, 0.5mm pitch 16-LGA | Reel | -40 to +85°C | 50MHz Internal |

"G" indicates RoHS 6.6 compliance.
"nnn" are decimal digits indicating a specific configuration.
"aa" are alphanumeric digits indicating a specific configuration.
"Q5" indicates internal 50MHz crystal.

# Revision History

| Revision Date | Description of Change |
|---|---|
| August 28, 2018 | Initial release. |

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