9UMS9633B

Ultra-Mobile PC/Mobile Internet Device

The 9UMS9633B is an ultra-mobile PC/mobile Internet device supporting Intel ULV CPUs requiring 67 to 167 MHz CPU outputs.

Output Features

- 3 – CPU low power differential push-pull pairs
- 3 – SRC low power differential push-pull pairs
- 1 – LCD100 SSCD low power differential push-pull pair
- 1 – DOT96 low power differential push-pull pair
- 1 – REF, 14.31818MHz, 3.3V SE output

Features

- 67 to 167 MHz CPU outputs
- Dedicated TEST/SEL and TEST/MODE pins saves isolation resistors on pins
- CPU STOP# input for power management
- Fully integrated Vreg
- Integrated series resistors on differential outputs
- 1.5V VDD IO operation, 3.3V VDD core and REF supply pin for REF
- Industrial temperature range (-40° to +85°C)

Applications

- Poulsbo Based Ultra-Mobile PC (UMPC)

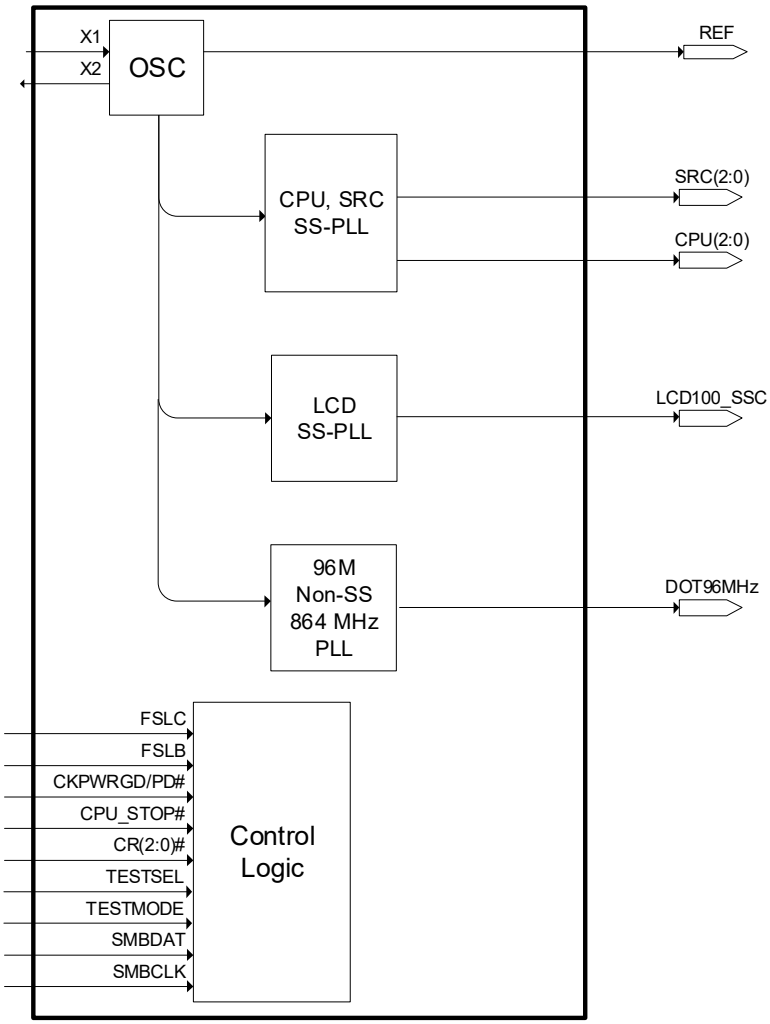
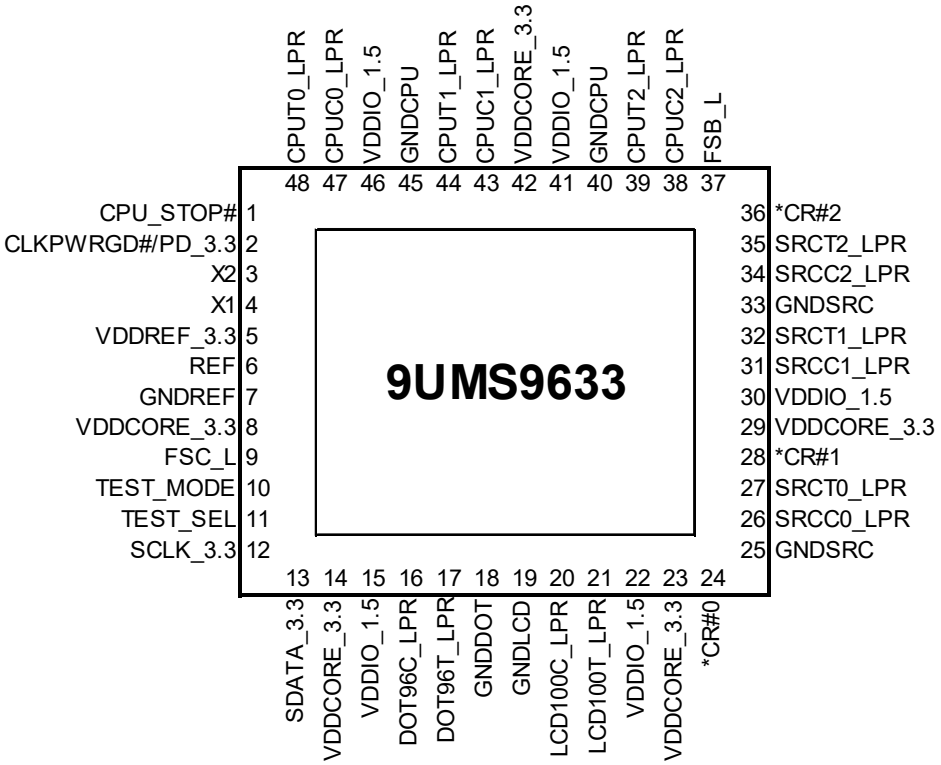


Figure 1. Functional Block Diagram

Contents

1. Pin Information

1.1 Pin Assignments



Note: * indicates inputs with internal pull-up of ~10kΩ to 3.3V.

Figure 2. 48-VFQFPN, 6 × 6 mm, Top View

1.2 Pin Descriptions

Pin Number	Pin Name	Pin Type	Description
1	CPU_STOP#	Input	Stops CPU0 clock when enabled.
2	CLKPWRGD#/PD_3.3	Input	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active low input. Asynchronous active high input pin used to place the device into a power down state.
3	X2	Output	Crystal output, Nominally 14.318MHz
4	X1	Input	Crystal input, Nominally 14.318MHz.
5	VDDREF_3.3	Power	Power pin for the XTAL and REF clocks, nominal 3.3V.
6	REF	Output	14.318MHz reference clock.
7	GNDREF	Power	Ground pin for the REF outputs.
8	VDDCORE_3.3	Power	3.3V power for the PLL core.
9	FSC_L	Input	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
10	TEST_MODE	Input	TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification table.

Pin Number	Pin Name	Pin Type	Description
11	TEST_SEL	Input	TEST_SEL: latched input to select Test Mode: 1 = All outputs are tri-stated for test. 0 = All outputs behave normally.
12	SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.
13	SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
14	VDDCORE_3.3	Power	3.3V power for the PLL core.
15	VDDIO_1.5	Power	Power supply for low power differential outputs, nominal 1.5V.
16	DOT96C_LPR	Output	Complementary clock of low power differential pair for 96.00MHz DOT clock. No 50Ω resistor to GND needed. No Rs needed.
17	DOT96T_LPR	Output	True clock of low power differential pair for 96.00MHz DOT clock. No 50Ω resistor to GND needed. No Rs needed.
18	GNDDOT	PWR	Ground pin for DOT clock output.
19	GNDLCD	PWR	Ground pin for LCD clock output.
20	LCD100C_LPR	Output	Complementary clock of low power differential pair for LCD100 SS clock. No 50Ω resistor to GND needed. No Rs needed.
21	LCD100T_LPR	Output	True clock of low power differential pair for LCD100 SS clock. No 50Ω resistor to GND needed. No Rs needed.
22	VDDIO_1.5	Power	Power supply for low power differential outputs, nominal 1.5V.
23	VDDCORE_3.3	Power	3.3V power for the PLL core.
24	CR#0	Input	Clock request for SRC0, 0 = enable, 1 = disable.
25	GNDSRC	Power	Ground pin for the SRC outputs.
26	SRCC0_LPR	Output	Complementary clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
27	SRCT0_LPR	Output	True clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
28	*CR#1	Input	Clock request for SRC1, 0 = enable, 1 = disable.
29	VDDCORE_3.3	Power	3.3V power for the PLL core.
30	VDDIO_1.5	Power	Power supply for low power differential outputs, nominal 1.5V.
31	SRCC1_LPR	Output	Complementary clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
32	SRCT1_LPR	Output	True clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
33	GNDSRC	Power	Ground pin for the SRC outputs
34	SRCC2_LPR	Output	Complementary clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
35	SRCT2_LPR	Output	True clock of differential 0.8V push-pull SRC output with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
36	CR#2	Input	Clock request for SRC2, 0 = enable, 1 = disable.
37	FSB_L	Input	Low threshold input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values.
38	CPUC2_LPR	Output	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
39	CPUT2_LPR	Output	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33Ω series resistor. No 50Ω resistor to GND needed.

Pin Number	Pin Name	Pin Type	Description
40	GNDCPU	Power	Ground pin for the CPU outputs.
41	VDDIO_1.5	Power	Power supply for low power differential outputs, nominal 1.5V.
42	VDDCORE_3.3	Power	3.3V power for the PLL core.
43	CPUC1_LPR	Output	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
44	CPUT1_LPR	Output	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33Ω series resistor. No 50Ω resistor to GND needed.
45	GNDCPU	Power	Ground pin for the CPU outputs.
46	VDDIO_1.5	Power	Power supply for low power differential outputs, nominal 1.5V.
47	CPUC0_LPR	Output	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
48	CPUT0_LPR	Output	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33Ω series resistor. No 50Ω resistor to GND needed.

1.3 Power Groups

Pin Number		Description	
VDD	GND		
41, 46	40, 45	CPUCLK	Low power outputs
42			VDDCORE_3.3V
30	25, 33	SRCCLK	Low power outputs
29			VDDCORE_3.3V
22	19	LCDCLK	Low power outputs
23			VDDCORE_3.3V
15	18	DOT 96Mhz	Low power outputs
14			VDDCORE_3.3V
5	7	Xtal, REF	

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Symbol	Test Conditions	Minimum	Maximum	Unit
3.3V Supply Voltage [1] [2]	VDDxxx_3.3	Supply voltage.	-	3.9	V
1.5V Supply Voltage [1] [2]	VDDxxx_1.5	Supply voltage.	-	3.9	V
3.3_Input High Voltage [1] [2] [3]	$V_{IH3.3}$	3.3V inputs.	-	VDD_3.3 + 0.3V	V
Minimum Input Voltage [1]	V_{IL}	Any input.	GND - 0.5	-	V
Storage Temperature [1] [2]	Ts	-	-65	150	°C
Input ESD Protection [1] [2]	ESD prot	Human Body Model.	2000	-	V
		Man Machine Model.	200	-	V

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied, nor guaranteed.
3. Maximum input voltage is not to exceed maximum VDD.

2.2 Electrical Characteristics – Input/Supply/Common Output Parameters

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Ambient Operating Temperature [1]	$T_{ambientITEMP}$	No airflow.	-40	25	85	°C
3.3V Supply Voltage [1]	VDDCORE3.3	3.3V ±5%.	3.135	3.30	3.465	V
1.5V Supply Voltage [1]	VDDIO_1.5	1.5V - 5% to 3.3V + 5%.	1.425	1.50	3.465	V
3.3V Input High Voltage [1]	$V_{IHSE3.3}$	Single-ended inputs.	2	-	VDD + 0.3	V
3.3V Input Low Voltage [1]	$V_{ILSE3.3}$	Single-ended inputs.	VSS - 0.3	-	0.8	V
Input Leakage Current [1]	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5	-	5	µA
Input Leakage Current [1]	I_{INRES}	Inputs with pull or pull down resistors. (CR# pins) $V_{IN} = V_{DD}$, V_{IN} = GND	-200	-	200	µA
Output High Voltage [1]	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA.	2.4	-	-	V
Output Low Voltage [1]	V_{OLSE}	Single-ended outputs, I_{OL} = 1mA.	-	-	0.4	V
Low Threshold Input-High Voltage [1]	V_{IH_FS}	3.3 V ±5%.	0.7	-	-	V
Low Threshold Input-Low Voltage [1]	V_{IL_FS}	3.3 V ±5%.	VSS - 0.3	-	0.35	V
Operating Supply Current [1]	$I_{DD\_DEFAULT}$	3.3V supply, LCDPLL off.	-	46	55	mA
	I_{DD_LCDEN}	3.3V supply, LCDPLL enabled.	-	56	60	mA
	I_{DD_IO}	1.5V supply, Differential IO current, all outputs enabled.	-	34	40	mA
Power Down Current [1]	$I_{DD\_PD3.3}$	3.3V supply, Power Down mode.	-	3.4	4.0	mA
	I_{DD_PDIO}	1.5V IO supply, Power Down mode.	-	1.5	2.5	mA

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Input Frequency [2]	F_i	V_{DD} = 3.3V.		14.318		MHz
Pin Inductance [1]	L_{pin}		-	-	7	nH
Input Capacitance [1]	C_{IN}	Logic inputs.	1.5	-	5	pF
	C_{OUT}	Output pin capacitance.	-	-	6	pF
	C_{INX}	X1 and X2 pins.	-	-	5	pF
Spread Spectrum Modulation Frequency [1]	f_{SSMOD}	Triangular modulation.	30	32.6	33	kHz

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through Vswing centered around differential zero.

2.3 AC Electrical Characteristics – Input/Common Parameters

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Clk Stabilization [1]	T_{STAB}	From VDD Power-Up or de-assertion of PD# to 1st clock.	-	0.91	1.8	ms
Tdrive_SRC [1]	T_{DRSRC}	SRC output enable after CR# assertion.	-	-	30	ns
Tdrive_PD# [1]	T_{DRPD}	Differential output enable after PD# de-assertion.	-	-	400	µs
Tdrive_CPU [1]	T_{DRSRC}	CPU output enable after CPU_STOP# de-assertion.	-	-	75	ns
Tfall_PD# [1]	T_{FALL}	Fall/rise time of PD# and CPU_STOP# inputs.	-	-	5	ns
Trise_PD# [1]	T_{RISE}		-	-	5	ns

1. Confirmed by design and characterization, not 100% tested in production.

2.4 AC Electrical Characteristics – Low Power Differential Inputs

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Rising Edge Slew Rate [1][2]	t_{SLR}	Differential Measurement.	1.5	3.2	5	V/ns
Falling Edge Slew Rate [1][2]	t_{FLR}	Differential Measurement.	1.5	3.1	5	V/ns
Rise/Fall Time Variation [1]	t_{SLVAR}	Single-ended Measurement.	-	-	125	ps
Maximum Output Voltage [1]	V_{HIGH}	Includes overshoot.	-	-	1150	mV
Minimum Output Voltage [1]	V_{LOW}	Includes undershoot.	-300	-	-	mV
Differential Voltage Swing [1]	V_{SWING}	Differential Measurement.	300	-	-	mV
Crossing Point Voltage [1][3][4]	V_{XABS}	Single-ended Measurement.	300	405	550	mV
Crossing Point Variation [1][3][5]	$V_{XABSVAR}$	Single-ended Measurement.	-	-	140	mV
Duty Cycle [1]	D_{CYC}	Differential Measurement.	45	49.48	55	%
CPU Jitter - Cycle to Cycle [1]	$CPUJ_{C2C}$	Differential Measurement.	-	20	85	ps
SRC Jitter - Cycle to Cycle [1]	$SRCJ_{C2C}$	Differential Measurement.	-	15	125	ps
DOT Jitter - Cycle to Cycle [1]	$DOTJ_{C2C}$	Differential Measurement.	-	13	250	ps
CPU[2:0] Skew [1]	CPU_{SKEW10}	Differential Measurement.	-	27	100	ps
SRC[2:0] Skew [1]	SRC_{SKEW}	Differential Measurement.	-	34	250	ps

1. Confirmed by design and characterization, not 100% tested in production.

2. Slew rate measured through Vswing centered around differential zero.
3. Vxabs is defined as the voltage where CLK = CLK#.
4. Only applies to the differential rising edge (CLK rising and CLK# falling).
5. Defined as the total variation of all crossing voltages of CLK rising and CLK# falling. Matching applies to rising edge rate of CLK and falling edge of CLK#. It is measured using a ±75mV window centered on the average cross point where CLK meets CLK#.

2.5 Electrical Characteristics – REF-14.318MHz

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
Long Accuracy [1][2][3]	ppm	See Tperiod min-max values.	-300	-	300	ppm
Clock Period [2][3]	T_{period}	14.318MHz output nominal.	69.8203	69.84	69.8622	ns
Absolute Min/Max Period [2]	T_{abs}	14.318MHz output nominal.	69.8203	69.84	70.8622	ns
Output High Voltage [1]	V_{OH}	I_{OH} = -1mA.	2.4	-	-	V
Output Low Voltage [1]	V_{OL}	I_{OL} = 1mA.	-	-	0.4	V
Output High Current [1]	I_{OH}	V_{OH} at MIN = 1.0V, V_{OH} at MAX = 3.135V.	-33	-	-33	mA
Output Low Current [1]	I_{OL}	V_{OL} at MIN = 1.95V, V_{OL} at MAX = 0.4V.	30	-	38	mA
Rising Edge Slew Rate [1]	t_{SLR}	Measured from 0.8V to 2.0V.	1	3.0	4	V/ns
Falling Edge Slew Rate [1]	t_{FLR}	Measured from 2.0V to 0.8V.	1	3.1	4.5	V/ns
Duty Cycle [1]	d_{t1}	V_T = 1.5V.	45	52.3	55	%
Jitter [1]	$t_{jcyc-cyc}$	V_T = 1.5V.	54	61	1000	ps

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through Vswing centered around differential zero.
3. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is at 14.31818MHz.

2.6 Electrical Characteristics – SMBus Interface

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Unit
SMBus Voltage [1]	V_{DD}		2.7	-	3.63	V
Low-level Output Voltage [1]	V_{OLSMB}	At I_{PULLUP}.	-	-	0.4	V
Current sinking at V_{OLSMB} = 0.4V [1]	I_{PULLUP}	SMB Data pin.	4	-	-	mA
SCLK/SDATA Clock/Data Rise Time [1]	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15).	-	-	1000	ns
SCLK/SDATA Clock/Data Fall Time [1]	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15).	-	-	300	ns
Maximum SMBus Operating Frequency [1]	F_{SMBUS}	Block Mode.	-	-	100	kHz

1. Confirmed by design and characterization, not 100% tested in production.

2.7 Clock Periods Differential Outputs with Spread Spectrum Enabled

Measurement Window		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock	
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+	
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Absolute Period	
		Minimum	Minimum	Minimum	Nominal	Maximum	Maximum	Maximum	Units
Signal Name	SRC 100 [1][2]	9.87400	9.99900	9.99900	10.00000	10.00100	10.05130	10.17630	ns
	CPU 100 [1][2]	9.91400	9.99900	9.99900	10.00000	10.00100	10.05130	10.13630	ns
	CPU 133 [1][2]	7.41425	7.49925	7.49925	7.50000	7.50075	7.53845	7.62345	ns
	CPU 166 [1][2]	5.91440	5.99940	5.99940	6.00000	6.00060	6.03076	6.11576	ns

1. Confirmed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz.

2.8 Clock Periods Differential Outputs with Spread Spectrum Disabled

Measurement Window		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock	
Symbol		Lg-	-SSC	-ppm error	0ppm	+ ppm error	+SSC	Lg+	
Definition		Absolute Period	Short-term Average	Long-Term Average	Period	Long-Term Average	Short-term Average	Absolute Period	
		Minimum	Minimum	Minimum	Nominal	Maximum	Maximum	Maximum	Units
Signal Name	SRC 100 [1][2]	9.87400	-	9.99900	10.00000	10.00100	-	10.17630	ns
	CPU 100 [1][2]	9.91400	-	9.99900	10.00000	10.00100	-	10.13630	ns
	CPU 133 [1][2]	7.41425	-	7.49925	7.50000	7.50075	-	7.62345	ns
	CPU 166 [1][2]	5.91440	-	5.99940	6.00000	6.00060	-	6.11576	ns
	DOT 96 [1][2]	10.16560	-	10.41560	10.41670	10.41770	-	10.66770	ns

1. Confirmed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 14.31818MHz.

2.9 Power Management

Table 1. REF Power Management

PD	SMBus Register OE	REF
0	Enable	Running
1	X	Low
0	Disable	Low

Table 2. CPU Power Management

PD	CPU_STOP#	SMBus Register OE	CPU	CPU#
0	**1**	Enable	Running	Running
1	X	Enable	Low/20K	Low
0	**0**	Enable	High	Low
0	X	**Disable**	Low/20K	Low

Table 3. SRC, LCD, DOT Power Management

PD	CR_x#	SMBus Register OE	SRC	SRC#	DOT/LCD	DOT#/LCD#
0	**0**	Enable	Running	Running	Running	Running
1	X	X	Low/20K	Low	Low/20K	Low
0	**1**	Enable	Low/20K	Low	Running	Running
0	X	**Disable**	Low/20K	Low	Low/20K	Low

2.10 Frequency and Spread Selection

Table 4. CPU Frequency Select

FS_LC [1]	FS_LB [1]	CPU MHz	SRC MHz	DOT MHz	LCD MHz	REF MHz
0	0	133.33	100.00	96.00	100.00	14.318
0	1	166.67				
1	0	100.00				
1	1	66.67				

1. FSLC is a low-threshold input. Please see VIL_FS and VIH_FS specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification table.

Table 5. LCD Spread Select (Pin 20/21)

B1b5	B1b4	B1b3	Spread %	Comment
0	0	0	-0.5%	LCD100
0	0	1	-1%	LCD100
0	1	0	-2%	LCD100
0	1	1	-2.5%	LCD100
1	0	0	±0.25%	LCD100

Table 5. LCD Spread Select (Pin 20/21)

B1b5	B1b4	B1b3	Spread %	Comment
1	0	1	±0.5%	LCD100
1	1	0	±1%	LCD100
1	1	1	±1.25%	LCD100

Table 6. CPU N-step Programming

CPU (MHz)	P	Default N (hex)	Fcpu
133.33	3	64	= 4MHz x N/P
166.67	3	7D	= 4MHz x N/P
100.00	4	64	= 4MHz x N/P
200.00	2	64	= 4MHz x N/P

3. General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 7. Byte 0 – PLL and Divider Enable Register

Bit(s)	Name	Description	Type	0	1	Default
7	PLL1 Enable	This bit controls whether the PLL driving the CPU and SRC clocks is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6	PLL2 Enable	This bit controls whether the PLL driving the DOT and clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5	PLL3 Enable	This bit controls whether the PLL driving the LCD clock is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4	Reserved					0
3	CPU Divider Enable	This bit controls whether the CPU output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
2	SRC Output Divider Enable	This bit controls whether the SRC output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 7 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
1	LCD Output Divider Enable	This bit controls whether the LCD output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 5 is set to '0'.	RW	0 = Disabled	1 = Enabled	1
0	DOT Output Divider Enable	This bit controls whether the DOT output divider is enabled or not. NOTE: This bit should be automatically set to '0' if bit 6 is set to '0'.	RW	0 = Disabled	1 = Enabled	1

Table 8. Byte 1 – PLL SS Enable/Control Register

Bit(s)	Name	Description	Type	0	1	Default
7	PLL1 SS Enable	This bit controls whether PLL1 has spread enabled or not. Spread spectrum for PLL1 is set at -0.5% down-spread. Note that PLL1 drives the CPU and SRC clocks.	RW	0 = Disabled	1 = Enabled	1
6	PLL3 SS Enable	This bit controls whether PLL3 has spread enabled or not. Note that PLL3 drives the SSC clock, and that the spread spectrum amount is set in bits 3-5.	RW	0 = Disabled	1 = Enabled	1
5	PLL3 FS Select	These 3 bits select the frequency of PLL3 and the SSC clock when Byte 1 Bit 6 (PLL3 Spread Spectrum Enable) is set.	RW	See LCD Spread Select (Pin 20/21) table		0
4						0
3						0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 9. Byte 2 – Output Enable Register

Bit(s)	Name	Description	Type	0	1	Default
7	CPU0 Enable	This bit controls whether the CPU[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
6	CPU1 Enable	This bit controls whether the CPU[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
5	CPU2 Enable	This bit controls whether the CPU[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4	SRC0 Enable	This bit controls whether the SRC[0] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
3	SRC1 Enable	This bit controls whether the SRC[1] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
2	SRC2 Enable	This bit controls whether the SRC[2] output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
1	DOT Enable	This bit controls whether the DOT output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
0	LCD100 Enable	This bit controls whether the LCD output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1

Table 10. Byte 3 – Output Control Register

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	REF Enable	This bit controls whether the REF output buffer is enabled or not.	RW	0 = Disabled	1 = Enabled	1
4	REF Slew	These bits control the edge rate of the REF clock.	RW	00 = Slow Edge Rate 01 = Medium Edge Rate 10 = Fast Edge Rate 11 = Reserved		10
3						
2	CPU0 Stop Enable	This bit controls whether the CPU[0] output buffer is free-running or stoppable. If it is set to stoppable the CPU[0] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
1	CPU1 Stop Enable	This bit controls whether the CPU[1] output buffer is free-running or stoppable. If it is set to stoppable the CPU[1] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0
0	CPU2 Stop Enable	This bit controls whether the CPU[2] output buffer is free-running or stoppable. If it is set to stoppable the CPU[2] output buffer will be disabled with the assertion of CPU_STP#.	RW	Free Running	Stoppable	0

Table 11. Byte 4 – CPU PLL N Register

Bit(s)	Name	Control Function	Type	0	1	Default
7	Reserved					1
6	Reserved					1
5	Reserved					1
4	Reserved					1
3	Reserved					1
2	Reserved					1
1	Reserved					1
0	CPU N Div8	N Divider Prog bit 8	RW			0

Table 12. Byte 5 – CPU PLL/N Register

Bit(s)	Name	Control Function	Type	0	1	Default
7	CPU N Div7	See CPU N-step Programming table	RW	Default depends on latched input frequency. Default for CPU = 166 is 7Dh. Default for all other frequencies is 64h.		X
6	CPU N Div6		RW			X
5	CPU N Div5		RW			X
4	CPU N Div4		RW			X
3	CPU N Div3		RW			X
2	CPU N Div2		RW			X
1	CPU N Div1		RW			X
0	CPU N Div0		RW			X

Table 13. Byte 6 – Reserved

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					1
6	Reserved					1
5	Reserved					1
4	Reserved					1
3	Reserved					0
2	Reserved					0
1	Reserved					1
0	Reserved					1

Table 14. Byte 7 – Reserved

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 15. Byte 8 – Reserved

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 16. Byte 9 – LCD100 PLL N Register

Bit(s)	Name	Description	Type	0	1	Default
7	LCD100 N Div7	LCD100 = (4MHz x N)/4 Default frequency is (4 x 64h)/4 = 100MHz	R	Write Byte 9 to 64h BEFORE enabling N programming		1
6	LCD100 N Div6		R			0
5	LCD100 N Div5		R			0
4	LCD100 N Div4		R			1
3	LCD100 N Div3		R			0
2	LCD100 N Div2		R			1
1	LCD100 N Div1		R			1
0	LCD100 N Div0		R			0

Table 17. Byte 10 – Status Readback Register

Bit(s)	Pin #	Name	Description	Type	0	1	Default
7	37	FSB	Frequency Select B	R	See CPU Frequency Select table		Latch
6	9	FSC	Frequency Select C	R			Latch
5	24	CR0# Readbk	Real time CR0# State Indicator	R	CR0# is Low	CR0# is High	X
4	28	CR1# Readbk	Real time CR1# State Indicator	R	CR1# is Low	CR1# is High	X
3	36	CR2# Readbk	Real time CR2# State Indicator	R	CR2# is Low	CR2# is High	X
2		Reserved					0
1		Reserved					0
0		Reserved					0

Table 18. Byte 11 – Revision ID/Vendor ID Register

Bit(s)	Name	Description	Type	0	1	Default
7	Rev Code Bit 3	Revision ID (0 for A rev)	R	Vendor specific		X
6	Rev Code Bit 2		R			X
5	Rev Code Bit 1		R			X
4	Rev Code Bit 0		R			X
3	Vendor ID bit 3	Vendor ID	R			0
2	Vendor ID bit 2		R			0
1	Vendor ID bit 1		R			0
0	Vendor ID bit 0		R			1

Table 19. Byte 12 – Device ID Register

Bit(s)	Name	Description	Type	0	1	Default
7	DEV_ID3	Device ID MSB	R			0
6	DEV_ID2	Device ID 2	R			0
5	DEV_ID1	Device ID 1	R			1
4	DEV_ID0	Device ID LSB	R			1
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 20. Byte 13 – Reserved

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 21. Byte 14 – Reserved

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	Reserved					0
0	Reserved					0

Table 22. Byte 15 – Byte Count Register

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	BC5	Byte Count 5	RW	Specifies Number of bytes to be read back during an SMBus read. Default is 0xF.		0
4	BC4	Byte Count 4	RW			0
3	BC3	Byte Count 3	RW			1
2	BC2	Byte Count 2	RW			1
1	BC1	Byte Count 1	RW			1
0	BC0	Byte Count LSB	RW			1

Bytes 16:40 are reserved

Table 23. Byte 41 – N Program Enable Register

Bit(s)	Name	Description	Type	0	1	Default
7	Reserved					0
6	Reserved					0
5	Reserved					0
4	Reserved					0
3	Reserved					0
2	Reserved					0
1	CPU N Enable	Enables CPU N programming	RW	Disabled	Enabled	0
0	LCD N Enable	Enables LCD N programming	RW	Disabled	Enabled	0

4. Test Clarification

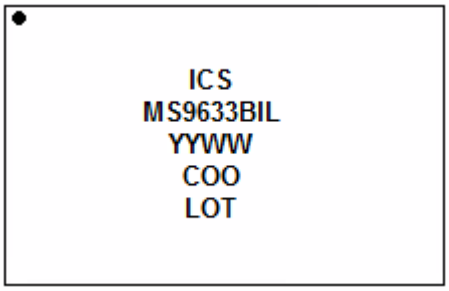
Table 24. Test Clarification

Comments	HW		
	TEST_SEL HW Pin	TEST_MODE HW Pin	Output
	<0.35V	X	Normal
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode TEST_MODE --> low Vth input TEST_MODE is a real time input	>0.7V	<0.35V	HI-Z
	>0.7V	>0.7V	REF/N

5. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

6. Marking Diagram



- Lines 1 and 2: truncated part number.
- Line 3: “YY” is the last two digits of the year; “WW” is the work week the part was assembled.
- Line 4: “COO” denotes country of origin.
- Line 5: “LOT” denotes sequential lot number.

7. Ordering Information

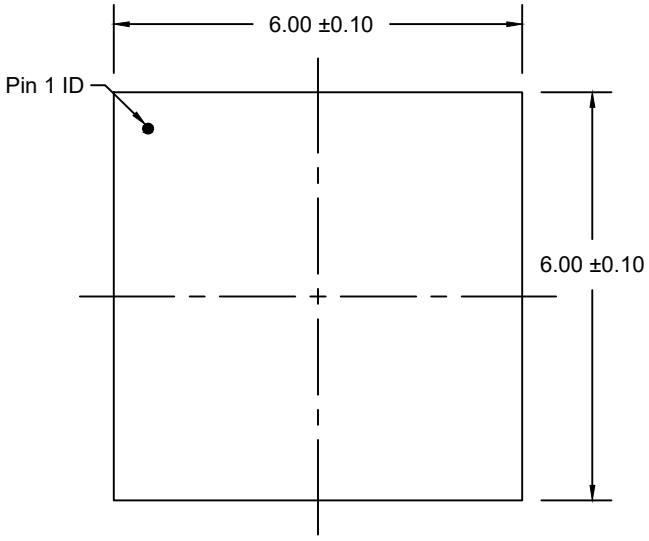
Part Number	Package Description	Carrier Type	Temperature Range
9UMS9633BKILF	48-VFQFPN, 6 × 6 mm	Tray	-40 to +85°C
9UMS9633BKILFT		Tape and Reel	

8. Revision History

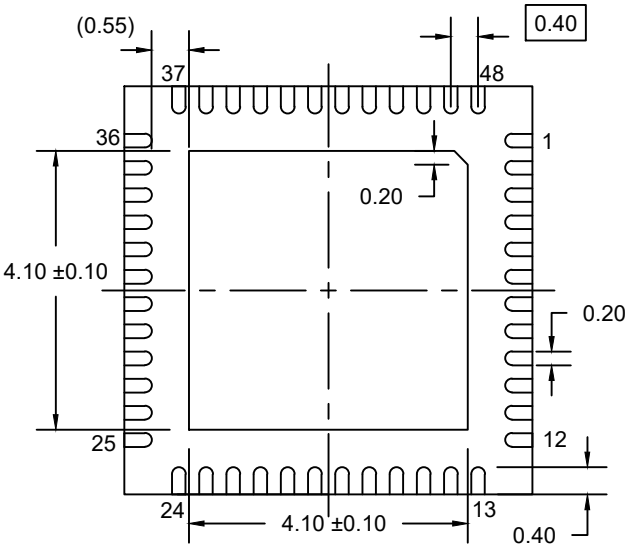
Revision	Date	Description
1.01	Jul 29, 2024	▪ Updated the package link in Ordering Information. ▪ Completed other minor changes.
1.00	Jan 18, 2022	Initial release.

Package Outline Drawing

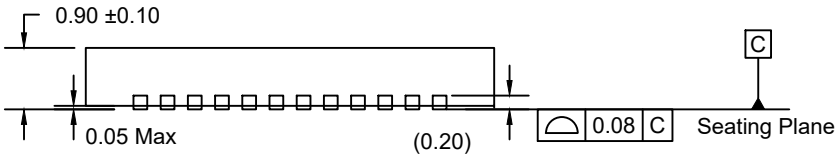
Package Code: NDG48P1
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4212-01, Revision: 02, Date Created: Nov 18, 2022



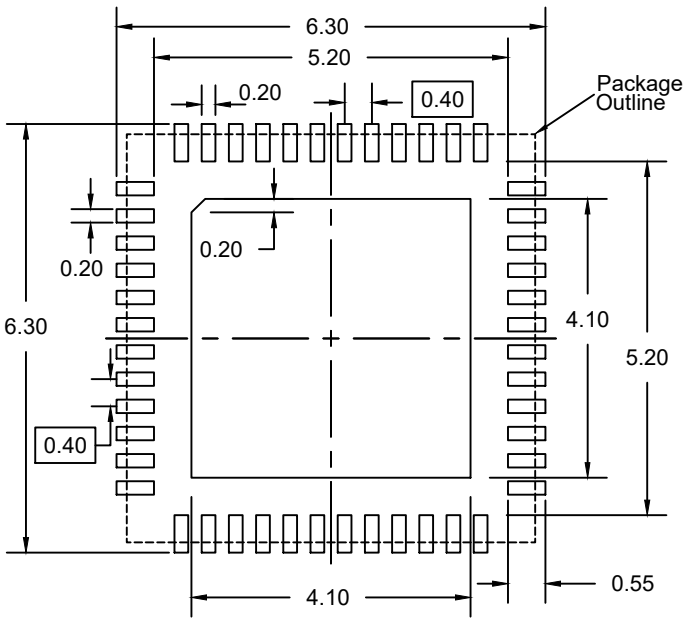
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.50 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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