

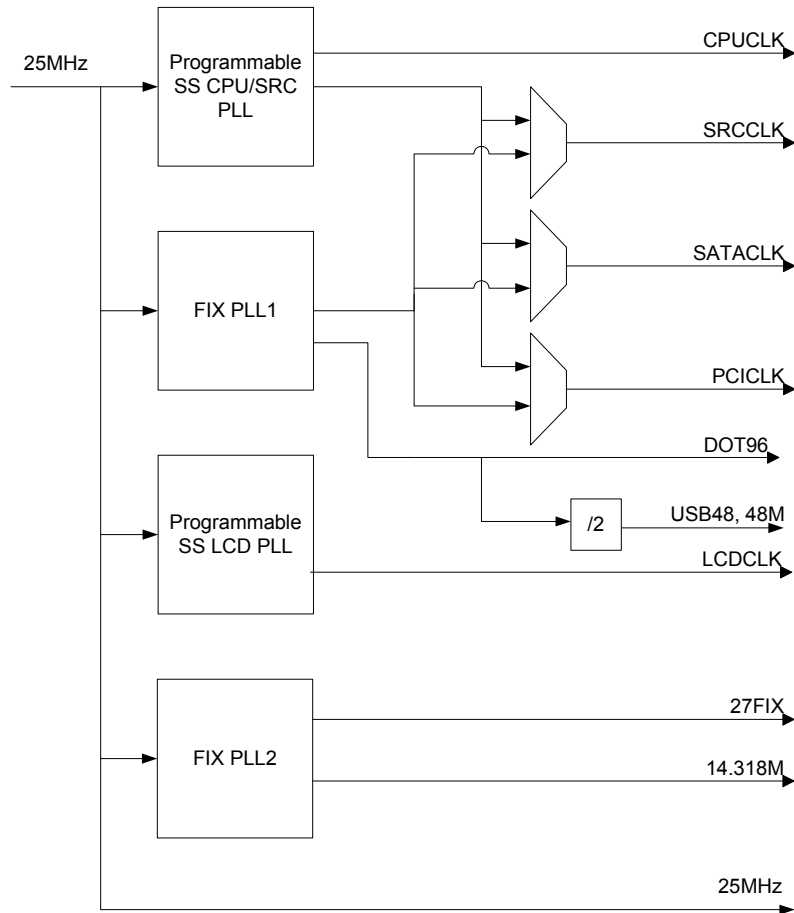
Pin Descriptions

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|-------|------------------------|------|--|
| 1 | X2 | OUT | Crystal output, nominally 25MHz |
| 2 | X1 | IN | Crystal input, nominally 25MHz |
| 3 | VDD25_3.3 | PWR | Power pin for crystal and 25MHz output, nominal 3.3V |
| 4 | 25M | OUT | 3.3V 25MHz clock output |
| 5 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 6 | SCLK_3.3 | OUT | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 7 | VDDPCI_3.3 | PWR | Power supply for PCI clocks, nominal 3.3V |
| 8 | vITP_EN/PCI_F1_2x | I/O | ITP enable latched input ITP_Enable Selects the functionality of the CPU_ITP/SRC output as follows: 1 = CPU_ITP output 0 = SRC1 output / Free-Running 3.3V PCI clock output, default to drive 2 loads. |
| 9 | FSLB/PCI2_2x | I/O | 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil_FS and Vih_FS values / 3.3V PCI clock output, default to drive 2 loads. |
| 10 | CLKREQA#/PCI3_2x | I/O | 3.3V real-time output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. Pin function is programmable through SMBus. See CLKREQ# Control Table and SRC Power Management Table for details 0 = controlled outputs are enabled 1 = controlled outputs are Low/Low / 3.3V PCI clock output, default to drive 2 loads. . |
| 11 | GNDPCI | PWR | Ground pin for the PCI outputs |
| 12 | GND14M | PWR | Ground pin for the 14.318MHz output |
| 13 | 14M_2X/FSLC | I/O | 3.3V 14.318 MHz clock output, default to drive 2 loads / 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. |
| 14 | VDD14_3.3 | PWR | Power pin for 14.318MHz output, nominal 3.3V |
| 15 | VDD48_3.3 | PWR | Power pin for 48MHz outputs, nominal 3.3V |
| 16 | ^DOT96_SEL/USB48M | I/O | Input latched pin to select Pin23/24 as DOT 96MHz clock or SRC clock 1 = DOT96 output 0 = SRC5 output / 3.3V 48MHz USB clock output. |
| 17 | CLKREQC#/48M | I/O | 3.3V real-time output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. Pin function is programmable through SMBus. See CLKREQ# Control Table and SRC Power Management Table for details 0 = controlled outputs are enabled 1 = controlled outputs are Low/Low / 3.3V 48MHz clock output |
| 18 | GND48 | PWR | Ground pin for 48MHz outputs |
| 19 | CLKREQB# | IN | 3.3V real-time output enable for PCI Express (SRC) outputs. SMBus selects which outputs are controlled. 0 = controlled outputs are enabled 1 = controlled outputs are Low/Low |
| 20 | VDD27 | PWR | Power pin for 27MHz output , nominal 3.3V |
| 21 | vSEL_PCI/27M_PCI4_2X | I/O | 3.3V input latch pin to select this pin as 27M output or PCI4 clock output. This pin has an internal pulldown resistor. Latch functionality is as follows: 0 = 27MHz output 1 = 33.33MHz PCI output |
| 22 | GND27 | PWR | Ground pin for the 27MHz output |
| 23 | DOT96_LPRS/SRC5_LPRS | OUT | True clock of push-pull DOT96 or SRC clock with integrated series resistor. No 50 ohm pull down needed. Default is pending on Pin16 DOT96_SEL. |
| 24 | DOT96#_LPRS/SRC5#_LPRS | OUT | Complement clock of push-pull DOT96 or SRC clock with integrated series resistor. No 50 ohm pull down needed. Default is pending on Pin16 DOT96_SEL. |
| 25 | VDD_CORE_1.5 | PWR | Power pin for core PLL's, nominal 1.5V. |
| 26 | LCD100_LPRS | OUT | True clock of differential push-pull LCD100 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 27 | LCD100#_LPRS | OUT | Complementary clock of differential push-pull LCD100 output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 28 | GNDLCD | PWR | Ground pin for LCD clock output |

Pin Descriptions (cont.)

| | | | |
|----|---------------------|-----|---|
| 29 | GNDSATA | PWR | Ground pin for the SATA outputs |
| 30 | SATA#_LPRS | OUT | Complementary clock of low power differential push-pull SATA clock pair with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 31 | SATA_LPRS | OUT | True clock of low power differential push-pull SATA clock pair with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 32 | SRC4#_LPRS | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 33 | SRC4_LPRS | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 34 | VDDSRC_LVIO | PWR | Power pin for SRC I/O, nominally 1.05V to 1.5V from external power supply |
| 35 | PCI_STOP#_3.3 | IN | Stops all stoppable PCI, SATA and SRC clocks when low. Free-Running PCI, SATA and SRC clocks are not effected by this input. This input is 3.3V tolerant. |
| 36 | SRC3#_LPRS | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 37 | SRC3_LPRS | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 38 | SRC6#_LPRS | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 39 | SRC6_LPRS | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 40 | GNDSRC | PWR | Ground pin for the SRC outputs |
| 41 | SRC2#_LPRS | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 42 | SRC2_LPRS | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 43 | SRC#7_LPRS | OUT | Complementary clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 44 | SRC7_LPRS | OUT | True clock of differential 0.8V push-pull SRC output with integrated 33ohm series resistor. No 50ohm resistor to GND needed. |
| 45 | CPU_STOP#_3.3 | IN | Stops all stoppable CPU clocks when enabled. This is a 3.3V tolerant input. |
| 46 | CPU_ITP#/SRC1#_LPRS | OUT | Complementary clock of low power differential CPU_ITP/SRC pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed. The pin function is determined by the latched value on ITP_EN: 0 = SRC1# 1 = CPU_ITP# |
| 47 | CPU_ITP/SRC1_LPRS | OUT | True clock of low power differential CPU_ITP/SRC pair with integrated 33ohm series resistor. No 50ohm resistor to GND needed. The pin function is determined by the latched value on ITP_EN: 0 = SRC1 1 = CPU_ITP |
| 48 | VDD_CORE_1.5 | PWR | Power pin for core PLL, nominal 1.5V |
| 49 | VDDCPU_LVIO | PWR | Power pin for CPU I/O, nominally 1.05V to 1.5V from external power supply |
| 50 | CPU1#_LPRS | OUT | Complementary clock of differential pair 0.8V push-pull CPU output with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 51 | CPU1_LPRS | OUT | True clock of differential pair 0.8V push-pull CPU output with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 52 | GNDCPU | PWR | Ground pin for the CPU outputs |
| 53 | CPU0#_LPRS | OUT | Complementary clock of differential pair 0.8V push-pull CPU output with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 54 | CPU0_LPRS | OUT | True clock of differential pair 0.8V push-pull CPU output with integrated 33ohm series resistor. No 50 ohm resistor to GND needed. |
| 55 | CLKPWRGD/PD#_3.3 | IN | This 3.3V LVTTTL input notifies device to sample latched inputs and start up on first high assertion or exit Power Down Mode on subsequent assertions. When WLAN enable in Byte13 bit 5 =1, device will enter Wake-On-LAN mode with 25MHz being free-running. 1 = Normal operation 0 = Power Down Mode or Wake-On-LAN mode Note: For lowest power saving during WOL mode, it is mandatory to connect 3.3V and 1.5V core VDD pins to standby power and suspend/remove VDDIO pins. |
| 56 | GND25 | PWR | Ground pin for 25MHz |

Block Diagram



Series Resistors for Single Ended Outputs

| D.C.Drive Strength | Number of Loads to Drive | Match Point for N & P Voltage / Current (mA) | Number of Loads Actually Driven. | | |
|--------------------|--------------------------|--|----------------------------------|-------------|--------------|
| | | | 1 Load Rs = | 2 Loads Rs= | 3 Loads Rs = |
| | 1 | 0.56 / 33 (17Ω) | 33Ω [39Ω] | - | - |
| | 2 | 0.92 / 66 (14Ω) | 39Ω [43Ω] | 22Ω [27Ω] | - |

Notes:

1. Preferred drive strengths using CK505 clock sources. Transmission lines to load do not share series resistors.
2. Desktop/Mobile Platforms with $Z_o = 50/55$ ohms use the first resistor value.
3. Systems with $Z_o = 60$ ohms use the resistor values in brackets [].

Table 1: CPU/SRC PLL Spread Frequency Selection

| CPU/SRC SS Select (B1b6) | SS1 (B1b5) | SS0 (B1b4) | FSLC (B0b7) | FSLB (B0b6) | SPREAD % | CPU MHz | SRC MHz | SATA MHz | PCI MHz |
|--------------------------------|---------------|---------------|----------------|----------------|---------------|---------------|---------------|---------------|--------------|
| 0 | 0 | 0 | 0 | 0 | -0.50% | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 0 | 0 | 1 | -0.50% | 166.67 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 0 | -0.50% | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 0 | 1 | 1 | -0.50% | 200.00 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 0 | 0 | -0.40% | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 0 | 1 | -0.40% | 166.67 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 0 | -0.40% | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 0 | 1 | 1 | 1 | -0.40% | 200.00 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 0 | 0 | -0.30% | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 0 | 1 | -0.30% | 166.67 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 1 | 0 | -0.30% | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 0 | 1 | 1 | -0.30% | 200.00 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 0 | 0 | OFF | 133.33 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 0 | 1 | OFF | 166.67 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 1 | 0 | OFF | 100.00 | 100.00 | 100.00 | 33.33 |
| 0 | 1 | 1 | 1 | 1 | OFF | 200.00 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 0 | 0 | +/-0.25% | 133.33 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 0 | 1 | +/-0.25% | 166.67 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 1 | 0 | +/-0.25% | 100.00 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 0 | 1 | 1 | +/-0.25% | 200.00 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 1 | 0 | 0 | +/-0.20% | 133.33 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 1 | 0 | 1 | +/-0.20% | 166.67 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 1 | 1 | 0 | +/-0.20% | 100.00 | 100.00 | 100.00 | 33.33 |
| 1 | 0 | 1 | 1 | 1 | +/-0.20% | 200.00 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 0 | 0 | 0 | +/-0.15% | 133.33 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 0 | 0 | 1 | +/-0.15% | 166.67 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 0 | 1 | 0 | +/-0.15% | 100.00 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 0 | 1 | 1 | +/-0.15% | 200.00 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 1 | 0 | 0 | OFF | 133.33 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 1 | 0 | 1 | OFF | 166.67 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 1 | 1 | 0 | OFF | 100.00 | 100.00 | 100.00 | 33.33 |
| 1 | 1 | 1 | 1 | 1 | OFF | 200.00 | 100.00 | 100.00 | 33.33 |

* Bold is default

Table 2: LCD Spread Selection Table

| FS2 | FS1 | FS0 | LCD SS | SPREAD | LCD100 |
|----------|----------|----------|----------|---------------|---------------|
| 0 | 1 | 0 | 0 | -0.50% | 100.00 |
| 0 | 1 | 1 | 0 | -1.0% | 100.00 |
| 1 | 0 | 0 | 0 | -1.5% | 100.00 |
| 1 | 0 | 1 | 0 | -2.0% | 100.00 |
| 1 | 1 | 0 | 0 | -2.50% | 100.00 |
| 0 | 1 | 0 | 1 | +/-0.25% | 100.00 |
| 0 | 1 | 1 | 1 | +/-0.5% | 100.00 |
| 1 | 0 | 0 | 1 | +/-0.75% | 100.00 |
| 1 | 0 | 1 | 1 | +/-1.0% | 100.00 |
| 1 | 1 | 0 | 1 | +/-1.25% | 100.00 |

* Bold is default

Power Distribution Table

| Pin Number | | | | Description |
|------------|----------|---------------|--------|---|
| 3.3V VDD | 1.5V VDD | 1.05-1.5V VDD | GND | |
| 3 | - | - | 56 | 25MHz Crystal I/O; Internal Control Logic; 25MHz Output |
| 7 | - | - | 11 | PCICLK Outputs |
| 14 | - | - | 12 | 14.318MHz & 27MHz outputs, 14/27MHz PLL Digital |
| 15 | - | - | 18 | 48MHz output |
| 20 | - | - | 22 | 27MHz output, 14/27MHz PLL analog |
| - | 25 | - | 28, 29 | DOT96 Fix PLL Analog & Digital, LCD100 PLL Analog & Digital |
| - | - | 34 | 40 | SRC Outputs |
| - | 48 | - | 52 | CPU/SRC PLL Analog & Digital |
| - | - | 49 | 52 | CPU Outputs |

CPU Power Management Table

| CLKPWRGD/P D#_3.3 | SMBus Register OE | CPU_STOP# | CPU (0, 1, ITP) | |
|----------------------|----------------------|-----------|-----------------|-----------|
| | | | True O/P | Comp. O/P |
| 1 | Enable | 1 | Running | Running |
| 1 | Enable | 0 | High | Low |
| 0 | X | X | Low/20K | Low |
| X | Disable | X | Low/20K | Low |

DOT96 and SATA Power Management Table

| CLKPWRGD/P D#_3.3 | SMBus Register OE | PCI_STOP# | CLKREQ# | SATA | | SATA | | DOT96 | |
|----------------------|----------------------|-----------|---------|--------------------|-----------|------------------------|-----------|----------|-----------|
| | | | | PEREQC# Controlled | | PEREQC# Not-Controlled | | True O/P | Comp. O/P |
| | | | | True O/P | Comp. O/P | True O/P | Comp. O/P | | |
| 1 | Enable | 1 | 0 | Running | Running | Running | Running | Running | Running |
| 1 | Enable | 1 | 1 | Low/20K | Low | Running | Running | Running | Running |
| 0 | X | X | X | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| X | Disable | X | X | Low/20K | Low | Low/20K | Low | Low/20K | Low |

SRC Power Management Table

| CLKPWRGD/P D#_3.3 | SMBus Register OE | PCI_STOP# | CLKREQx# | SRC controlled by CLKREQx# | | SRC not controlled by CLKREQx# | | SRC controlled by CLKREQx# | | SRC not controlled by CLKREQx# | |
|----------------------|----------------------|-----------|----------|-------------------------------|-----------|-----------------------------------|-----------|-------------------------------|-----------|-----------------------------------|-----------|
| | | | | Free-Running | | | | Stoppable | | | |
| | | | | True O/P | Comp. O/P | True O/P | Comp. O/P | True O/P | Comp. O/P | True O/P | Comp. O/P |
| 1 | Enable | 1 | 0 | Running | Running | Running | Running | Running | Running | Running | Running |
| 1 | Enable | 1 | 1 | Low/20K | Low | Running | Running | Low/20K | Low | Running | Running |
| 1 | Enable | 0 | 0 | Running | Running | Running | Running | High | Low | High | Low |
| 1 | Enable | 0 | 1 | Low/20K | Low | Running | Running | Low/20K | Low | High | Low |
| 0 | Enable | X | X | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low |
| X | Disable | X | X | Low/20K | Low | Low/20K | Low | Low/20K | Low | Low/20K | Low |

Single-ended Power Management Table

| CLKPWRGD/P D#_3.3 | SMBus Register OE | PCI_STOP# | PCL_F1, PCI2, PCI4 | | PCI3 | | 25M | | 14.318M | USB48 | 48M | 27MHz |
|----------------------|----------------------|-----------|--------------------|-----------|----------|-----------|----------------|-----------------|---------|---------|---------|---------|
| | | | Free-run | Stoppable | Free-run | Stoppable | WOL Enabled | WOL Disabled | | | | |
| | | | | | | | | | | | | |
| 1 | Enable | 1 | Running | Running | Running | Running | Running | Running | Running | Running | Running | Running |
| 1 | Enable | 0 | Running | Low | Running | Low | Running | Running | Running | Running | Running | Running |
| 0 | Enable | X | Hi-Z | Hi-Z | Low | Low | Running | Low | Hi-Z | Hi-Z | Low | Hi-Z |
| 0 | Disable | X | Hi-Z | Hi-Z | Low | Low | Low | Low | Hi-Z | Hi-Z | Low | Hi-Z |
| 1 | Disable | X | Low | Low | Low | Low | Low | Low | Low | Low | Low | Low |

CLKREQ# Control Table

| CLKREQ# | SRC/SATA controlled |
|---------|------------------------|
| A | SRC1, 2, 3 |
| B | SRC4, 6 |
| C | SRC5, 7, SATA |

General SMBus Serial Interface Information for 9VRS4339

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- IDT clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a Stop bit

| Index Block Write Operation | | | |
|-----------------------------|-----------|----------------------|-----|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

| Read Address | Write Address |
|-------------------|-------------------|
| D3 _(H) | D2 _(H) |

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte N+X-1
- IDT clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation | | | |
|----------------------------|-----------------|----------------------|-------------------|
| Controller (Host) | | IDT (Slave/Receiver) | |
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | Data Byte Count=X |
| ACK | | | |
| ACK | | X Byte | Beginning Byte N |
| | | | O |
| | | | O |
| | | | O |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

SMBus Table: Frequency Select, PD Config Source Select Register

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|--------|--------------|---------------------------------------|------|---|-----------------|---------|
| Bit 7 | FSLC | Freq Select Bit 1 | RW | See Table 1: CPU/SRC PLL Frequency & Spread Selection Table | | Latch |
| Bit 6 | FSLB | Freq Select Bit 0 | RW | | | Latch |
| Bit 5 | CPU1 STOP EN | Enables Control of CPU1 with CPU_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 4 | CPU0 STOP EN | Enables Control of CPU0 with CPU_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 3 | PCI_SSEL | PCI Source Select | RW | CPU/SRC SS PLL | FIX PLL | 0 |
| Bit 2 | SRC_SSEL | SRC Source Select | RW | CPU/SRC SS PLL | FIX PLL | 0 |
| Bit 1 | SATA_SSEL | SATA Source Select | RW | CPU/SRC SS PLL | FIX PLL | 0 |
| Bit 0 | PD Config | Forces "cold" start during PD | RW | Reset and Relatch | Normal PD# mode | 1 |

SMBus Table: CPU, LCD SS and DOT96/SRC5 Control Register

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------|---|------|---|---------------|---------|
| Bit 7 | DOT96_SEL | Selects DOT96 or SRC5 | R | SRC5 | DOT96 | Latch |
| Bit 6 | CPU/SRC SS Select | Selects Center or Down Spread for CPU & SRC | RW | Down Spread | Center Spread | 0 |
| Bit 5 | CPU SS1 | CPU SS Magnitude MSB | RW | See Table 1: CPU/SRC PLL Frequency & Spread Selection Table | | 0 |
| Bit 4 | CPU SS0 | CPU SS Magnitude LSB | RW | | | 0 |
| Bit 3 | LCD SS2 | LCD SS Magnitude MSB | RW | See Table 2: LCDCLK Spread Spectrum Table | | 1 |
| Bit 2 | LCD SS1 | LCD SS Magnitude | RW | | | 1 |
| Bit 1 | LCD SS0 | LCD SS Magnitude LSB | RW | | | 0 |
| Bit 0 | LCD SS Select | Selects Center or Down Spread for LCDCLK | RW | Down Spread | Center Spread | 0 |

SMBus Table: Output Enable Control Register

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------|--|------|--------------|-----------|---------|
| Bit 7 | REF OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | 48M OE (Pin17) | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | USB48M OE (Pin16) | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | 25M OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | PCI3 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | PCI2 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | PCI_F1 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | CPU_ITP STOP EN | Enables Control of CPU_ITP with CPU_STOP | RW | Free-Running | Stoppable | 0 |

SMBus Table: Output Enable Control Register

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|------------------------|------|----------------|------------|---------|
| Bit 7 | SRC7 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | SRC6 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | CLKREQC# Control | SRC5 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 4 | CLKREQC# Control | SRC7 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 3 | PCI4/27M OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | LCDCLK OE | LCDPLL & Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | SRC4 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 0 | SATA OE | Output Enable | RW | Disable | Enable | 1 |

SMBus Table: Output Enable and SS Enable Control Register

| Byte 4 | Name | Control Function | Type | 0 | 1 | Default |
|--------|-------------------|--------------------|------|----------------|------------|---------|
| Bit 7 | SRC3 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 6 | SRC2 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 5 | CPU_ITP/SRC1 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 4 | DOT96/SRC5 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 3 | CPU1 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 2 | CPU0 OE | Output Enable | RW | Disable | Enable | 1 |
| Bit 1 | CPU/SRC PLL SS EN | Output Enable | RW | SS OFF | SS ON | 1 |
| Bit 0 | CLKREQC# Control | SATA is controlled | RW | Not Controlled | Controlled | 0 |

SMBus Table: CLKREQ Control Register

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------------------|--------------------|------|----------------|------------|---------|
| Bit 7 | CLKREQA# EN | CLKREQA# Enable | RW | Disable | Enable | 0 |
| Bit 6 | CLKREQA# Control | SRC1 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 5 | CLKREQA# Control | SRC2 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 4 | CLKREQA# Control | SRC3 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 3 | CLKREQB# EN | CLKREQB# Enable | RW | Disable | Enable | 0 |
| Bit 2 | CLKREQB# Control | SRC4 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 1 | CLKREQB# Control | SRC6 is controlled | RW | Not Controlled | Controlled | 0 |
| Bit 0 | CLKREQC# EN | CLKREQC# Enable | RW | Disable | Enable | 0 |

Note: To enable CLKREQC function, please write "0" to Byte 9 bit 7 and "1" to Byte 5 bit 0. To select which output to control, please make necessary selection in Bytes 3 & 4.

Byte 6 Reserved Register

SMBus Table: Revision and Vendor ID Register

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|--------|------|------------------|------|----------------|---|---------|
| Bit 7 | RID3 | Revision ID | R | B rev = 0001 | | 0 |
| Bit 6 | RID2 | | R | | | 0 |
| Bit 5 | RID1 | | R | | | 0 |
| Bit 4 | RID0 | | R | | | 1 |
| Bit 3 | VID3 | VENDOR ID | R | 0001 = ICS/IDT | | 0 |
| Bit 2 | VID2 | | R | | | 0 |
| Bit 1 | VID1 | | R | | | 0 |
| Bit 0 | VID0 | | R | | | 1 |

SMBus Table: Output Control Register

| Byte 8 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------------|----------------------------|------|--------------|--------------|---------|
| Bit 7 | 48M (Pin17) SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 6 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 5 | 27M / PCI4 SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 4 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 3 | Reserved | Reserved | RW | - | - | 0 |
| Bit 2 | PCI_SKEW_MODE | PCICLK Skew Mode Control | RW | PCI Aligned | PCI Delayed | 0 |
| Bit 1 | LCD_AMP<1> | LCD Amplitude Control bit1 | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 0 | LCD_AMP<0> | LCD Amplitude Control bit0 | RW | 10 = 900mV | 11 = 1000mV | 1 |

Note: A system reset maybe required when switching between PCICLK aligned and skew mode

SMBus Table: Byte Count Register

| Byte 9 | Name | Control Function | Type | 0 | 1 | Default |
|--------|----------|------------------------|------|---|-----|---------|
| Bit 7 | 48M_SEL | Selects 48M or CLKREQC | RW | CLKREQC | 48M | 1 |
| Bit 6 | Reserved | Reserved | RW | - | - | 0 |
| Bit 5 | Reserved | Reserved | RW | - | - | 0 |
| Bit 4 | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is 0F or 1F = 15 bytes. | | 0 |
| Bit 3 | BC3 | | RW | | | 1 |
| Bit 2 | BC2 | | RW | | | 1 |
| Bit 1 | BC1 | | RW | | | 1 |
| Bit 0 | BC0 | | RW | | | 1 |

Note: To enable CLKREQC function, please write "0" to Byte 9 bit 7 and "1" to Byte 5 bit 0. To select which output to control, please make necessary selection in Bytes 3 & 4.

SMBus Table: Output Control Register

| Byte 10 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------------------|-------------------|------|--------------|--------------|---------|
| Bit 7 | USB48M (Pin16) SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 6 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 5 | REF SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 4 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 3 | PCI3 SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 2 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 1 | 25M SR | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 0 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |

SMBus Table: Output Control Register

| Byte 11 | Name | Control Function | Type | 0 | 1 | Default |
|---------|-------|------------------------|------|--------------|--------------|---------|
| Bit 7 | CPU | Differential Slew Rate | RW | 0=2.5V/ns | 1=4V/ns | 1 |
| Bit 6 | SRC | Differential Slew Rate | RW | 0=2.5V/ns | 1=4V/ns | 1 |
| Bit 5 | SATA | Differential Slew Rate | RW | 0=2.5V/ns | 1=4V/ns | 1 |
| Bit 4 | DOT96 | Differential Slew Rate | RW | 0=2.5V/ns | 1=4V/ns | 1 |
| Bit 3 | PCI2 | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 2 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |
| Bit 1 | PCI1 | Slew Rate Control | RW | 00 = 1.5V/ns | 01 = 2.0V/ns | 0 |
| Bit 0 | | | RW | 10 = 2.6V/ns | 11 = 3.3V/ns | 0 |

SMBus Table: M/N Enable & Output Stop Control Register

| Byte 12 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------------|---|------|--------------|-----------|---------|
| Bit 7 | CPU/SRC PLL M/N En | Enables M/N programming for CPU/SRC PLL | RW | Disable | Enable | 0 |
| Bit 6 | SRC1 STOP EN | Enables Control of SRC1 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 5 | SRC2 STOP EN | Enables Control of SRC2 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 4 | SRC3 STOP EN | Enables Control of SRC3 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 3 | SRC4 STOP EN | Enables Control of SRC4 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 2 | SRC5 STOP EN | Enables Control of SRC5 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 1 | SRC6 STOP EN | Enables Control of SRC6 with PCI_STOP | RW | Free-Running | Stoppable | 0 |
| Bit 0 | SRC7 STOP EN | Enables Control of SRC7 with PCI_STOP | RW | Free-Running | Stoppable | 0 |

SMBus Table: Output Control Register

| Byte 13 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|---------------------------------------|------|--------------|-------------|---------|
| Bit 7 | ITP_EN | ITP_EN readback | R | SRC1 | CPU_ITP | Latch |
| Bit 6 | SEL_PCI | Select PCI Readback | R | 27M | PCI4 | Latch |
| Bit 5 | WOL Enable | WOL Enable for 25M | RW | WOL Disabled | WOL Enabled | 1 |
| Bit 4 | PCI_F1 | Free Running with PCI_STOP# | RW | Free-Running | Stoppable | 0 |
| Bit 3 | PCI2 | Free Running with PCI_STOP# | RW | Free-Running | Stoppable | 1 |
| Bit 2 | PCI3 | Free Running with PCI_STOP# | RW | Free-Running | Stoppable | 1 |
| Bit 1 | PCI4 | Free Running with PCI_STOP# | RW | Free-Running | Stoppable | 1 |
| Bit 0 | SATA STOP EN | Enables Control of SATA with PCI_STOP | RW | Free-Running | Stoppable | 0 |

* For lowest power saving during WOL mode, it is mandatory to connect 3.3V and 1.5V core VDD pins to standby power and suspend/remove VDDIO pins.

SMBus Table: Differential Output Amplitude Control Register

| Byte 14 | Name | Control Function | Type | 0 | 1 | Default |
|---------|--------------|-------------------------------|------|------------|-------------|---------|
| Bit 7 | PCIEX_AMP<1> | PCIEX Amplitude Control bit1 | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 6 | PCIEX_AMP<0> | PCIEX Amplitude Control bit0 | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 5 | DOT96_AMP<1> | DOT96 Amplitude Control bit1 | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 4 | DOT96_AMP<0> | DOT96 Amplitude Control bit0 | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 3 | SATA_AMP<1> | SATA Amplitude Control bit1 | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 2 | SATA_AMP<0> | SATA Amplitude Control bit0 | RW | 10 = 900mV | 11 = 1000mV | 1 |
| Bit 1 | CPU_AMP<1> | CPUCLK Amplitude Control bit1 | RW | 00 = 700mV | 01 = 800mV | 0 |
| Bit 0 | CPU_AMP<0> | CPUCLK Amplitude Control bit0 | RW | 10 = 900mV | 11 = 1000mV | 1 |

Bytes 15+ Reserved Registers

All reserved bits and reserved bytes in this SMBus table should not be overwritten at any instance. Writing to these reserved bits and bytes may cause unexpected behavior. IDT does not warrant any application issue going forward if continuing to overwrite these reserve bits and bytes.

Absolute Maximum Ratings—DC Parameters

Stresses above the ratings listed below can cause permanent damage to the 9VRS4339B. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|-------------------|------------------------------|-----------|-----|-------|-------|
| Maximum Supply Voltage | VDD27, VDD_3.3 | Supply Voltage | | 4.6 | V | 1,4 |
| Maximum Supply Voltage | VDD_CORE_1.5 | Supply Voltage | | 1.9 | V | 1,4 |
| Maximum Supply Voltage | VDD_LVIO | Supply Voltage | | 1.9 | V | 1,4 |
| Maximum Input Voltage | V _{IH} | 3.3V Inputs, including SMBus | | 4.6 | V | 1,2,4 |
| Minimum Input Voltage | V _{IL} | Any Input | GND - 0.5 | | V | 1,4 |
| Storage Temperature | T _s | - | -65 | 150 | °C | 4 |
| Case Temperature | T _{case} | - | | 115 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | V | 3,4 |

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹ Intentionally blank

² Maximum V_{IH} is not to exceed VDD

³ Human Body Model

⁴ Operation under these conditions is neither implied, nor guaranteed.

Electrical Characteristics—PCICLK/PCICLK_F

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---------------------------------------|-------------------------|--|---------------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | T _{period} | 33.33MHz output no spread | 29.99700 | 30.00300 | ns | 1,2,5 |
| | | 33.33MHz output spread | 30.08421 | 30.23459 | ns | 1,2,5 |
| Absolute min/max period | T _{abs} | 33.33MHz output no spread | 29.49700 | 30.50300 | ns | 1,2 |
| | | 33.33MHz output nominal/spread | 29.56617 | 30.58421 | ns | 1,2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @MIN = 1.0 V | -33 | | mA | 1 |
| | | V _{OH} @MAX = 3.135 V | | -33 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @MIN = 1.95 V | 30 | | mA | 1 |
| | | V _{OL} @MAX = 0.4 V | | 38 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1,3 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1,3 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 1,4 |
| Adjacent Pin to Pin Skew | t _{skew} | V _T = 1.5 V, PCI Aligned Mode (Default) | | 250 | ps | 1,4,7 |
| Adjacent Pin to Pin Intentional Delay | t _{skew_delay} | V _T = 1.5 V, PCI Delayed Mode | 200ps typical | | ps | 1,4,8 |
| Total PCI Skew Window | t _{skew_total} | V _T = 1.5 V, PCI Delayed Mode | | 800 | ps | 1,4,9 |
| Jitter, Cycle to cycle | t _{cyc-cyc} | V _T = 1.5 V | | 500 | ps | 1,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, R_s=39ohm, CL=5pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Edge rate in system is measured from 0.8V to 2.0V.

⁴ Duty cycle, Period, Skew and Jitter are measured with respect to 1.5V

⁵ The average period over any 1us period of time

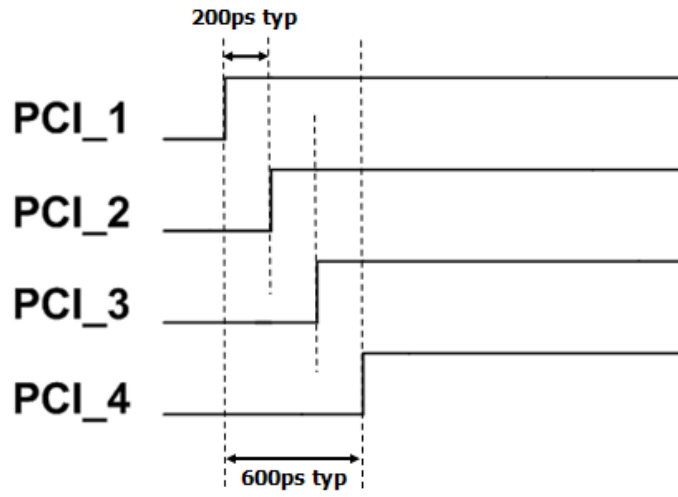
⁶ Using frequency counter with the measurement interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 25.000000MHz, 33.333333MHz, 27.000000MHz and 48.000000MHz

⁷ Adjacent pin to pin skew is the pin to pin skew between PCI1 and PCI2, PCI2 and PCI3, or PCI3 to PCI4.

⁸ Adjacent pin to pin intentional delay is the intentional delay between PCI1 and PCI2, PCI2 and PCI3, or PCI3 to PCI4.

⁹ Total PCI skew window is absolute skew between PCI1 and PCI4.

PCICLK Relationship Timing Diagram During Delayed Mode



Electrical Characteristics—Input/Supply/Common Output DC Parameters

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|--|------------------------|---|-----------------------|-----------------------|--------|-------|
| Ambient Operating Temp | Tambient | - | 0 | 70 | °C | |
| Supply Voltage | VDD27, VDD_3.3 | Supply Voltage | 3.135 | 3.465 | V | |
| | VDD_CORE_1.5 | Supply Voltage | 1.425 | 1.575 | V | |
| | VDD_LVIO | Supply Voltage | 0.9975 | 1.575 | V | |
| Input High Voltage | V _{IHSE} | Single-ended 3.3V inputs | 2 | V _{DD} + 0.3 | V | 3 |
| Input Low Voltage | V _{ILSE} | Single-ended 3.3V inputs | V _{SS} - 0.3 | 0.8 | V | 3 |
| Latched Input High Voltage | V _{IH_LI} | Single-ended 3.3V Latched Inputs | 2 | V _{DD} + 0.3 | V | |
| Latched Input Low Voltage | V _{IL_LI} | Single-ended 3.3V Latched Inputs | V _{SS} - 0.3 | 0.8 | V | |
| Low Threshold Latched Input-High Voltage | V _{IH_FS} | Low threshold inputs FSL[C:B] | 0.7 | V _{DD} +0.3 | V | |
| Low Threshold Latched Input-Low Voltage | V _{IL_FS} | Low threshold inputs FSL[C:B] | V _{SS} - 0.3 | 0.35 | V | |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | 5 | µA | 2 |
| Input Leakage Current | I _{INRES} | Inputs with pull up or pull down resistors V _{IN} = V _{DD} , V _{IN} = GND | -200 | 200 | µA | |
| Output High Voltage | V _{OHSE} | Single-ended outputs, I _{OH} = -1mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OLSE} | Single-ended outputs, I _{OL} = 1 mA | | 0.4 | V | 1 |
| Operating Supply Current | I _{DDOP3.3} | Full Active, C _L = Full load; IDD 3.3V | | 38 | mA | |
| | I _{DDOP1.5} | Full Active, C _L = Full load; IDD 1.5V | | 40 | mA | |
| | I _{DDOP1.05} | Full Active, C _L = Full load; IDD LVIO | | 46 | mA | |
| Powerdown Current | I _{DDPD3.3} | Power down mode, 3.3V Rail | | 1.2 | mA | 5 |
| | I _{DDPD1.5} | Power down mode, 1.5V Rail | | 1 | mA | 5 |
| | I _{DDPDLVIO} | Power down mode, 1.05V Rail | | 0 | mA | 5 |
| Wake-On-Lan Current | I _{DDWOL3.3} | Wake On LAN mode, 3.3V Rail | | 10 | mA | 6 |
| | I _{DDWOL1.5} | Wake On LAN mode, 1.5V Rail | | 1 | mA | 6 |
| | I _{DDWOLLVIO} | Wake On LAN mode, LVIO Rail | | 0 | mA | 6 |
| Input Frequency | F _i | V _{DD} = 3.3 V | 25MHz Typical | | MHz | 4 |
| Pin Inductance | L _{pin} | | | 7 | nH | |
| Input Capacitance | C _{IN} | Logic Inputs | 1.5 | 5 | pF | |
| | C _{OUT} | Output pin capacitance | | 6 | pF | |
| | C _{INX} | X1 & X2 pins | | 6 | pF | |
| Clk Stabilization | T _{STAB} | From VDD Power-Up or de-assertion of PD to 1st clock | | 1.8 | ms | |
| T _{stop_CR_off} | T _{CR OFF} | Output stop after CLKREQ# deasserted | 2 | 3 | Clocks | |
| Trun_CR_on | T _{CR ON} | Output run after CLKREQ# asserted | 2 | 3 | Clocks | |
| T _{stop} | T _{STOP} | CPU or PCI stop after CPU or PCI STOP# assertion | 2 | 3 | Clocks | |
| Trun | T _{RUN} | CPU or PCI run after CPU or PCI STOP# de-assertion | 2 | 3 | Clocks | |
| T _{fall_SE} | T _{FALL} | Fall/rise time of all 3.3V control inputs from 20-80% | | 10 | ns | |
| T _{rise_SE} | T _{RISE} | | | 10 | ns | |
| SMBus Voltage | V _{DD} | | 2.7 | 3.3 | V | |
| Low-level Output Voltage | V _{OL SMB} | @ I _{PULLUP} | | 0.4 | V | |
| Current sinking at V _{OL SMB} = 0.4 V | I _{PULLUP} | SMB Data Pin | 4 | | mA | |
| SCLK/SDATA Clock/Data Rise Time | T _{RI2C} | (Max V _{IL} - 0.15) to (Min V _{IH} + 0.15) | | 1000 | ns | |
| SCLK/SDATA Clock/Data Fall Time | T _{FI2C} | (Min V _{IH} + 0.15) to (Max V _{IL} - 0.15) | | 300 | ns | |
| Maximum SMBus Operating Frequency | F _{SMBUS} | | | 100 | kHz | |
| Spread Spectrum Modulation Frequency | f _{SSMOD} | Triangular Modulation | 30 | 33 | kHz | |

NOTES on DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

¹Signal is required to be monotonic in this region.

²input leakage current does not include inputs with pull-up or pull-down resistors

³3.3V referenced inputs are: PCI_STOP#, CPU_STOP#, ITP_EN, SCLK, SDATA, CLKPWRGD/PD#, DOT96_SEL, SEL_PCI, 48M_SEL and PEREQ# inputs if selected.

⁴For margining purposes only. Normal operation should have F_{in} = 25MHz +/-50ppm

⁵Standard powerdown with Wake on LAN disabled.

⁶Powerdown with Wake on LAN enabled

AC Electrical Characteristics–CPU, SRC, SATA, DOT96MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|------------------------------|----------------------|--------------------------|------|------|-------|-------|
| Rising Edge Slew Rate | t _{SLR} | Differential Measurement | 2.5 | 4 | V/ns | 1,3 |
| Falling Edge Slew Rate | t _{FLR} | Differential Measurement | 2.5 | 4 | V/ns | 1,3 |
| Slew Rate Variation | t _{SLVAR} | Single-ended Measurement | | 20 | % | 1,3 |
| Maximum Output Voltage | V _{HIGH} | Includes overshoot | | 1150 | mV | 1 |
| Minimum Output Voltage | V _{LOW} | Includes undershoot | -300 | | mV | 1 |
| Differential Voltage Swing | V _{SWING} | Differential Measurement | 300 | | mV | 1 |
| Crossing Point Voltage | V _{XABS} | Single-ended Measurement | 300 | 550 | mV | 1,3,4 |
| Crossing Point Variation | V _{XABSVAR} | Single-ended Measurement | | 140 | mV | 1,3,5 |
| Duty Cycle | DCYC | Differential Measurement | 45 | 55 | % | 1 |
| CPU Jitter - Cycle to Cycle | CPUJC2C | Differential Measurement | | 85 | ps | 1 |
| SRC Jitter - Cycle to Cycle | SRCJC2C | Differential Measurement | | 85 | ps | 1 |
| SATA Jitter - Cycle to Cycle | SATAJC2C | Differential Measurement | | 125 | ps | 1 |
| DOT Jitter - Cycle to Cycle | DOTJC2C | Differential Measurement | | 250 | ps | 1 |
| CPU[1:0] Skew | CPU10SKEW | Differential Measurement | | 100 | ps | 1,6 |
| CPU[ITP:0] Skew | CPU20SKEW | Differential Measurement | | 150 | ps | 1,6 |
| PCIEX(6, 4:2) Skew | PCIEXSKEW | Differential Measurement | | 250 | ps | 1 |
| PCIEX(7:1) Skew | PCIEXSKEW | Differential Measurement | | 500 | ps | 1 |

Notes: T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L=2pF, R_s=0Ω (unless specified otherwise)

¹ Guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Slew rate emasured through V_{swing} voltage range centered about differential zero

⁴ V_{cross} is defined at the voltage where Clock = Clock#.

⁵ Only applies to the differential rising edge (Clock rising, Clock# falling.)

⁶ CPU group skew is nominally 0ps.

Electrical Characteristics–USB48MHz/48MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---------------------------------|----------------------|--|----------|----------|-------|-------|
| Long Accuracy | ppm | see T _{period} min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | T _{period} | 48.00MHz output nominal | 20.83125 | 20.83542 | ns | 1,2,5 |
| Absolute min/max period | T _{abs} | 48.00MHz output nominal | 20.48125 | 21.18542 | ns | 1,2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @MIN = 1.0 V | -29 | | mA | 1 |
| | | V _{OH} @MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @MIN = 1.95 V | 29 | | mA | 1 |
| | | V _{OL} @MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate (USB48M) | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 2 | V/ns | 1,3 |
| Falling Edge Slew Rate (USB48M) | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 2 | V/ns | 1,3 |
| Rising Edge Slew Rate (48M) | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1,3 |
| Falling Edge Slew Rate (48M) | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1,3 |
| Duty Cycle | d _T | V _T = 1.5 V | 45 | 55 | % | 1,4 |
| Jitter, Cycle to cycle | t _{cyc-cyc} | V _T = 1.5 V | | 350 | ps | 1,4 |

*T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%, R_s=39ohm, C_L=5pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Edge rate in system is measured from 0.8V to 2.0V.

⁴ Duty cycle, Period and Jitter are measured with respect to 1.5V

⁵ The average period over any 1us period of time

⁶ Using frequency counter with the measurement interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 25.000000MHz, 33.333333MHz, 27.000000MHz and 48.000000MHz

Electrical Characteristics–25MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|------------------------|----------------------|---------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -30 | 30 | ppm | 1,2 |
| Clock period | T _{period} | 25.00MHz output nominal | 39.99880 | 40.00120 | ns | 1,2,5 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -29 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 29 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 0.5 | 2 | V/ns | 1,3 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 0.5 | 2 | V/ns | 1,3 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 1,4 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | V _T = 1.5 V | | 200 | ps | 1,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=39ohm, CL=5pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Edge rate in system is measured from 0.8V to 2.0V.

⁴ Duty cycle, Period and Jitter are measured with respect to 1.5V

⁵ The average period over any 1us period of time

⁶ Using frequency counter with the measurement interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 25.000000MHz, 33.333333MHz, 27.000000MHz and 48.000000MHz

Electrical Characteristics–REF-14.318MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|-------------------------|----------------------|---------------------------------|----------|----------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -100 | 100 | ppm | 1,2 |
| Clock period | Tperiod | 14.318MHz output nominal | 69.82033 | 69.86224 | ns | 1,2,5 |
| Absolute min/max period | Tabs | 14.318MHz output nominal | 69.83400 | 70.84800 | ns | 1,2 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @ MIN = 1.0 V | -29 | | mA | 1 |
| | | V _{OH} @ MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @ MIN = 1.95 V | 29 | | mA | 1 |
| | | V _{OL} @ MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1,3 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1,3 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 1,4 |
| Jitter, Cycle to cycle | t _{jyc-cyc} | V _T = 1.5 V | | 1000 | ps | 1,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs=39ohm, CL=5pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Edge rate in system is measured from 0.8V to 2.0V.

⁴ Duty cycle, Period and Jitter are measured with respect to 1.5V

⁵ The average period over any 1us period of time

⁶ Using frequency counter with the measurement interval equal or greater that 0.15s. Target frequencies are 14.318181 MHz, 25.000000MHz, 33.333333MHz, 27.000000MHz and 48.000000MHz

Electrical Characteristics–27MHz

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | Notes |
|------------------------|----------------------|--|---------|---------|-------|-------|
| Long Accuracy | ppm | see Tperiod min-max values | -50 | 50 | ppm | 1,2 |
| | | | -15 | 15 | ppm | 1,2,7 |
| Clock period | T _{period} | 27.000MHz output nominal | 37.0365 | 37.0376 | ns | 1,4,5 |
| Output High Voltage | V _{OH} | I _{OH} = -1 mA | 2.4 | | V | 1 |
| Output Low Voltage | V _{OL} | I _{OL} = 1 mA | | 0.4 | V | 1 |
| Output High Current | I _{OH} | V _{OH} @MIN = 1.0 V | -29 | | mA | 1 |
| | | V _{OH} @MAX = 3.135 V | | -23 | mA | 1 |
| Output Low Current | I _{OL} | V _{OL} @MIN = 1.95 V | 29 | | mA | 1 |
| | | V _{OL} @MAX = 0.4 V | | 27 | mA | 1 |
| Rising Edge Slew Rate | t _{SLR} | Measured from 0.8 to 2.0 V | 1 | 4 | V/ns | 1,3 |
| Falling Edge Slew Rate | t _{FLR} | Measured from 2.0 to 0.8 V | 1 | 4 | V/ns | 1,3 |
| Duty Cycle | d _{t1} | V _T = 1.5 V | 45 | 55 | % | 1,4 |
| Jitter | t _{ij} | Long Term (10us), V _T = 1.5 V | | 400 | ps | 1,4 |
| | t _{cyc-cyc} | Cycle to Cycle, V _T = 1.5 V | | 200 | ps | 1,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, Rs = 39ohm, CL = 5pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REFOUT is at 25.000000MHz

³ Edge rate in system is measured from 0.8V to 2.0V.

⁴ Duty cycle, Period and Jitter are measured with respect to 1.5V

⁵ The average period over any 1us period of time

⁶ Using frequency counter with the measurement interval equal or greater than 0.15s. Target frequencies are 14.318181 MHz, 25.000000MHz, 33.333333MHz, 27.000000MHz and 48.000000MHz

⁷ At nominal voltage and temperature.

Clock Jitter Specifications - Low Power Differential Outputs

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|--------------------|------------------------|--|-----|-----|----------|-------|
| PCIEX Phase Jitter | t _{phasePLL} | PCIe Gen 1 | | 86 | ps (p-p) | 1,2 |
| | t _{phaseLo} | PCIe Gen 2 10kHz < f < 1.5MHz | | 3.0 | ps (RMS) | 1,3,4 |
| | t _{phaseHigh} | PCIe Gen 2 1.5MHz < f < Nyquist (50MHz) | | 3.1 | ps (RMS) | 1,3,4 |

*TA = 0 - 70°C; Supply Voltage VDD = 1.5V +/- 5%, Rs=0ohm, CL=2pF

¹ Unless otherwise noted, guaranteed by design and characterization, not 100% tested in production.

² Jitter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system

³ Phase jitter requirement: The designated Gen2 outputs will meet the reference clock jitter requirements from the PCI Express Gen2 Base Spec. The test is performed

⁴ See <http://www.pcisig.com> for complete specs

Differential Clock Tolerances

| | CPU | SRC | DOT96 | SATA | |
|-----------------------|--------|--------|-------|--------|-----|
| PPM tolerance | 100 | 100 | 100 | 100 | ppm |
| Cycle to Cycle Jitter | 85 | 85 | 250 | 125 | ps |
| Spread | -0.50% | -0.50% | 0.00% | -0.50% | % |

Clock Periods–Differential Outputs with Spread Spectrum Disabled

| SSC OFF | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|---------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 100.00 | 9.91400 | | 9.99900 | 10.00000 | 10.00100 | | 10.08600 | ns | 1,2 |
| | 133.33 | 7.41425 | | 7.49925 | 7.50000 | 7.50075 | | 7.58575 | ns | 1,2 |
| | 166.67 | 5.91440 | | 5.99940 | 6.00000 | 6.00060 | | 6.08560 | ns | 1,2 |
| | 200.00 | 4.91450 | | 4.99950 | 5.00000 | 5.00050 | | 5.08550 | ns | 1,2 |
| SRC | 100.00 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.12600 | ns | 1,2 |
| SATA | 100.00 | 9.87400 | | 9.99900 | 10.00000 | 10.00100 | | 10.12600 | ns | 1,2 |
| DOT96 | 96.00 | 10.16563 | | 10.41563 | 10.41667 | 10.41771 | | 10.66771 | ns | 1,2 |

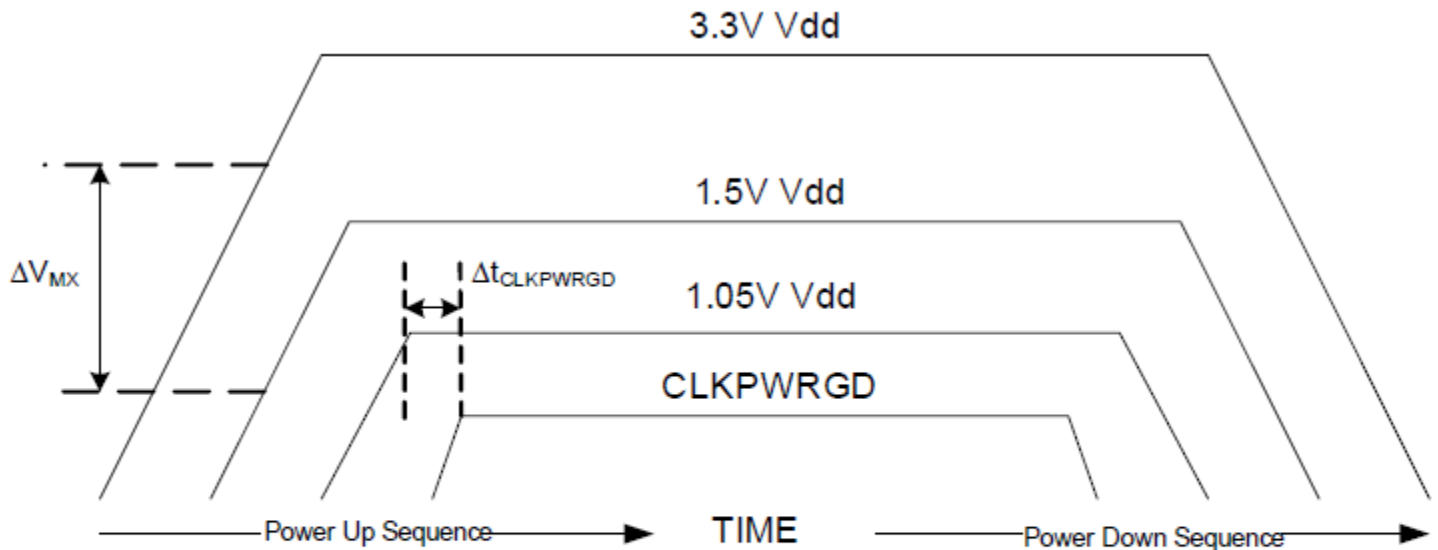
Clock Periods–Differential Outputs with Spread Spectrum Enabled

| SSC ON | Center Freq. MHz | Measurement Window | | | | | | | Units | Notes |
|--------|------------------|------------------------|-----------------------------|-----------------------------|----------------------|-----------------------------|-----------------------------|------------------------|-------|-------|
| | | 1 Clock | 1us | 0.1s | 0.1s | 0.1s | 1us | 1 Clock | | |
| | | -c2c jitter AbsPer Min | -SSC Short-Term Average Min | - ppm Long-Term Average Min | 0 ppm Period Nominal | + ppm Long-Term Average Max | +SSC Short-Term Average Max | +c2c jitter AbsPer Max | | |
| CPU | 99.75 | 9.91406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.13607 | ns | 1,2 |
| | 133.00 | 7.41430 | 7.49930 | 7.51805 | 7.51880 | 7.51955 | 7.53830 | 7.62330 | ns | 1,2 |
| | 166.25 | 5.91444 | 5.99944 | 6.01444 | 6.01504 | 6.01564 | 6.03064 | 6.11564 | ns | 1,2 |
| | 199.50 | 4.91453 | 4.99953 | 5.01203 | 5.01253 | 5.01303 | 5.02553 | 5.11053 | ns | 1,2 |
| SRC | 99.75 | 9.87406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.17607 | ns | 1,2 |
| SATA | 99.75 | 9.87406 | 9.99906 | 10.02406 | 10.02506 | 10.02607 | 10.05107 | 10.17607 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²All Long Term Accuracy specifications are guaranteed with the assumption that the crystal input is tuned to exactly 25.000000MHz.

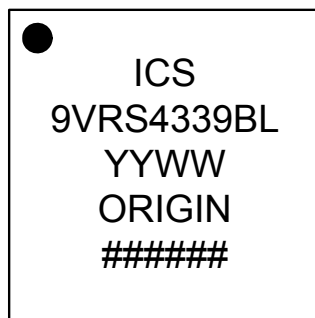
Power-up Sequencing Requirements



Notes:

1. The maximum difference (ΔV_{MX}) between any two voltages is 0.7V if the lower power supply is powered up first.
2. There are no timing requirements between the higher and lower voltages if the higher voltages power up first.
3. The minimum time before CLKPWRGD can be set ($\Delta t_{CLKPWRGD} = 0$) is 0 sec from the last power supply that is powered up.

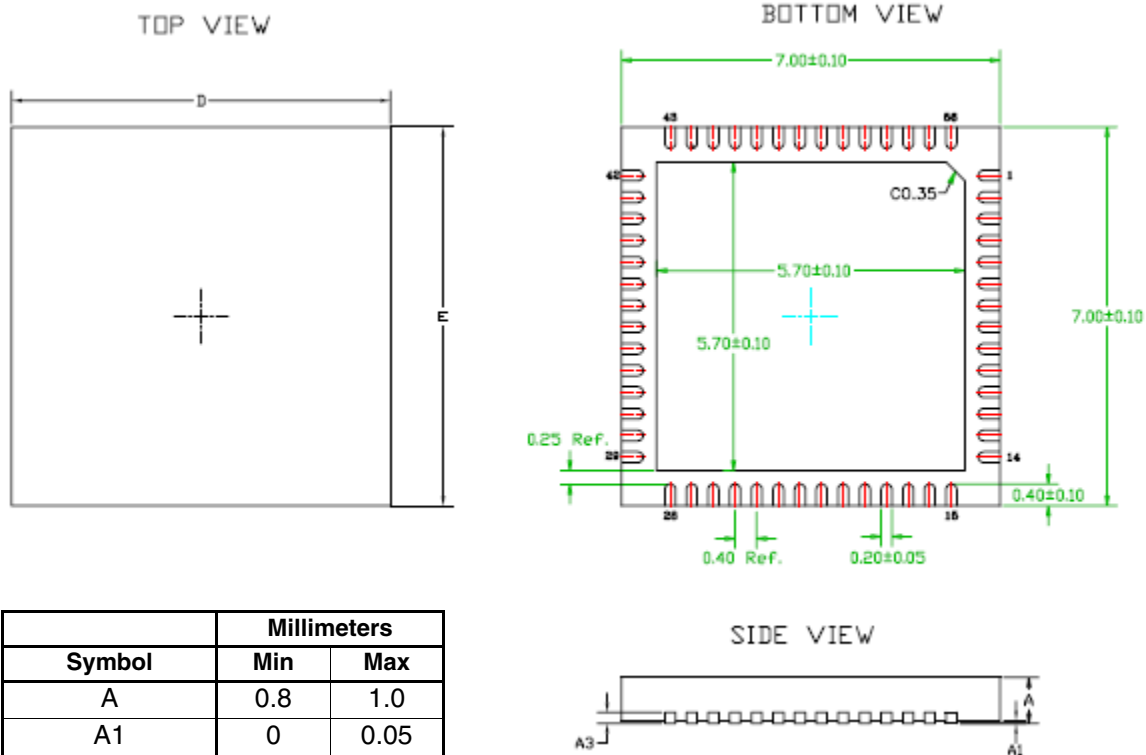
Marking Diagram



Notes:

1. ##### is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "L" denotes RoHS compliant package.
4. "ORIGIN" is the country of origin.

Package Outline and Package Dimensions (56-pin MLF)



| Symbol | Millimeters | |
|----------------|---------------|------|
| | Min | Max |
| A | 0.8 | 1.0 |
| A1 | 0 | 0.05 |
| A3 | 0.2 Reference | |
| b | 0.15 | 0.25 |
| e | 0.40 BASIC | |
| D x E BASIC | 7.00 x 7.00 | |
| D2 MIN./MAX. | 5.60 | 5.80 |
| E2 MIN./MAX. | 5.60 | 5.80 |
| L MIN./MAX. | 0.30 | 0.50 |
| N | 56 | |
| N _D | 14 | |
| N _E | 14 | |

Ordering Information

| Part / Order Number | Marking | Shipping Packaging | Package | Temperature |
|---------------------|-------------|--------------------|------------|-------------|
| 9VRS4339BKLF | see page 18 | Trays | 56-pin MLF | 0 to +70° C |
| 9VRS4339BKLF | | Tape and Reel | 56-pin MLF | 0 to +70° C |

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

"B" is the device revision designator (will not correlate with the datasheet revision).

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Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|------|-----------|------------|--|---------|
| 0.1 | DC | 4/25/2011 | Initial Release | - |
| 0.2 | DC | 10/11/2011 | 1. Updated "Features/Benefits" section 2. Updated Power Distribution table 3. Updated Byte 13 4. Updated pin 55 description | Various |
| A | DC | 1/3/2012 | 1. Updated "General Description" 2. Updated "Features/Benefits" 3. Updated pin descriptions 4. Updated Byte13 5. Updated "Absolute Max Ratings" and "Electrical Characteristics - Input/Supply/Common Output DC Parameters" tables | Various |

9VRS4339B

VERY LOW POWER CLOCK FOR 2011 NETBOOKS

SYNTHESIZERS

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