Description

The 9ZXL0451E is a second generation enhanced performance DB800ZL derivative for PCIe Gen4 and 5 applications. In fanout (bypass) mode, it is DB2000Q compatible. A fixed external feedback in ZDB mode maintains low drift for critical QPI/UPI applications.

PCIe Clocking Architectures Supported

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers
- Storage
- Networking
- eSSDs
- PCIe expansion

Output Features

- 4 Low-power HCSL (LP-HCSL) output pairs with 85Ω Zout

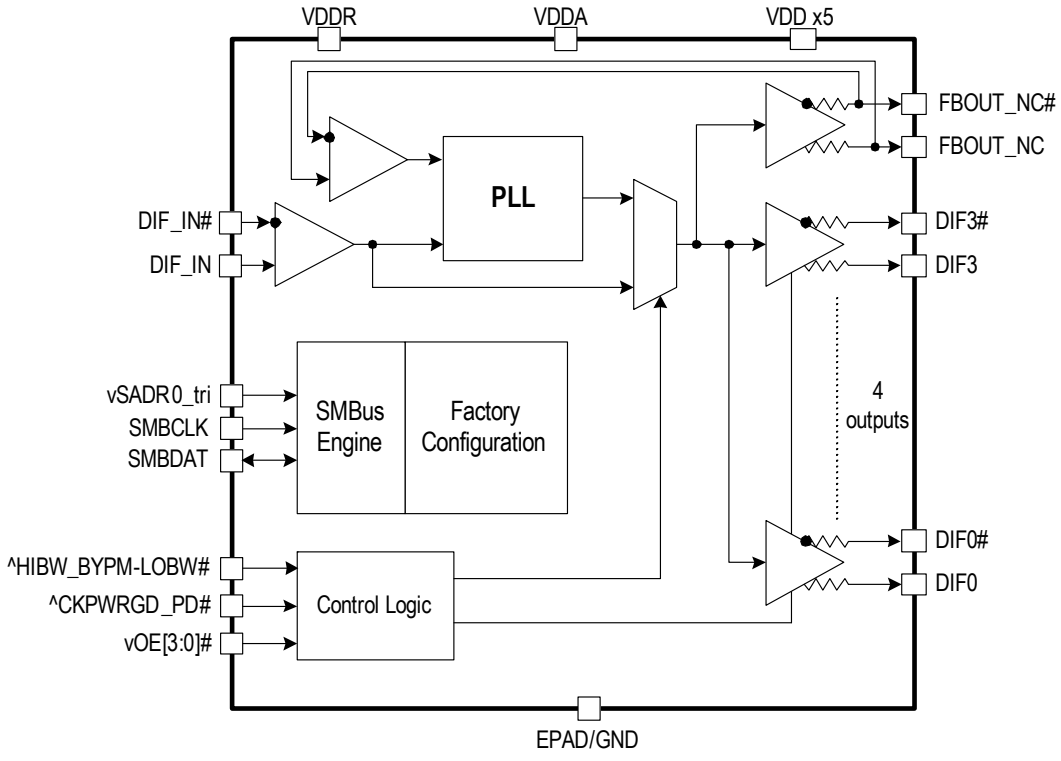
Features

- LP-HCSL outputs eliminate 16 resistors; save 32mm^2 of area
- 4 OE# pins; SMBus control also available
- 3 selectable SMBus addresses
- 2 selectable ZDB bandwidths; minimizes jitter peaking in cascaded PLL topologies
- Hardware/SMBus control of ZDB bandwidth and fanout modes
- Spread spectrum compatible
- 100MHz ZDB mode
- 5 × 5 mm 32-VFQFPN package; small board footprint

Key Specifications

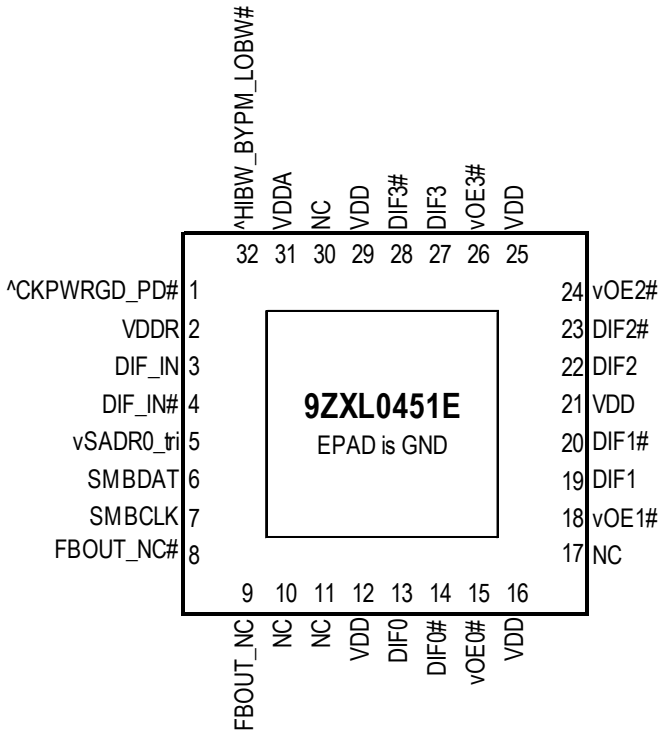
- Cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50 ps
- Input-to-output delay variation (ZDB mode): < 50ps
- Phase jitter ZDB mode: PCIe Gen4 < 0.35ps rms
- Additive phase Jitter (fanout mode): PCIe Gen4 < 0.05ps rms
- Additive phase Jitter (fanout mode): PCIe Gen5 < 0.05ps rms
- Additive phase Jitter (fanout mode): DB2000Q < 0.05ps rms
- Phase jitter (all modes): UPI > 9.6GB/s < 0.1ps rms
- Additive phase jitter (all modes): IF-UPI < 1.0ps rms

Block Diagram



Contents

Pin Assignments



32-VFQFPN, 5 x 5 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Power Management

CKPWRGD_PD#	DIF_IN	SMBus EN bit	OE[x]#	DIF[x]	PLL State (if not in Bypass Mode)
0	X	X	X	Low/Low	OFF
1	Running	0	0	Low/Low	ON
		0	1	Low/Low	ON
		1	0	Running	ON
		1	1	Low/Low	ON

PLL Operating Mode

HIBW_BYPM_LOBW#	Mode
Low	PLL Low BW
Mid	Bypass
High	PLL High BW

SMBus Addressing

SMB_A0_tri	SMBus Address
0	D8
M	DA
1	DE

Note: PLL is OFF in Bypass Mode.

Power Connections

Pin Number		
V_{DD}	GND	Description
31	33	Analog PLL
2		Analog input
12, 16, 21, 25, 29		DIF clocks

PLL Operating Mode Readback

HIBW_BYPM_LOBW#	Byte 0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.
2	VDDR	Power	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
3	DIF_IN	Input	HCSL true input.
4	DIF_IN#	Input	HCSL complementary input.
5	vSADR0_tri	Input	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has an internal pull down resistor. See the SMBus Addressing table.
6	SMBDAT	I/O	Data pin of SMBUS circuitry.
7	SMBCLK	Input	Clock pin of SMBUS circuitry.
8	FBOUT_NC#	Output	Complementary half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
9	FBOUT_NC	Output	True half of differential feedback output. This pin should NOT be connected to anything outside the chip. It exists to provide delay path matching to get 0 propagation delay.
10	NC	—	No connection.
11	NC	—	No connection.
12	VDD	Power	Power supply, nominally 3.3V.
13	DIF0	Output	Differential true clock output.
14	DIF0#	Output	Differential complementary clock output.
15	vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
16	VDD	Power	Power supply, nominally 3.3V.
17	NC	—	No connection.
18	vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
19	DIF1	Output	Differential true clock output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
20	DIF1#	Output	Differential complementary clock output.
21	VDD	Power	Power supply, nominally 3.3V.
22	DIF2	Output	Differential true clock output.
23	DIF2#	Output	Differential complementary clock output.
24	vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
25	VDD	Power	Power supply, nominally 3.3V.
26	vOE3#	IN	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
27	DIF3	OUT	Differential true clock output.
28	DIF3#	OUT	Differential complementary clock output.
29	VDD	PWR	Power supply, nominally 3.3V.
30	NC	N/A	No connection.
31	VDDA	PWR	Power supply for PLL core.
32	^HIBW_BYPM_LOBW#	Latched In	Tri-level input to select High BW, Bypass or Low BW Mode. This pin has an internal pull-up resistor. See PLL Operating Mode table for details.
33	EPAD	GND	Ground pad.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9ZXL0451E at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	$V_{DD}x$				3.9	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface.			V_{DD}+0.5	V	1,3
Input High Voltage	V_{IHSMB}	SMBus clock and data pins.			3.9	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj	Maximum during normal operation.			125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2500			V	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 3.9V.

Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 3. SMBus

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.			0.4	V	
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4			mA	
Nominal Bus Voltage	V_{DDSMB}		2.7		3.6	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max V_{IL} - 0.15V) to (Min V_{IH} + 0.15V).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min V_{IH} + 0.15V) to (Max V_{IL} - 0.15V).			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	SMBus operating frequency.			400	kHz	5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

[5] The differential input clock must be running for the SMBus to be active.

Table 4. DIF_IN Clock Input Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage – DIF_IN	V_{CROSS}	Crossover voltage.	150		900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND.	-5		5	µA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through ±75mV window centered around differential zero.

Table 5. Input/Supply/Common Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDx}	Supply voltage for core and analog.	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	Industrial range (T_{IND}).	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, tri-level inputs.	2		V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, tri-level inputs.	GND - 0.3		0.8	V	
Input High Voltage	V_{IH}	Tri-level Inputs.	2.2		V_{DD} + 0.3	V	
Input Mid Voltage	V_{IL}	Tri-level Inputs.	1.2	$V_{DD}/2$	1.8	V	
Input Low Voltage	V_{IL}	Tri-level Inputs.	GND - 0.3		0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5		5	µA	
	I_{INP}	Single-ended inputs. V_{IN} = 0 V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-50		50	µA	
Input Frequency	F_{ibyp}	V_{DD} = 3.3V, Bypass Mode.	1		400	MHz	
	F_{ipll}	V_{DD} = 3.3V, 100MHz PLL Mode.	98.5	100.00	102.5	MHz	
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or de-assertion of PD# to 1st clock.		1	1.8	ms	1,2
Input SS Modulation Frequency PCIe	$f_{MODINPCIe}$	Allowable frequency for PCIe applications (Triangular modulation).	30		33	kHz	
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	4	5	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion.		49	300	µs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	2
Trise	t_R	Rise time of control inputs.			5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] DIF_IN input.

Table 6. Current Consumption

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I_{DDA}	V_{DDA}, ZDB Mode at 100 MHz.		37	44	mA	1
		V_{DDA}, Fanout Buffer Mode at 100MHz.		4	5	mA	1
Operating Supply Current	I_{DD}	All other V_{DD} pins, any mode at 100MHz.		33	40	mA	
Power Down Current	I_{DDAPD}	V_{DDA} pin, CKPWRGD_PD# = 0.		3.2	5	mA	
	I_{DDPD}	All other V_{DD} pins, CKPWRGD_PD# = 0.		1.3	2	mA	

[1] Includes V_{DDR} if applicable.

Table 7. Skew and Differential Jitter Parameters

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-output skew in PLL Mode at 100MHz, nominal temperature and voltage.	-100	-21.3	100	ps	1,2,4, 5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-output skew in Bypass Mode at 100MHz, nominal temperature and voltage.	2	2.6	3.5	ns	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-output skew variation in PLL Mode at 100MHz, across voltage and temperature.	-50	0.0	50	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = 0 to 70°C.	-250		250	ps	1,2,3, 5,8
		Input-to-output skew variation in Bypass Mode at 100MHz, across voltage and temperature, T_{AMB} = -40 to 85°C.	-350		350	ps	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random differential tracking error between two 9ZX devices in Hi BW Mode.		3	5	ps (rms)	1,2,3, 5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random differential spread spectrum tracking error between two 9ZX devices in Hi BW Mode.		23	50	ps	1,2,3, 5,8
DIF[x:0]	t_{SKEW_ALL}	Output-to-output skew across all outputs, common to PLL and Bypass Mode, at 100MHz.		32	50	ps	1,2,3, 8
PLL Jitter Peaking	$j_{peak\text{-}hibw}$	LOBW#_BYPASS_HIBW = 1.	0	1.3	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak\text{-}lobw}$	LOBW#_BYPASS_HIBW = 0.	0	1.3	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1.	2	2.6	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0.	0.7	1.0	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode.	45	50.3	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode at 100MHz.	-1	0	1	%	1,10
Jitter, Cycle to Cycle	$t_{jcyc\text{-}cyc}$	PLL Mode.		14	50	ps	1,11

[1] Measured into fixed 2pF load cap. Input-to-output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode input-to-output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device.

[5] Measured with scope averaging on to find mean value.

[6] "t" is the period of the input clock.

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass Mode.

[11] Measured from differential waveform.

Table 8. LP-HCSL Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	2	2.9	4	1–4	V/ns	1,2,3
Slew Rate Matching	ΔdV/dt	Single-ended measurement.		7.1	20	20	%	1,4,7
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value (scope averaging off).	660	792	850	1150	mV	7
Minimum Voltage	Vmin		-150	-35	150	-300		7
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	250	372	550	250–550	mV	1,5,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.		15	140	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, ZDB Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1.		13.4	31	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.2	0.7	3	ps (rms)	1,2
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		1.0	1.6	3.1	ps (rms)	1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.2	0.38	1	ps (rms)	1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.2	0.38	0.5	ps (rms)	1,2
Additive Phase Jitter, Bypass (fanout) Mode	$t_{jphPCIeG1-CC}$	PCIe Gen1.		0.01	0.06	Not Applicable	ps (p-p)	1,2,3,4
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Low Band 10kHz < f < 1.5MHz (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.004	0.005		ps (rms)	1,4,6
		PCIe Gen2 High Band 1.5MHz < f < Nyquist (50MHz) (PLL BW of 5–16MHz or 8–16MHz, CDR = 5MHz).		0.07	0.09		ps (rms)	1,4,6
	$t_{jphPCIeG3/4-CC}$	PCIe Gen3, Gen4 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.03	0.04		ps (rms)	1,4,6
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (see PCIe Gen5 specifications for details).		0.012	0.015		ps (rms)	1,4,6

Table 10. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, PLL Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.9	1.1	2	ps (rms)	1,2,5
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.6	0.65	0.7	ps (rms)	1,2,5
Additive Phase Jitter, Bypass Mode	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (PLL BW of 16MHz, CDR = 5MHz).		0.09	0.113	Not Applicable	ps (rms)	1,4,6
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.02	0.030		ps (rms)	1,4,6

Notes for PCIe Filtered Phase Jitter tables (CC) and (IR)

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel-supplied clock jitter tool, when driven by 9SQL495x or equivalent with spread on and off.

[3] Sample size of at least 100K cycles. This figure extrapolates to 108ps pk-pk at 1M cycles for a BER of 1^{-12}.

[4] For RMS values, additive jitter is calculated by solving for "b" [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

[5] IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRNS) PCIe clock architectures. According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. There are no accepted filters or limits for IR clock architectures at PCIe Gen1 or Gen4 data rates.

[6] Measured using SMA100B signal source and a phase noise analyzer.

Table 11. Filtered Phase Jitter Parameters – QPI/UPI

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, ZDB Mode	t_{jphQPI_UPI}	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI).		0.14	0.31	0.5	ps (rms)	1,2
		QPI & UPI (100MHz, 8.0Gb/s, 12UI).		0.07	0.10	0.3		1,2
		QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI).		0.06	0.08	0.2		1,2
	$t_{jphIF-UPI}$	IF-UPI (low bandwidth).		0.10	0.14	1		1,4
		IF-UPI (high bandwidth).		0.17	0.22	1		1,4
Additive Phase Jitter, Bypass (Fanout) Mode	t_{jphQPI_UPI}	QPI & UPI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI).		0.01	0.05	Not Applicable	ps (rms)	1,2,3
		QPI & UPI (100MHz, 8.0Gb/s, 12UI).		0.01	0.03			1,2,3
		QPI & UPI (100MHz, ≥ 9.6Gb/s, 12UI).		0.01	0.03			1,2,3
	$t_{jphIF-UPI}$	IF-UPI.		0.06	0.07			1,4

Notes for QPI/UPI Filtered Phase Jitter table

[1] Applies to all differential outputs, guaranteed by design and characterization.

[2] Calculated from Intel™-supplied clock jitter tool, when driven by 9SQL495x or equivalent with spread on and off.

[3] For RMS values, additive jitter is calculated by solving for "b" [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

[4] Calculated from phase noise analyzer when driven by Wenzel Associates source with Intel-specified brick-wall filter applied.

Table 12. Filtered Phase Jitter Parameters – DB2000Q Filter

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Additive Phase Jitter	$t_{jph12k-20Madd}$	100MHz (fanout mode).		23	40	80	fs (rms)	1,2,3

[1] Measured using SMA100B signal source and a phase noise analyzer.

[2] DB2000Q filter.

[3] For RMS values, additive jitter is calculated by solving for "b" [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

Table 13. Unfiltered Phase Jitter Parameters – 12kHz to 20MHz

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Phase Jitter, ZDB Mode	$t_{jph12k-20MHi}$	100MHz, SSC OFF (ZDB high BW).		171	225	Not Applicable	fs (rms)	1,2
	$t_{jph12k-20MLo}$	100MHz, SSC OFF (ZDB low BW).		184	225		fs (rms)	1,2
Additive Phase Jitter, Bypass (Fanout) Mode	$t_{jph12k-20MByp}$	100MHz, SSC OFF (fanout mode).		107	125		fs (rms)	1,2,3

[1] Measured using SMA100B signal source and a phase noise analyzer.

[2] 12kHz to 20MHz brick wall filter.

[3] For RMS values, additive jitter is calculated by solving for "b" [$b = sqrt(c^2 - a^2)$], where "a" is rms input jitter and "c" is rms total jitter.

Clock Periods

Table 14. Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2cjitter AbsPer Minimum	-SSC Short-Term Average Minimum	-ppm Long-Term Average Minimum	0 ppm Period Nominal	+ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2cjitter AbsPer Maximum		
DIF	100.00	9.94900	—	9.99900	10.00000	10.00100	—	10.05100	ns	1,2,3

Table 15. Differential Outputs with Spread Spectrum Enabled

SSC OFF	Center Frequency MHz	Measurement Window							Units	Notes
		1 Clock	1µs	0.1s	0.1s	0.1s	1µs	1 Clock		
		-c2cjitter AbsPer Minimum	-SSC Short-Term Average Minimum	-ppm Long-Term Average Minimum	0 ppm Period Nominal	+ppm Long-Term Average Maximum	+SSC Short-Term Average Maximum	+c2cjitter AbsPer Maximum		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ accuracy requirements (±100ppm). The buffer itself does not contribute to ppm error.

[3] Driven by output of main clock, 100MHz PLL Mode or Bypass Mode.

Test Loads

Low-Power HCSL Output Test Load
(standard PCIe source-terminated test load)

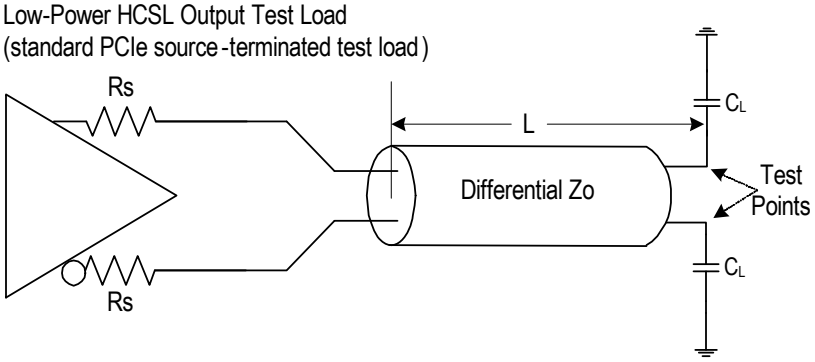


Table 16. Parameters for Low-Power HCSL Output Test Load

Device	Rs (Ω)	Zo (Ω)	L (inches)	C_L (pF)
9ZXL0451	Internal	85	10	2
	7.5	100	10	2

* Contact factory for versions of this device with Zo = 100Ω.

Alternate Terminations

The LP-HCSL output can easily drive other logic families. See "AN-891 Driving LVPECL, LVDS, and CML Logic with IDT's "Universal" Low-Power HCSL Outputs" for termination schemes for LVPECL, LVDS, CML and SSTL.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			IDT (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBus Table: PLL Mode and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	32	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback table		Latch
Bit 6	32	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	—	PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2	—	PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback table		1
Bit 1	—	PLL Mode 0	PLL Operating Mode 1	RW			1
Bit 0	Reserved						1

Note: Setting bit 3 to '1' allows the user to override the latch value from pin 32 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback table. Note that bits 7 and 6 will keep the value originally latched on pin 5. If these bits are changed, a warm reset of the system must be completed.

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	22/23	DIF2_En	Output Control - '0' overrides OE# pin	RW	Low/Low	OE# pin control	1
Bit 5	19/20	DIF1_En	Output Control - '0' overrides OE# pin	RW			1
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	13/14	DIF0_En	Output Control - '0' overrides OE# pin	RW	Low/Low	OE# pin control	1
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	27/28	DIF3_En	Output Control - '0' overrides OE# pin	RW	Low/Low	OE# pin control	1
Bit 0	Reserved						0

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	RID3	REVISION ID	R	E rev = 0100		0
Bit 6	—	RID2		R			1
Bit 5	—	RID1		R			0
Bit 4	—	RID0		R			0
Bit 3	—	VID3	VENDOR ID	R	–	–	0
Bit 2	—	VID2		R	–	–	0
Bit 1	—	VID1		R	–	–	0
Bit 0	—	VID0		R	–	–	1

SMBus Table: Device ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	Device ID 7 (MSB)		R	F3 Hex		1
Bit 6	—	Device ID 6		R			1
Bit 5	—	Device ID 5		R			1
Bit 4	—	Device ID 4		R			1
Bit 3	—	Device ID 3		R			0
Bit 2	—	Device ID 2		R			0
Bit 1	—	Device ID 1		R			1
Bit 0	—	Device ID 0		R			1

SMBus Table: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	—	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8.		0
Bit 3	—	BC3		RW			1
Bit 2	—	BC2		RW			0
Bit 1	—	BC1		RW			0
Bit 0	—	BC0		RW			0

SMBus Table: Reserved Register

Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/32-vfqfpn-package-outline-drawing-50-x-50-x-090-mm-body-epad-315-x-315-mm-nlg32p1

Marking Diagram

- Line 2 is the truncated part number.
- “YYWW” is the last digits of the year and work week that the part was assembled.
- “COO” denotes the country of origin.
- “LOT” denotes sequential lot number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9ZXL0451EKILF	5 × 5 mm, 0.5mm pitch 32-VFQFPN	Tray	-40° to +85°C
9ZXL0451EKILFT	5 × 5 mm, 0.5mm pitch 32-VFQFPN	Reel	-40° to +85°C

Revision History

Revision Date	Description of Change
March 4, 2019	▪ Updated Current Consumption table–Power Down Current specifications. ▪ Removed “Additive Jitter in bypass Mode” condition/values in Skew and Differential Jitter Parameters table.
February 20, 2019	Initial release.

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