Doc. version: 0.1
Total pages: 67
Date: 2010/01/29

Product Specification

2.5″ COLOR TFT-LCD MODULE

Model Name : A025CN04 V2

Planned Lifetime:	From 2008/Aug To 2011/Dec
Phase-out Control:	From 2011/Jul To 2011/Dec
EOL Schedule:	2011/Dec

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change without prior notice.

Record of Revision

Version	Revise Date	Page	Content
0.0	2010/1/4		First draft
0.1	2010/1/29	14	Update UPS051 mode using 13.5MHz

Contents

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution（dot）	480(W) x 240(H)	
2	Active area（mm）	49.92x37.44	
3	Screen size（inch）	2.46 (Diagonal)	
4	Dot pitch（um）	104x156	
5	Color configuration	R, G, B delta	
6	Overall dimension（mm）	59.63 x 42.94x2.6	Note 1
7	Weight（g）	10.9 typ	
8	Panel surface treatment	Hard Coating / 3H	

Note 1: Refer to F. Outline Dimension

B. Electrical specifications

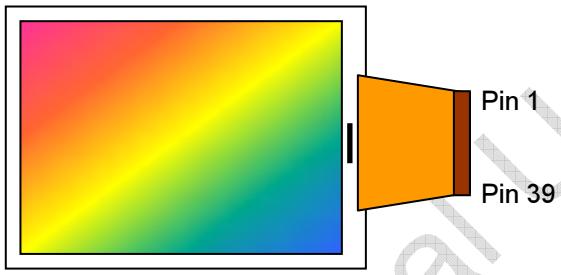
1. Pin assignment

Pin no	Symbol	I/O	I/O Structure	Description	Remark
1	VCOM	I	-	Panel common voltage	
2	CS	I	Type 3	Serial command enable	
3	SDA	I	Type 2	Serial command data input	
4	SCL	I	Type 1	Serial command clock input	
5	HSYNC	I	Type 1	Horizontal sync input	
6	VSYNC	I	Type 1	Vertical sync input	
7	DCLK	I	Type 1	Data clock input	
8	D7	I	Type 1	Data input; MSB	
9	D6	I	Type 1	Data input	
10	D5	I	Type 1	Data input	
11	D4	I	Type 1	Data input	
12	D3	I	Type 1	Data input	
13	D2	I	Type 1	Data input	
14	D1	I	Type 1	Data input	
15	D0	I	Type 1	Data input; LSB	
16	GND	P	-	Ground for digital circuit	
17	VDD	P	-	System power	3.0V~3.6V
18	DVDD	C	-	Power setting capacitor connect pin	
19	V1	C	-	Power setting capacitor connect pin	
20	V2	C	-	Power setting capacitor connect pin	
21	V3	C	-	Power setting capacitor connect pin	
22	V4	C	-	Power setting capacitor connect pin	
23	VDD2	C	-	Power setting capacitor connect pin	
24	V5	C	-	Power setting capacitor connect pin	
25	V6	C	-	Power setting capacitor connect pin	
26	VDD3	C	-	Power setting capacitor connect pin	
27	VDD5	C	-	Power setting capacitor connect pin	
28	V7	C	-	Power setting capacitor connect pin	
29	V8	C	-	Power setting capacitor connect pin	
30	VGH	C	-	Power setting capacitor connect pin	
31	VGL	C	-	Power setting capacitor connect pin	
32	AGND	P	-	Ground for analog circuit	

33	FRP	O	Type 4	Frame polarity output for VCOM	
34	COMDC	O	Type 5	VCOM DC voltage output pin	
35	VCAC	C	-	Power setting capacitor for VCOM AC	
36	DRV	O	Type 6	VLED boost transistor driving signal	
37	VLED	P	-	LED power anode	
38	FB	P	Type 7	LED power cathode	
39	VCOM	I	-	Panel common voltage	

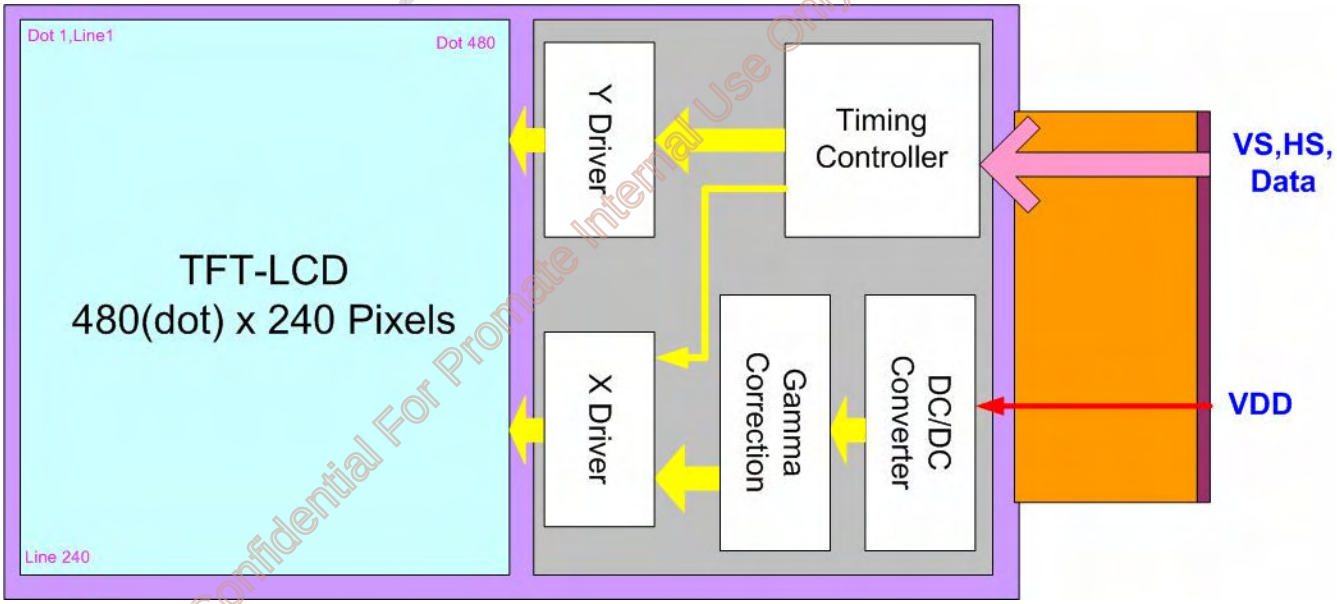
I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

Note: Definition of scanning direction, Refer to figure as below：



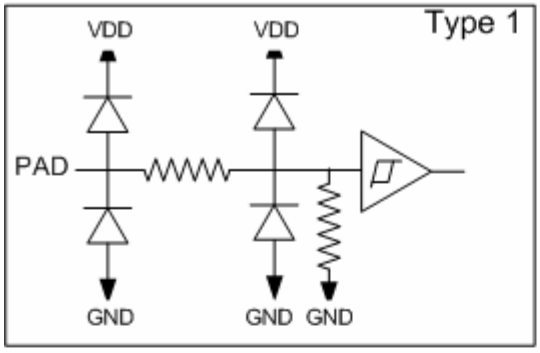
Function block diagram

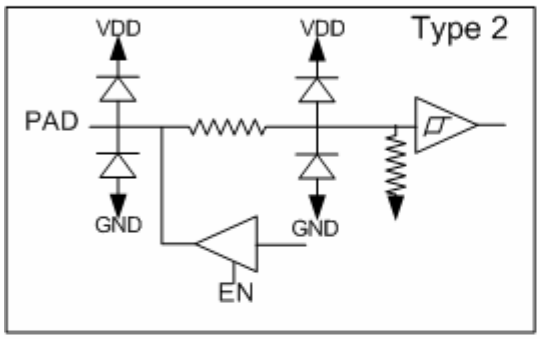
The following diagram shows the function block of the 2.5inch LCD module.

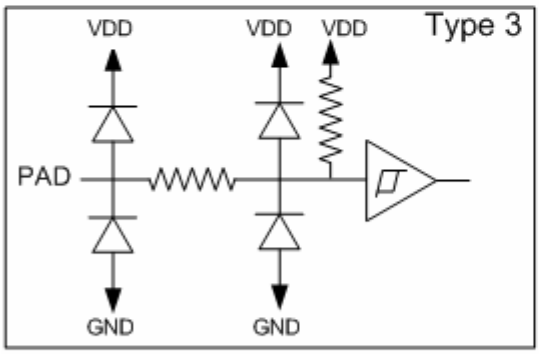


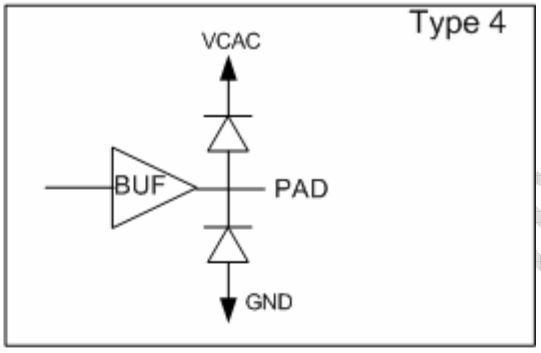
I/O Pin Structure:

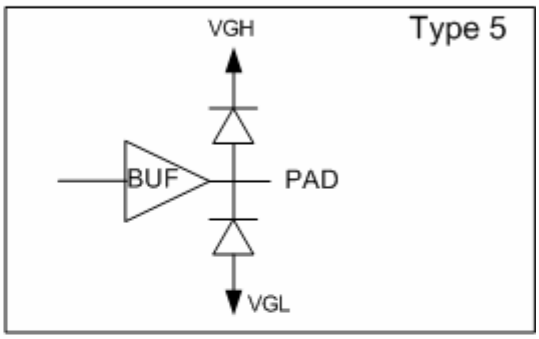
Pull high/low resistor is **700kΩ**

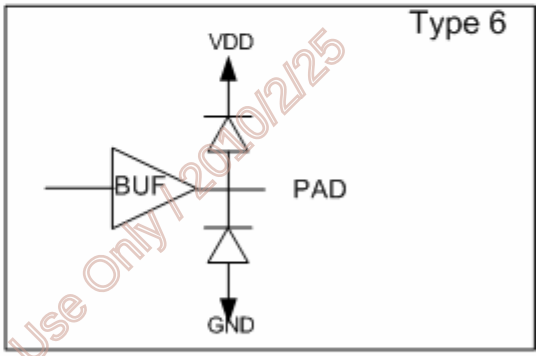


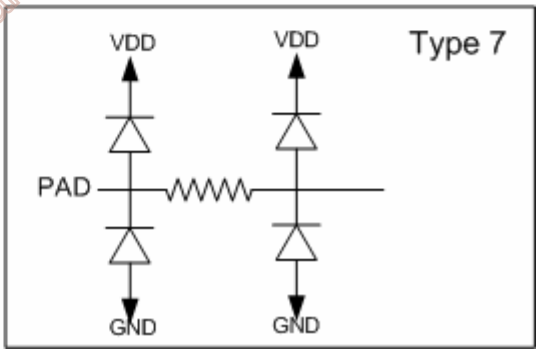












2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Supply Voltage	VDD	AGND=GND=0V	-0.3	4.5	V	
TFT-LCD Power Voltage	VGH	AGND=GND=0V	-0.3	16	V	
	VGL	AGND=GND=0V	-16	0.3	V	
Input Signal Voltage	CS,SDA,SCL,Vsync, Hsync,DCLK,D0~D7	AGND=GND=0V	-0.3	4.5	V	
VCOM AC Output Voltage	FRP	AGND=GND=0V	-0.3	8	V	
VCOM AC Power Voltage	VCAC	AGND=GND=0V	-0.3	8	V	
VCOM DC Output Voltage	COMDC	AGND=GND=0V	-0.3	8	V	
VCOM Input Voltage	VCOM	AGND=GND=0V	-0.3	8	V	
Charge Pump Voltage	VDD2	AGND=GND=0V	-0.3	8	V	
	VDD3	AGND=GND=0V	-0.3	16	V	
	VDD5	AGND=GND=0V	-0.3	20	V	
	V1	AGND=GND=0V	-0.3	8	V	
	V2	AGND=GND=0V	-0.3	8	V	
	V3	AGND=GND=0V	-0.3	8	V	
	V4	AGND=GND=0V	-0.3	8	V	
	V5	AGND=GND=0V	-0.3	16	V	
	V6	AGND=GND=0V	-0.3	16	V	
	V7	AGND=GND=0V	-0.3	16	V	
	V8	AGND=GND=0V	-16	8	V	
Storage Temperature	Tstg	-	-25	70	□	Ambient temperature
Operating Temperature	Topa	-	0	60	□	Ambient temperature

3. Electrical characteristics

3.1 Recommended operating conditions (GND=AGND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		VDD	3.0	3.3	3.6	V	Note 1
Input Signal	H Level	V_{IH}	0.7* VDD	-	VDD	V	
	L Level	V_{IL}	GND	-	0.3* VDD	V	

Note 1: A build-in power on reset circuit for VDD is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after VDD power on through serial control. Please refer to the register STB setting for detail.

3.2 Electrical characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{DD}	I_{DD}	V_{DD}=3.3V		4		mA	Note 1
	$I_{DD(STANDBY)}$			20		uA	Note 1
DC-DC voltage	V_{GH}	V_{DD}=3.3V	14.5	15	15.5	V	Note 2
	V_{GL}	V_{DD}=3.3V	-10.5	-10	-9.5	V	Note 2
VCOM voltage	V_{CAC}	-	3.6	4.2	4.8	Vp-p	AC component, Note 3
	V_{CDC}	-		0.54		V	DC component, Note 4

Note 1: Test Condition: 8colorbar+Grayscale pattern, UPS051 mode, DCLK=27MHz, Frame rate: 60Hz, other registers are default setting.

Note 2: V_{GH} and V_{GL} are output voltages of integrated LCD driver IC.

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: V_{CDC} could be adjusted, so as to minimize flicker and maximum contrast on each module.

3.3 Recommended Capacitance Values of External Capacitor

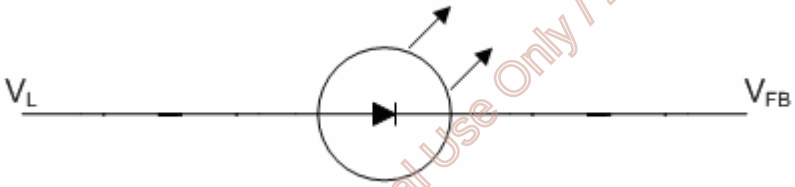
The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
VGH	4.7 to 10	25
VGL	4.7 to 10	16
VDD5	4.7 to 10	25
VDD3	4.7 to 10	16
VDD2	4.7 to 10	10
DVDD	4.7 to 10	6.3
VCAC	4.7 to 10	10
V1, V2	2.2 to 10	10
V3, V4	2.2 to 10	10
V5, V6	2.2 to 10	16
V7, V8	2.2 to 10	16

3.4 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.[Note1]	Unit	Remark
Backlight Current			25	27.5	mA	**Note2**
Backlight voltage	V_L		3.2	-	V	
Feedback voltage	V_{FB}	-	0.6	-	V	

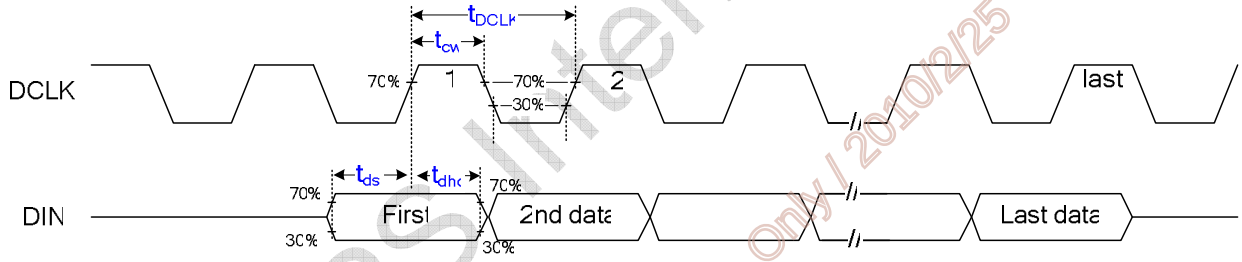
Note1: To consider LED driver and feedback resistor tolerance.
Note2: If using LCD internal LED driver controller the maximum setting should be typical value. Ta=25℃

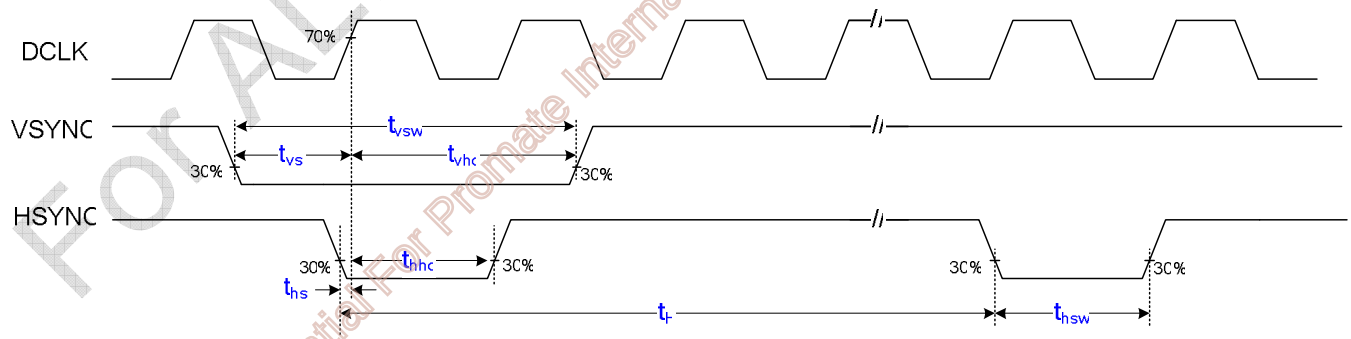


4. Input timing AC characteristic

(VDD=3.0 ~3.6V, AGND=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
CLK time	t_{DCLK}	33	-	188	ns	
DCLK width	t_{cw}	16.5	-	94	ns	D_{cw}=50%
DCLK duty cycle	Tcw	40	50	60	%	
VSYNC setup time	Tvst	6	-	-	ns	
VSYNC hold time	Tvhd	6	-	-	ns	
HSYNC setup time	Thst	6	-	-	ns	
HSYNC hold time	Thhd	6	-	-	ns	
Data setup time	Tdst	6	-	-	ns	
Data hold time	Tdhd	6	-	-	ns	
HSYNC width	Thsw	1	1	254	t_{DCLK}	
VSYNC width	Tvsw	1 t_{DCLK}	1 t_{DCLK}	6H		





t_H means: HSYNC period

5. Input timing format

5.1 UPS051 timing conditions (Refer to Fig.1 Fig.2 Fig.3)

Parameter			Symbo	Min.	Typ.	Max.	ALPS	Unit.	Remark
DCLK frequency			$1/t_{DCLK}$	8.43	9.71	12.69	13.5	MHz	
HSYNC	Period		t_H	580	617	765	858	t_{DCLK}	
	Display period		t_{hd}	480			480	t_{DCLK}	
	Back porch		t_{hbp}	20	30	255	125	t_{DCLK}	Note 1
	Front porch		t_{hfp}	80	107	30	253	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	t_{hbp} - 1	63	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	276.5	262.5	t_H	
		Even							
	Display period	Odd	t_{vd}	240			240	t_H	
		Even							
	Back porch	Odd	t_{vb}	1	21	31	18	t_H	Note 2
		Even		1.5	21.5	31.5	18.5		
	Front porch	Odd	t_{vfp}	1.5	1	5.5	4.5	t_H	
		Even		1	1	5	4		
	Pulse width	Odd	t_{vsw}	$1t_{DCLK}$	$1t_{DCLK}$	$6t_H$	3H		
		Even							
	1 frame			485	525	553	525	t_H	

Note 1: The t_{hbp} time is adjustable by setting register HBLK; requirement of minimum blanking time and minimum front porch time must be satisfied.

Note 2: The t_{vbp} time is adjustable by setting register VBLK. UPS051 accepts both interlace and non-interlace vertical input timing.

Note 3: If frequency wants to use 13.5MHz, timing setting must follow above table.

Fig.1 UPS051 Input Horizontal Timing Chart

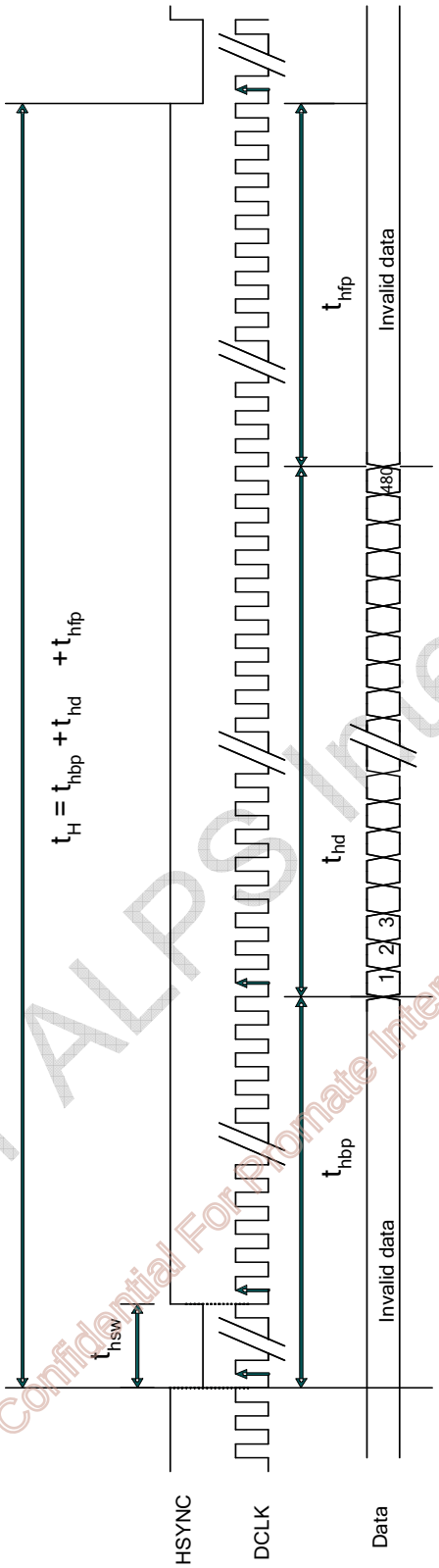
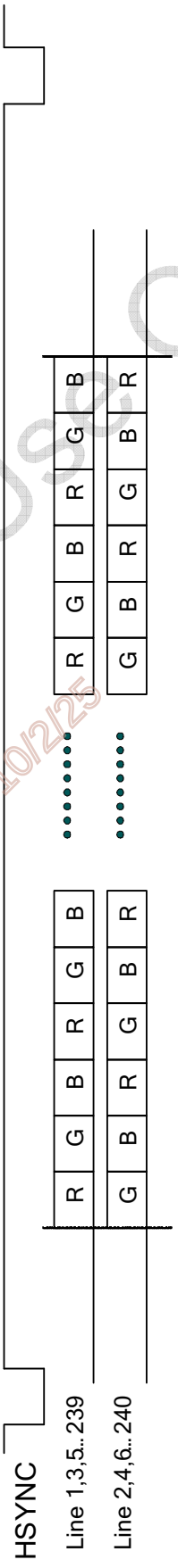


Fig.2 UPS051 Input Horizontal Data Sequence



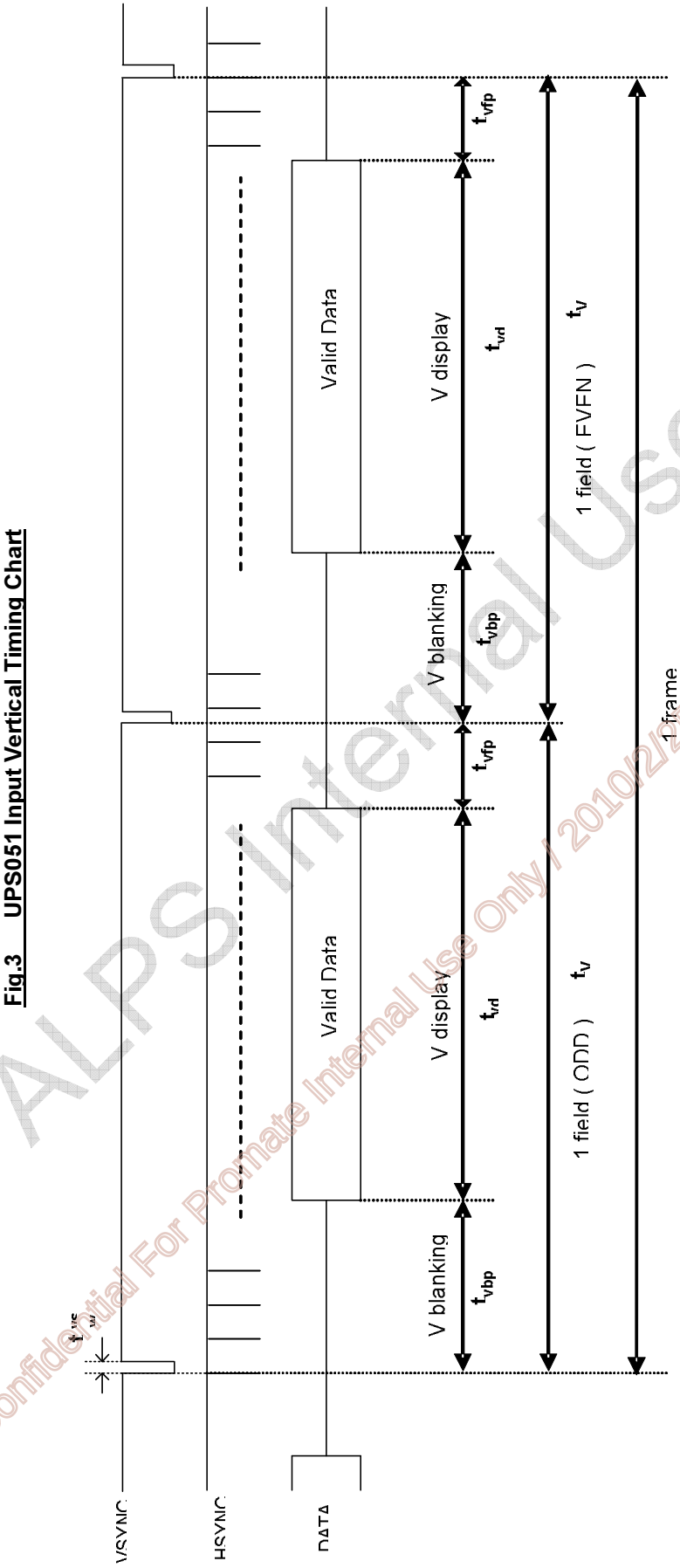


Fig.3 UPS051 Input Vertical Timing Chart

5.2 UPS052 timing

5.2.1 UPS052 (320 mode/NTSC/24.535MHz) timing specifications. (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20.54	24.535	30	MHz	
HSYNC	Period		t_H	1306	1560	1907	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	2	241	255	t_{DCLK}	
	Front porch		t_{hfp}	24	39	372	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	1	21	31	t_H	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	179.5	t_H	
		Even		1	1	179		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			485	525	901	t_H	

5.2.2 UPS052 (320 mode/PAL/24.375MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symb	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20.4	24.375	30	MHz	
HSYNC	Period		t_H	1306	1560	1920	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	3	241	255	t_{DCLK}	
	Front porch		t_{hfp}	23	39	385	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	3	24	34	t_H	
		Even		3.5	24.5	34.5		
	Front porch	Odd	t_{vfp}	1.5	0.5	128.5	t_H	
		Even		1	0	128		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			585	625	901	t_H	

5.2.3 UPS052 (360 mode/NTSC/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period		t_H	1466	1716	1907	t_{DCLK}	
	Display period		t_{hdisp}	1440			t_{DCLK}	
	Back porch		t_{hbp}	2	241	255	t_{DCLK}	
	Front porch		t_{hfp}	24	35	212	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	1	21	31	t_H	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	179.5	t_H	
		Even		1	1	179		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			485	525	901	t_H	

5.2.4 UPS052 (360 mode/PAL/27MHz) timing specifications (refer to Fig.4 Fig.5)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period		t_H	1466	1728	1920	t_{DCLK}	
	Display period		t_{hdisp}	1440			t_{DCLK}	
	Back porch		t_{hbp}	3	241	255	t_{DCLK}	
	Front porch		t_{hfp}	23	47	225	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	3	24	34	t_H	
		Even		3.5	24.5	34.5		
	Front porch	Odd	t_{vfp}	1.5	0.5	128.5	t_H	
		Even		1	0	128		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			585	625	901	t_H	

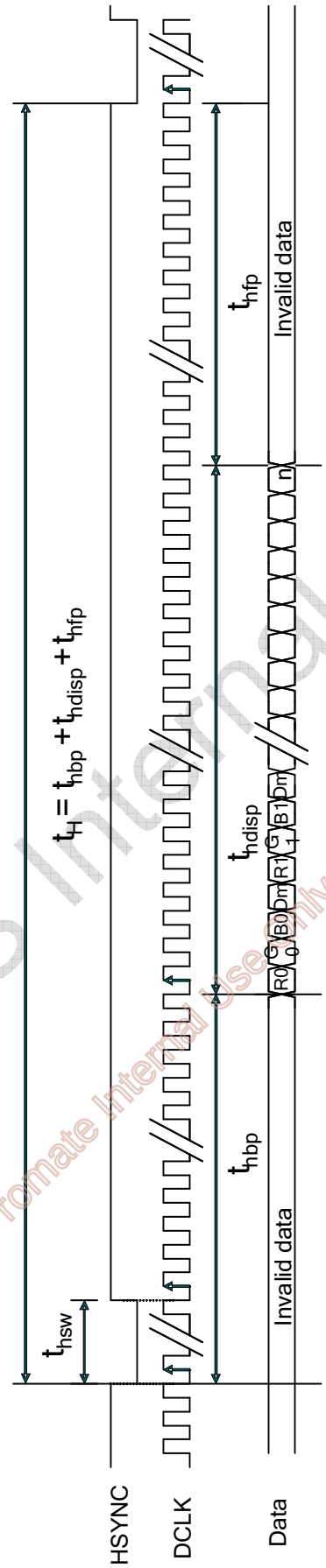


Fig.4 UPS052 Input Horizontal Timing Chart

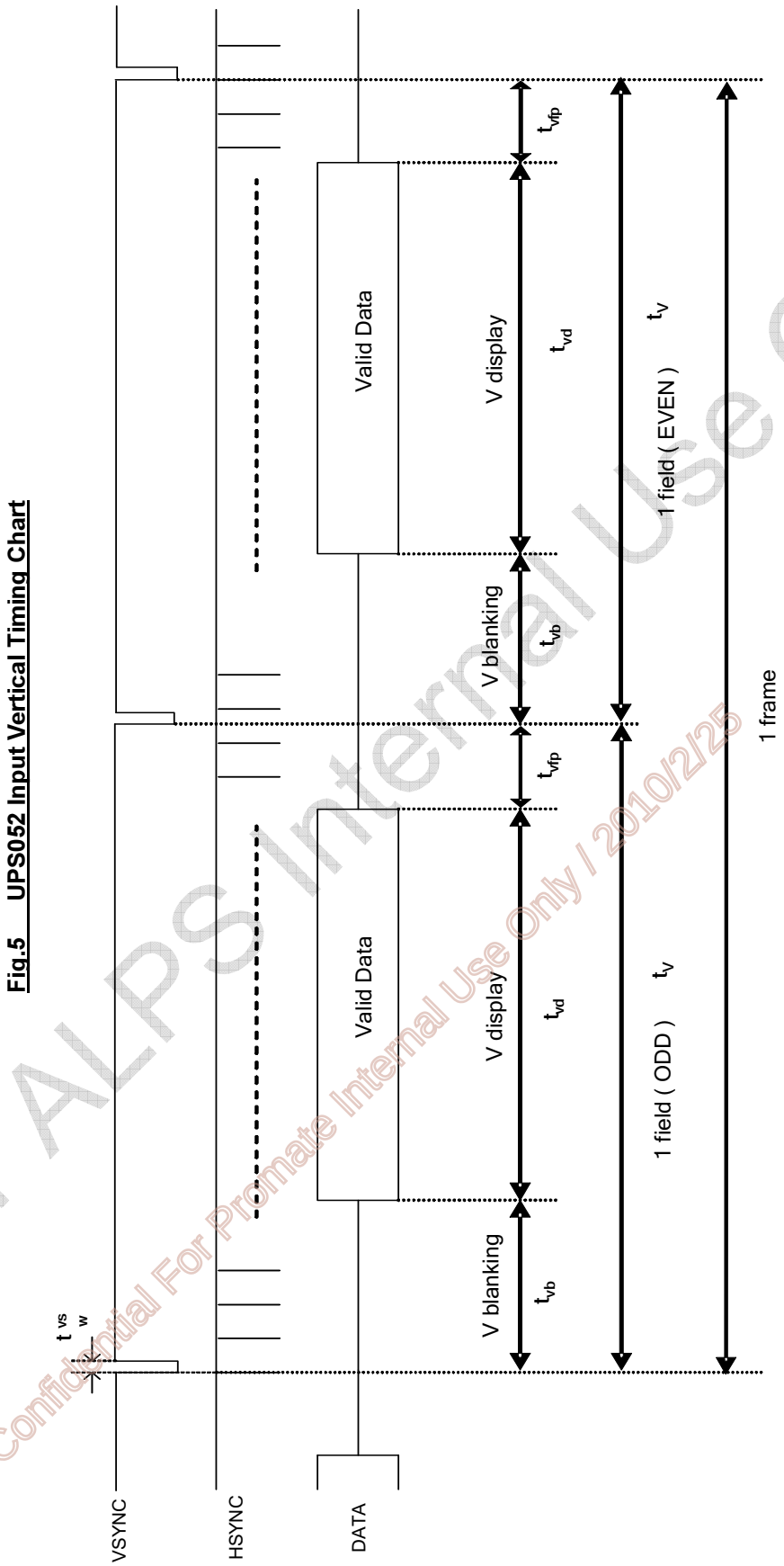
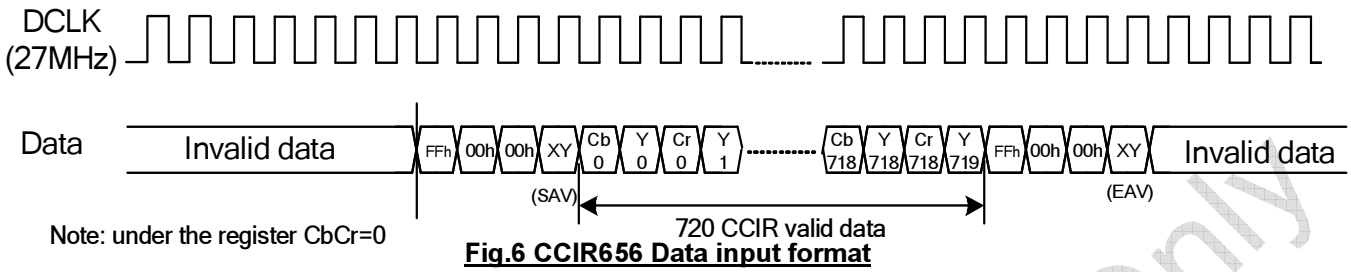


Fig.5 UPS052 Input Vertical Timing Chart

5.3 CCIR656 Timing



Note: under the register CbCr=0

Fig.6 CCIR656 Data input format

5.3.1 CCIR656 decoding

- FF 00 00 < XY > signals are involved with HSYNC, VSYNC and Field
- <XY> encode following bits:

F=field select : F=0 for field 1, F=1 for field 2;

V=1 during vertical blanking

H=0 at SAV , H=1 at EAV ,

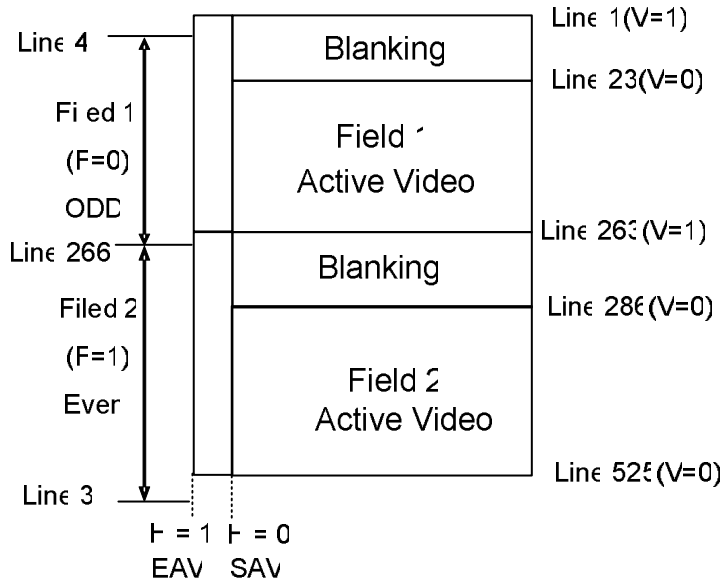
P3-P0=protection bits :

P3=V □ H P2=F □ H P1=F □ V P0=F □ V □ H □: represents the exclusive-OR function

- Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.
- Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0(LSB)**
1	F	V	H	P3	P2	P1	P0

5.3.2 CCIR656 NTSC



Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-22	0	1	1	0
23-262	0	0	1	0
263-265	0	1	1	0
266-285	1	1	1	0
286-525	1	0	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

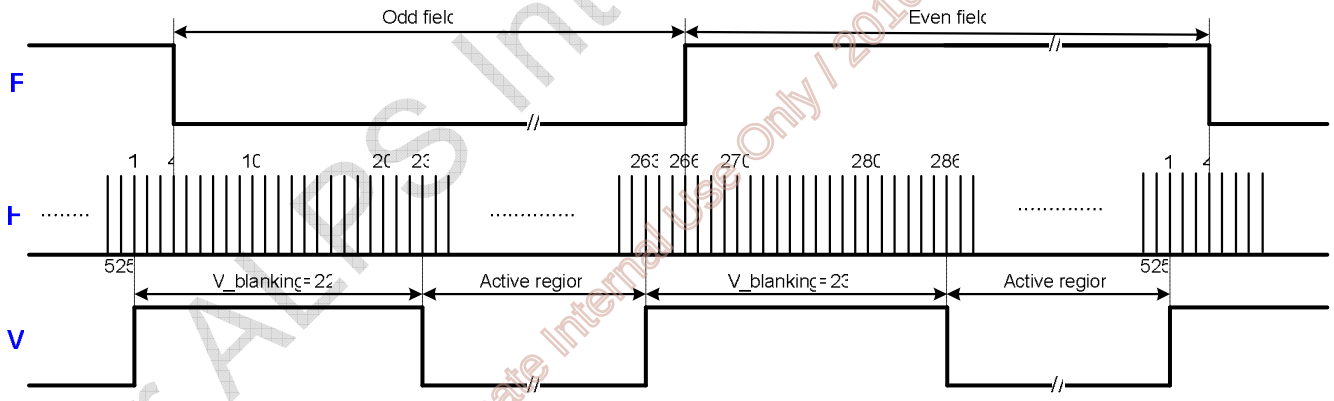
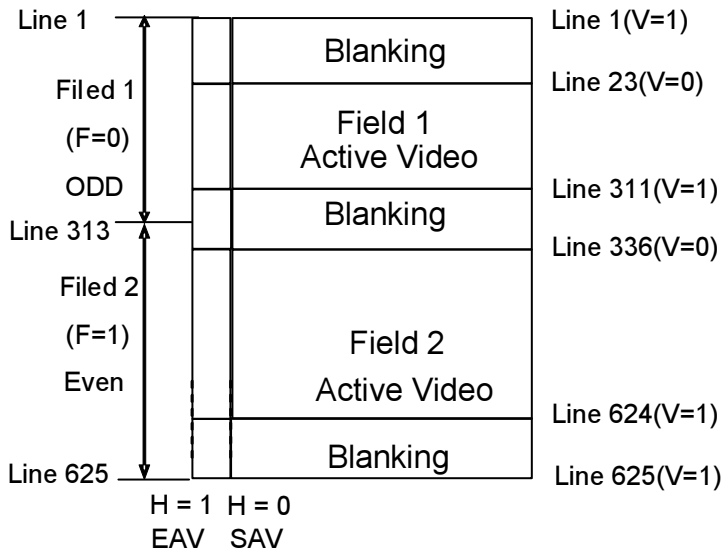


Fig.7 CCIR656 NTSC Mode Vertical Timing Format

5.3.3 CCIR656 PAL



Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
335-623	1	0	1	0
624-625	1	1	1	0

	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

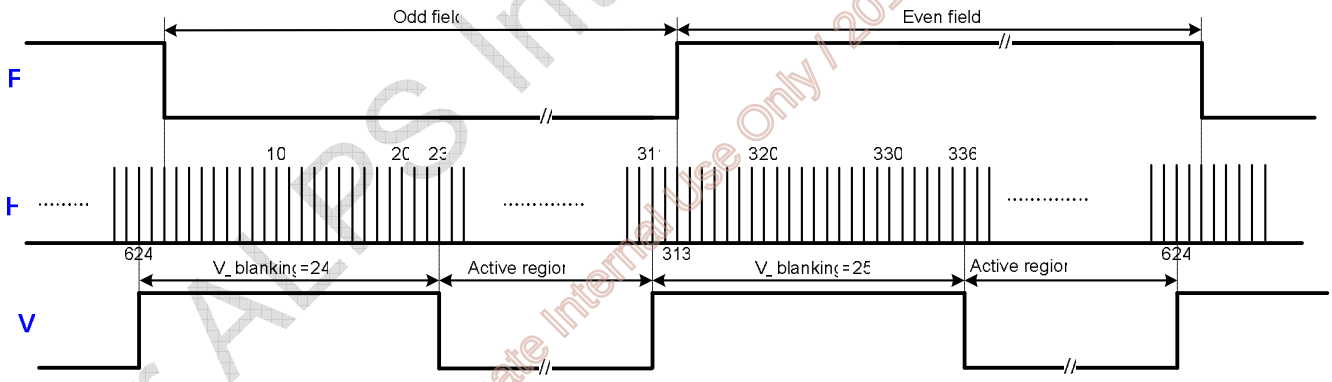


Fig.8 CCIR656 PAL Mode Vertical Timing Format

5.4 YUV 720 and YUV 640 timing

5.4.1 YUV 720 mode/NTSC timing specifications (refer to Fig.9 Fig.11)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period		t_H	1476	1716	1907	t_{DCLK}	
	Display period		t_{hdisp}	1440			t_{DCLK}	
	Back porch		t_{hbp}	2	240	255	t_{DCLK}	
	Front porch		t_{hfp}	34	36	212	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	1	21	31	t_H	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	179.5	t_H	
		Even		1	1	179		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			485	525	901	t_H	

5.4.2 YUV 720 mode/PAL timing specifications (refer to Fig.9 Fig.11)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	23	27	30	MHz	
HSYNC	Period		t_H	1476	1728	1920	t_{DCLK}	
	Display period		t_{hdisp}	1440			t_{DCLK}	
	Back porch		t_{hbp}	3	240	255	t_{DCLK}	
	Front porch		t_{hfp}	33	48	225	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	3	24	34	t_H	
		Even		3.5	24.5	34.5		
	Front porch	Odd	t_{vfp}	1.5	0.5	128.5	t_H	
		Even		1	0	128		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			585	625	901	t_H	

5.4.3 YUV 640 mode/NTSC timing specifications (refer to Fig.10 Fig.11)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20.65	24.535	30	MHz	
HSYNC	Period		t_H	1314	1560	1907	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	2	240	255	t_{DCLK}	
	Front porch		t_{hfp}	32	40	372	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	242.5	262.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	1	21	31	t_H	
		Even		1.5	21.5	31.5		
	Front porch	Odd	t_{vfp}	1.5	1.5	179.5	t_H	
		Even		1	1	179		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			485	525	901	t_H	

5.4.4 YUV 640 mode/PAL timing specifications (refer to Fig.10 Fig.11)

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20.5	24.375	30	MHz	
HSYNC	Period		t_H	1314	1560	1920	t_{DCLK}	
	Display period		t_{hdisp}	1280			t_{DCLK}	
	Back porch		t_{hbp}	3	240	255	t_{DCLK}	
	Front porch		t_{hfp}	33	40	385	t_{DCLK}	
	Pulse width		t_{hsw}	1	1	200	t_{DCLK}	
VSYNC	Period	Odd	t_V	292.5	312.5	450.5	t_H	
		Even						
	Display period	Odd	t_{vdisp}	288			t_H	
		Even						
	Back porch	Odd	t_{vbp}	3	24	34	t_H	
		Even		3.5	24.5	34.5		
	Front porch	Odd	t_{vfp}	1.5	0.5	128.5	t_H	
		Even		1	0	128		
	Pulse width	Odd	t_{vsw}	1 t_{DCLK}	1 t_{DCLK}	6 t_H		
		Even						
	1 frame			585	625	901	t_H	

Fig.9 YUV720 Input Horizontal Timing Chart

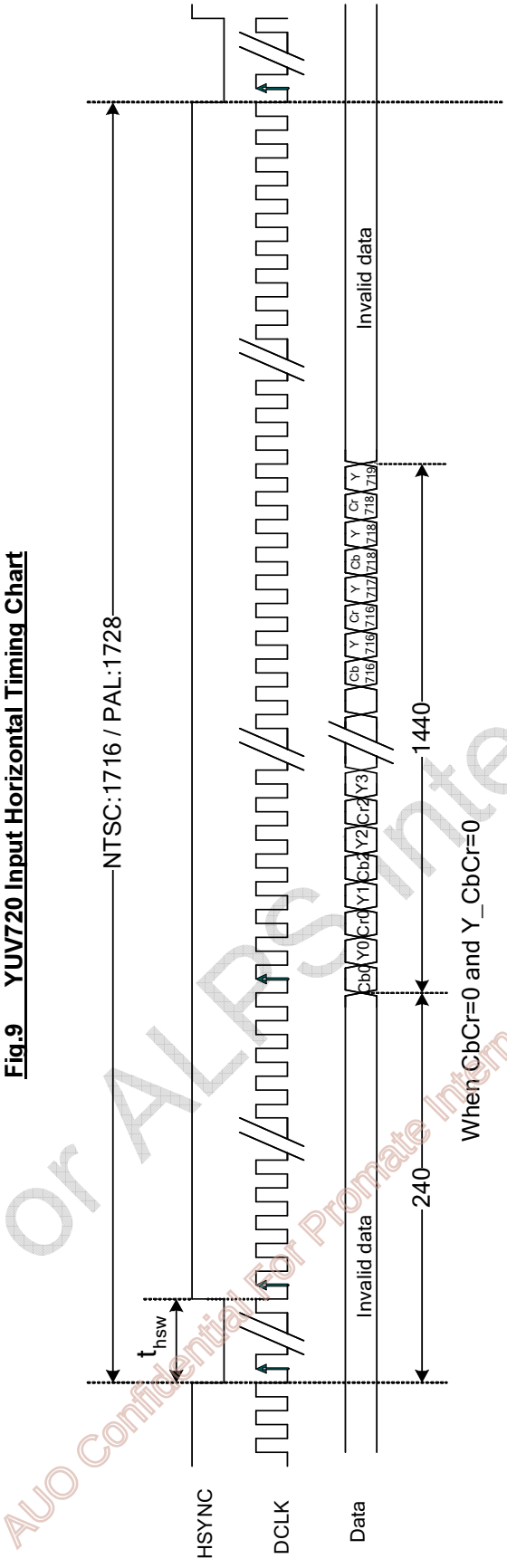
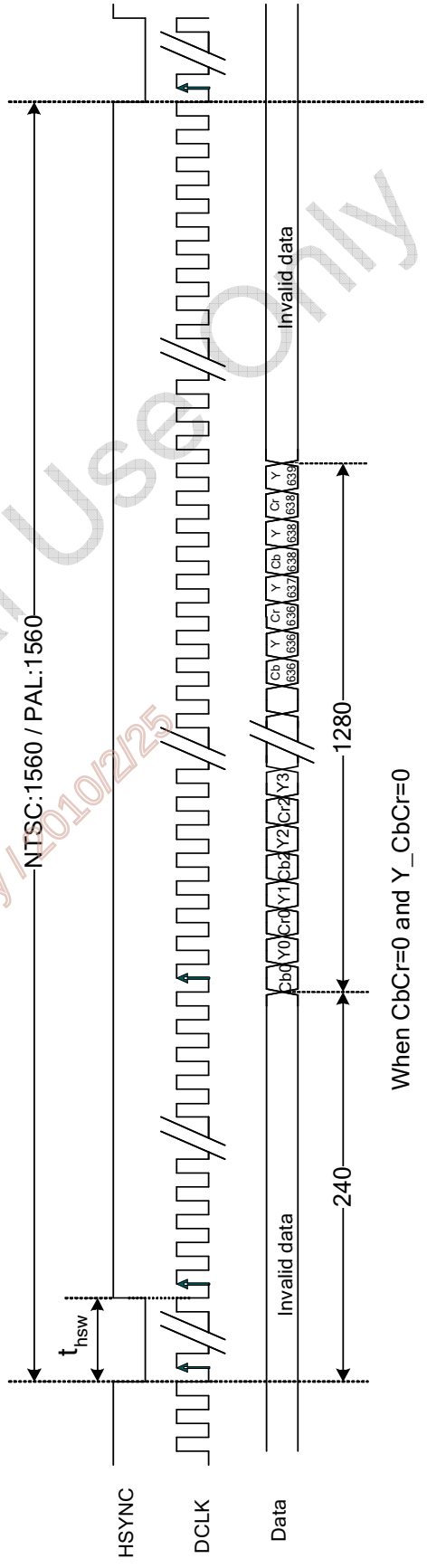


Fig.10 YUV640 Input Horizontal Timing Chart



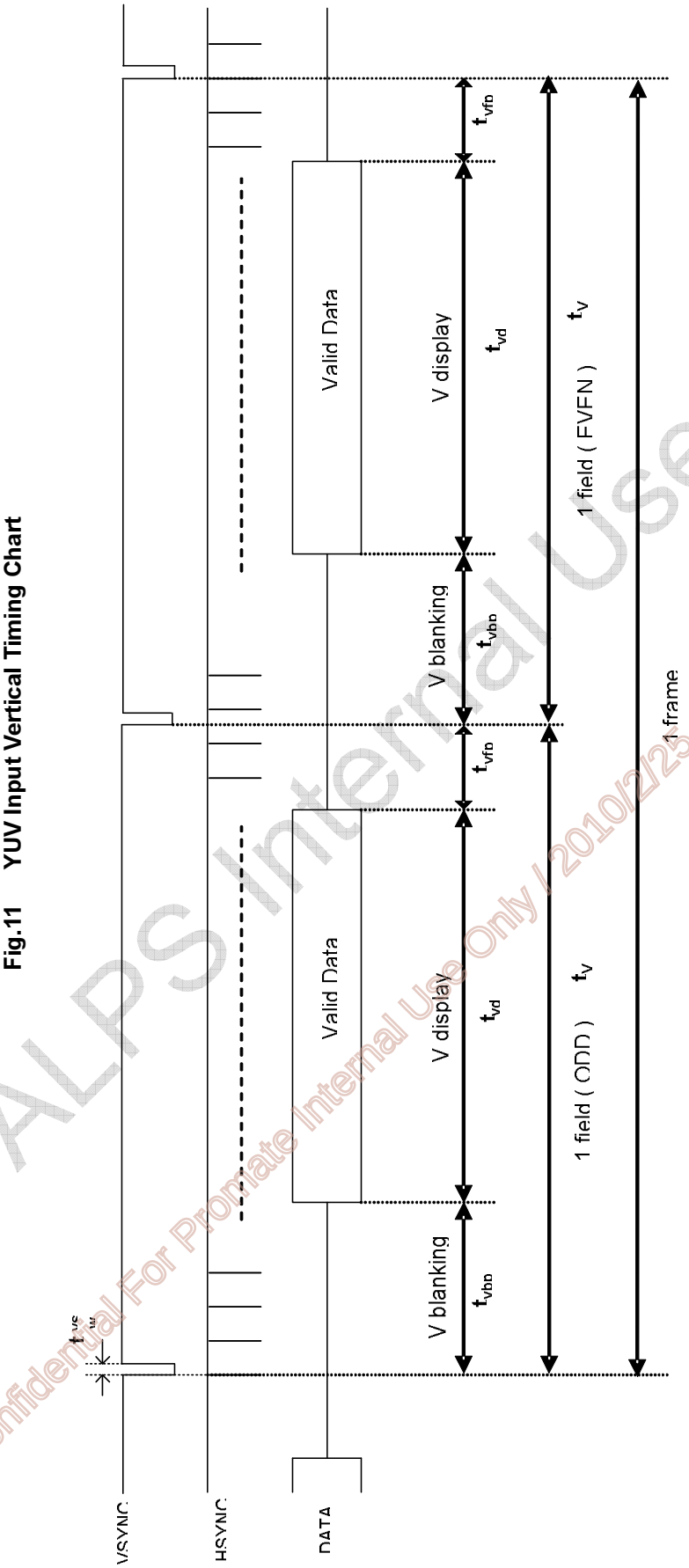


Fig.11 YUV Input Vertical Timing Chart

5.5 CCIR656/YUV 720/YUV 640 to RGB conversion

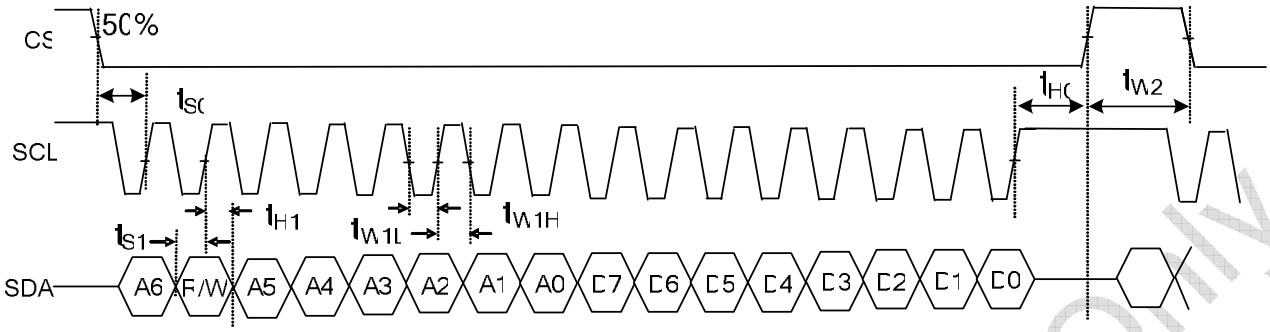
$R_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 1.596*(C_{rn}-128)$

$G_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] - 0.813*(C_{rn}-128) - 0.392*(C_{bn}-128)$

$B_n=1.164*[(Y_{2n-1}+Y_{2n})/2-16] + 2.017*(C_{bn}-128)$

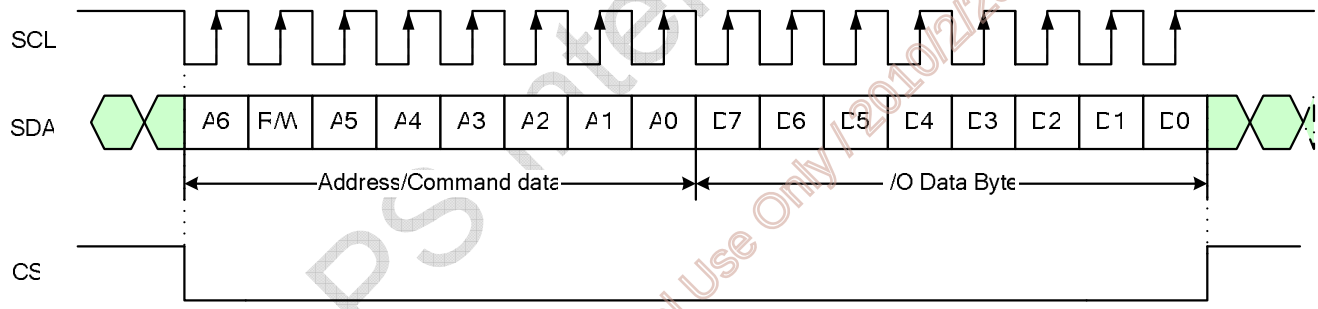
Where Y:16~235 C_r:16~240 C_b:16~240

6. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50	-	-	ns
Serial data input setup Time	t_{S1}	50	-	-	ns
CS input hold Time	t_{H0}	50	-	-	ns
Serial data input hold Time	t_{H1}	50	-	-	ns
SCL pulse low width	t_{W1L}	50	-	-	ns
SCL pulse high width	t_{W1H}	50	-	-	ns
CS pulse high width	t_{W2}	400	-	-	ns

6.1 Timing chart



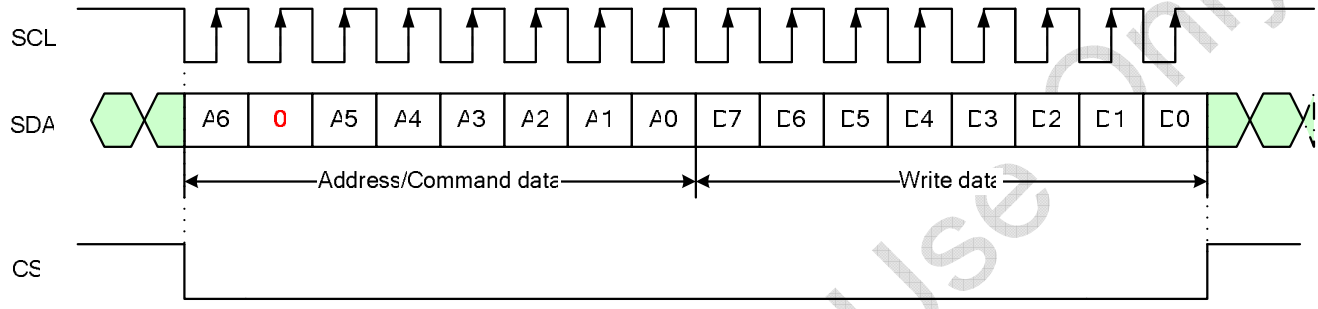
1. Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
2. Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
3. The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
4. If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
5. If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
6. Serial block operates with the SCL clock.
7. Serial data can be accepted in the standby (power save) mode.
8. Do not keep SPI interface CS rising to Hsync falling is 35 dclk.

6.2 The configuration of serial data at SDA terminal is at below

MSB LSB

A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address	R/W	Address						DATA							

Write Mode:



6.3 Register table

- When GRB is low, all registers reset to default values
- Serial commands are executed at next VSYNC signal
- ( ) is default

No.	Register address								MSB			Register data				LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	0	0	Y_CbCr (0)	CCIR601 (0)	x	x	VCAC (0)	VCOM_AC (011)		
R1	0	0	0	0	0	0	0	1	VCDCE(1)	0	VCOM_DC(0Ah)					
R3	0	0	0	0	0	0	1	1	Brightness (40h)							
R4	0	0	0	0	0	1	0	0	Narrow (0)	YUV (0)	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	PFM_DUTY (011)			SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	HBLK_EN (0)	LED_Current (00)	VBLK (15h)					
R7	0	0	0	0	0	1	1	1	HBLK(1Eh)							
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							
R14	0	0	0	0	1	1	1	0	x	SUB_CONTRAST_R(40h)						
R15	0	0	0	0	1	1	1	1	x	SUB_BRIGHTNESS_R(40h)						
R16	0	0	0	1	0	0	0	0	x	SUB_CONTRAST_B(40h)						
R17	0	0	0	1	0	0	0	1	x	SUB_BRIGHTNESS_B(40h)						
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE(0111)				LED_ON_RATIO(1111)			
R22	0	0	0	1	0	1	1	0	x	x	x	x	x	GAMMA set (1)	x	x
R23	0	0	0	1	0	1	1	1	x	x	GMA_V8(01)		x	x	GMA_V4(01)	
R24	0	0	0	1	1	0	0	0	x	x	GMA_V25(10)		x	x	GMA_V16(10)	
R25	0	0	0	1	1	0	0	1	x	x	GMA_V48(10)		x	x	GMA_V36(10)	
R26	0	0	0	1	1	0	1	0	x	x	GMA_V60(10)		x	x	GMA_V55(10)	

Note: 1. “x” => please set to ‘0’.

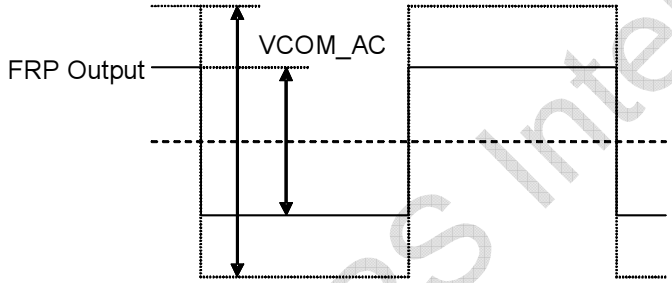
6.4 Register description

R0:

No.	Register address								Register data							
	A6	R/W	A5	A4	A3	A2	A1	A0	MSB D7	D6	D5	D4	D3	D2	D1	LSB D0
R0	0	0	0	0	0	0	0	0	Y_CbCr(0)	CCIR601 (0)	x	x	VCAC(0)	VCOM_AC(011)		

VCOM_AC: Common voltage AC level selection (deviation ±0.1V)

VCOM_AC			VCAC	Voltage (V)
D2	D1	D0	D3	
0	0	0	0	3.6
0	0	0	1	3.7
0	0	1	0	3.8
0	0	1	1	3.9
0	1	0	0	4.0
0	1	0	1	4.1
0	1	1	0	4.2(Default)
0	1	1	1	4.3
1	0	0	0	4.4
1	0	0	1	4.5
1	0	1	0	4.6
1	0	1	1	4.7
1	1	X	X	4.8



CCIR601: CCIR601 input timing selection

CCIR601	Function
0(Default)	Disable CCIR601 (Default)
1	Enable CCIR601. (Please refer to the table of R4(SEL) for detail description)

Y_CbCr: Y & CbCr exchange position (only valid for 8-bit input YUV640 / YUV720)

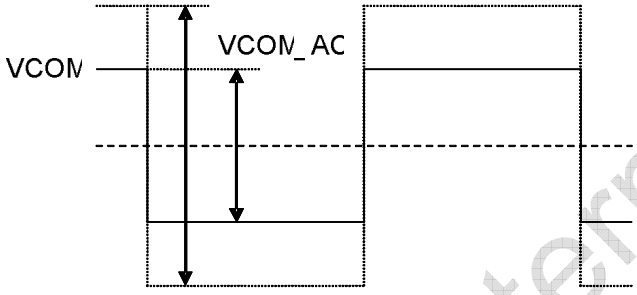
	CbCr(R12[4])='0'								CbCr(R12[4])='1'							
Y_CbCr='0' (Default)	Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3	Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3
Y_CbCr='1'	Y0	Cb0	Y1	Cr0	Y2	Cb2	Y3	Cr2	Y0	Cr0	Y1	Cb0	Y2	Cr2	Y3	Cb2

R1:

No	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R1	0	0	0	0	0	0	0	1	VCDCE (1)	0	VCOM_DC (0Ah)					

VCOM_DC: Common voltage DC level selection (20mV/step)

D5~D0	VCOM DC level (V)
00h	0.1
:	:
0Ah(Default)	0.3(Default)
:	:
3Fh	1.36



VCDCE: VCOM_DC function enable setting

VCDCE	Function
0	VCOM _DC function disable. The COMDC pin is Hi-Z.
1	VCOM_DC function enable. The COMDC voltage follows VCOM_DC setting. (Default)

R3:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	0	0	0	0	1	1	Brightness (40h)							

BRIGHTNESS: RGB bright level setting, setting accuracy: 1 step / bit

D7 ~ D0	Brightness gain
00h	Dark (-64)
40h(Default)	Center (0) (Default)
FFh	Bright (+191)

R4:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R4	0	0	0	0	0	1	0	0	Narrow(0)	YUV(0)	SEL(00)		NTSC/PAL(10)		VDIR(1)	HDIR(1)

HDIR: Horizontal scan direction setting

HDIR	Function
0	Right to left scan
1	Left to right scan (Default)

VDIR: Vertical scan direction setting

VDIR	Function
0	Down to up scan
1	Up to down scan (Default)

NTSC/PAL: NTSC or PAL input mode selection (for UPS052 input timing)

NTSC/PAL		Mode
D3	D2	
0	0	PAL
0	1	NTSC
1	X	Auto detection (Default)

SEL: Input data timing format selection

CCIR601	YUV	SEL		INPUT TIMING FORMAT
		D5	D4	
0	0	0	0	UPS051 (Default)
0	0	0	1	UPS052 320 × 240
0	0	1	X	UPS052 360 × 240
0	1	X	X	CCIR656
1	1	0	X	YUV 640(*)
1	1	1	0	YUV 720(*)

(*)Please refer to YUV640/YUV720 horizontal timing spec for detailed description.

YUV: YUV (CCIR656, YUV640, YUV720) or RGB input selection

YUV	Function
0	RGB input (Default)
1	CCIR656 / YUV640 / YUV720 input.

When this command is sent to ASIC, it will be executed immediately

Narrow: Normal display and Narrow display selection.

Narrow	Function
0	Normal display (Default)
1	Narrow Display

Narrow=0

Narrow=1

R5:

No	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R5	0	0	0	0	0	1	0	1	DRV_FREQ(0)	GRB(1)	PFM_DUTY(011)			SHDB2(1)	SHDB1(1)	STB(0)

STB: Standby (Power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

SHDB1: Shut down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by power on/off sequence (Default)

SHDB2: Shut down for VGH/VGL charge pump

SHDB2	Function
0	VGH/VGL charge pump is always off
1	VGH/VGL charge pump is controlled by power on/off sequence (Default)

PFM_DUTY: PFM duty cycle selection for back light power converter

PFM_DUTY			Function
D5	D4	D3	PFM duty cycle
0	0	0	50%
0	0	1	60%
0	1	0	65%
0	1	1	70%(Default)
1	0	0	75%
1	0	1	80%
1	1	0	85%
1	1	1	90%

GRB: Register reset setting

GRB	Function
0	Reset all registers to default value
1	Normal operation (Default)

DRV_FREQ: DRV signal frequency setting

DRV_FREQ	DRV frequency
0(Default)	DCLK / 64
1	DCLK / 128

R6:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(15h)				

VBLK: Vertical blanking setting

UPS051, UPS052, YUV640 and YUV720 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
15h	21(Default)	
1Fh	31	

CCIR656 NTSC mode

D4 ~ D0	VBLK	Unit
01h	1	H (line)
16h	22(Default)	
1Fh	31	

UPS052, CCIR656 and YUV640 and YUV720 PAL mode(Vertical blanking + 3)

D4 ~ D0	VBLK	Unit
00h	3	H (line)
15h	24(Default)	
1Fh	34	

Note: V-blanking must be adjusted based on the input data.

LED_CURRENT: adjust LED current

DC-DC feedback voltage

D6	D5	Feedback Threshold voltage
0	0	0.6V(20mA) (default)
0	1	0.75V(25mA)
1	0	0.45V(15mA)
1	1	0.3V(10mA)

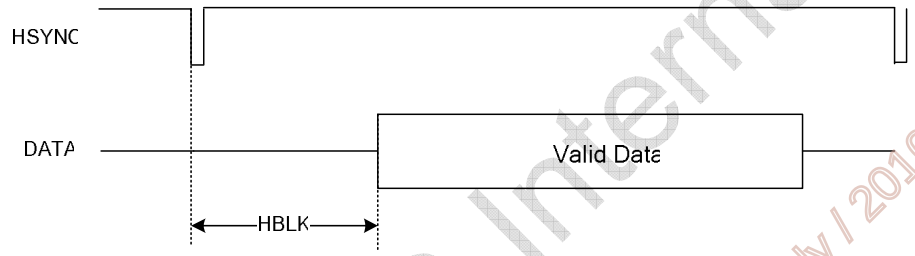
R6 & R7:

No	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R6	0	0	0	0	0	1	1	0	HBLK_EN(0)	LED_Current(00)		VBLK(15h)				
R7	0	0	0	0	0	1	1	1	HBLK(46h)							

HBLK_EN & HBLK: Horizontal blanking setting

HBLK_EN	HBLK(D7~D0)	HBLK	Unit	Remark
x	14h	20	DCLK(*)	UPS051
x	1Eh	30(Default)		
x	FFh	255		
0	x	241(fixed)	DCLK(*)	UPS052
1	02h ~ FFh	2 ~ 255	DCLK(*)	
0	xxh	240(fixed)	DCLK(*)	YUV640, YUV720
1	02h ~ FFh	2 ~ 255	DCLK(*)	

*The frequency of DCLK is different under different input timing.



R8:

No.	Register address								MSB		Register data					LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		x	x	x	x	x	x

BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

R12:

No.	Register address								MSB			Register data				LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R12	0	0	0	0	1	1	0	0	PAIR(00)		x	CbCr(0)	x	Vdpol(1)	Hdpol(1)	DCLKpol(0)

DCLKpol: DCLK polarity selection

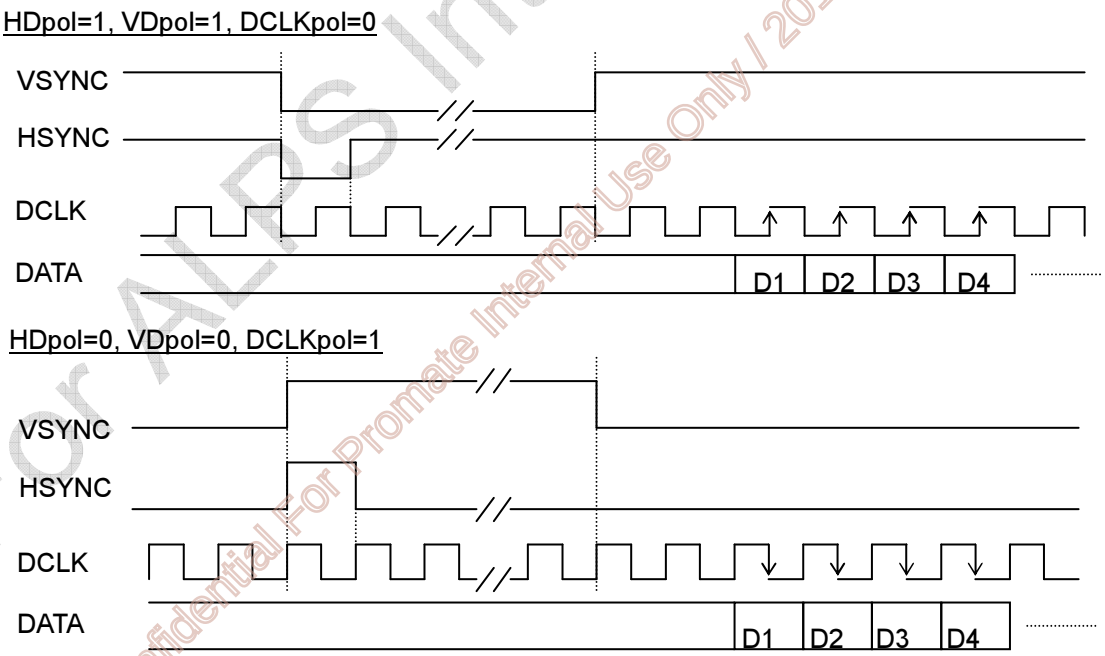
DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)



CbCr: Cb & Cr exchange position, (Please refer to the table of R0(Y_CbCr) for detail description)

CbCr='0'		Cb0	Y0	Cr0	Y1	Cb2	Y2	Cr2	Y3
CbCr='1'		Cr0	Y0	Cb0	Y1	Cr2	Y2	Cb2	Y3

PAIR: Vertical start time setting for Odd/Even frame

UPS051 / UPS052 NTSC / UPS052 PAL (*)

PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
x	0	21/21(Default)	H (line)
x	1	21/20	

CCIR656/YUV640/YUV720 NTSC/PAL (**)

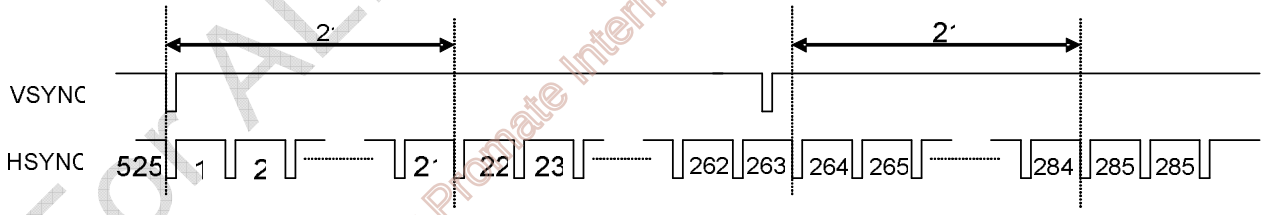
PAIR		VBLK	Unit
D7	D6	ODD/EVEN	
0	0	22/22(Default)	H (line)
0	1	22/23	
1	0	23/22	
1	1	23/23	

(*)The typical value of VBLK of UPS052 PAL(24 H) is different than UPS051/UPS052 NTSC(21H).

(**) The typical value of VBLK of CCIR656 PAL(24 H) is different than CCIR656 NTSC(22H).

Note: V-blanking must be adjusted based on the input data.

For example:



Field \ Line	PAIR=0		PAIR=1	
	START	END	START	END
ODD	22	26'	22	26'
EVEN	285	524	284	523

This table is based on VBLK=2'

R13:

No.	Register address								MSB Register data LSB							
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R13	0	0	0	0	1	1	0	1	CONTRAST_RGB(40h)							

CONTRAST_RGB: RGB contrast level setting, the gain changes (1/64) / bit

D7 ~ D0	Contrast gain
00h	0
40h	1(Default)
FFh	3.984

R14~R17:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R14	0	0	0	0	1	1	0	1	x	SUB-CONTRAST_R(40h)						
R16	0	0	0	1	0	0	0	0	X	SUB-CONTRAST_B(40h)						

SUB-CONTRAST: R/B sub-contrast level setting, the gain changes (1/256) / bit

D6 ~ D0	Brightness gain
00h	0.75
40h	1(Default)
7Fh	1.246

DOUT_G[7:0] = DIN[7:0] x Contrast[0 to 1.0 to 3.984]

DOUT_R[7:0] = DIN[7:0] x Contrast[0 to 1.0 to 3.984] x sub-contrast R [0.75 to 1.0 to 1.246]

DOUT_B[7:0] = DIN[7:0] x Contrast[0 to 1.0 to 3.984] x sub-contrast B [0.75 to 1.0 to 1.246]

Note: output values above “255” clipped

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R15	0	0	0	0	1	1	1	1	X	SUB-BRIGHTNESS_R(40h)						
R17	0	0	0	1	0	0	0	1	X	SUB-BRIGHTNESS_B(40h)						

SUB-BRIGHTNESS: R/B sub-bright level setting, setting accuracy: 1 step / bit

D6 ~ D0	Brightness gain
00h	Dark (-64)
40h	Center (0)(Default)
7Fh	Bright (+63)

DOUT_G[7:0] = DIN_G[7:0] + Bright[-64 to 0 to +191]

DOUT_R[7:0] = DIN_R[7:0] + Bright[-64 to 0 to +191] + Sub-bright R[-64 to 0 to +63]

DOUT_B[7:0] = DIN_B[7:0] + Bright[-64 to 0 to +191] + Sub-bright B[-64 to 0 to +63]

Note: Output values below “0” and above “255” clipped

R21:

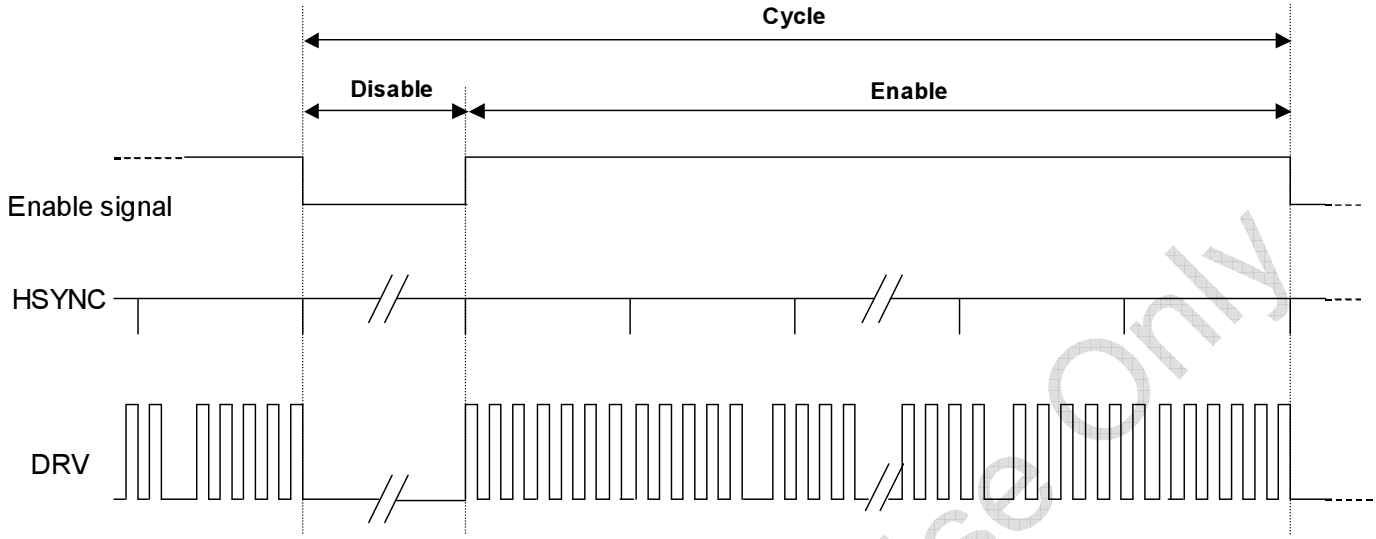
No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R21	0	0	0	1	0	1	0	1	LED_ON_CYCLE (0111)				LED_ON_RATIO (1111)			

LED_ON_RATIO: Set the active ratio of enable signal, and we can use it to adjust brightness of the LEDs.

LED_ON_RATIO				Value
D3	D2	D1	D0	
0	0	0	0	1/16
0	0	0	1	2/16
0	0	1	0	3/16
0	0	1	1	4/16
0	1	0	0	5/16
0	1	0	1	6/16
0	1	1	0	7/16
0	1	1	1	8/16
1	0	0	0	9/16
1	0	0	1	10/16
1	0	1	0	11/16
1	0	1	1	12/16
1	1	0	0	13/16
1	1	0	1	14/16
1	1	1	0	15/16
1	1	1	1	16/16(Default)

LED_ON_CYCLE : Set the cycle of enable signal , and we can use it to adjust brightness of the LEDs.

LED_ON_CYCLE				Value
D7	D6	D5	D4	
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8(Default)
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16



$16 * LED\_ON\_CYCLE = LED\_ON\_CYCLE * (LED\_ON\_RATIO * 16) + LED\_ON\_CYCLE * (16 - LED\_ON\_RATIO * 16)$

(Cycle) **(Enable)** **(Disable)** Unit : HSYNC

for example:
LED_ON_RATIO is **"1001"**, and LED_ON_CYCLE is **"0111"**, then:
Cycle = 16 * **8** = 128(HSYNC)
Enable = **8** * ((**10/16**) * 16) = 80(HSYNC)
Disable = **8** * (16-(**10/16**) * 16) = 48(HSYNC) ➔62.5% on

R22:

No.	Register address								MSB Register data							LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R22	0	0	0	1	0	1	1	0	x	x	x	x	x	GAMMA set (1)	x	x

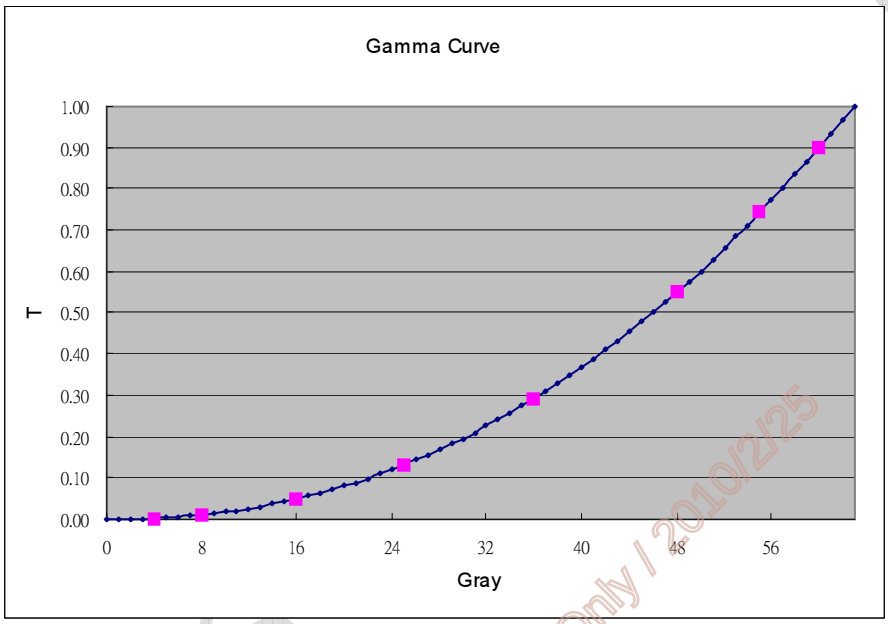
GAMMA set: Select auto or manual gamma setting

GAMMA set	Description
0	Manual set gamma by R23 ~ R26.
1	Auto set to gamma default.(Default).

R23 ~ R26:

No.	Register address								MSB	Register data						LSB
	A6	R/W	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
R23	0	0	0	1	0	1	1	1	x	x	GMA_V8 (01)		x	x	GMA_V4 (01)	
R24	0	0	0	1	1	0	0	0	x	x	GMA_V25 (10)		x	x	GMA_V16 (10)	
R25	0	0	0	1	1	0	0	1	x	x	GMA_V48 (10)		x	x	GMA_V36 (10)	
R26	0	0	0	1	1	0	1	0	x	x	GMA_V60 (10)		x	x	GMA_V55 (10)	

8 adjustable points



C. Optical Specification (Note1, Note 2 and Note 3)

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time Rise Fall		 Tr Tf	θ=0°	 -- --	 10 25	 40 50	 ms ms	 Note 4
Contrast ratio		CR	At optimized viewing angle	200	300	--		Note 5,6
Viewing Angle	Top Bottom Left Right	Φ_H Φ_L θ_L θ_R	CR□10	10 30 40 40	20 40 45 45	-- -- -- --	deg.	Note 7
Brightness		Y_L	θ=0°	200	250	--	cd/m^2	Note 8
Chromaticity	White	X θ	=0°	0.256	0.306	0.356		
		Y θ	=0°	0.281	0.331	0.381		
	Red	X θ	=0°	0.551	0.601	0.651		
		Y θ	=0°	0.280	0.330	0.380		
	Green	X θ	=0°	0.296	0.346	0.396		
		Y θ	=0°	0.532	0.582	0.632		
	Blue	X θ	=0°	0.108	0.158	0.208		
		Y θ	=0°	0.097	0.147	0.197		
Uniformity		ΔY_L	%	70	75	--	%	Note 10

Note 1. Ambient temperature =25℃.

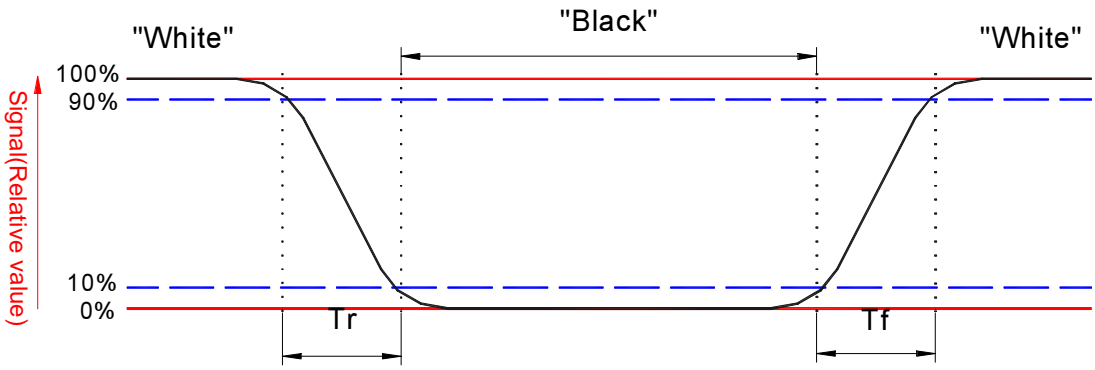
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White Vi=V_{i50} + $\overline{1.5V}$

Black Vi=V_{i50} ± 2.0V

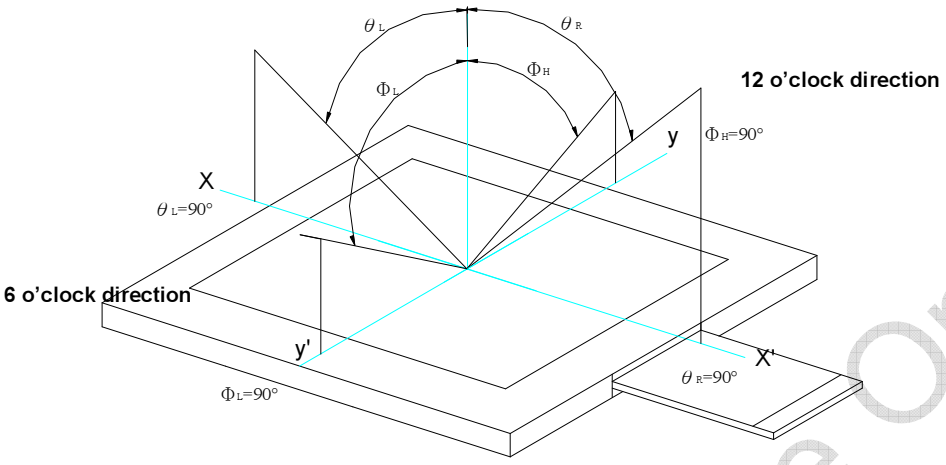
“±” Means that the analog input signal swings in phase with COM signal.

“ $\overline{+}$ ” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

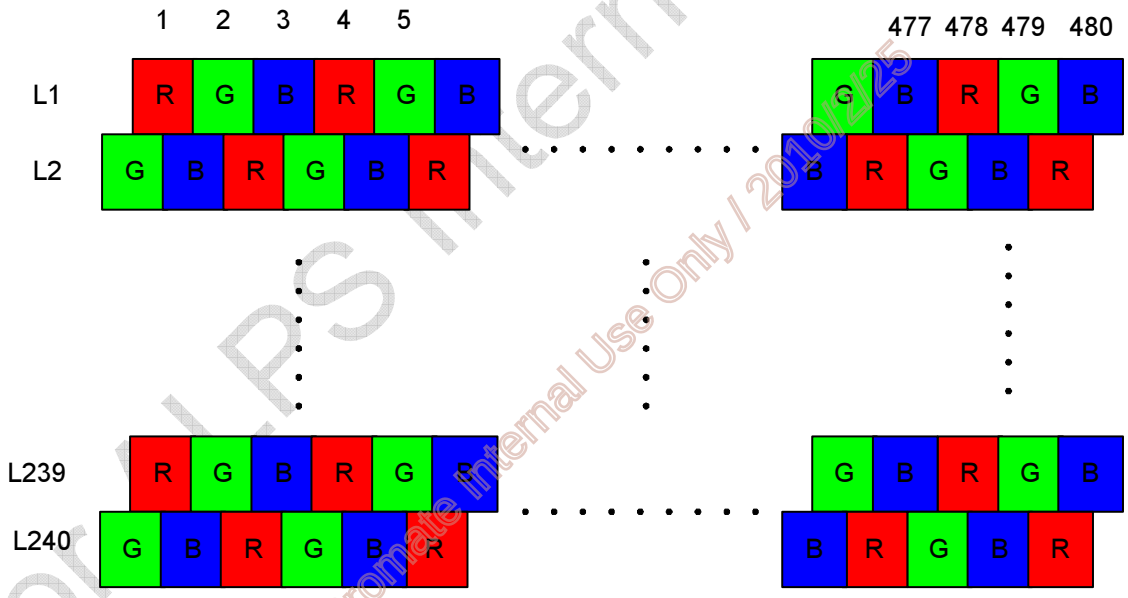
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, ϕ, Refer to figure as below.

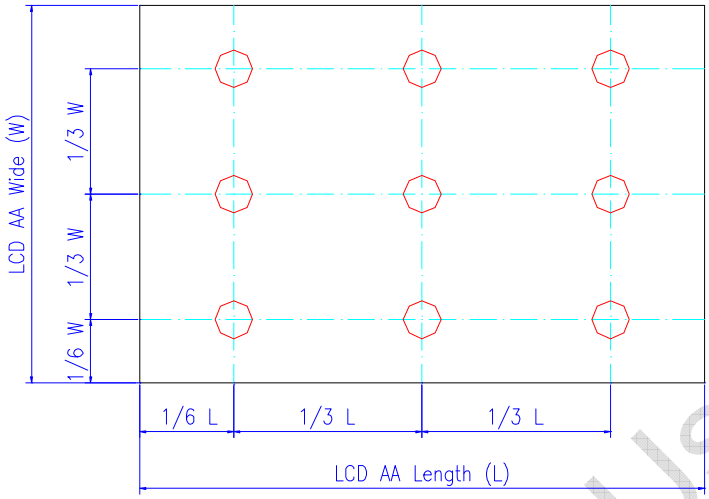


Note 8. Measured at the center area of the panel in gray level 255

Note 9. Color Filter Arrangement



Note 10. Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

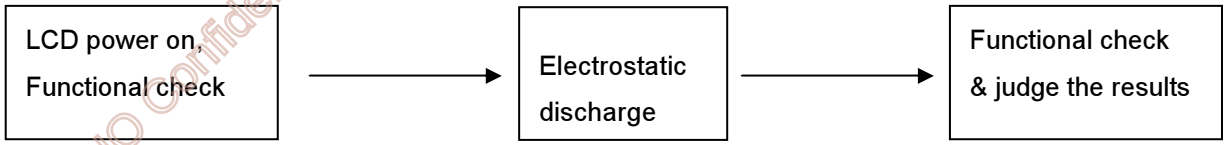
D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -25□ 240Hrs	
3	High Ttemperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= 0□ 240Hrs	
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~80□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 2,3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.

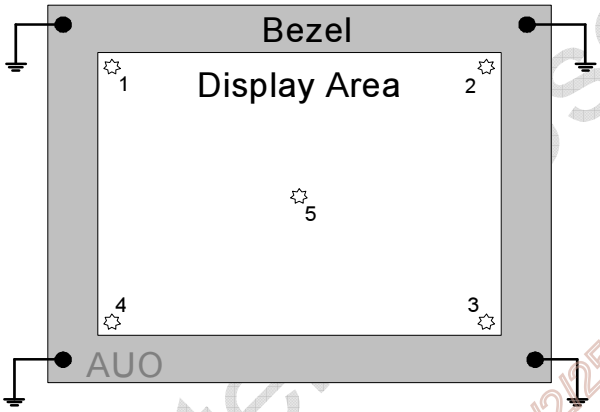
Note 2. ESD Testing Flow as the below,

Note 3. Make sure protection film(s) on top of polarizer or back of LCD module is(are) removed before test.



Note 3. ESD testing method.

1. Ambient: 24~26□, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B” and adapter “A025CN04”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
    a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
    b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing form

Palletizing sequence (if necessary)

(1). Box placement on wooden pallet

a. Place max 30 of corrugated boxes on wooden pallet and should not be pushed out of the pallet. (as showed below)

b. (420 *6) *5 layers: Max 30 boxes / pallet. (12600 pcs modules)

(2). Apply stretch film. Corner angle and PE band

a. Stretch film should cover around whole pallet.

b. Apply corner angle to 4 top edge and 4 side edge of the pallet.

c. Select corner angle length by height of palletizing.

d. PE band number is depended on customer requirement and height of palletizing.

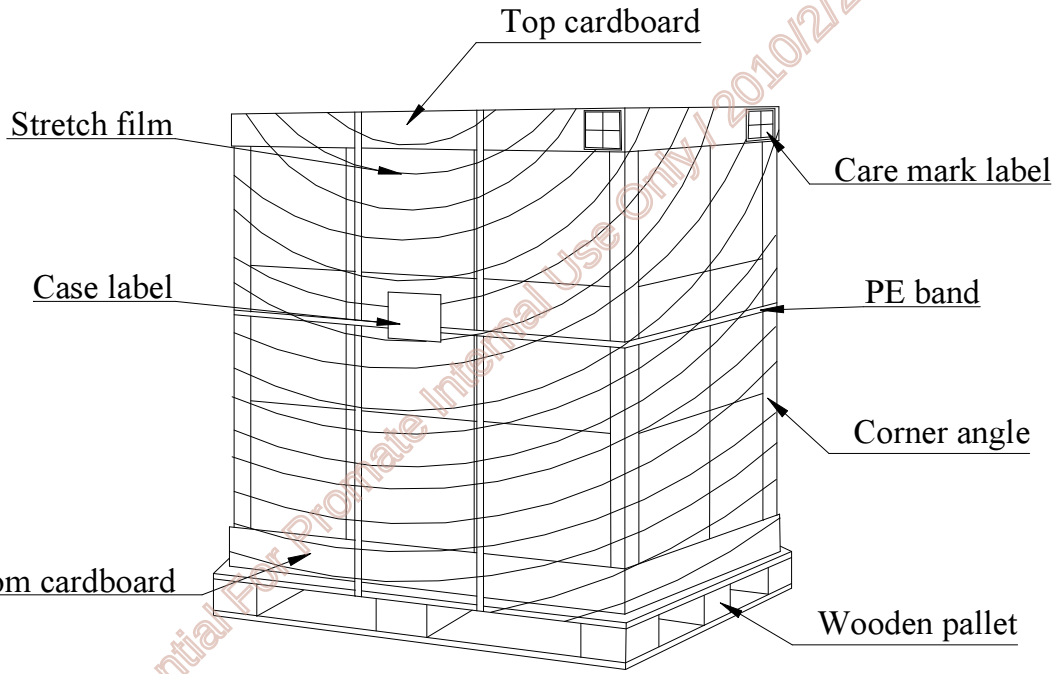
(3). Labeling

a. Apply shipping case label is depended on customer requirement.

b. Apply care mark label at 4 side (Front / Back / Left / Right)on the pallet.

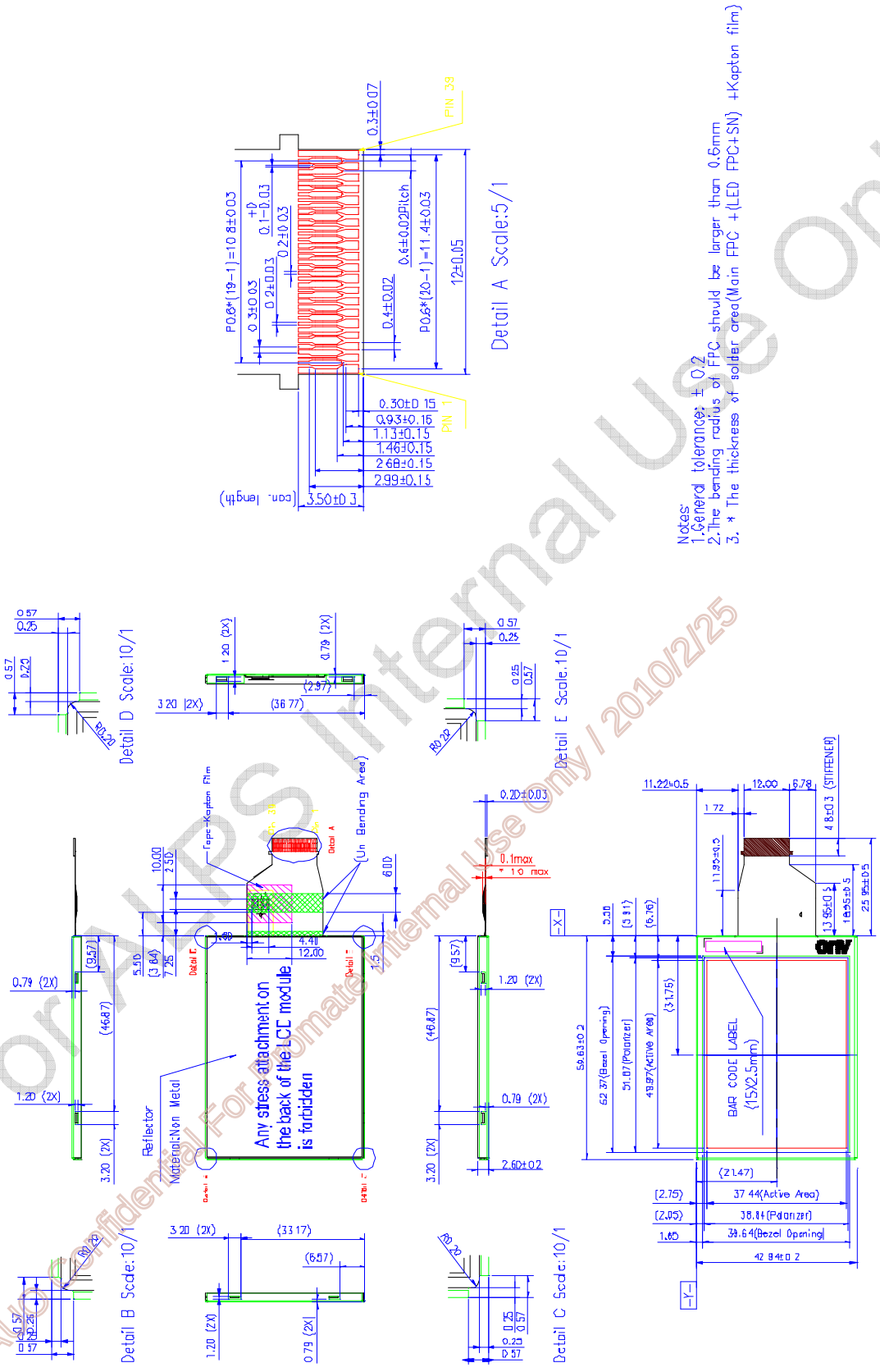
c. Empty box label is applied if needed.

d. Other package method or label are depended on customer requirement.

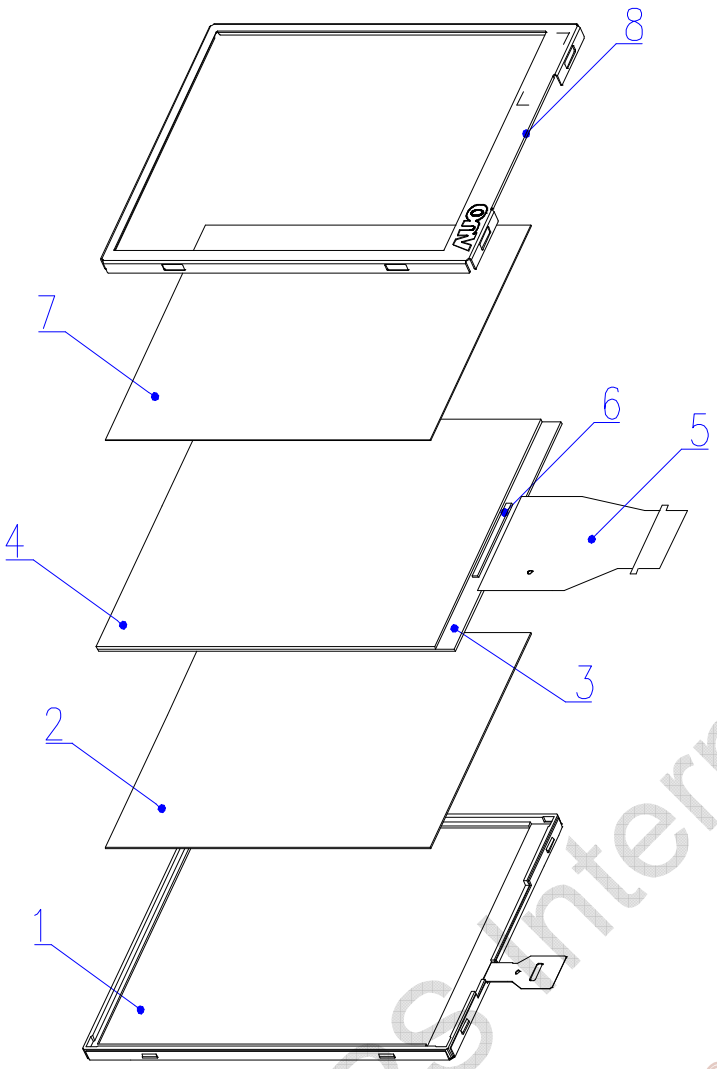


Note: Limit of box palletizing=Max 5 layers (ship and stock conditions) for air transport and marine transit.

F. Outline dimension



Exploding drawing

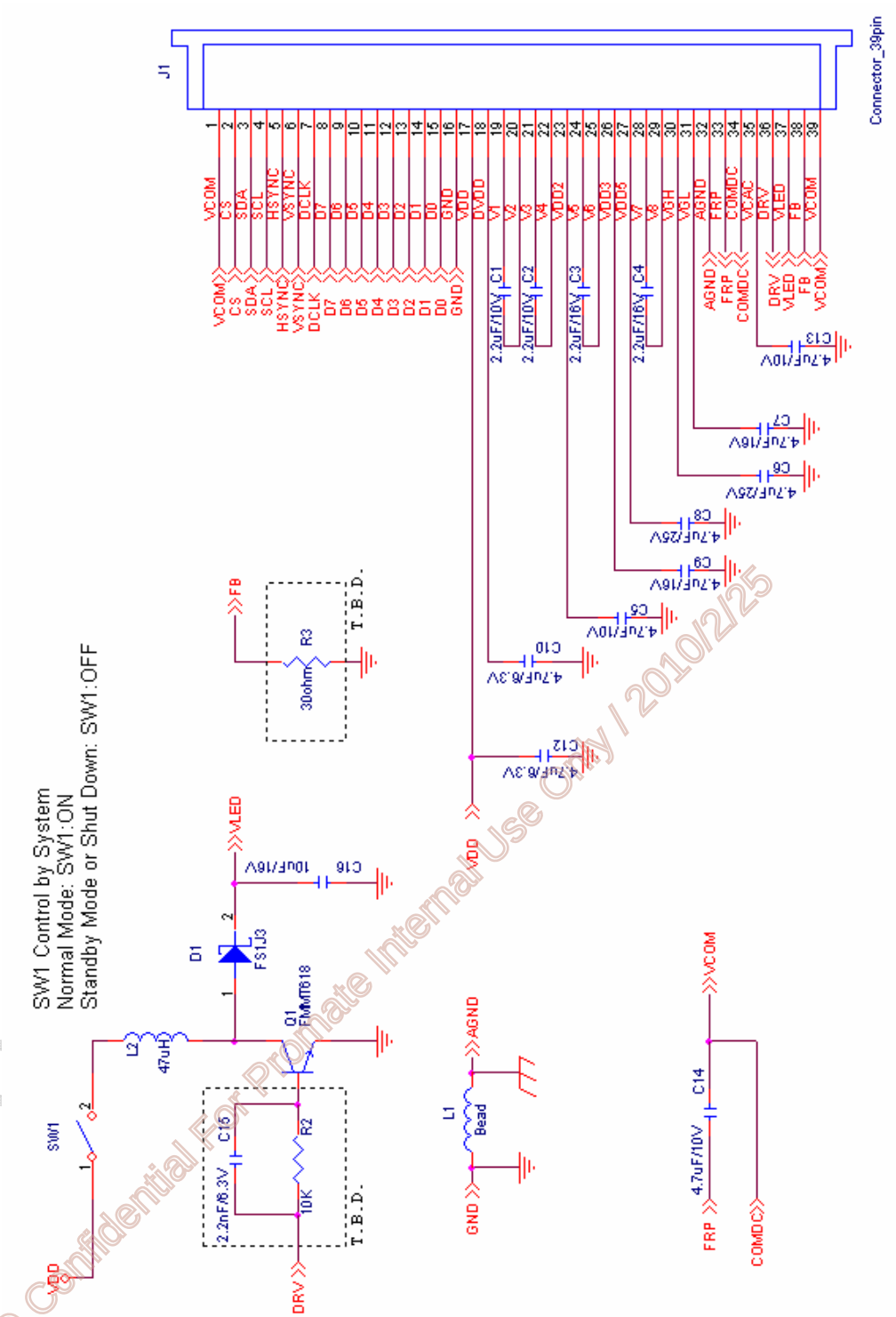


8	Bezel	1
7	Polarizer	1
6	IC	1
5	FPC	1
4	Color Filter	1
3	TFT	1
2	Polarizer	1
1	Back Light Unit	1
	Part Name	Q'TY

G. Application note

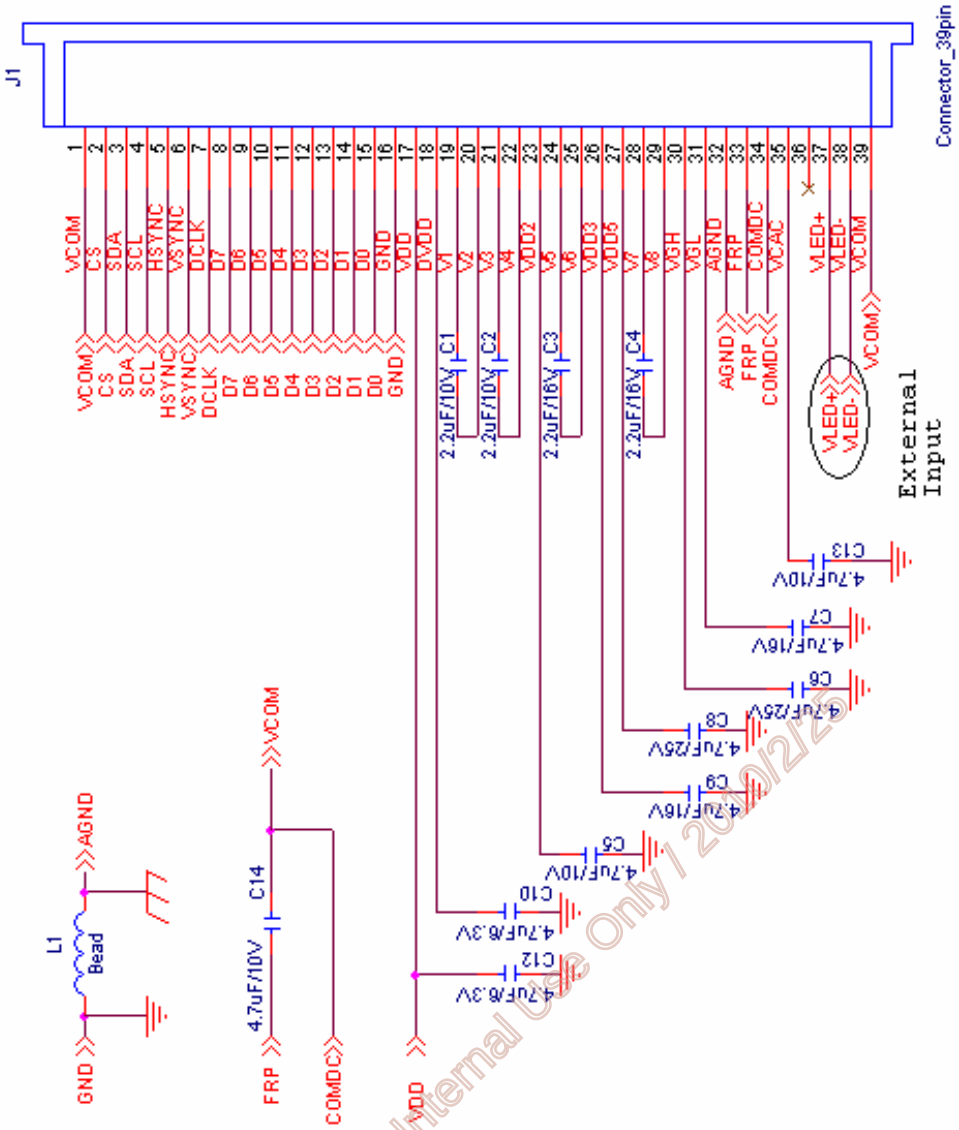
1. Application circuit

1.1 With internal LED driver circuit



Note1: Use internal LED driver must set R5[1](SHDB1)= ”1”.

1.2 With external LED driver circuit



Note2: Use external LED driver must set R5[1](SHDB1)= ”0”.

2. Power on/off sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

2.1 Power on (Standby Disabling)

After VDD power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. The LCD driver is in default standby mode after VDD power-on, and setting register R5: STB to '1' to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The LCD positive and negative power supplies VGH/VGL are pumped first, and followed by the LED power VLED. Please refer to Fig.12 for the detail timing of power on sequence.

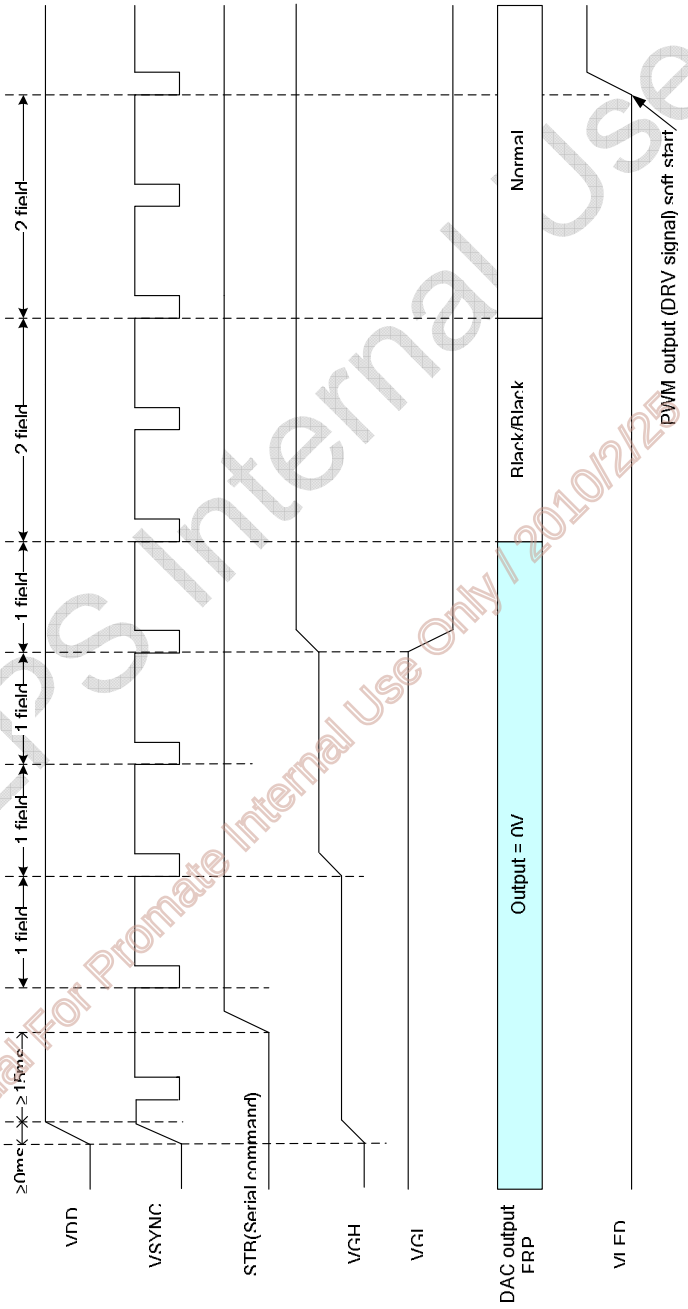


Fig.12 Power on sequence

2.2 Power off (Standby Enabling)

When the register STB is set to '0' to enable standby mode, a build-in power off sequence is started. Please refer to Fig.13 for the detail timing of power off sequence.

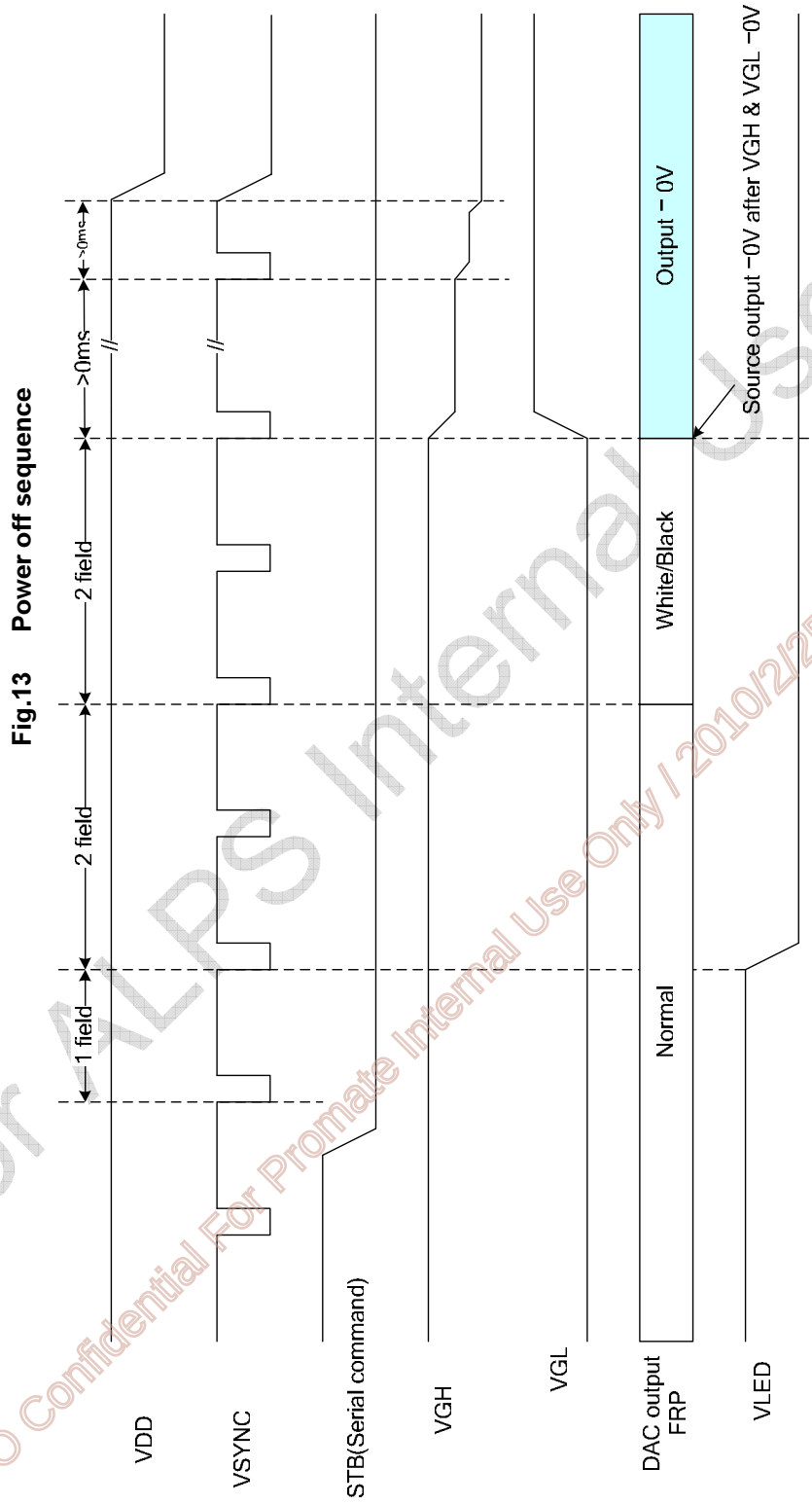
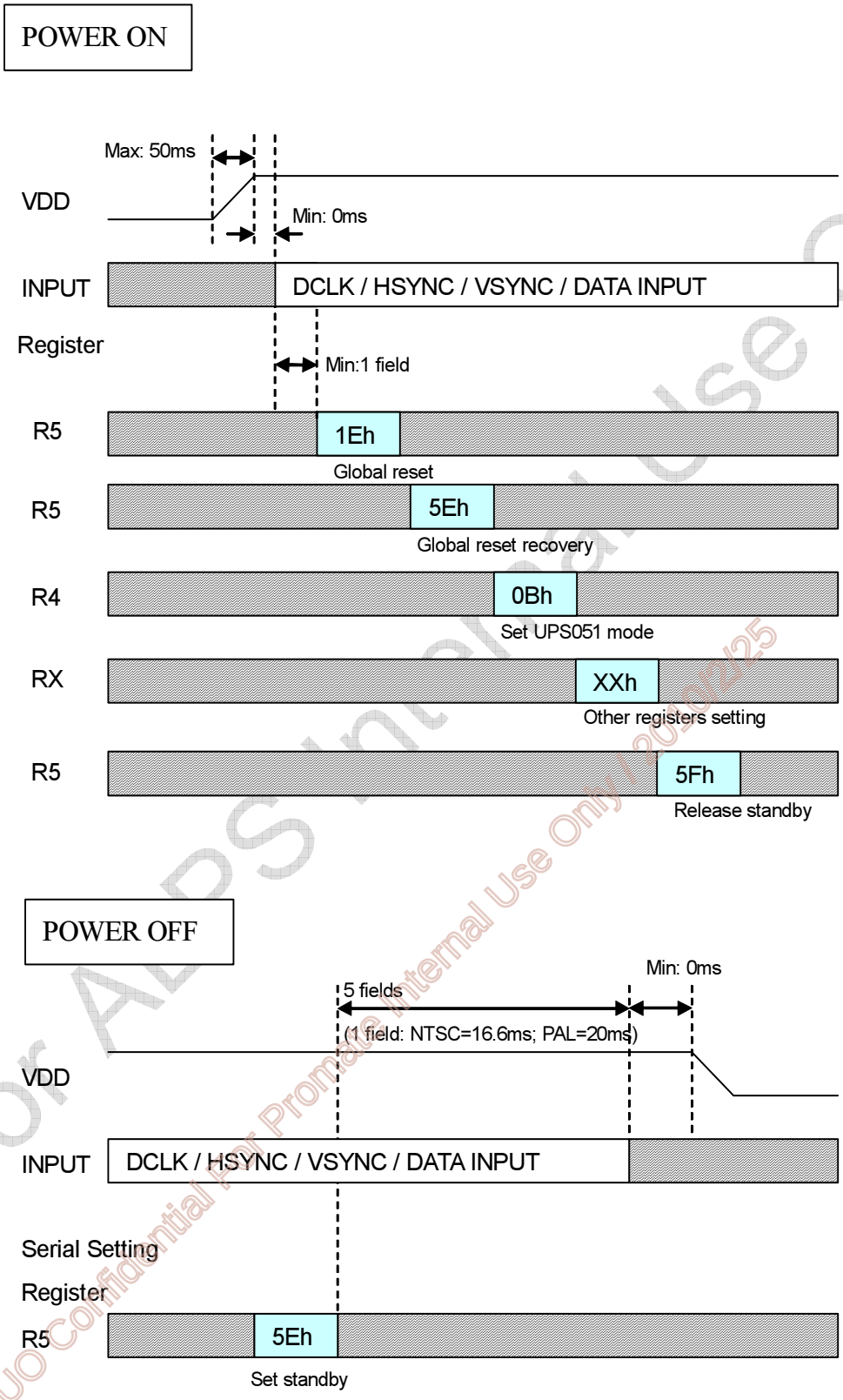


Fig.13 Power off sequence

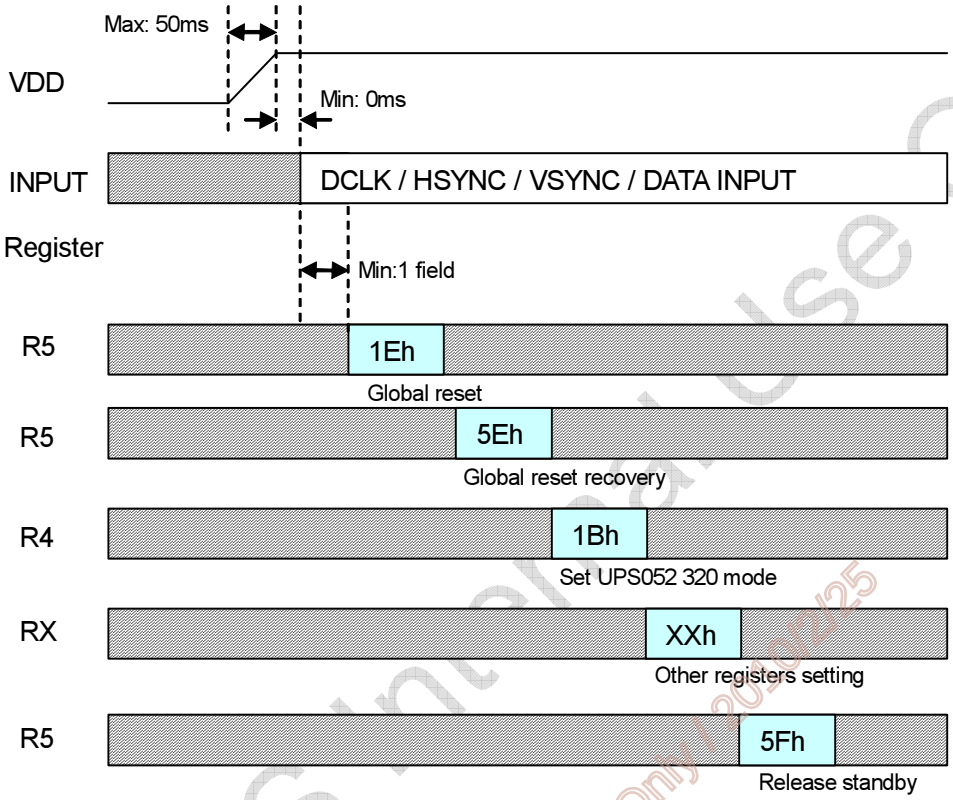
3. Recommended power on/off serial command settings

3.1 UPS051

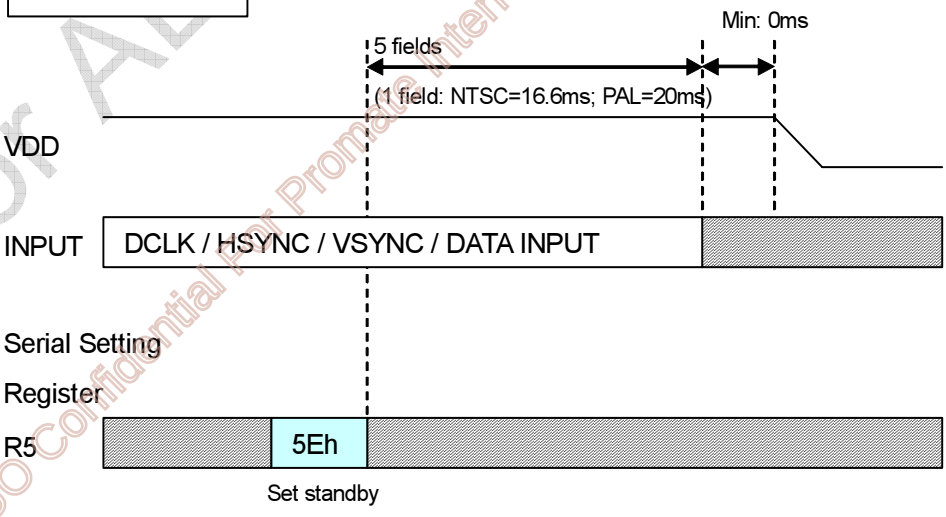


3.2 UPS052 320 mode

POWER ON

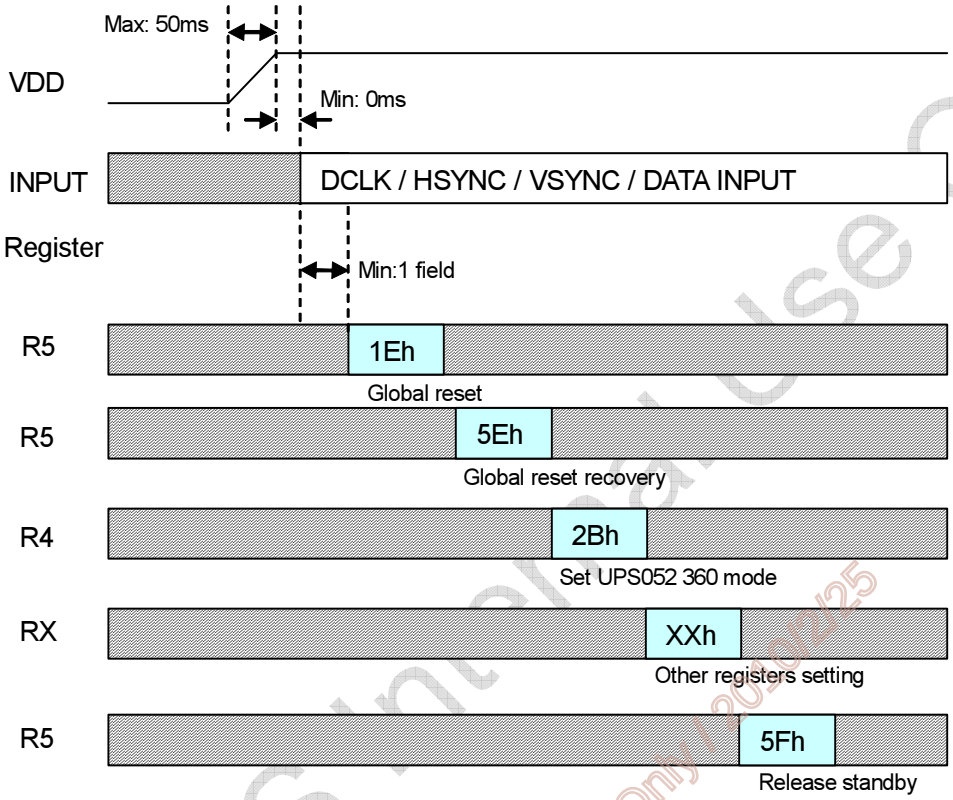


POWER OFF

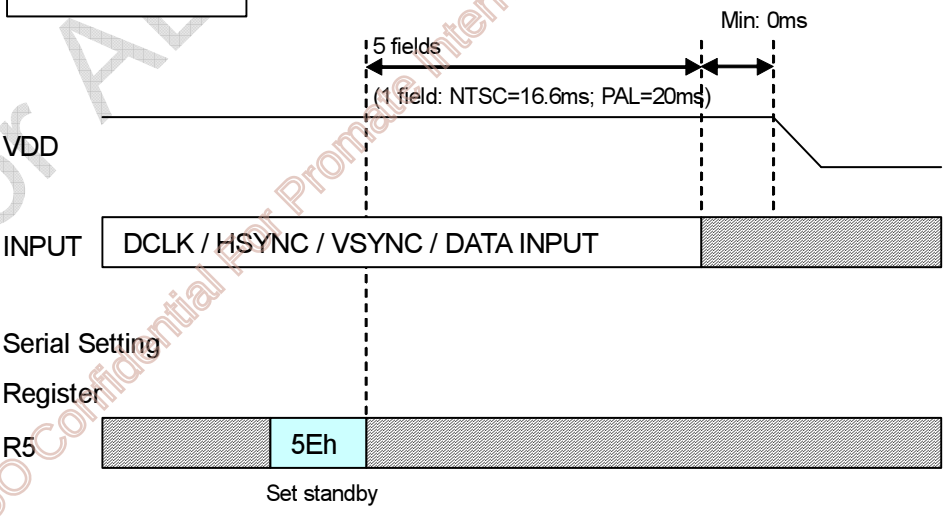


3.3 UPS052 360 mode

POWER ON

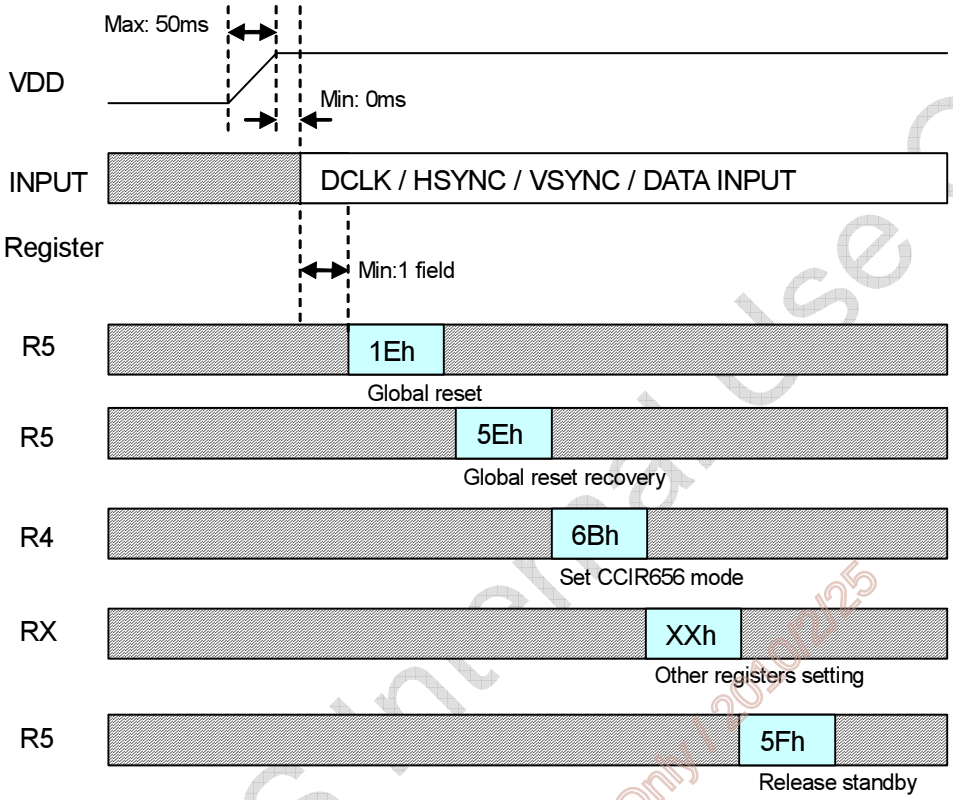


POWER OFF

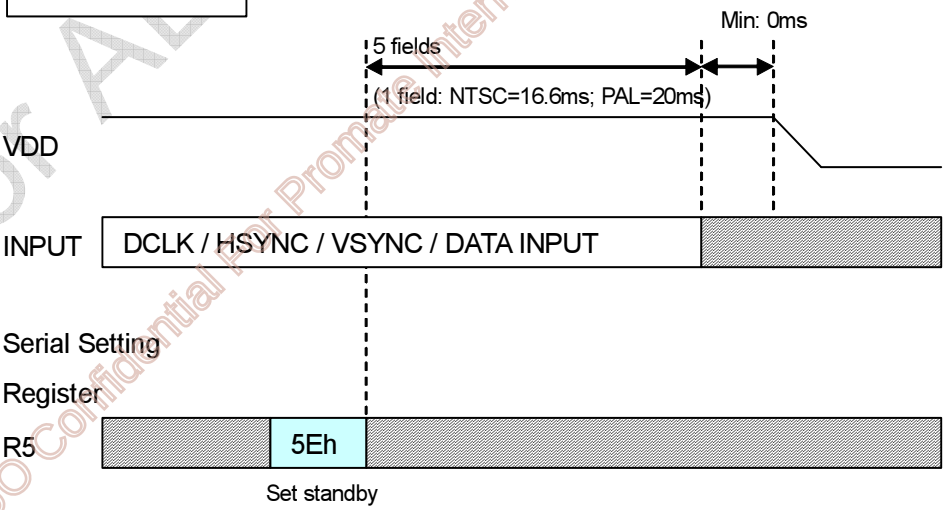


3.4 CCIR656

POWER ON

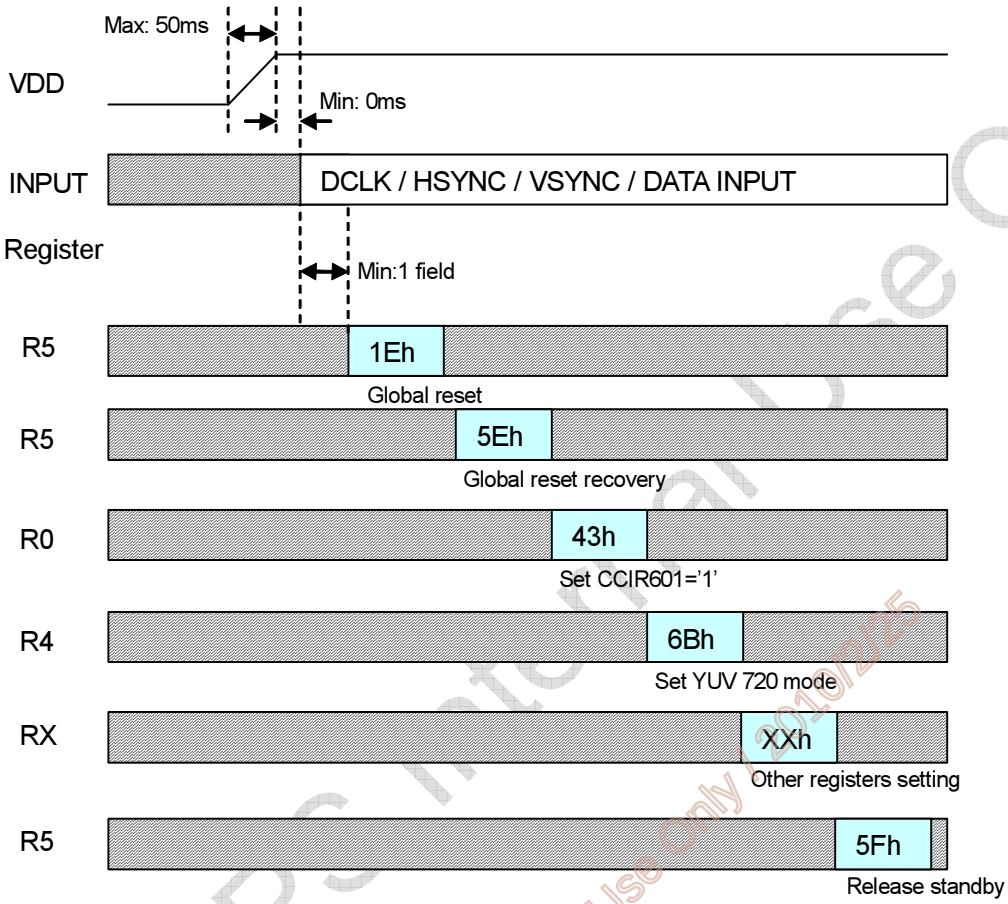


POWER OFF

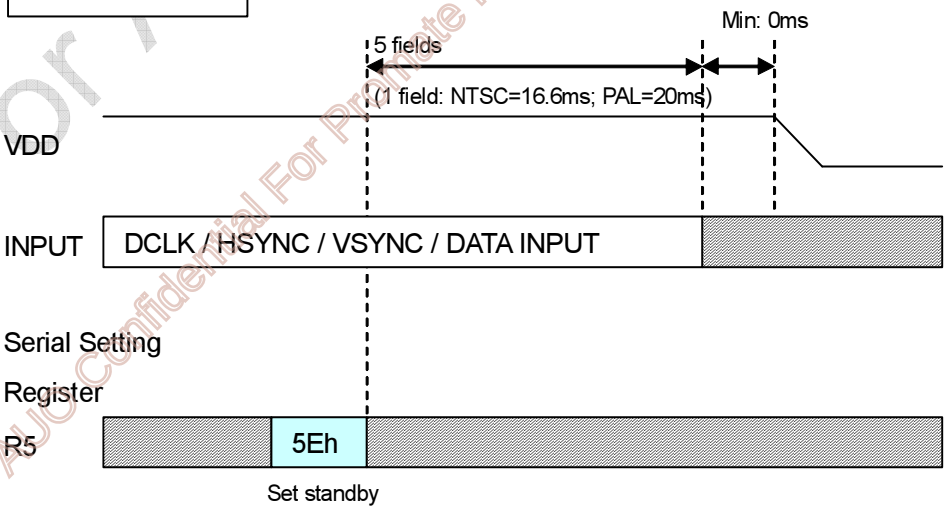


3.5 YUV 720

POWER ON

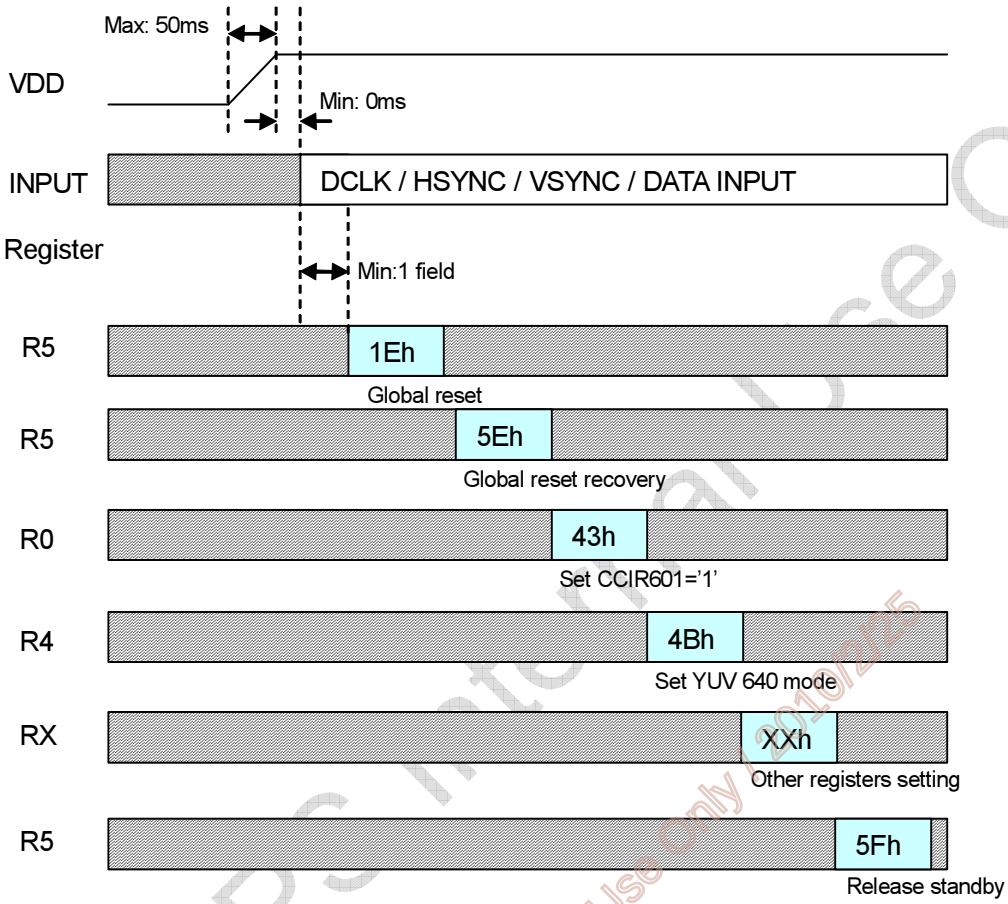


POWER OFF

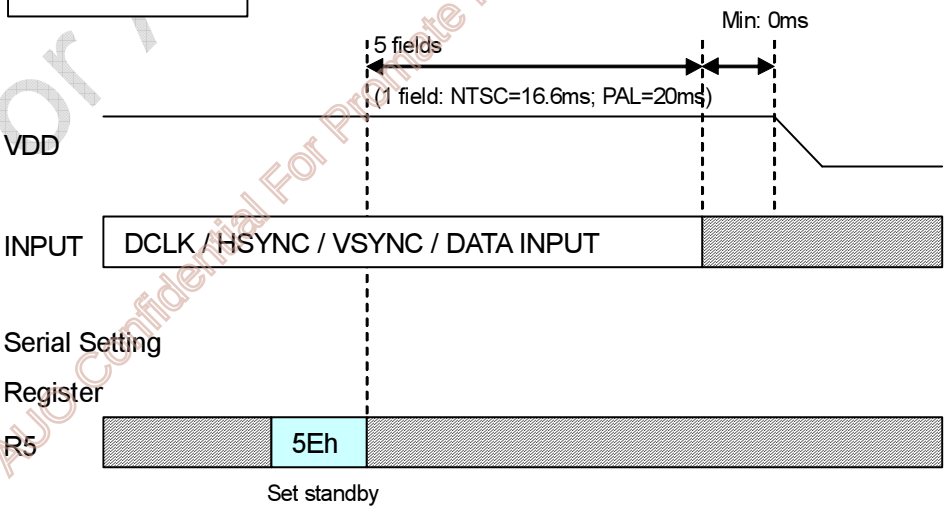


3.6 YUV 640

POWER ON

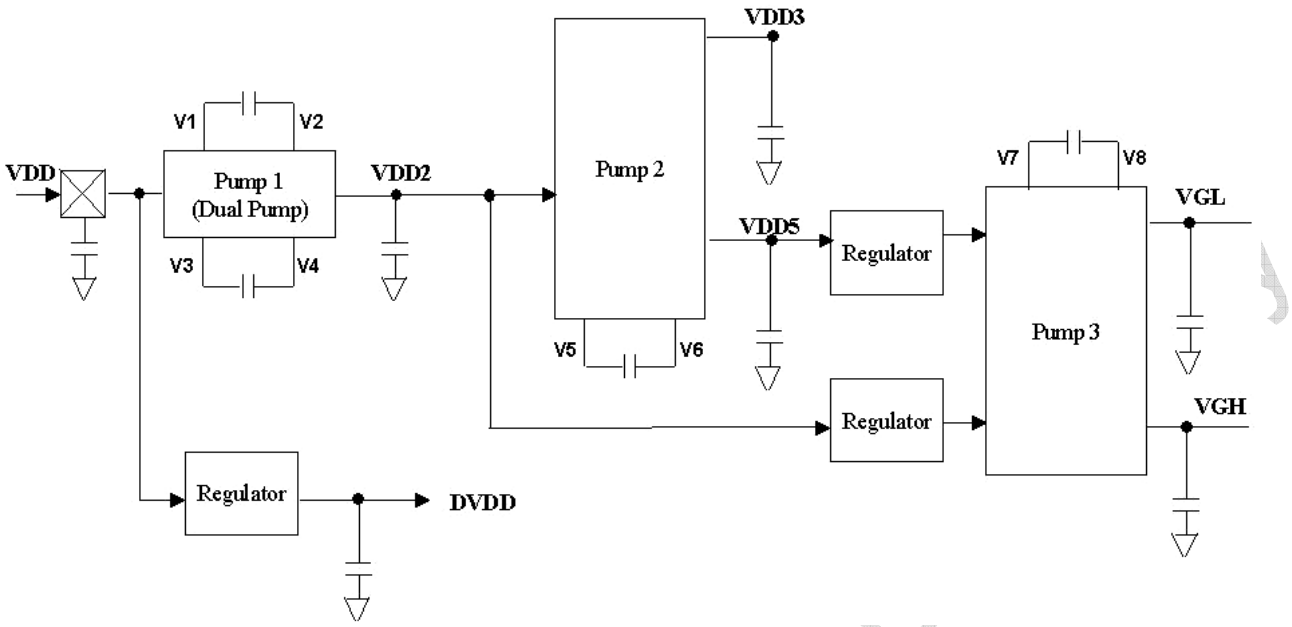


POWER OFF



4. Power generation circuit

The black diagram of built-in power generation circuit for TFT-LCD supply power is shown as below:



5. Handling precaution

1) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnectiing from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or crack id dropped or bumped on hard surface.

6) Do not open or modify the modul assembly.

7) At the insertion or removal of sigal interface connector, be sure not to rotate nor tilt the interface connector of the TFT LCD module..

8) After installation of the TFT Module into an enclosure,do not twist nor bend the TFT module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT module outside. Otherwise the TFTF module may be damaged.