



A025CTN01.0 Product Spec	Version	1.0
	Page	2/52

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Product Specification

2.5" COLOR TFT-LCD MODULE

Model Name :	A025CTN01.0
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< > Preliminary Specification

< ◆ > Final Specification

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A025CTN01.0 Product Spec	Version	1.0
	Page	3/52

Record of Revision

Version	Revise Date	Page	Content
0.0	2011/05/13	all	First draft
0.1	2011/06/23	10	Update LED current and Power Consumption
1.0	2011/08/16	4	Add Weight 13±2 g
		10	Correct LED life time remark: $I_L = 22\text{mA}$
		32	Update Response Time & Add Chromaticity specification
		34	Add Note 10. Chromaticity Diagram
		38, 39	Add Packing form & update packing information.
		41	Add one Schottky diode in the signal of VGL

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A025CTN01.0 Product Spec	Version	1.0
	Page	4/52

Contents

A. General Information	5
B. Electrical specifications	6
1. Pin assignment	6
2. Absolute maximum ratings	10
3. Electrical characteristics	10
3.1 Typical operating conditions (GND=0V)	10
3.2 Current characteristics (GND=0V)	10
3.3 Backlight Driving Conditions	10
4. Input timing AC characteristic	11
a. Digital Signal AC Characteristic	11
b. UPS051 Timing conditions	12
c. UPS052 Timing conditions	15
d. CCIR656 Timing conditions	19
5. Serial control interface AC characteristic	21
5.1 Timing chart	21
5.2 The configuration of serial data at SDA terminal is at below	22
5.3 Register table	23
5.4 Register description	24
C. Optical Specification (Note1, Note 2 and Note 3)	32
D. Reliability Test Items	36
E. Packing form	38
F. Outline dimension	40
G. Application note	41
1. Application circuit	41
2. Stand-by timing	42
3. Power on sequence	43
4. Power off sequence	44
5. Recommended power on/off serial command settings	45
5.1. Recommend UPS051 (9.7 MHz) power on/off setting	45
5.2. Recommend UPS052 320RGB mode (24.54 MHz) power on/off setting	46
5.3. Recommend UPS052 360RGB mode (27MHz) power on/off setting	47
5.4. Recommend YUV mode A 640Y 320CrCb (24.54 MHz) power on/off setting	48
5.5. Recommend YUV mode A 720Y 360CrCb (27 MHz) power on/off setting	49
5.6. Recommend YUV mode B 640Y 320CrCb (24.54 MHz) power on/off setting	50
5.7. Recommend YUV mode B 720Y 320CrCb (27 MHz) power on/off setting	51
5.8. Recommend CCIR656 mode (27 MHz) power on/off setting	52

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A025CTN01.0 Product Spec	Version	1.0
	Page	5/52

A. General Information

NO.	Item	Unit	Specification	Remark
1	Screen Size	inch	2.5 (Diagonal)	
2	Display Resolution	dot	480(W) x 240(H)	
3	Overall Dimension	mm	57.48 x 48.51 x2.6	Note 1
4	Active Area	mm	50.88 x38.16	
5	Pixel Pitch	mm	0.318(R.G.B)×0.159(V)	
6	Color Configuration	--	R, G, B delta	
7	Color Depth	--	16.7M Colors	
8	NTSC Ratio	%	45	
9	Display Mode	--	Normally White	
10	Weight	g	13±2	
11	Viewing direction	--	6 o'clock (gray inversion)	
12	Panel surface treatment	--	Anti-glare	

Note 1: Refer to F. Outline Dimension



A025CTN01.0 Product Spec	Version	1.0
	Page	6/52

B. Electrical specifications

1. Pin assignment

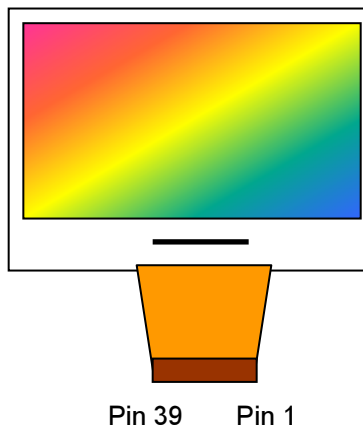
Pin no	Symbol	I/O	I/O Structure	Description	Remark
1	VCOM	I	-	Common electrode driving voltage	
2	VGL	C	-	Negative low power supply for gate driver output: -12.5V	
3	C4P	C	-	Pins to connect capacitance for power circuitry	
4	C4M	C	-	Pins to connect capacitance for power circuitry	
5	VGH	C	-	Positive power supply for gate driver output: +12.5V	
6	FRP	O	TYPE6	Frame polarity output for VCOM	
7	VCAC	C	-	Define the amplitude of the VCOM swing	
8	Vint3	C	-	Intermediate voltage for charge Pump	
9	C3P	C	-	Pins to connect capacitance for power circuitry	
10	C3M	C	-	Pins to connect capacitance for power circuitry	
11	Vint2	C	-	Intermediate voltage for charge Pump	
12	C2P	C	-	Pins to connect capacitance for power circuitry	
13	C2M	C	-	Pins to connect capacitance for power circuitry	
14	Vint1	C	-	Intermediate voltage for charge Pump	
15	C1P	C	-	Pins to connect capacitance for power circuitry	
16	C1M	C	-	Pins to connect capacitance for power circuitry	
17	PGND	P	-	Charge Pump Power GND	
18	PVDD	P	-	Charge Pump Power VDD	
19	DRV	O	TYPE10	Gate signal for the power transistor of the boost converter	
20	LED+	P	-	For Led Anode voltage	
21	LED+	P	-	For Led Anode voltage	
22	FB	P/I	TYPE9	Led Cathode and main boost regulator feedback input	
23	GND	P	-	Digital GND	
24	GND	P	-	Digital GND	
25	VCC	P	-	Digital power supply	
26	CS	I	TYPE5	Serial communication chip select	
27	SDA	I/O	TYPE3	Serial communication data input/output	
28	SCL	I	TYPE4	Serial communication clock input	
29	HSYNC	I	TYPE1	Horizontal sync input	

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30	VSYNC	I	TYPE1	Vertical sync input	
31	DCLK	I	TYPE1	Clock Input:	
32	D7	I	TYPE1	Data Input: MSB	
33	D6	I	TYPE1	Data Input:	
34	D5	I	TYPE1	Data Input:	
35	D4	I	TYPE1	Data Input:	
36	D3	I	TYPE1	Data Input:	
37	D2	I	TYPE1	Data Input:	
38	D1	I	TYPE1	Data Input:	
39	D0	I	TYPE1	Data Input: LSB	

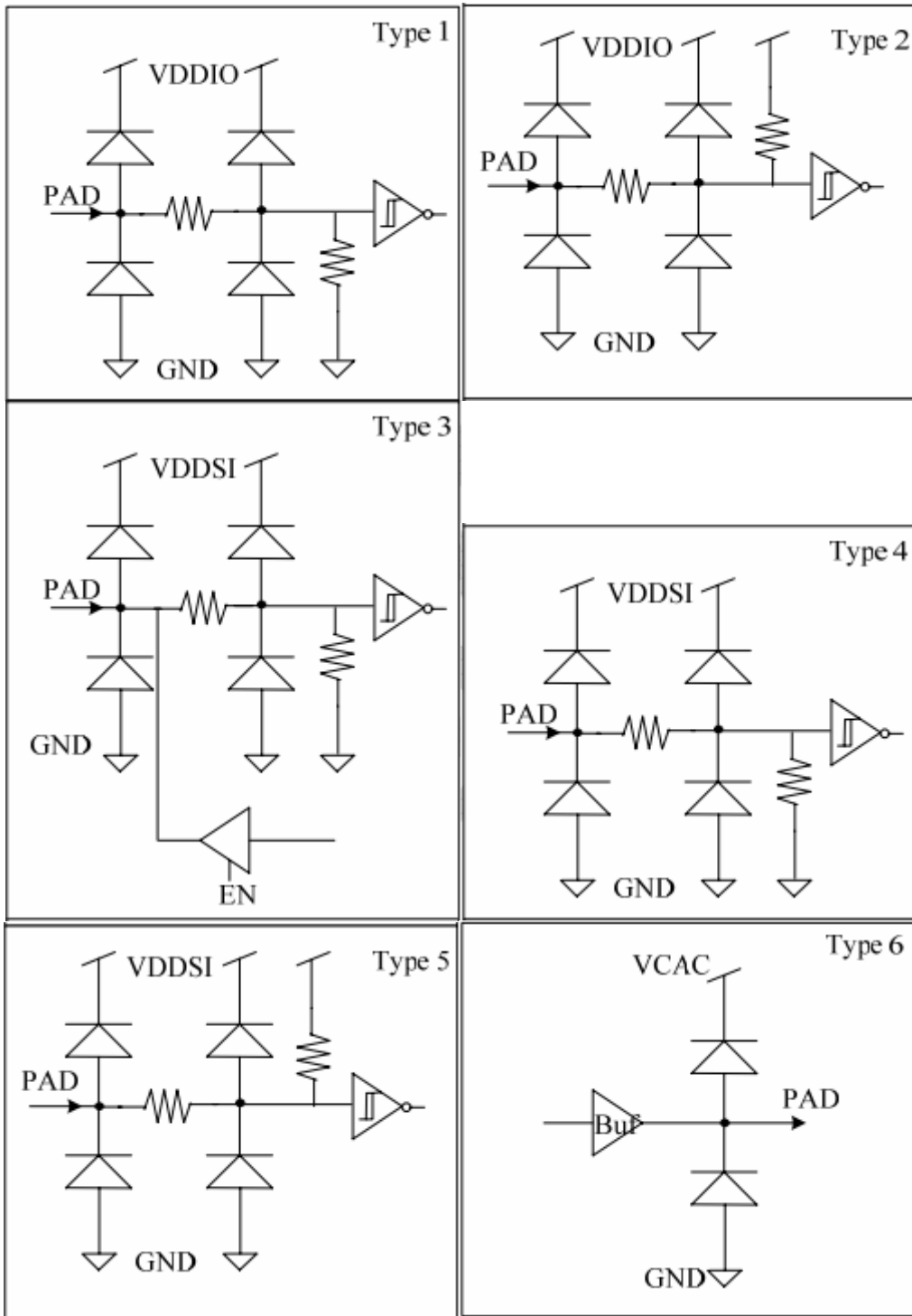
I : Input, O : Output, C : Capacitor, P : Power, D : Dummy

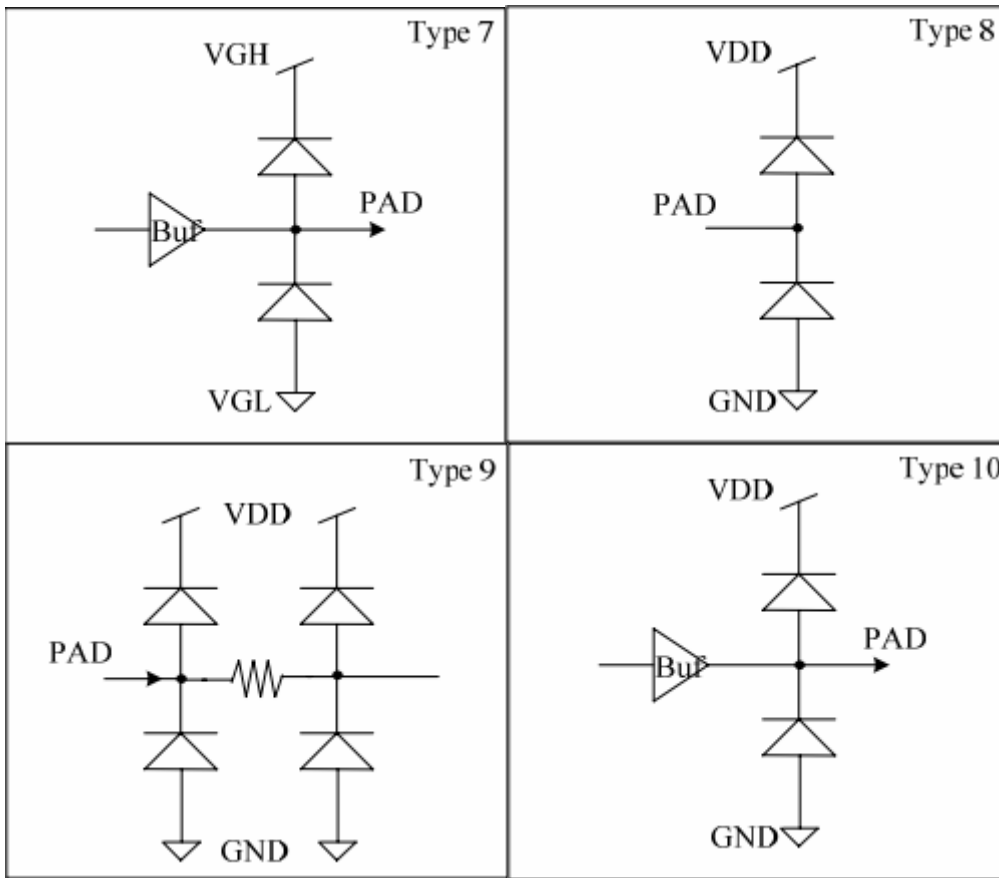
Note: Definition of scanning direction, Refer to figure as below :



I/O Pin Structure:

Pull high/low resistor is **700kΩ**





2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V _{CC}	GND=0	-0.5	7.0	V	
	PV _{DD}	PGND=0	-0.5	7.0	V	
Input signal voltage	D0~D7	-	-0.3	3.6	V	
Input signal voltage	VCOM	-	-2.9	5.2	V	VCOM DC Voltage
Operating temperature	Topa	-	0	60		Ambient temperature
Storage temperature	Tstg	-	-25	70		Ambient temperature

3. Electrical characteristics

3.1 Typical operating conditions (GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Voltage	V _{CC}	2.7	3.3	3.6	V	Note 1
	PV _{DD}	3.0	3.3	3.6	V	
TFT-LCD Power Voltage	V _{GH}	11.0	12.5	14.0	V	GND=PGND=0V
	V _{GL}	-14.0	-12.5	-11.0	V	GND=PGND=0V
VCOM Voltage	V _{CAC}		5.0		V	V
	V _{CDC}		1.2		V	V

Note 1: A build-in power on reset circuit for PV_{DD} and V_{CC} is provided within the integrated LCD driver IC.

3.2 Current characteristics (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V _{CC}	I _{VCC} (Pin 26)	V _{CC} =3.3V	--	0.5	0.8	mA	Note 1
Input Current for PV _{DD}	I _{PVDD} (Pin 19)	PV _{DD} =3.3V	--	3	7	mA	Note 1

Note 1: Use UPS051 mode and F_{DCLK}=9.7MHz, other registers are default setting.

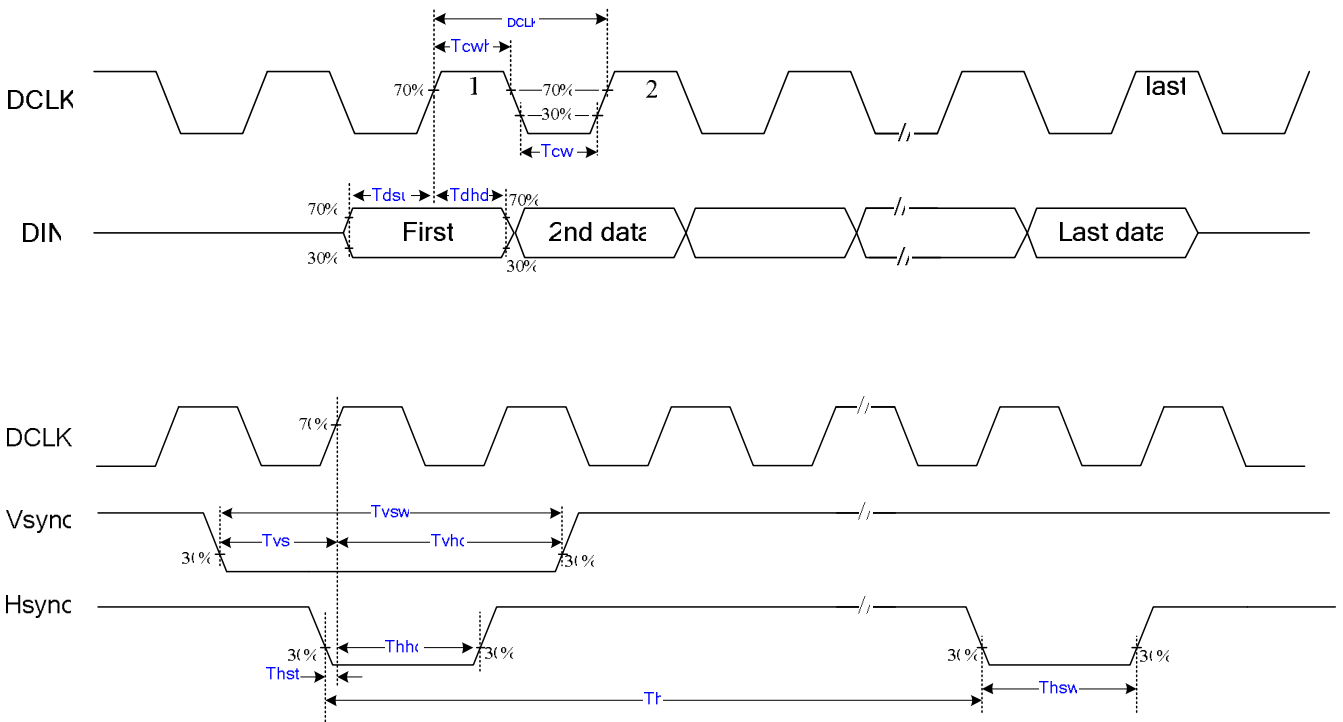
3.3 Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I _L		22	24.2	mA	
Power Consumption	P _L	-	136.4	164.6	mW	
LED Life Time	hrs	10000				Ta. = 25 I _L = 22mA

4. Input timing AC characteristic

a. Digital Signal AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK duty cycle	Tcwh/Tcwl	40	50	60	% t _{DCLK}
VSYNC setup time	Tvst	12	-	-	ns
VSYNC hold time	Tvhd	12	-	-	ns
HSYNC setup time	Thst	12	-	-	ns
HSYNC hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
HSYNC width	Thsw	1	1	254	t _{DCLK}
VSYNC width	Tvsw	1 t _{DCLK}	1 t _{DCLK}	6t _H	



b. UPS051 Timing conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency		$1/t_{DCLK}$	8.1	9.7	11.3	MHz		
HSYNC	Period	t_H	572	617	695	t_{DCLK}	Note 1	
	Display period	t_{hd}	480			t_{DCLK}		
	Back porch	t_{hbp}	84	100	115	t_{DCLK}		
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}		
	Pulse width	t_{hsw}	1	1	96	t_{DCLK}		
VSYNC	Period	Odd	t_V	247.5	262.5	277.5	t_H	Note 2, 3, 4
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	6	13	21	t_H	
		Even		6.5	13.5	21.5		
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vbp}$			t_H	
		Even						
	Pulse width	Odd	t_{vsw}	$1t_H$				
		Even						

Note 1: UPS051 Horizontal back porch time (t_{hbp}) is adjustable by setting register DDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical back porch time (t_{vbp}) is adjustable by setting register HDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 3: Both interlace and non-interlace mode can be accepted.

Note 4: AUO suggests frame rate at least 50 Hz to get the better display quality.

Fig.1 UPS051 Input Horizontal Timing Chart

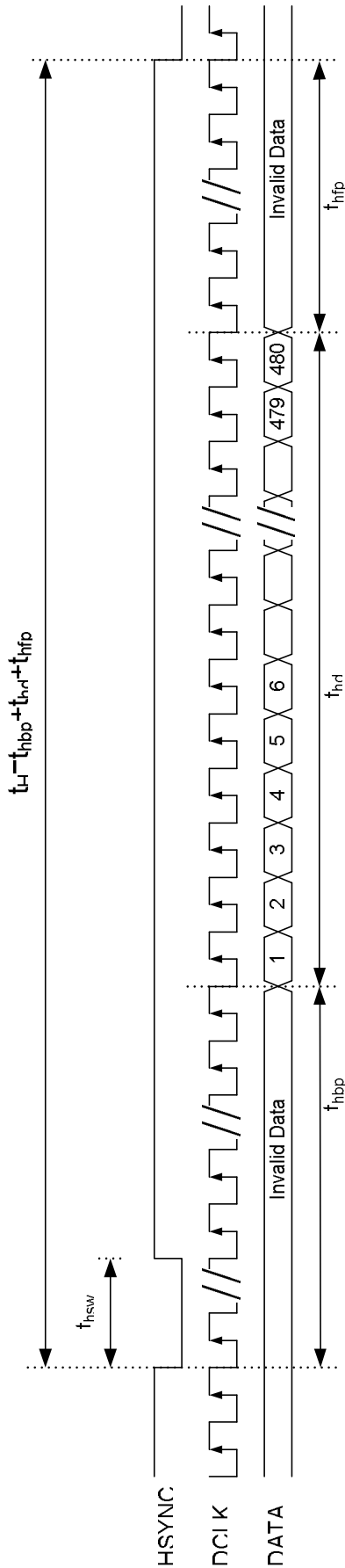


Fig.2 UPS051 Input Horizontal Data Sequence

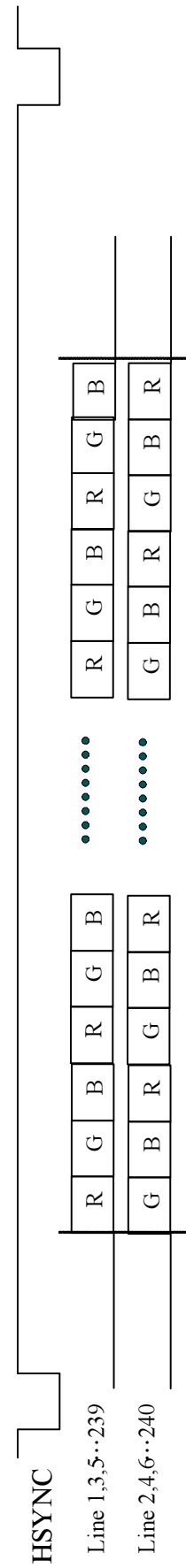
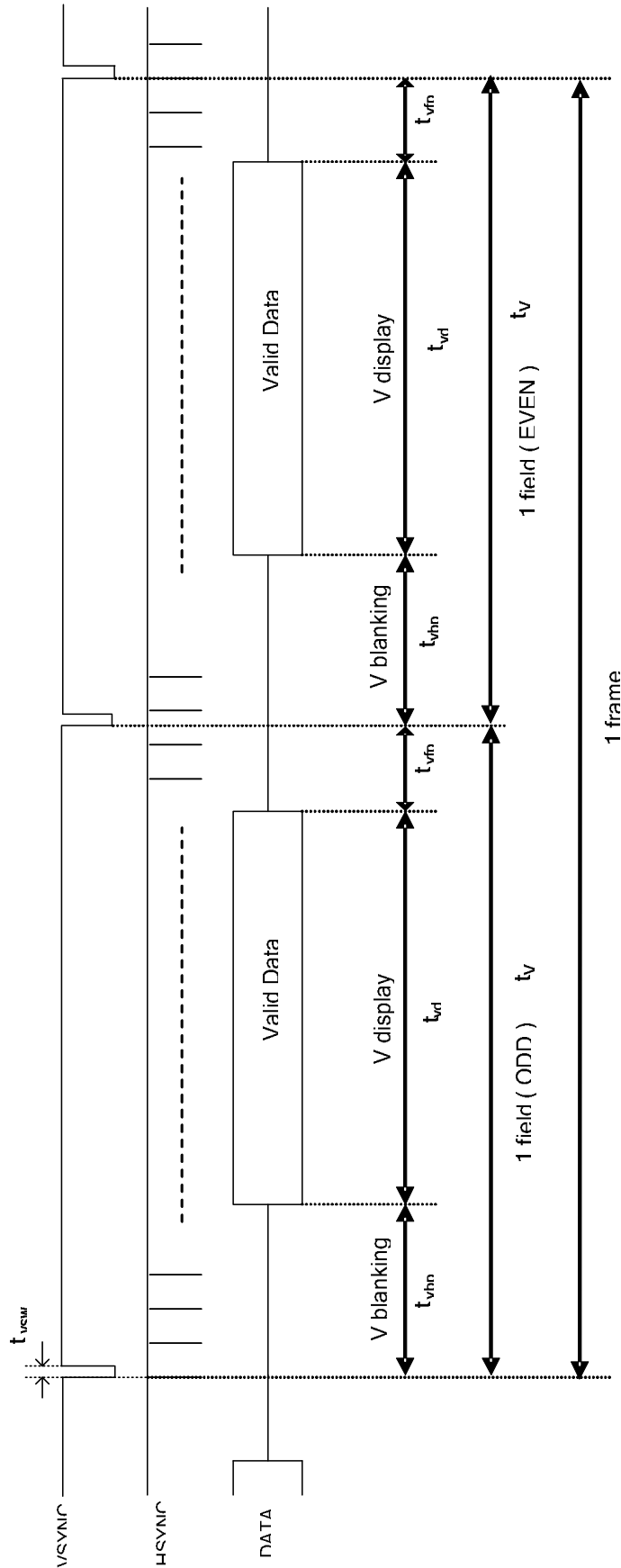


Fig.3 UPS051 Input Vertical Timing Chart



c. UPS052 Timing conditions

c - 1. UPS052 (320 mode 24.55MHz) timing specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency		$1/t_{DCLK}$	20.47	24.55	28.66	MHz		
HSYNC	Period	t_H	1524	1560	1647	t_{DCLK}		
	Display period	t_{hd}	1280			t_{DCLK}		
	Back porch	t_{hbp}	236	252	267	t_{DCLK}		
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}		
	Pulse width	t_{hsw}	1	1	96	t_{DCLK}		
VSYNC	Period	Odd	t_V	247.5	262.5	277.5	t_H	Note 1, 2
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	6	13	21	t_H	
		Even		6.5	13.5	21.5		
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vbp}$			t_H	
		Even						
	Pulse width	Odd	t_{vsw}	$1t_H$				
		Even						

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

c - 2. UPS052 (360 mode 27MHz) timing specifications

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark	
DCLK Frequency		$1/t_{DCLK}$	22.5	27	31.5	MHz		
HSYNC	Period	t_H	1684	1716	1807	t_{DCLK}		
	Display period	t_{hd}	1440			t_{DCLK}		
	Back porch	t_{hbp}	236	252	267	t_{DCLK}		
	Front porch	t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}		
	Pulse width	t_{hsw}	1	1	96	t_{DCLK}		
VSYNC	Period	Odd	t_V	247.5	262	277.5	t_H	Note 1, 2
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	6	13	21	t_H	
		Even		6.5	13.5	21.5		
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vbp}$			t_H	
		Even						



A025CTN01.0 Product Spec	Version	1.0
	Page	16/52

	Pulse width	Odd	t_{vsw}		$1t_H$			
		Even						

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

Fig.4 UPS052 Input Horizontal Timing Chart

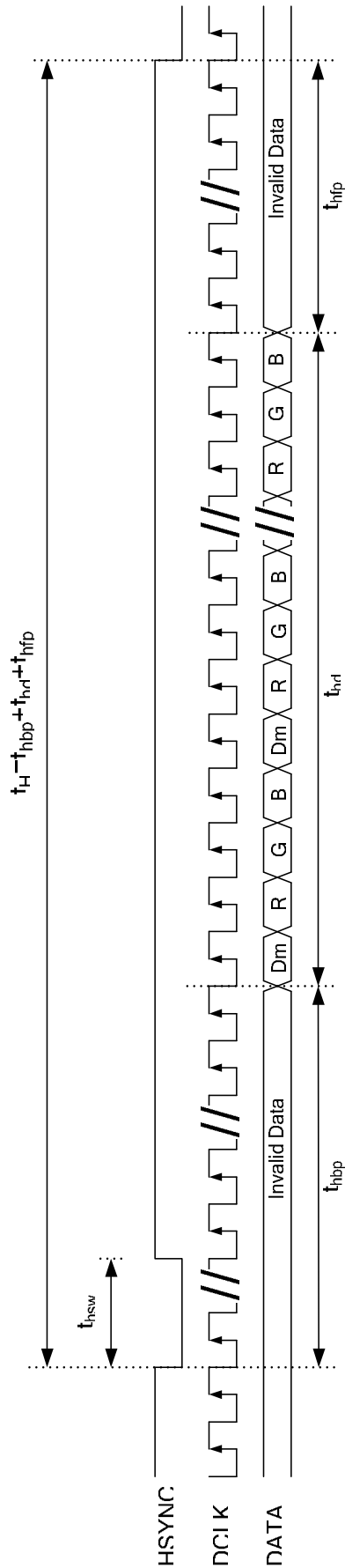
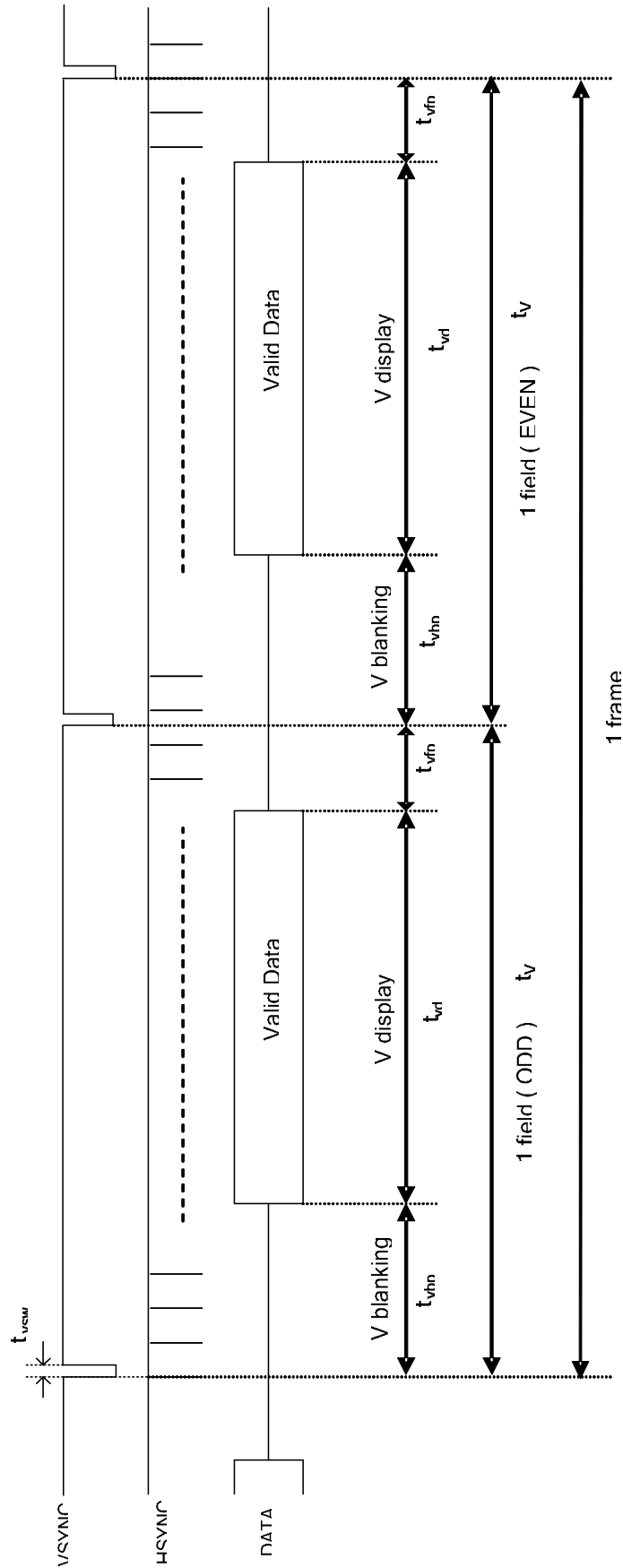


Fig.5 UPS052 Input Vertical Timing Chart

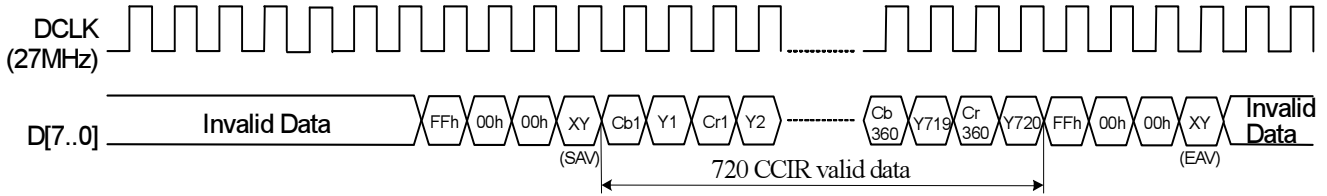




A025CTN01.0 Product Spec	Version	1.0
	Page	19/52

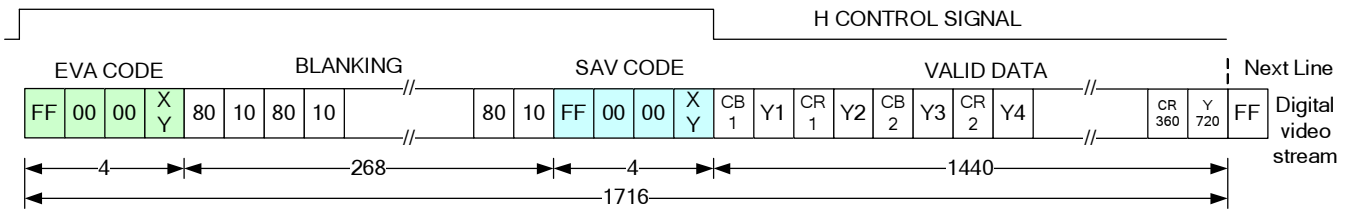
d. CCIR656 Timing conditions

d - 1. CCIR656 timing specifications



CCIR656 Data input format

Example:
 H control signal =1 at EAV;
 H control signal =0 at SAV;



d- 2. CCIR656 decoding

FF 00 00 XY signals are involved with HSYNC,VSYNC and Field

XY encode following bits:

- F=field select
- V=indicate vertical blanking
- H=1 if EAV else 0 for SAV
- P3-P0=protection bits
- $P3 = V \oplus H$ $P2 = F \oplus H$ $P1 = F \oplus V$ $P0 = F \oplus V \oplus H$
- \oplus represents the exclusive-OR function.

Control is provided through “End of Video” (EAV) and “Start of Video” (SAV) timing references.

Horizontal blanking section consists of repeating pattern 80 10 80 10

XY							
D7(MSB)	D6	D5	D4	D3	D2	D1	D0(LSB)
1	F	V	H	P3	P2	P1	P0

d- 3. CCIR656 to RGB conversion

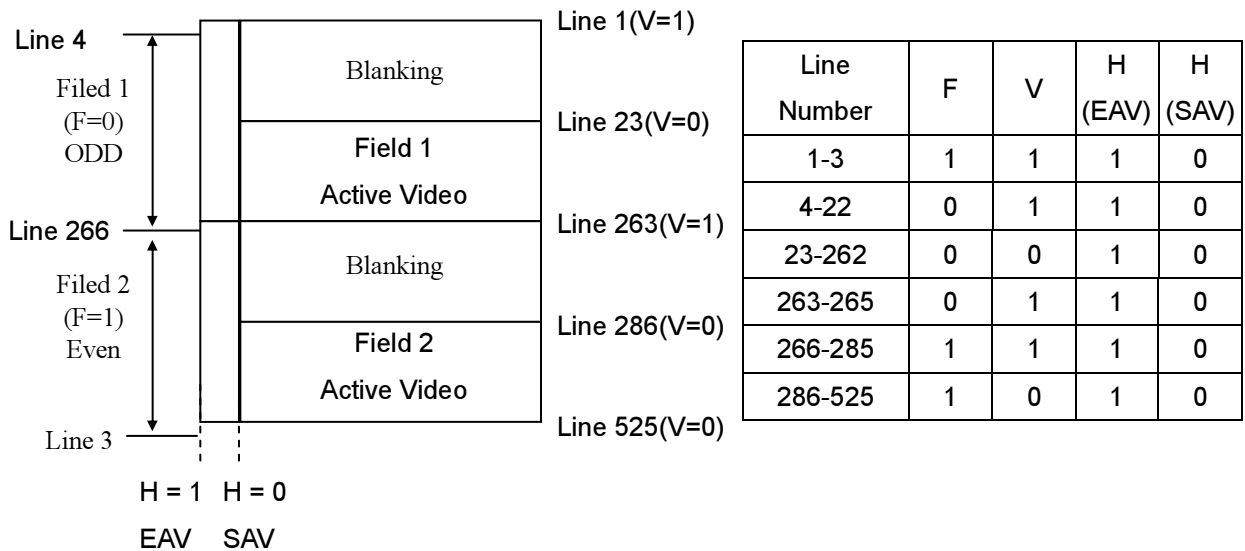
$$R=1.164 (Y-16) +1.596(Cr-128)$$

$$G=1.164 (Y-16) -0.813(Cr-128)-0.392(Cb-128)$$

$$B=1.164 (Y-16) +2.017(Cb-128)$$

Where Y: 16~235 Cr: 16~240 Cb: 16~240

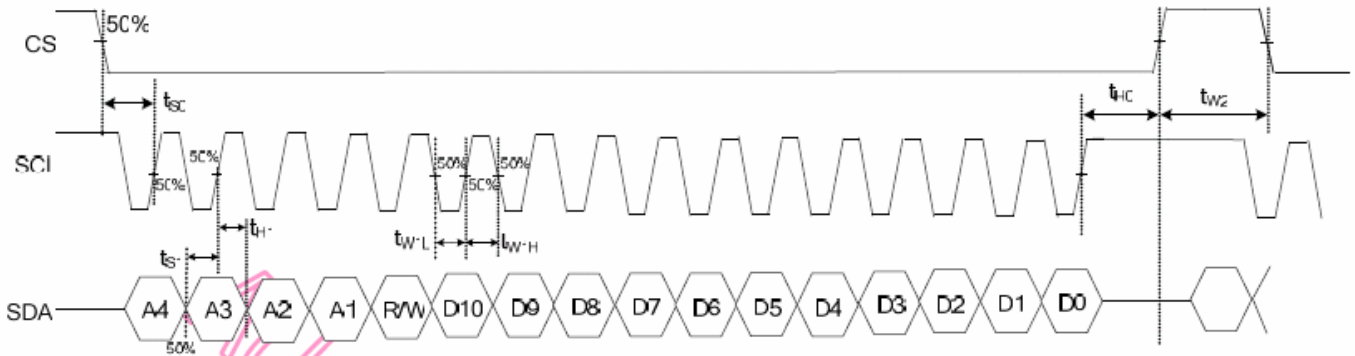
d- 4. CCIR656 Vertical Timing Format (NTSC)



	F	H	V
1	Even Field	EAV	Blanking
0	Odd Field	SAV	Active Video

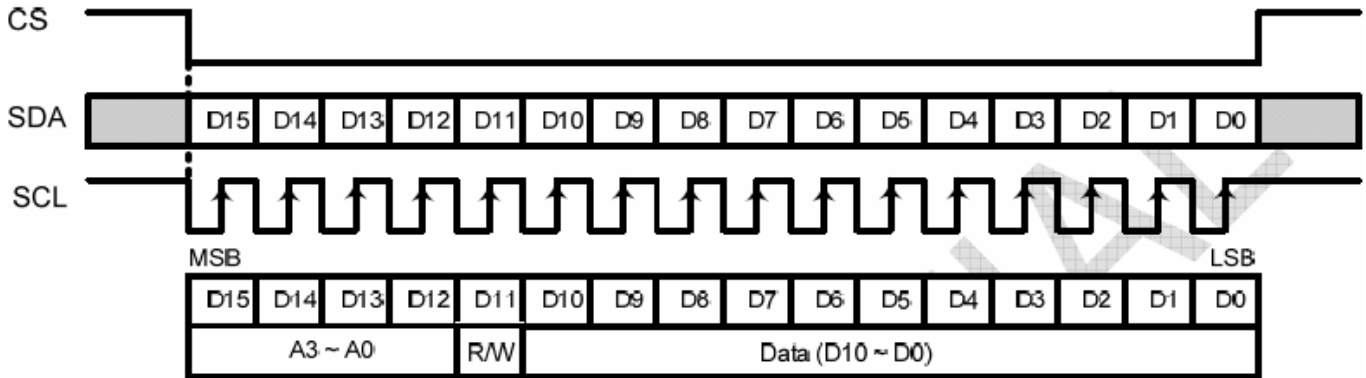
Note: After setting CCIR656 vertical timing value, the frame might be shift. AUO suggests to set the register R5 = "A010h", then the frame should be filled.

5. Serial control interface AC characteristic



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	120	-	-	ns
Serial data input setup Time	t_{S1}	120	-	--	ns
CS input hold Time	t_{H0}	120	-	-	ns
Serial data input hold Time	t_{H1}	120	-	-	ns
SCL pulse low width	t_{WL1}	120	-	-	ns
SCL pulse high width	t_{WH1}	120	-	-	ns
CS pulse high width	t_{W2}	1000	-	-	ns

5.1 Timing chart



- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 16 bits of transferred data after the falling edge of CS pulse are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the standby (power save) mode.

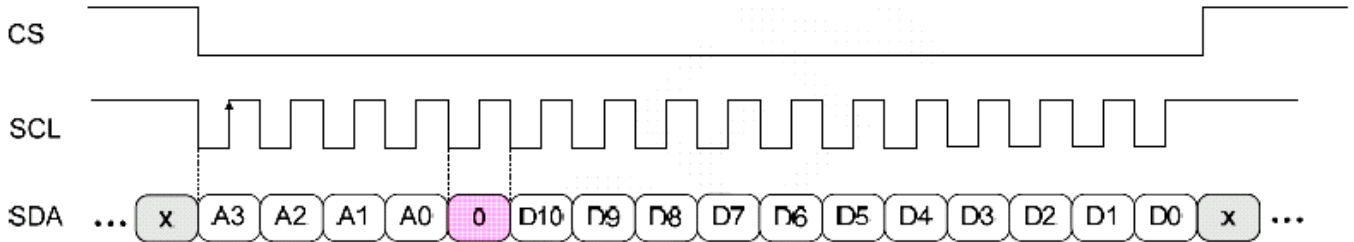


A025CTN01.0 Product Spec	Version	1.0
	Page	22/52

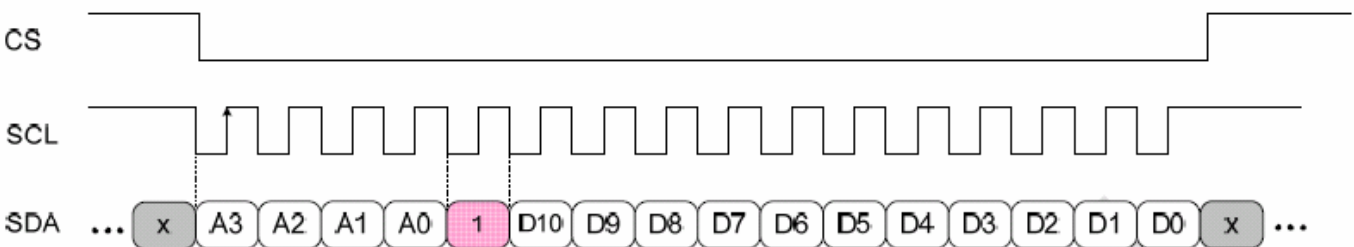
5.2 The configuration of serial data at SDA terminal is at below

MSB																LSB	
A3	A2	A1	A0	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
Address				R/W	DATA												

Write Mode: R/W bit is set to 0



Read Mode: R/W bit is set to 1



5.3 Register table

- When GRB is low, all registers reset to default values
- Serial commands are executed at next VSYNC signal
- () is default

No	Address	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
R0	0x0	X	X	X	X	X	X	X	GRB (1)	STB (1)	SHDB (0)	SHCB (1)	
R1	0x2	X	X	X	X	X	SWD (000)			0	PFON (0)	1	
R2	0x4	X	X	X	X	X	X	X	FPOL (0h)	X	UD (1)	SHL (1h)	
R3	0x6	X	X	X	X	X	X	PALM (0)	PAL (0)	SEL (001)			
R4	0x8	X	X	X	X	X	X	DDL (00h)					
R5	0xa	X	X	X	X	X	FRAD (00)		HDL (0000)				
R6	0xc	X	X	X	X	X	X	X	X	VCSL (110)			
R7	0xe	X	X	X	X	X	X	GAMSEL (0)	X	VLNC (0)	AVGY (1)	1	
T0	0x1	X	X	X	AVDDADJ (000)			PDTY (00)		FBV (100)			
T1	0x3	X	X	X	X	AVG (0)	X	T352 (0)	CONST (1000)				
T2	0x5	X	X	X	X	VDCEN (0)	VCOMDC (20h)						
T3	0x7	X	X	X	X	BRADJ (40h)							
T4	0x9	X	X	X	X	X	X	X	X	X	WNSEL (00)		
T5	0xb	X	X	X	SAT (8h)				HUE (8h)				



A025CTN01.0 Product Spec	Version	1.0
	Page	24/52

5.4 Register description

R0:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0x0	'hd	X	X	X	X	X	X	X	GRB (1)	STB (1)	SHDB (0)	SHCB (1)

SHCB: Shut down charge pump setting

D0	Function
0	Charge pump will be shut down
1	Charge pump normal operating, default

SHDB: Shut down PWM control circuit setting

D1	Function
0	PWM control circuit will be shut down, default
1	PWM control circuit normal operating

STB: Standby mode setting

D2	Function
0	Timing controller, source driver and DC-DC converter is off, and all outputs are High-Z
1	normal operating, default

GRB: Global reset for 3-wire registers

D3	Function
0	The controller is resets, the charge pump and DCDC is off. Reset all register to default value.
1	normal operating, default

R1:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R1	0x2	'h1	X	X	X	X	X	SWD (000)			0	PFON (0)	1

PFON: Pre-filtering setting

D1	Function
0	Pre-filter off, default
1	Pre-filter on

Remark: Disable this function in UPS051 mode



A025CTN01.0 Product Spec	Version	1.0
	Page	25/52

SWD: Control and switch the relationship between the R, G, B and outputs. This switch-able function is useful to match different types of color filters

D[5:3]	Output(n=0 to 159)			
	3n+1	3n+2	3n+3	
000 (Default)	R	G	B	Odd Line
	G	B	R	Even Line
001	G	B	R	Odd Line
	B	R	G	Even Line
01X	B	R	G	Odd Line
	R	G	B	Even Line
100	G	B	R	Odd Line
	R	G	B	Even Line
101	B	R	G	Odd Line
	G	B	R	Even Line
11X	R	G	B	Odd Line
	B	R	G	Even Line

Remark: Disable this function in UPS051 mode

R2:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R2	0x4	'h3	X	X	X	X	X	X	X	FPOL (0)	X	UD (1)	SHL (1)

SHL: Horizontal scan direction setting

D0	Function
0	Right to left scan.
1	Left to right scan, default

UD: Vertical scan direction setting

D1	Function
0	Down to up scan.
1	Up to down scan, default

FPOL: Control FRP is inverted or not

D3	Function
0	The FRP polarity the same as FRP, is negative at the first line, default
1	The FRP polarity will be inverted



A025CTN01.0 Product Spec	Version	1.0
	Page	26/52

R3:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R3	0x6	'h1	X	X	X	X	X	X	PALM (0)	PAL (0)	SEL (1h)		

SEL: Input data timing format selection

D[2:0]	Data input format	Operating frequency
000	UPS051	9.7 MHz
001	UPS052	24.54 MHz(Default)
010	UPS052	27 MHz
011	YUV (mode A)	24.54 MHz
100	YUV (mode A)	27 MHz
101	YUV (mode B)	24.54 MHz
110	YUV (mode B)	27 MHz
111	CCIR_656	27 MHz

Remark: YUV mode A: Data sequence are “Cb_Y_Cr_Y...”.

YUV mode B: Data sequence are “Cr_Y_Cb_Y...”.

PAL: Select NTSC or PAL interface mode

D3	Function
0	Select NTSC interface mode, default
1	Select PAL interface mode

Remark: Disable this function in UPS051 mode

PALM: Select skip method in PAL mode interface

D4	Function
0	Vertical line 280, default
1	Vertical line 288

Remark: Disable this function in UPS051 mode

R4:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R4	0x8	'h0	X	X	X	X	X	X	DDL (0h)				

DDL: Select the data delay timing, normally pulled low.

D[4:0]	NO.	D[4:0]	NO.
00000	0(Default)	10000	-1
00001	+1	10001	-2
00010	+2	10010	-3



A025CTN01.0 Product Spec	Version	1.0
	Page	27/52

00011	+3	10011	-4
00100	+4	10100	-5
00101	+5	10101	-6
00110	+6	10110	-7
00111	+7	10111	-8
01000	+8	11000	-9
01001	+9	11001	-10
01010	+10	11010	-11
01011	+11	11011	-12
01100	+12	11100	-13
01101	+13	11101	-14
01110	+14	11110	-15
01111	+15	11111	-16

R5:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R5	0xa	'h0	X	X	X	X	X	FRAD (0h)		HDL (0h)			

HDL: Select the Data delay timing, normally pulled low.

D[3:0]	NO.	D[3:0]	NO.
0000	0(Default)	1000	+8
0001	+1	1001	-1
0010	+2	1010	-2
0011	+3	1011	-3
0100	+4	1100	-4
0101	+5	1101	-5
0110	+6	1110	-6
0111	+7	1111	-7

FRAD: Odd frame or Even frame advance select, default low.

D[5:4]	Advance Frame	Notes
00	Default	Odd/Even frame Tstv are the same
01	Odd Frame	Even frame Tstv = HDL setting +1
10	Even Frame	Odd frame Tstv = HDL setting +1

Remark: This function is enable in SEL[2:0]="111" mode

R6:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
----	---------	--	-----	----	----	----	----	----	----	----	----	----	----



A025CTN01.0 Product Spec	Version	1.0
	Page	28/52

R6	0xc	'h6	X	X	X	X	X	X	X	X	VCSL (6h)
----	-----	-----	---	---	---	---	---	---	---	---	--------------

VCSL: VCAC level selection (deviation +/-0.1V)

D[2]	D[1]	D[0]	Voltage	D[2]	D[1]	D[0]	Voltage
0	0	0	4.4V	1	0	0	4.8V
0	0	1	4.5V	1	0	1	4.9V
0	1	0	4.6V	1	1	0	5.0V(Default)
0	1	1	4.7V	1	1	1	5.1V

Remark: VCAC is restrained by VDD2.

R7:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R7	0xe	'h3	X	X	X	X	X	X	GAMSEL (0)	X	VLNC (0)	AVGY (1)	1

AVGY: Average YUV interface Luminance Y setting

D1	Function
0	Only used odd Y sample for YUV conversion.
1	Used odd and even Y sample for YUV conversion, default

Remark: This function disable in UPS051/UPS052 mode

VLNC: Vertical line function (240/234 lines).

D2	Function
0	Vertical line are 240, default
1	Vertical line are 234.

Remark: This function disable in UPS051 mode and [280x222 mode](#)

GAMSEL: Gamma R table selection

D4	Function
0	Select GAM1 value, this is S-Gamma, default
1	Select GAM2 value, this is Gamma2.2

Remark: please send the command about the bit of GAMSEL= 1 to register if you want to use Gamma2.2



A025CTN01.0 Product Spec	Version	1.0
	Page	29/52

T0:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T0	0x1	'h4	X	X	X	AVDDADJ (0h)			PDTY (0h)		FBV (4h)		

FBV: DC-DC feedback voltage

D2	D1	D0	FB Voltage	D2	D1	D0	FB Voltage
0	0	0	0.4V	1	0	0	0.6V(Default)
0	0	1	0.45V	1	0	1	0.65V
0	1	0	0.5V	1	1	0	0.7V
0	1	1	0.55V	1	1	1	0.75V

PDTY: PWM duty cycle selection for back light power converter

D4	D3	PFM duty cycle
0	0	75%(Default)
0	1	55%
1	0	60%
1	1	65%

AVDDADJ: AVDD voltage generator setting

D7	D6	D5	Voltage	D7	D6	D5	Voltage
0	0	0	4.3V(Default)	1	0	0	4.7V
0	0	1	4.4V	1	0	1	4.8V
0	1	0	4.5V	1	1	0	4.9V
0	1	1	4.6V	1	1	1	5.0V

T1:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T1	0x3	'h8	X	X	X	X	AVG (0)	X	T352 (0)	CONST (8h)			

CONST: RGB contrast level adjustment. (0.125/Step)

D3	D2	D1	D0	Level
0	0	0	0	0
:	:	:	:	:
1	0	0	0	1.00(Default)
:	:	:	:	:
1	1	1	1	1.875



A025CTN01.0 Product Spec	Version	1.0
	Page	30/52

T352: Select UPS052 path and input data format for 352RGB

D4	Function
0	SEL setting timing, default
1	SEL setting don't care, input data for 352RGB (f= 27MHz).

AVG: Data alignment to scaling down function select.

D6	Function
0	Data alignment by DMDA settling, default
1	Data alignment with averaged and input data

T2:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T2	0x5	'h20	X	X	X	X	VDCEN (0)	VCOMDC (20h)					

VCOMDC: VCOM DC level adjustment. (16mV/LSB)

D5	D4	D3	D2	D1	D0	Voltage
0	0	0	0	0	0	0.688V
0	0	0	0	0	1	0.704V
:	:	:	:	:	:	:
1	0	0	0	0	0	1.200V(Default)
1	0	0	0	0	1	1.216V
:	:	:	:	:	:	:
1	1	1	1	1	1	1.696V

VDCEN: Setting FRP output to add DC level

D6	Function
0	External VCOM DC level, default
1	Internal VCOM DC level

T3:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T3	0x7	'h4	X	X	X	X	BRADJ (40h)						

BRADJ: Brightness level adjustment. (4LSB/Step)

D6	D5	D4	D3	D2	D1	D0	Level
0	0	0	0	0	0	0	-256



A025CTN01.0 Product Spec	Version	1.0
	Page	31/52

:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	+0(Default)
:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	+252

T4:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T4	0x9	'h0	X	X	X	X	X	X	X	X	X	WNSEL (0h)	

WNSEL: Wide and narrow display select.

D[1:0]	Description
00	Normal display (Default)
01	Narrow display
10	Wide display
11	Normal display

Remark: This function disable in UPS051 mode

T5:

No	Address		D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
T5	0xb	'h88	X	X	X	SAT (8h)				HUE (8h)			

HUE: YUV Hue adjustment (5Deg/LSB)

D3	D2	D1	D0	Level
0	0	0	0	-40
:	:	:	:	:
1	0	0	0	0(Default)
:	:	:	:	:
1	1	1	1	35

SAT: YUV Saturation constant adjustment. (0.125/Step)

D7	D6	D5	D4	Level
0	0	0	0	0
:	:	:	:	:
1	0	0	0	1(Default)
:	:	:	:	:
1	1	1	1	1.875

C. Optical Specification (Note1, Note 2 and Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	$\theta=0^\circ$	--	10	20	ms	Note 4
Fall	Tf		--	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	200	300	--		Note 5,6
Viewing Angle	Top	Φ_H	30	45	--	deg.	Note 7
	Bottom	Φ_L	50	60	--		
	Left	θ_L	45	55	--		
	Right	θ_R	45	55	--		
Brightness	Y_L	$\theta=0^\circ$	200	250	--	cd/m ²	Note 8
Chromaticity	White	X	$\theta=0^\circ$	0.250	0.300	0.350	Note 9,10
		Y	$\theta=0^\circ$	0.263	0.313	0.363	
	Red	X	$\theta=0^\circ$	0.542	0.592	0.642	
		Y	$\theta=0^\circ$	0.285	0.335	0.385	
	Green	X	$\theta=0^\circ$	0.289	0.339	0.389	
		Y	$\theta=0^\circ$	0.520	0.570	0.620	
	Blue	X	$\theta=0^\circ$	0.112	0.162	0.212	
		Y	$\theta=0^\circ$	0.067	0.117	0.167	
Uniformity	ΔY_L	%	70	75	--	%	Note 11

Note 1. Ambient temperature =25°C.

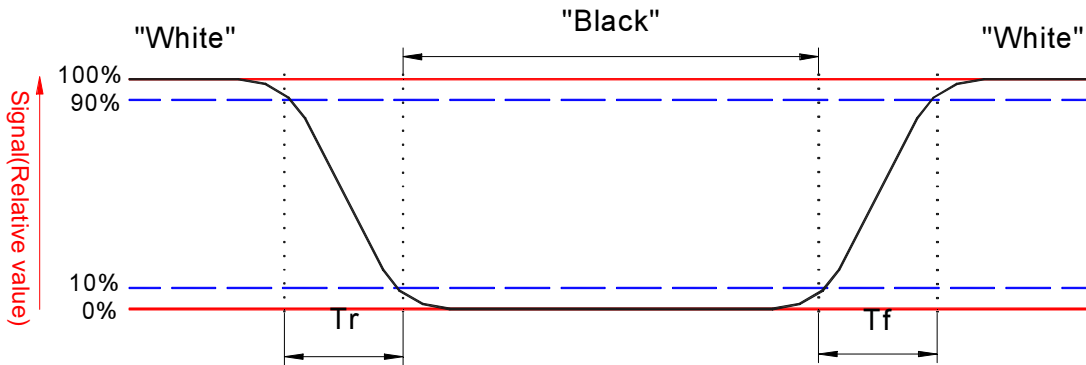
Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-5A, after 10 minutes operation.

Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White $V_i = V_{i50} + 1.5V$

Black $V_i = V_{i50} \pm 2.0V$

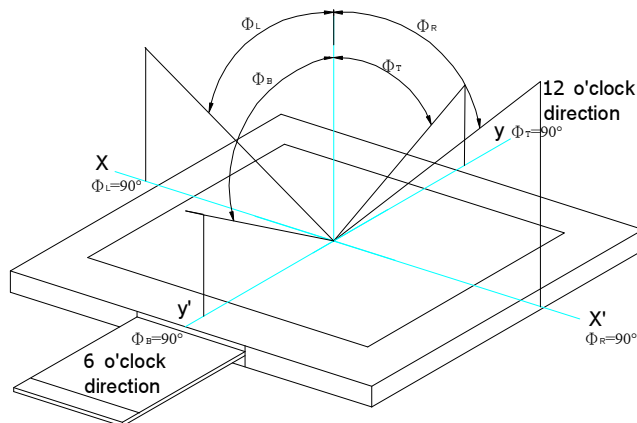
“±” Means that the analog input signal swings in phase with COM signal.

“+” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

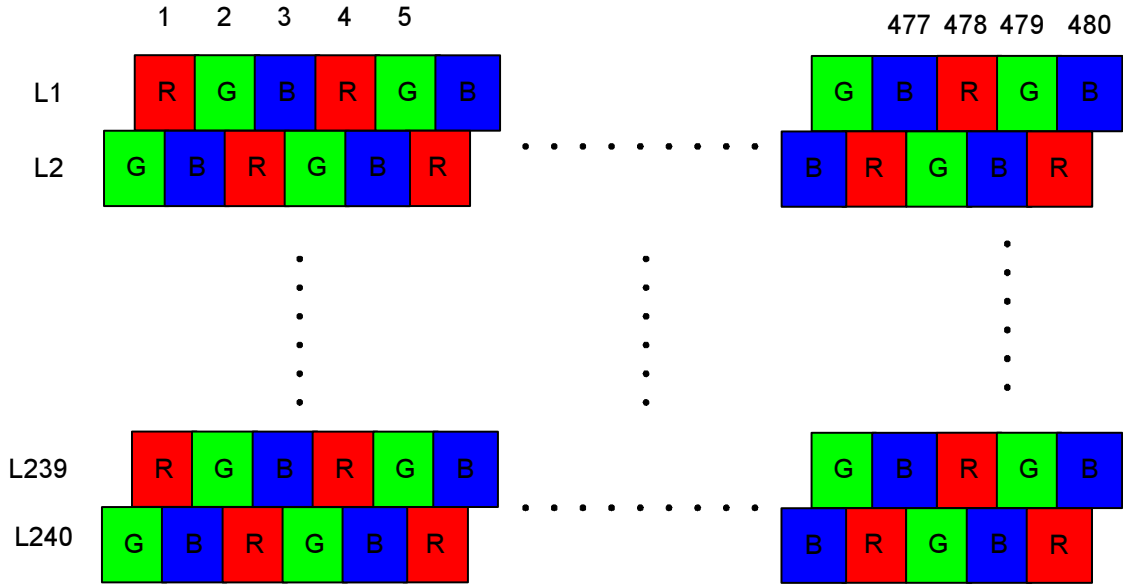
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle, ϕ , Refer to figure as below.

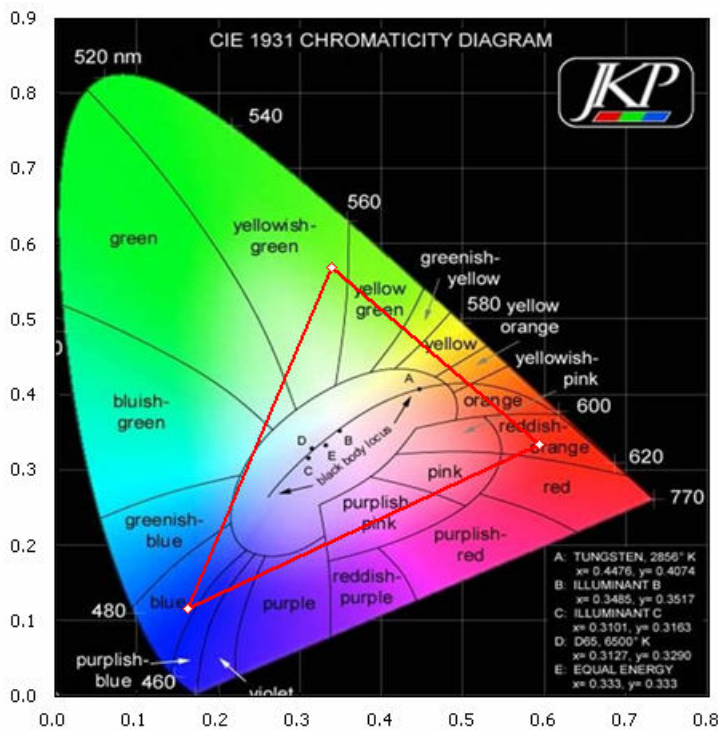


Note 8. Measured at the center area of the panel in gray level 255

Note 9. Color Filter Arrangement

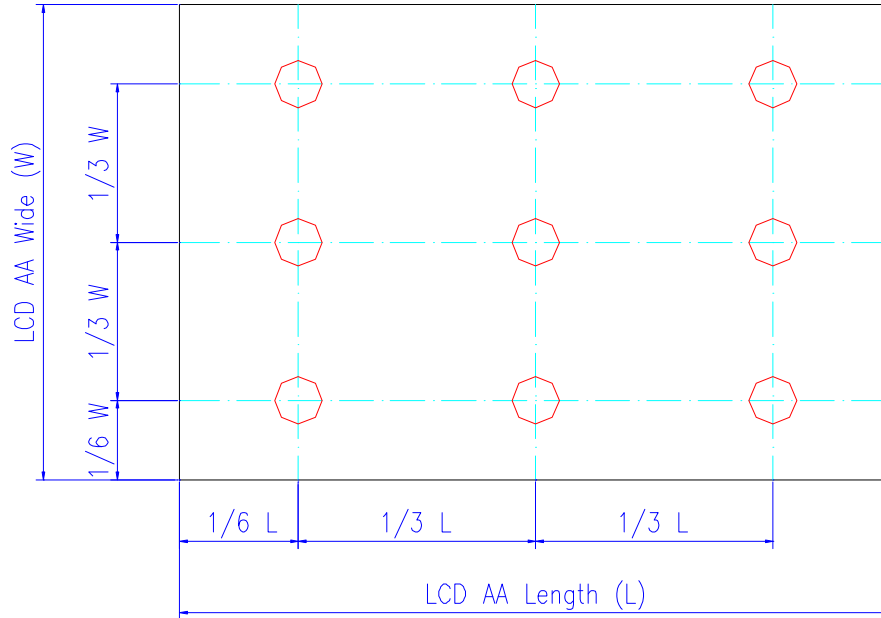


Note 10. Chromaticity Diagram



A025CTN01.0 Product Spec	Version	1.0
	Page	35/52

Note 11. Luminance Uniformity of these 9 points is defined as below:



$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

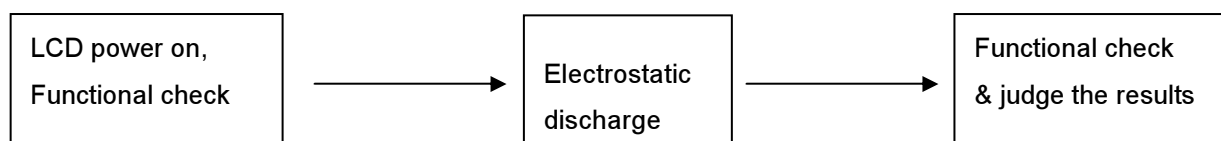
D. Reliability Test Items

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 70□ 240Hrs	
2	Low Temperature Storage	Ta= -25□ 240Hrs	
3	High Temperature Operation	Tp= 60□ 240Hrs	
4	Low Temperature Operation	Ta= 0□ 240Hrs	
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~80□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note 2,3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
10	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
11	Vibration (With Carton)	Random vibration: 0.015G ² /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
12	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note 1. Ta: Ambient temperature.

Note 2. ESD Testing Flow as the below,

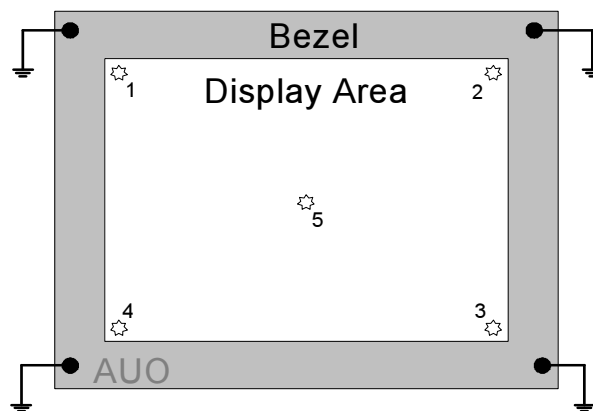
Note 3. Make sure protection film(s) on top of polarizer or back of LCD module is(are) removed before test.



A025CTN01.0 Product Spec	Version	1.0
	Page	37/52

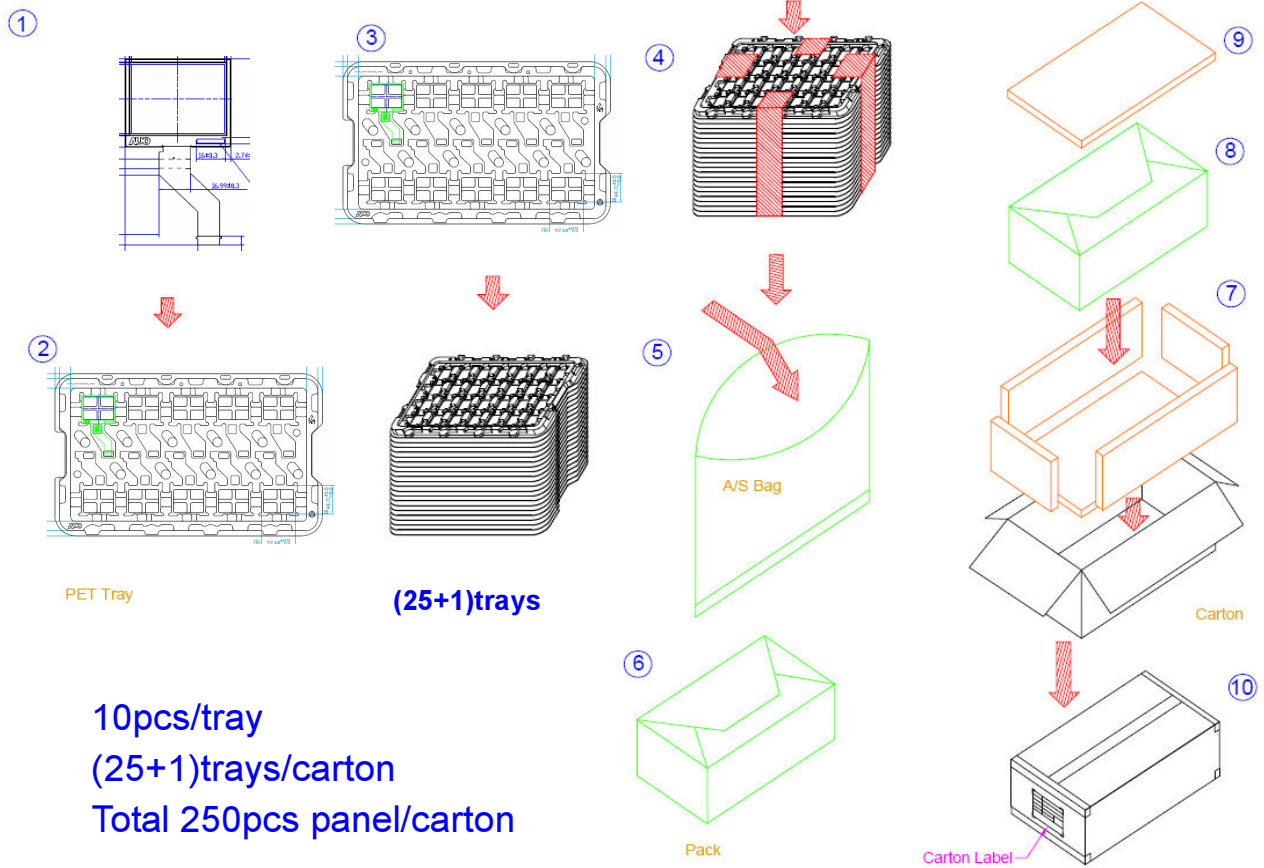
Note 3. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments: Noiseken ESS-2000,
3. Operation System: "CX40FL-B" and adapter "A025CN05"
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
 - a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
 - b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing form



Palletizing sequence (if necessary)

(1). Box placement on wooden pallet

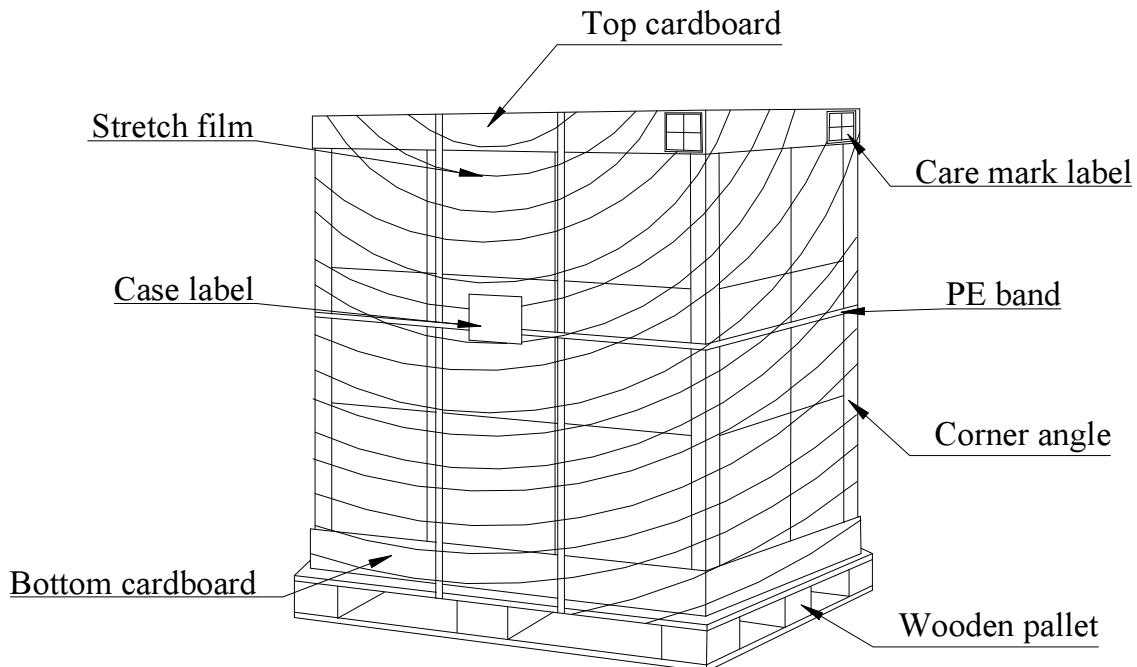
- a. Place max 30 of corrugated boxes on wooden pallet and should not be pushed out of the pallet. (as showed below)
- b. (250 *6) *5 layers: Max 30 boxes / pallet. (7500 pcs modules)

(2). Apply stretch film. Corner angle and PE band

- a. Stretch film should cover around whole pallet.
- b. Apply corner angle to 4 top edge and 4 side edge of the pallet.
- c. Select corner angle length by height of palletizing.
- d. PE band number is depended on customer requirement and height of palletizing.

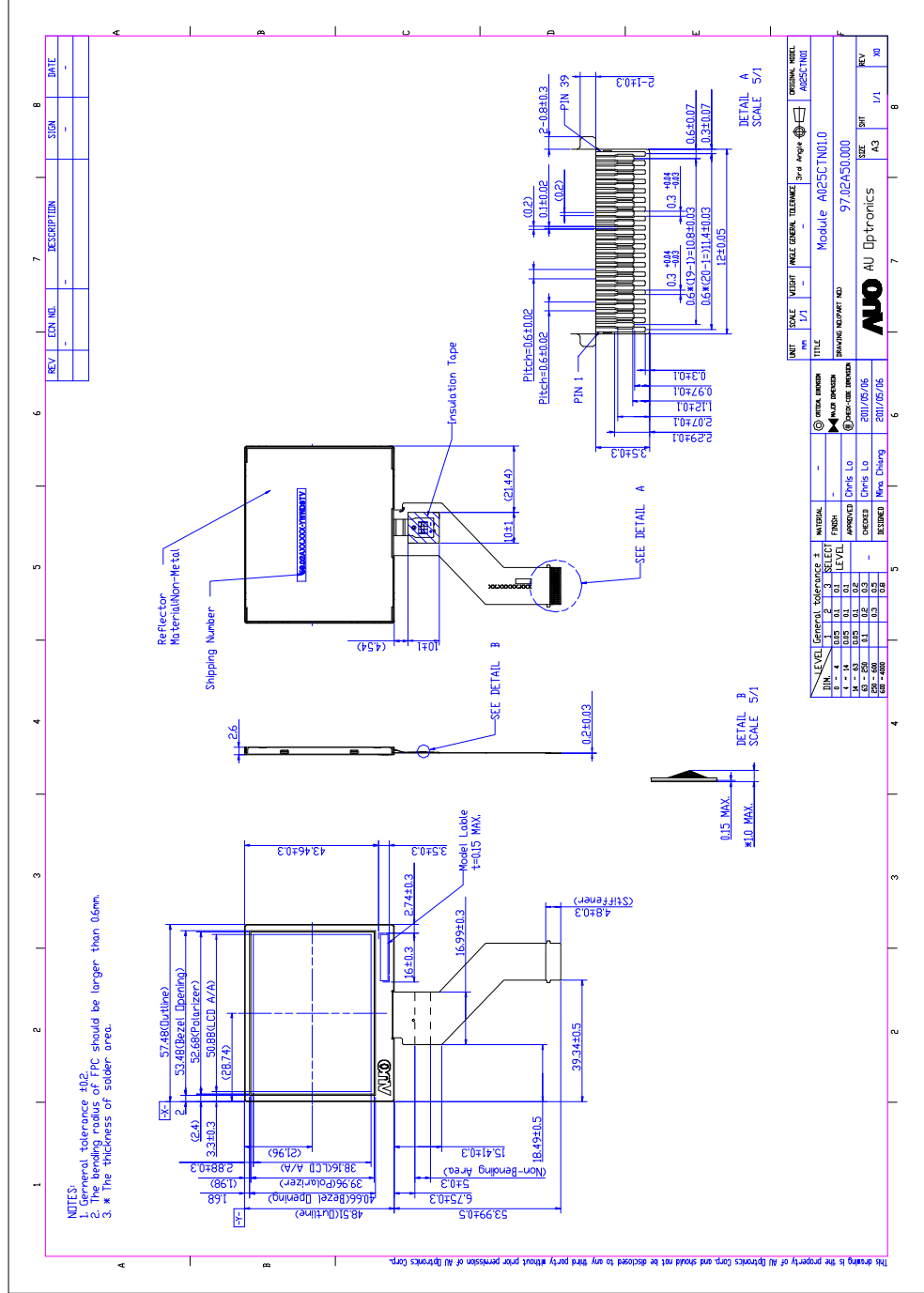
(3). Labeling

- a. Apply shipping case label is depended on customer requirement.
- b. Apply care mark label at 4 side (Front / Back / Left / Right)on the pallet.
- c. Empty box label is applied if needed.
- d. Other package method or label are depended on customer requirement.



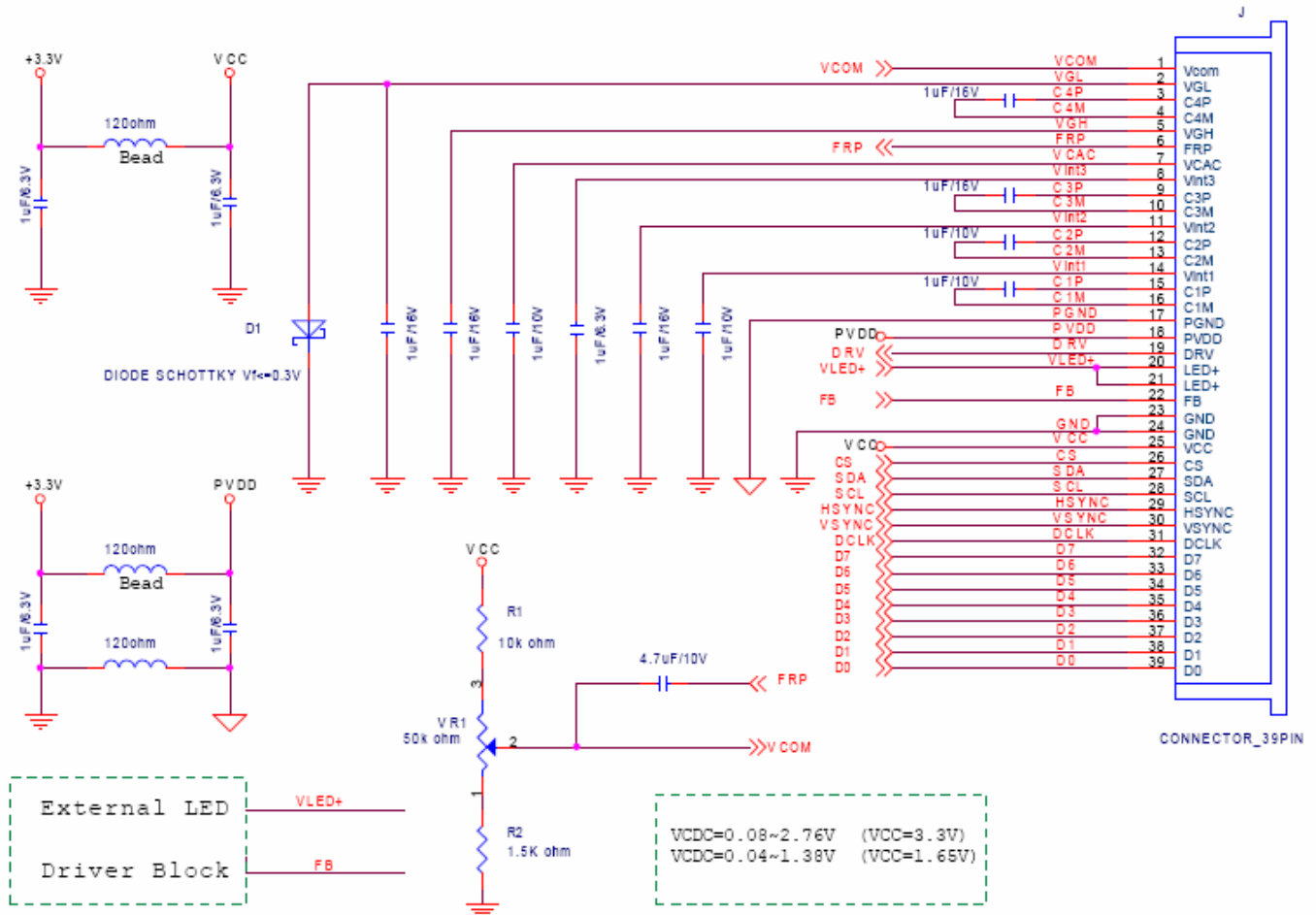
Note: Limit of box palletizing=Max 5 layers (ship and stock conditions) for air transport and marine transit.

F. Outline dimension



G. Application note

1. Application circuit



Note 1: In order to avoid external noise >0.7V from AGND to VGL, Schottky diode D1 ($V_f \leq 0.3V$) is added on VGL to ensure the abnormal trigger would be lower than 0.7V

2. Stand-by timing

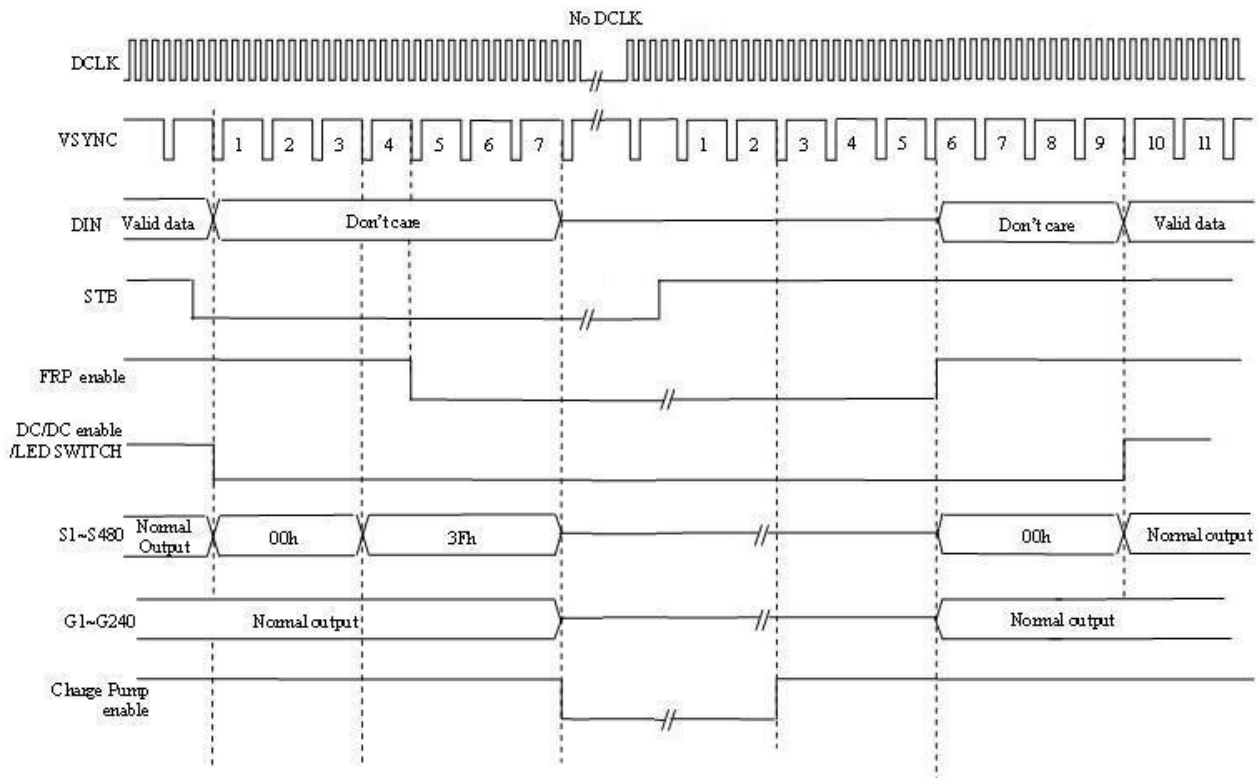


Fig. 1 Stand-by timing diagram

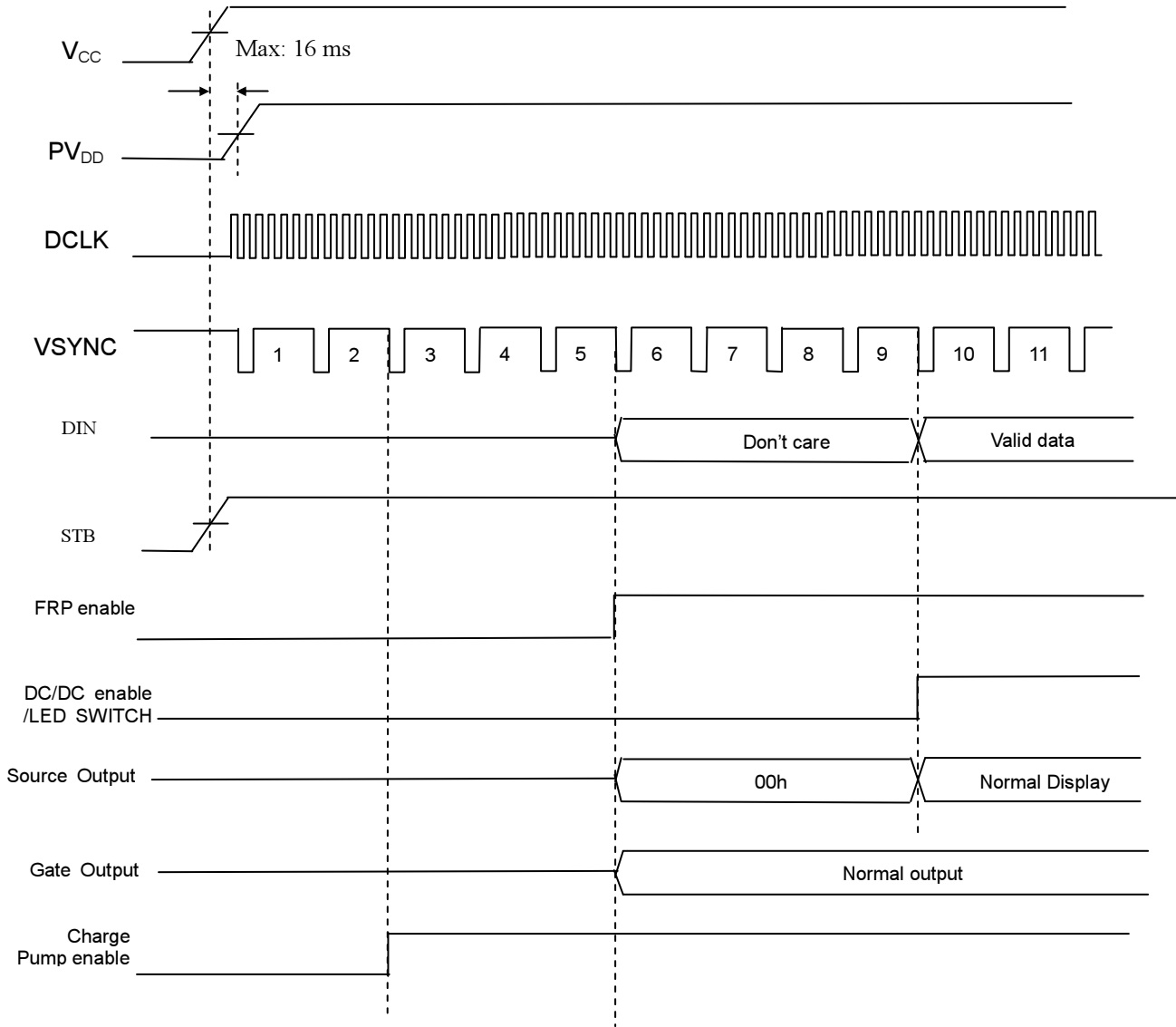
Note 1: During No DCLK, HSYNC and VSYNC can be stopped. But in all other cases HSYNC and VSYNC must be active.

Note 2: External signal: DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)

Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable

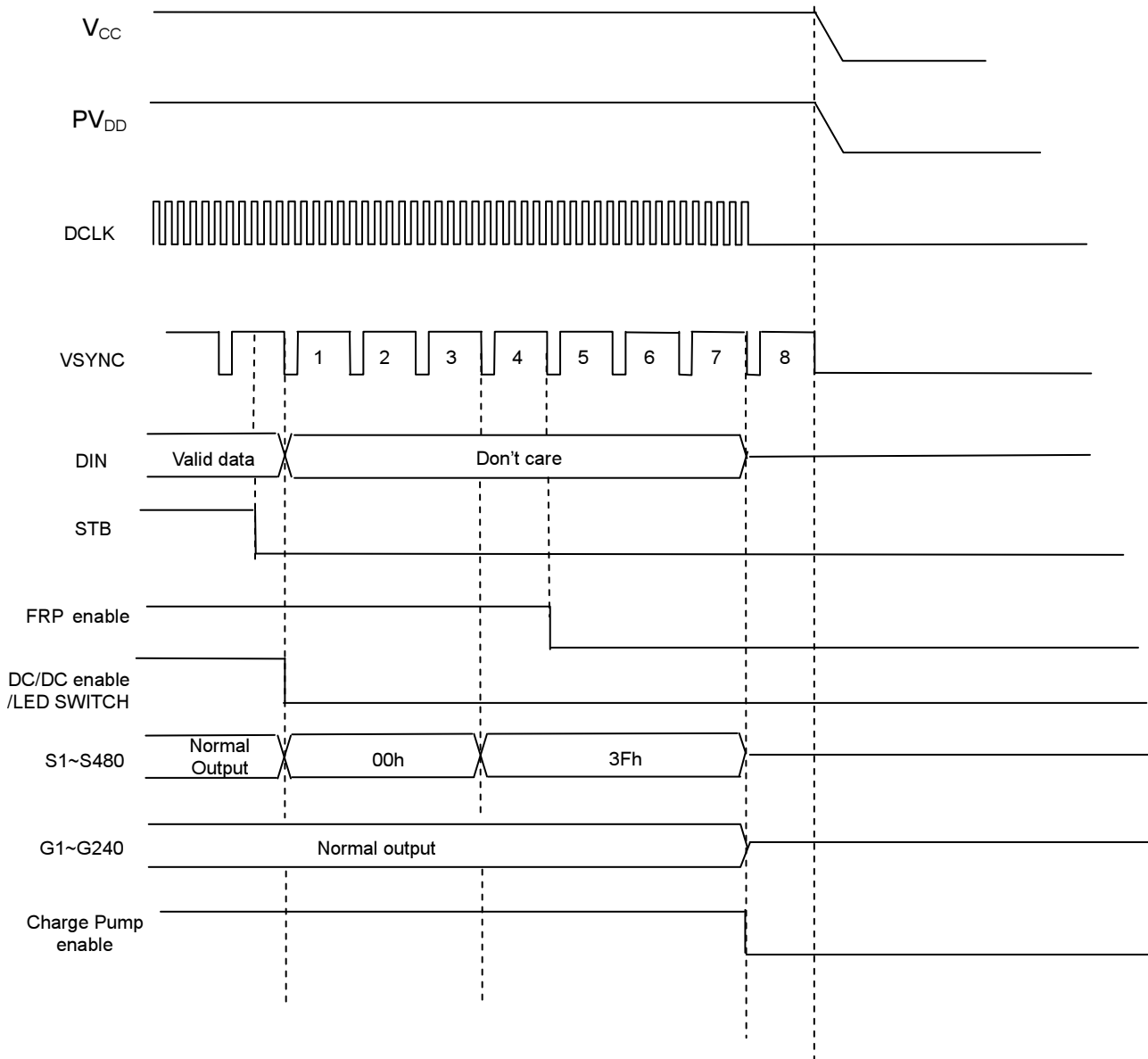
G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

3. Power on sequence



Note 1: External signal: V_{CC}, PV_{DD}, DCLK, VSYNC, DIN (D0 ~ D7), STB (By register)
 Internal signal: DC/DC enable S1 ~ S480 (Source Driver output signal), FRP enable,
 G1 ~ G240 (Gate Driver output signal) and Charge Pump enable.

4. Power off sequence

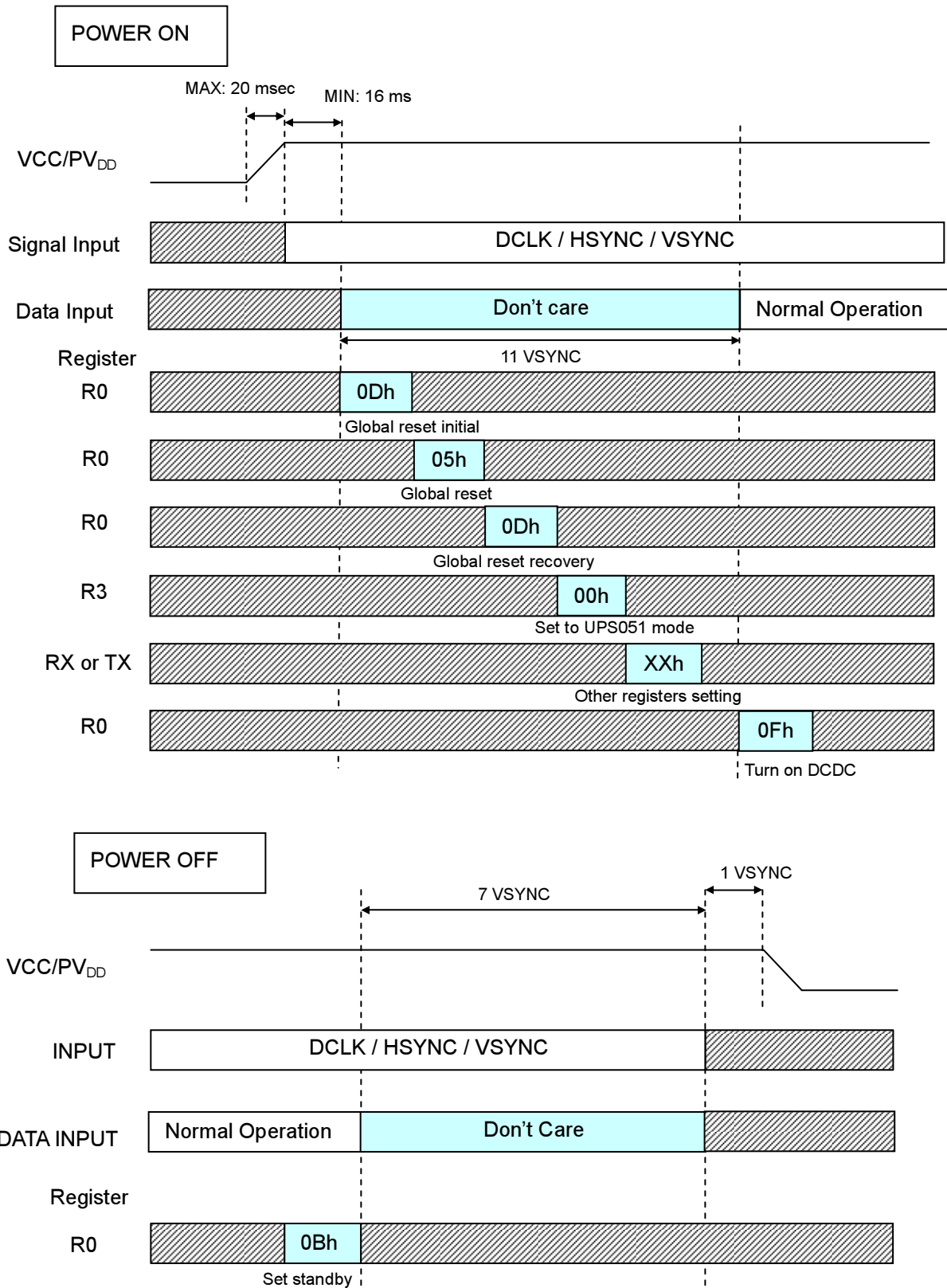


Note 1: External signal: V_{CC} , PV_{DD} , $DCLK$, $VSYNC$, DIN (D0 ~ D7), STB (By register)

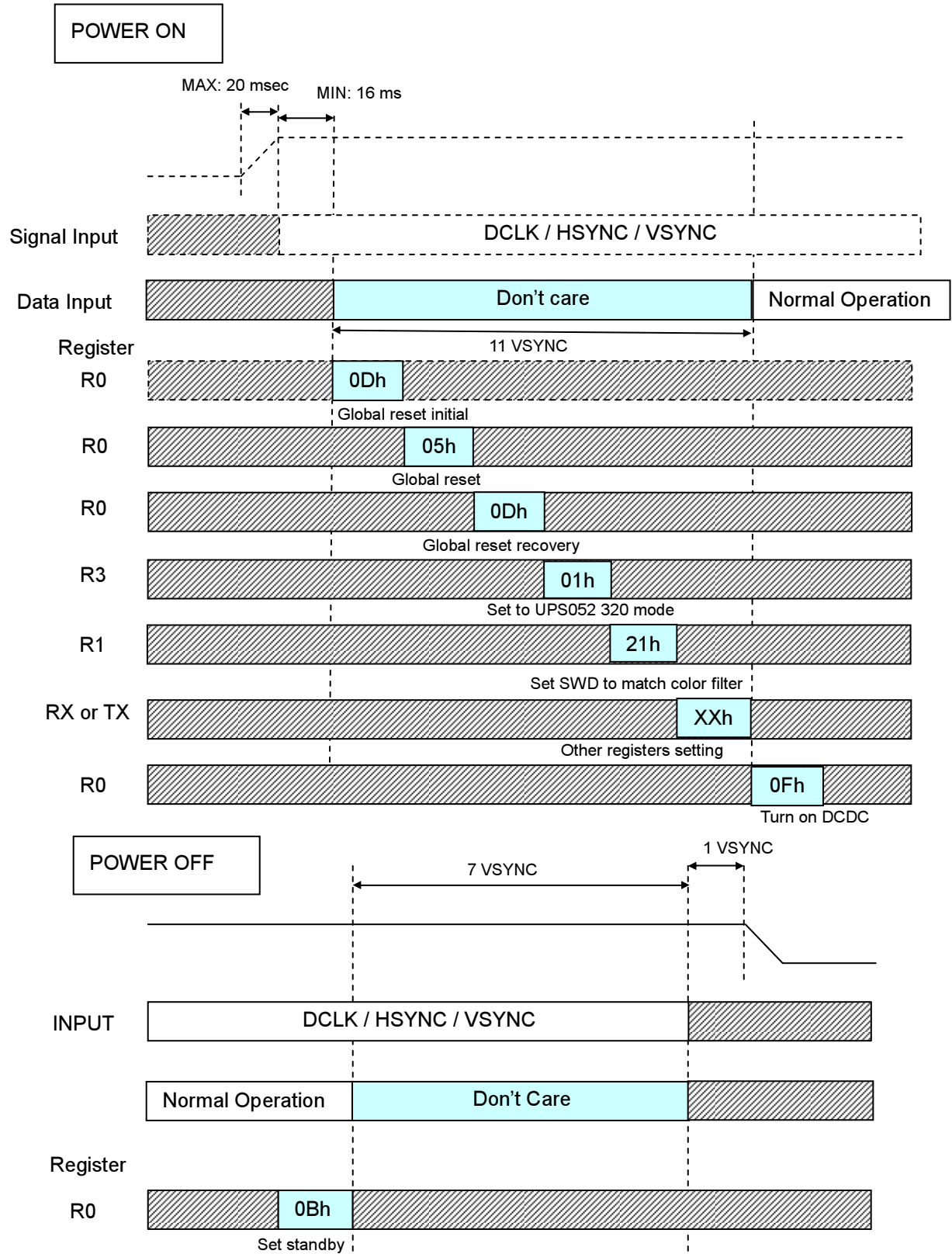
Internal signal: DC/DC enable $S1 \sim S480$ (Source Driver output signal), FRP enable, $G1 \sim G240$ (Gate Driver output signal) and Charge Pump enable.

5. Recommended power on/off serial command settings

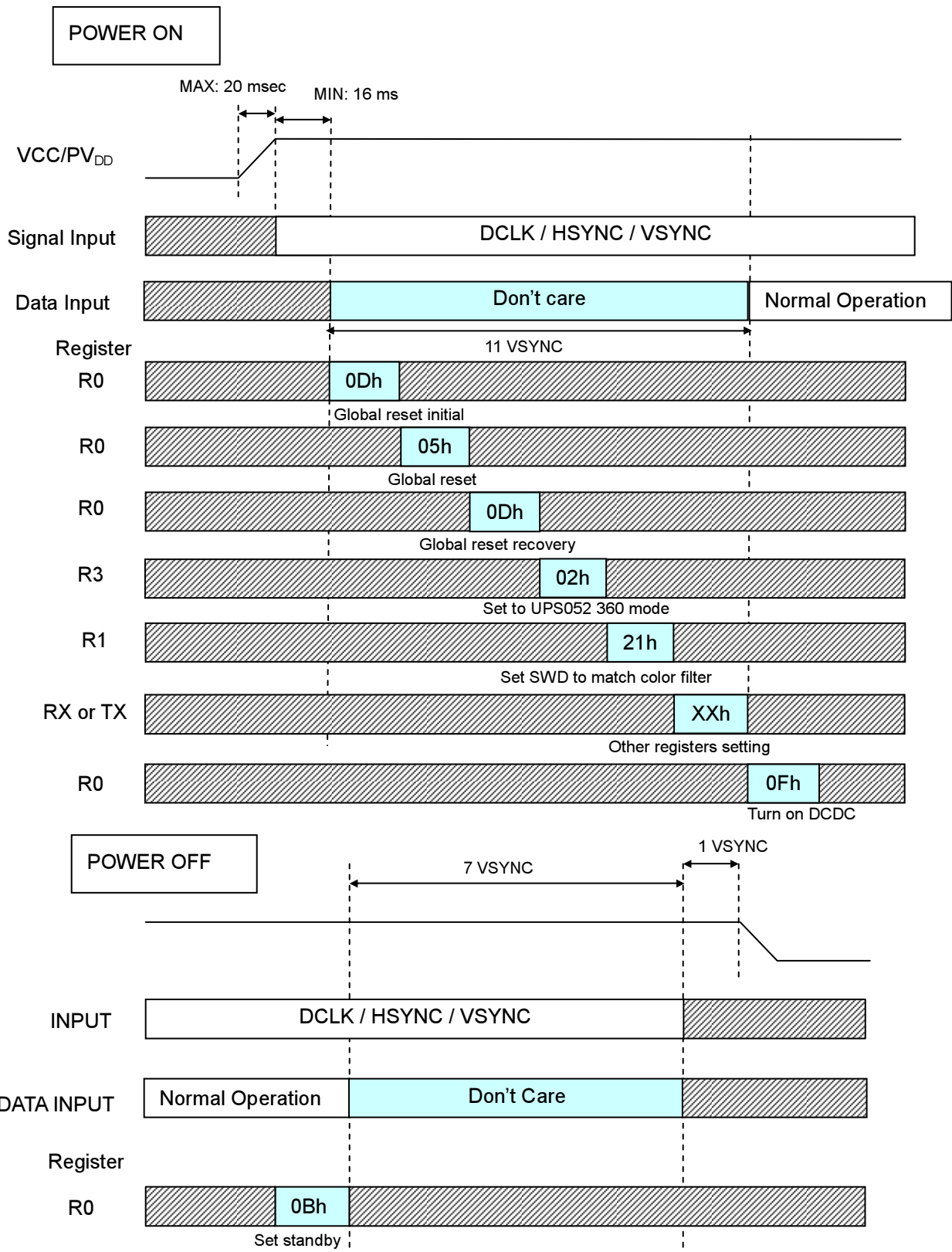
5.1. Recommend UPS051 (9.7 MHz) power on/off setting



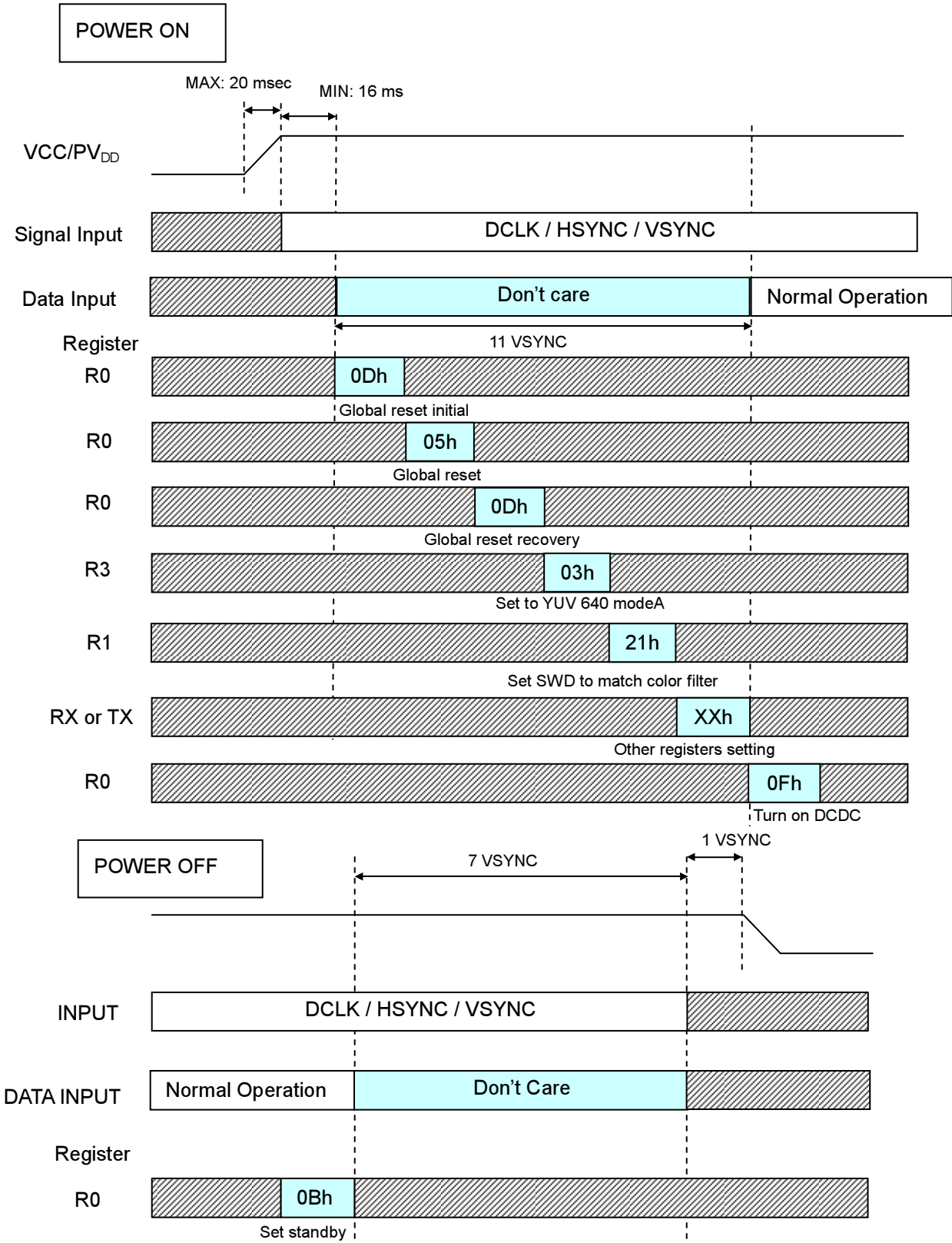
5.2. Recommend UPS052 320RGB mode (24.54 MHz) power on/off setting



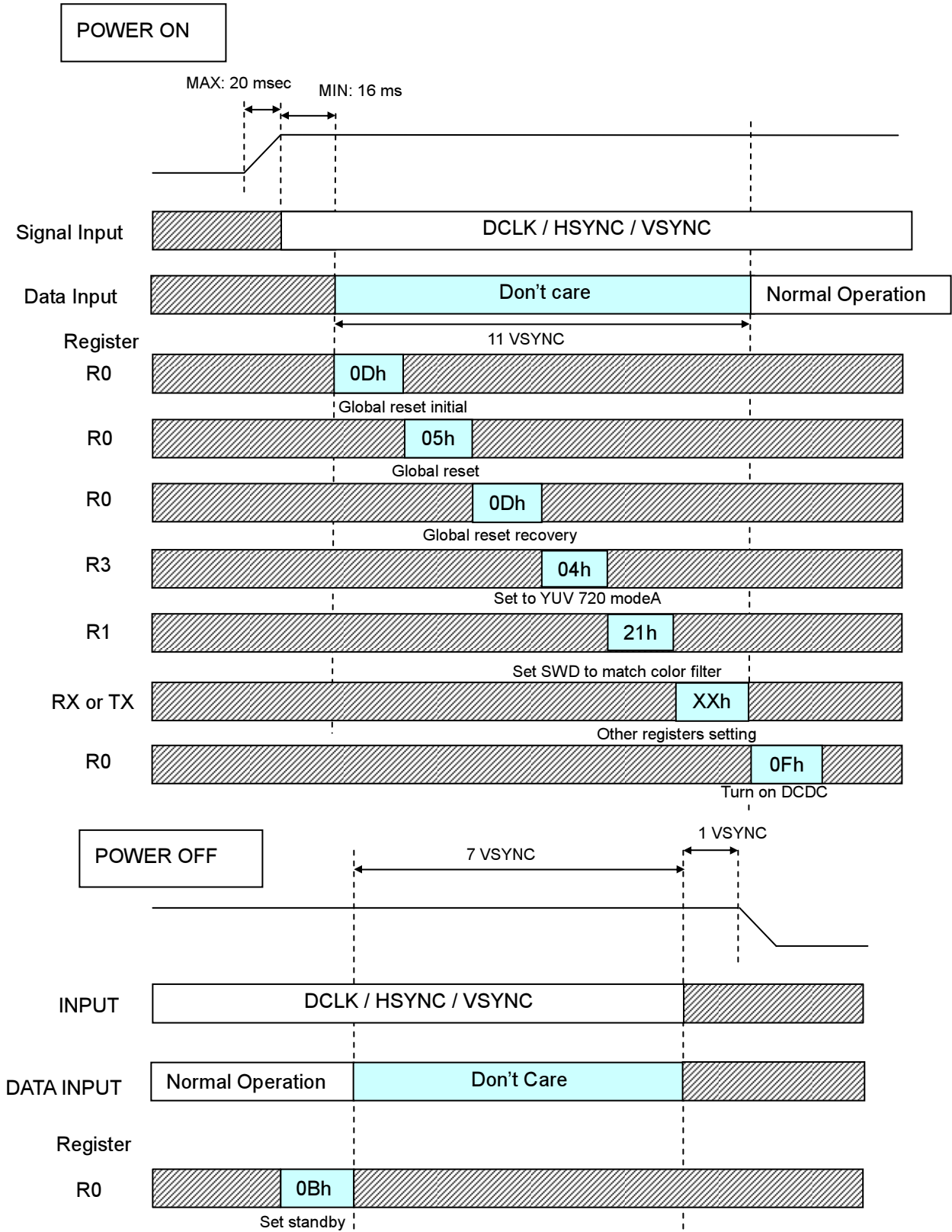
5.3. Recommend UPS052 360RGB mode (27MHz) power on/off setting



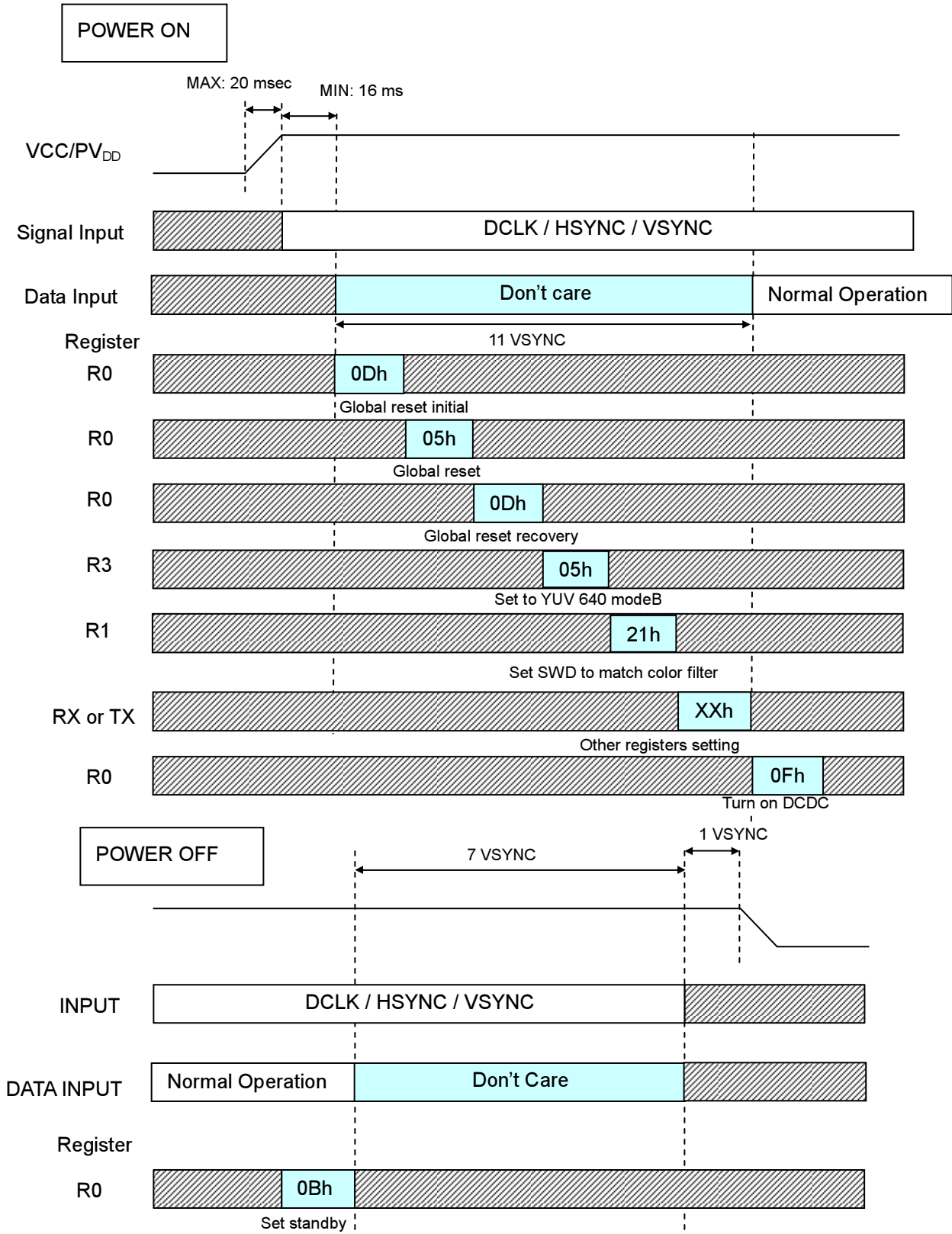
5.4. Recommend YUV mode A 640Y 320CrCb (24.54 MHz) power on/off setting



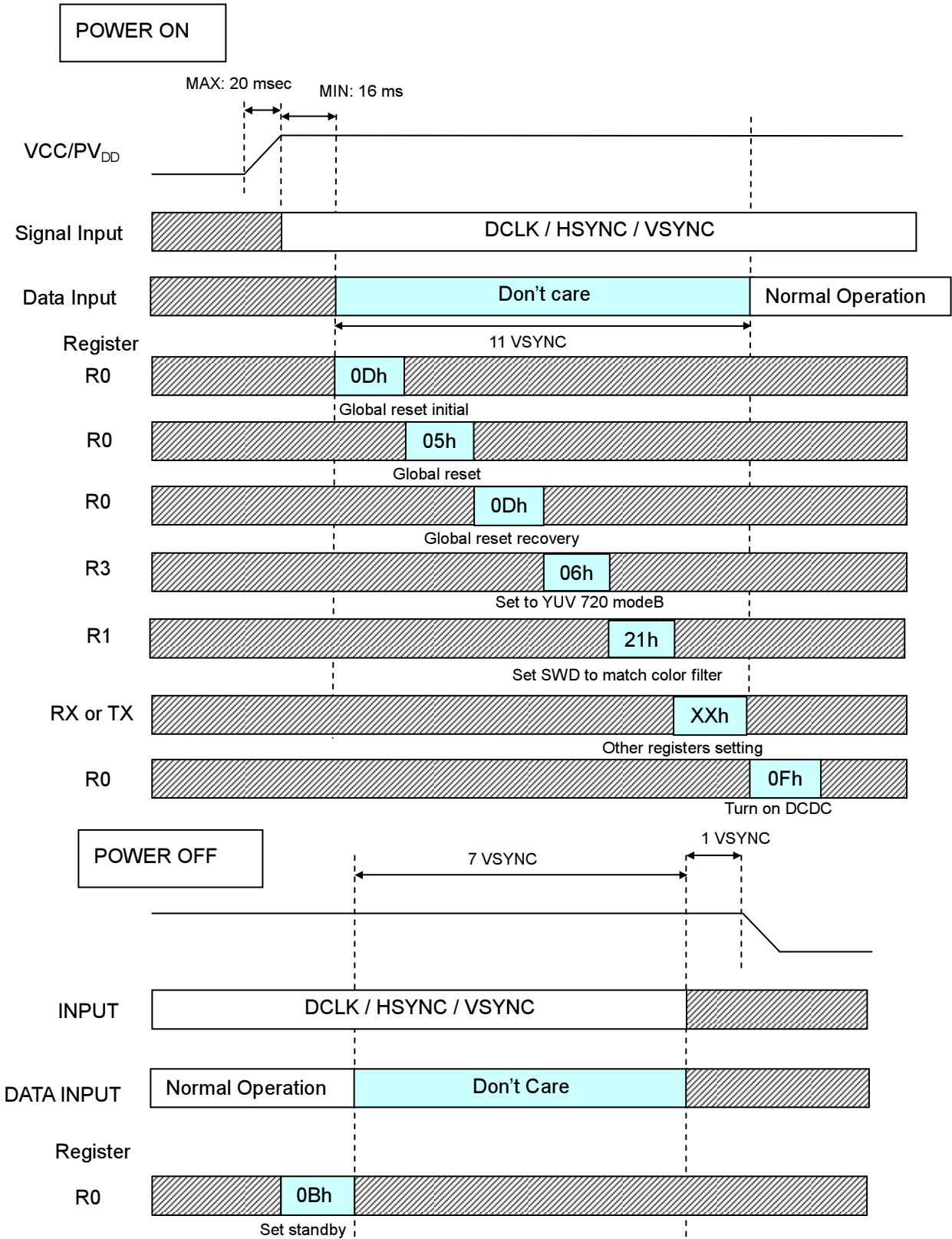
5.5. Recommend YUV mode A 720Y 360CrCb (27 MHz) power on/off setting



5.6. Recommend YUV mode B 640Y 320CrCb (24.54 MHz) power on/off setting



5.7. Recommend YUV mode B 720Y 320CrCb (27 MHz) power on/off setting



5.8. Recommend CCIR656 mode (27 MHz) power on/off setting

