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Product Specifications

2.5″ COLOR LTPS TFT-LCD MODULE

MODEL NAME: A025DL02 V4

<◆>Preliminary Specifications

< > Final Specifications

Note: The content of the specifications is subject to change.

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Record of Revision

Version	Revise Date	Page	Content
0	2006/02/22	28	First Draft
0.1	2006/03/02	15 27	Modified description of SHDB1 Add application circuit for external LED driver case
0.2	2006/07/13	16	Update VBLK register setting range
0.3	2007/1/18	8	Add PAL mode parameter

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A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	960 (W) x 240 (H)	
2	Active area (mm)	50.4 x 37.8	
3	Screen size (inch)	2.5” (Diagonal)	
4	Dot pitch (mm)	0.0525 x 0.1575	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	60.73 x 45.07 x 2.54	
7	Weight (g)	17	
8	Panel Surface treatment	Hard coating (3H)	

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B. Electrical specifications

1. Pin assignment

a. TFT-LCD panel driving section

Pin No.	Symbol	I/O	Description	Remark
1	VCOM	I	Common voltage	
2	ParaSeri	I	Parallel or serial data input selection	Note 1
3	CS	I	Serial command enable signal	Note 2
4	SDA	I	Serial command data input	Note 2
5	SCL	I	Serial command clock input	Note 2
6	HSYNC	I	Horizontal sync input	
7	VSYNC	I	Vertical sync input	
8	DCLK	I	Input data clock	
9	DB5	I	B data input; MSB	
10	DB4	I	B data input	
11	DB3	I	B data input	
12	DB2	I	B data input	
13	DB1	I	B data input	
14	DB0	I	B data input; LSB	
15	DG5	I	G data input; MSB	
16	DG4	I	G data input	
17	DG3	I	G data input	
18	DG2	I	G data input	
19	DG1	I	G data input	
20	DG0	I	G data input; LSB	
21	DR5	I	R data input; MSB	
22	DR4	I	R data input	
23	DR3	I	R data input	
24	DR2	I	R data input	
25	DR1	I	R data input	
26	DR0	I	R data input; LSB	
27	DRV	O	VLED boost transistor driving signal	

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28	VLED	P	LED power: anode	
29	FB	I / P	LED power: cathode	
30	AVDD	C	Power setting capacitor	
31	AGND	P	Ground for analog circuit	
32	DGND	P	Ground for digital circuit	
33	VDC	P	Power supply for ASIC	
34	VDC	P	Power supply for ASIC	
35	V1	C	Power setting capacitor	
36	V2	C	Power setting capacitor	
37	V3	C	Power setting capacitor	
38	V4	C	Power setting capacitor	
39	V5	C	Power setting capacitor	
40	V6	C	Power setting capacitor	
41	V7	C	Power setting capacitor	
42	V8	C	Power setting capacitor	
43	V9	C	Power setting capacitor	
44	V10	C	Power setting capacitor	
45	FRP	O	VCOM driving signal	Note 3
46	VGL	C	Power setting capacitor	
47	VGH	C	Power setting capacitor	
48	VCOML	C	Power setting capacitor for VCOM	
49	VCOMH	C	Power setting capacitor for VCOM	
50	VCOM	I	Common voltage	

I: Input; O: Output; P: Power; C: Capacitor

Note 1: ParaSeri must be pulled low.

Note 2: 3-wire serial control interface is operational after V_{DC} power on reset, but execution of programmed commands is synchronized at front edge of next VSYNC pulse.

Note 3: FRP is the output of Vcom driver. It is the same phase and amplitude with common electrode driving signal (Vcom). The Vcom amplitude and DC level setting can be adjusted through serial control.

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No.	Symbol	I/O	Description	Remark
Pin 28	VLED	I	LED Anode	
Pin 29	FB	-	LED Cathode	

2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V_{DC}	GND=0	-0.5	5	V	
Operating temperature	Topa		0	60	℃	Ambient temperature
Storage temperature	Tstg		-25	80	℃	Ambient temperature

3. Electrical characteristics

a. Recommended operating conditions (GND=AGND=0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply		V_{DC}	3.1	3.3	3.5	V	Note 1
Input Signal voltage	H Level	V_{IH}	0.8* V_{DC}	-	V_{DC}	V	
	L Level	V_{IL}	GND	-	0.2* V_{DC}	V	

Note 1: A build-in power on reset circuit for V_{DC} is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after V_{DC} power on through serial control. Please refer to the register STB setting for detail.

b. Electrical Characteristics (GND=AGND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{DC}	I_{DC}	V_{DC}=3.3V	-	23	-	mA	Note 1
	$I_{DC(STANDBY)}$	V_{DC}=3.3V	-	25	-	uA	Note 1
DC-DC voltage	V_{GH}	V_{DC}=3.3V		11.5		V	Note 2
	V_{GL}	V_{DC}=3.3V		-5.3		V	Note 2
VCOM voltage	V_{CAC}		5.0	5.6	6.4	Vp-p	AC component, Note 3
	V_{CDC}		1.75	2.4	3.5	V	DC component, Note 4
DRV output voltage	V_{DRV}		0	-	V_{DC}	V	
DRV output current	I_{DRV}		-	-	10	mA	Note 5
Feedback voltage	V_{FB}		0.54	0.6	0.66	V	

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Note 1: Test Condition: 8colorbar+Grayscale pattern, RGB666 mode, DCLK=5.5MHz, other registers are default setting
Note 2: VGH and VGL are output voltages of integrated LCD driver IC.
Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.
Note 4: V_{CDC} could be adjusted, so as to minimize flicker and maximum contrast on each module.
Note 5: I_{DRV} (typ.) based on the recommend application circuit

c. Recommended Capacitance Values of External Capacitor

Recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
AVDD	4.7 to 10	16
VGH	4.7 to 10	16
VGL	4.7 to 10	16
VCOMH	4.7 to 10	16
VCOML	4.7 to 10	16
V1, V2	2.2 to 10	16
V3, V4	2.2 to 10	16
V5, V6	2.2 to 10	16
V7, V8	2.2 to 10	16
V9, V10	2.2 to 10	16

d. Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	I_{LED}	-	20	30	mA	
LED voltage	V_{LED}	-	7.8		V	Note1
LED Life Time	L_{LED}	10000	-	-	Hr	Note2,3

Note 1: For 2 LEDs and I_{LED} = 20mA, V_{LED} = 3.6*2+0.6 = 7.8V. Please refer to Figure 6(page 26).
Note 2: Ta. = 25℃, I_{LED} = 20mA
Note 3: Brightness to be decreased to 50% of the initial value.

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4. AC Timing

a. RGB666 (320 mode/NTSC) timing specifications (refer to Fig. 1, Fig. 2)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency		$1/t_{DCLK}$		TBD		5.00	MHz	V_{DC}=3.1V
				5.00		5.25	MHz	V_{DC}=3.2V
				5.00		5.50	MHz	V_{DC}=3.3V
				5.00		5.75	MHz	V_{DC}=3.4V
				5.00		6.00	MHz	V_{DC}=3.5V
HSYNC	Period	t_H			390		t_{DCLK}	
	Display	t_{hdisp}			320		t_{DCLK}	
	Blanking	t_{hblk}			61		t_{DCLK}	
	Pulse width	t_{hsw}			1		t_{DCLK}	
VSYNC	Period	t_V	NTSC		262.5		t_H	
			PAL		312.5			
	Display period	t_{vdisp}	NTSC		240		t_H	
			PAL		288			
	Blanking	t_{vblk}	NTSC		21		t_H	
			PAL		24			
	Pulse width	t_{vsw}			1		t_{DCLK}	
DCLK/HSYNC	Alignment tolerance	t_{skew}		-5		5	ns	Note 1

Note 1: The falling edge of HSYNC should be aligned to the falling edge of DCLK. The timing tolerance is 5ns. For detail timing illustration, please refer to Fig. 1.

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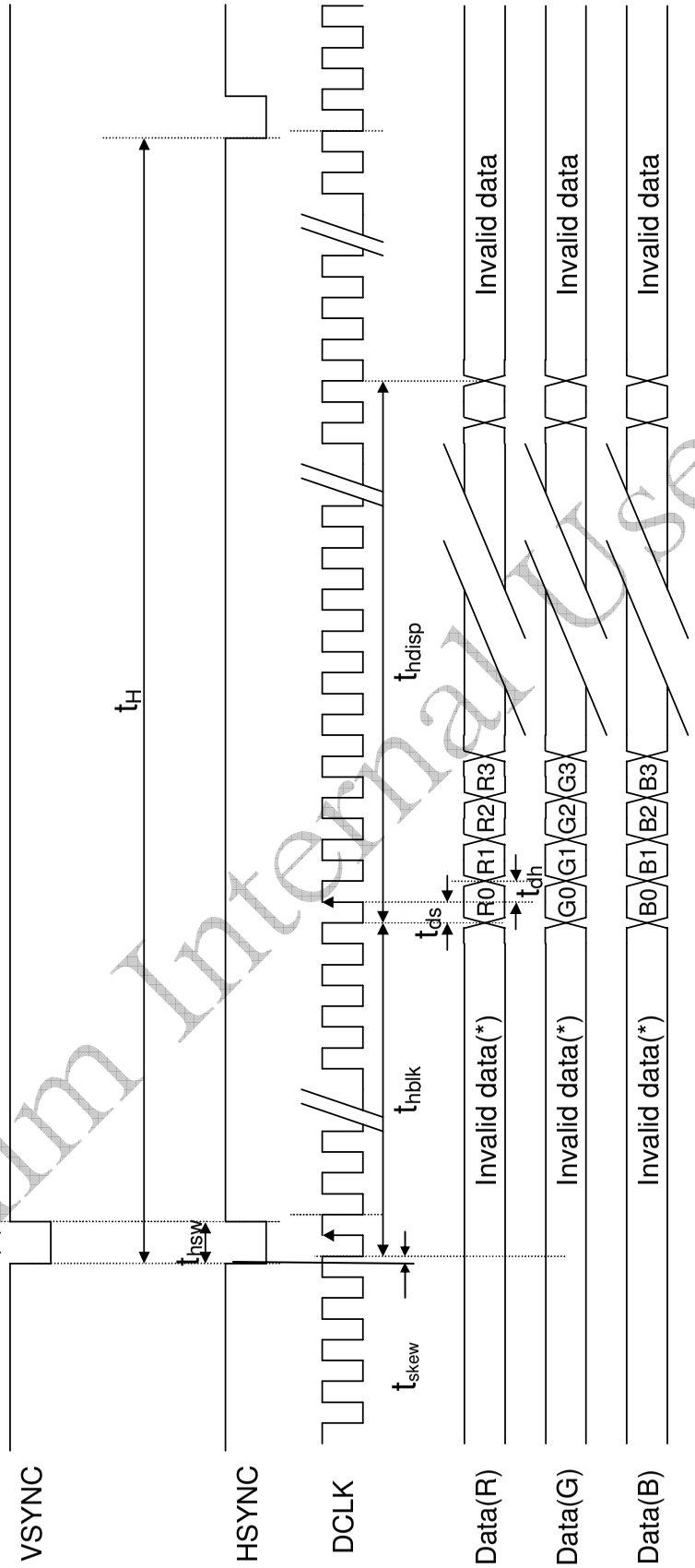

* Please send 00h as blanking data.

Fig. 1 RGB666 Input Horizontal Signal

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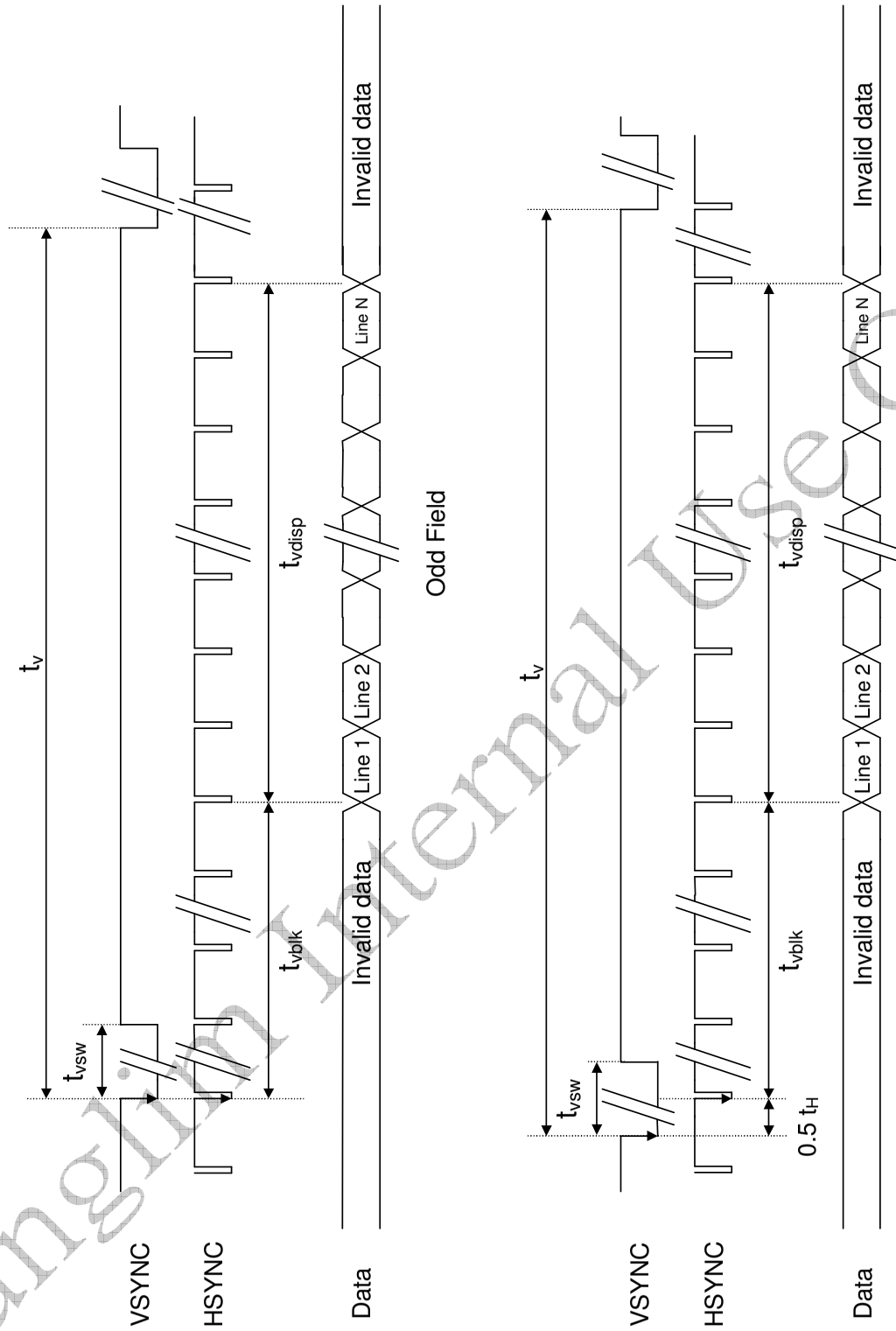

Fig. 2 RGB666 Input Vertical Signal

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5. Serial Control Interface

a. Timing condition (refer to Fig. 4)

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Serial load input setup time	t_{s0}	100			ns	
Serial load input hold time	t_{h0}	100			ns	
Serial data input setup time	t_{s1}	100			ns	
Serial data input hold time	t_{h1}	100			ns	
SCL pulse width	t_{w1L}	200			ns	
	t_{w1H}	200			ns	
CS pulse width	t_{W2}	600			ns	

b. Serial setting map

No	Test				Register Address				Register Data (Default setting)							
	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
R0	0	0	0	0	0	0	0	0	×	×	×	×	×	VCOM_AC(011)		
R1	0	0	0	0	0	0	0	1	×	FLK(0)	VCOM_DC(18h)					
R3	0	0	0	0	0	0	1	1	BRIGHTNESS(40h)							
R4	0	0	0	0	0	1	0	0	×	×	SEL (00)		NTSC/PAL (10)		VDIR (1)	HDIR (1)
R5	0	0	0	0	0	1	0	1	DRV_FREQ (0)	GRB (1)	×	PWM_DUTY(10)		SHDB2 (1)	SHDB1 (1)	STB (0)
R6	0	0	0	0	0	1	1	0	×	LED_CURRENT (00)		VBLK (15h)				
R8	0	0	0	0	1	0	0	0	BL_DRV(00)		×	×	×	×	×	×
R12	0	0	0	0	1	1	0	0	PAIR(00)		CSYNC (1)	×	×	VDpol (1)	HDpol (1)	DCLKpol (0)
R13	0	0	0	0	1	1	0	1	CONTRAST(40h)							
R14	0	0	0	0	1	1	1	0	×	SUB-CONTRAST_R(40h)						
R15	0	0	0	0	1	1	1	1	×	SUB-BRIGHTNESS_R(40h)						
R16	0	0	0	1	0	0	0	0	×	SUB-CONTRAST_B(40h)						
R17	0	0	0	1	0	0	0	1	×	SUB-BRIGHTNESS_B(40h)						
R18	0	0	0	1	0	0	1	1	Gamma_VR2(8h)				Gamma_VR1(8h)			
R19	0	0	0	1	0	0	1	1	Gamma_VR4(8h)				Gamma_VR3(8h)			

× : reserved, please set to '0'

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c. Description of Serial Control Operations

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge
- The serial control block is operational after power on reset, but commands are established by the VSYNC signal. If command is transferred multiple times for the same register, the last command before the VSYNC signal is valid. Please refer to Fig. 5.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the first 16 bits of transferred data before the rising edge of CS pulse are valid data.
- Serial block operates with the SCL clock and serial data can be accepted in the power save mode

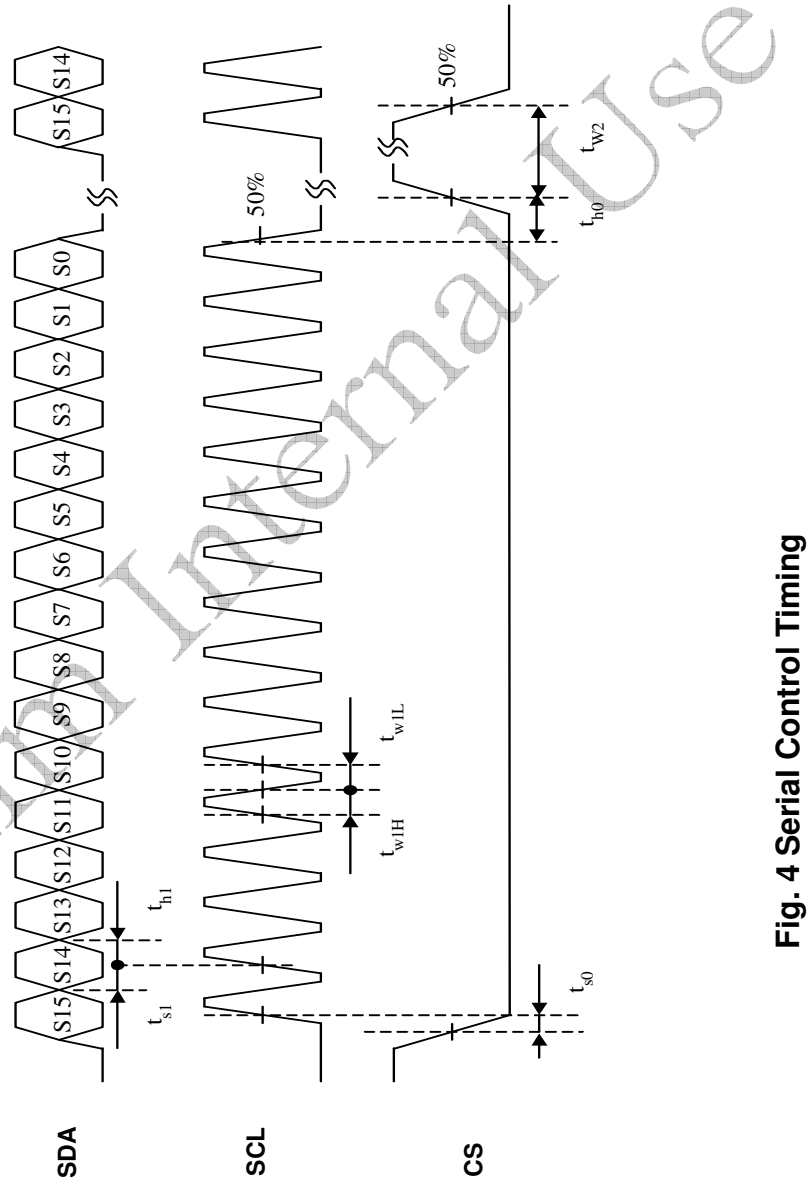

Fig. 4 Serial Control Timing

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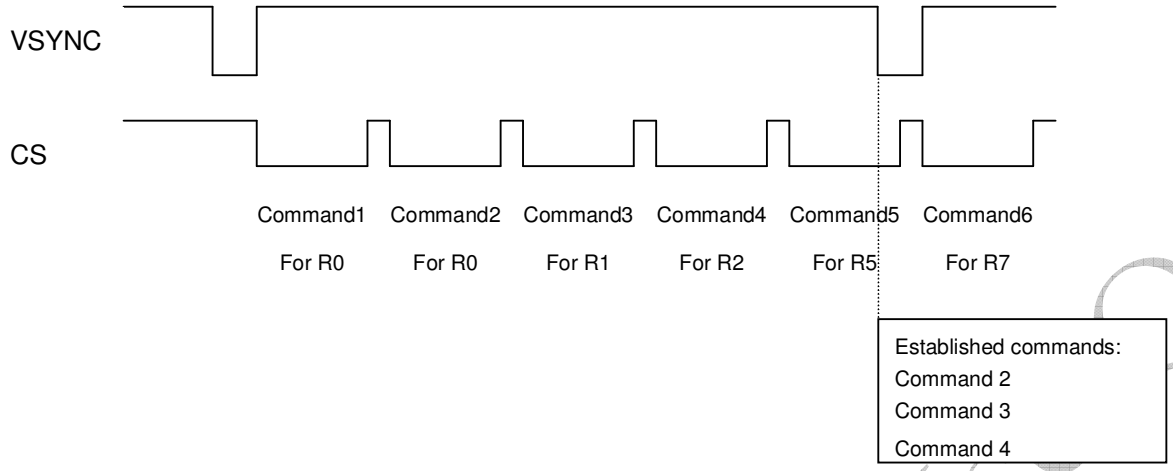
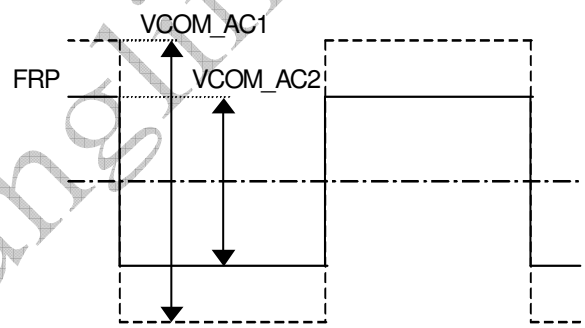


Fig. 5Illustration of Serial Command Operation

d. Description of serial control data

(1) VCOM_AC: Common voltage AC level selection; 3 bit setting, 0.2V / LSB (deviation ±4%)

(MSB – LSB)	VCOM AC LEVEL	UNIT
000	5.0	V
001	5.2	
010	5.4	
011	5.6 (Default)	
100	5.8	
101	6.0	
110	6.2	
111	6.4	



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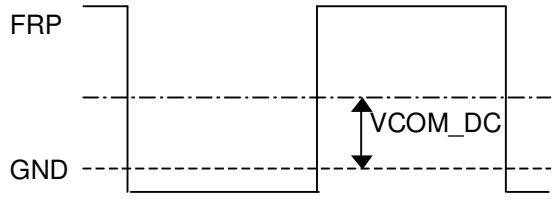
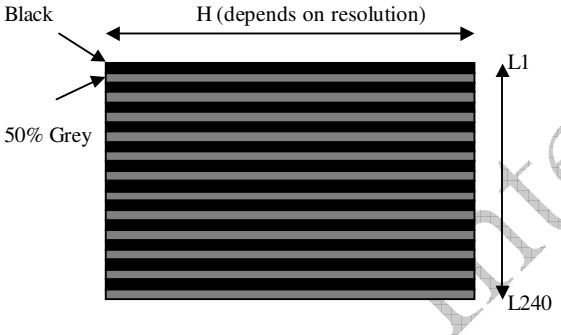
(2) VCOM_DC: Common voltage DC level selection; 6 bit setting, 27.8mV / LSB

(MSB – LSB)	VCOM AC LEVEL	UNIT
00h	1.75	V
18h	2.4(Default)	
3Fh	3.5	



(3) FLK: flicker pattern output

FLK	Function
0	Normal operation (Default)
1	Flicker patttern output



(4) BRIGHTNESS: RGB bright level setting; 8-bit setting

(MSB-LSB)	Function
00h	Dark
40h	Center (Default)
FFh	Bright

(5) HDIR: Horizontal scan direction setting

HDIR	Function
0	Right-to-left scan
1	Left-to-right scan (Default)

(6) VDIR: Vertical scan direction setting

VDIR	Function
0	Down-to-up scan
1	Up-to-down scan (Default)

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(7) NTSC/PAL: NTSC or PAL mode selection (for RGB666 input timing)

(MSB-LSB)	Function
00	PAL mode
01	NTSC mode
1X	Auto-detection mode (Default)

(8) SEL: Input data timing format selection; please refer to AC timing section for detail specifications.

(MSB-LSB)	Input Timing Format
01	RGB666: 320x240

Note: Please set SEL to “01” for RGB666

(9) DRV_FREQ: DRV signal frequency setting

DRV_FREQ	Function
0	DCLK / 64 (default)
1	DCLK / 32

Note: For better efficiency, the setting DRV_FREQ=’1’ and BL_DRV=”11” are recommended.

(10) STB: Standby (power saving) mode setting

STB	Function
0	Standby mode (Default)
1	Normal operation

(11) SHDB1: Shut-down for back light power converter

SHDB1	Function
0	The back light power converter is off
1	The back light power converter is controlled by build-in on/off sequence (Default)

(12)SHDB2: Shut-down for VGH/VGL charge pump

SHDB2	Function
0	The VGH/VGL charge pump is off
1	The VGH/VGL charge pump is controlled by build-in on/off sequence (Default)

(13) PWM_DUTY: PWM duty cycle selection for back light power converter

(MSB-LSB)	Function(PWM duty cycle)
00	50%
01	60%
10	65%(Default)
11	70%

(14) GRB: Register reset setting

GRB	Function
0	Reset all registers to default values
1	Normal operation (Default)

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(15) VBLK: Vertical blanking setting for RGB666 ; 5-bit setting, 1 line/LSB

For RGB666 I/F; 5-bit setting, 1 line/LSB

(MSB-LSB)	V-blanking t_{vblk}	UNIT
03h(min)	3	Line
15h(typical)	21 (Default)	
1Fh(max)	31	

(16) LED_CURRENT: Adjust LED current

DC-DC feedback voltage

(MSB-LSB)	Function
00	0.6 V(default, 20mA)
01	0.75V (25mA)
10	0.45V (15mA)
11	0.3V (10mA)

(17) BL_DRV: Backlight driving capability setting

D7	D6	BL_DRV capability
0	0	Normal capability (Default)
0	1	2 times the Normal capability
1	0	4 times the Normal capability
1	1	8 times the Normal capability

Note: For better efficiency, the setting DRV_FREQ='1' and BL_DRV="11" are recommended.

(18) DCLKpol: DCLK polarity selection

DCLKpol	Function
0	Positive polarity (Default)
1	Negative polarity

(19) HDpol: HSYNC polarity selection

HDpol	Function
0	Positive polarity
1	Negative polarity (Default)

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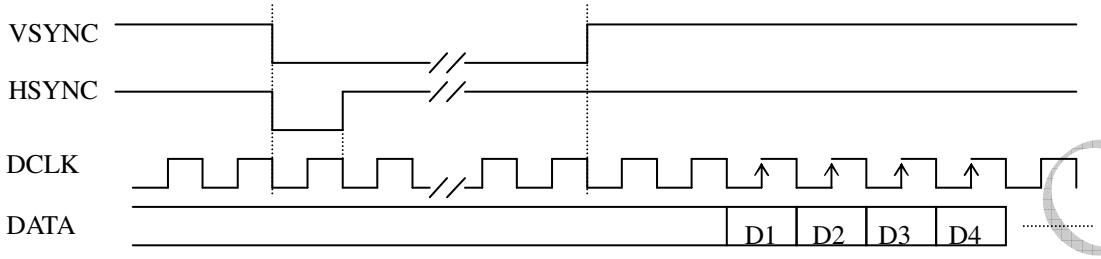
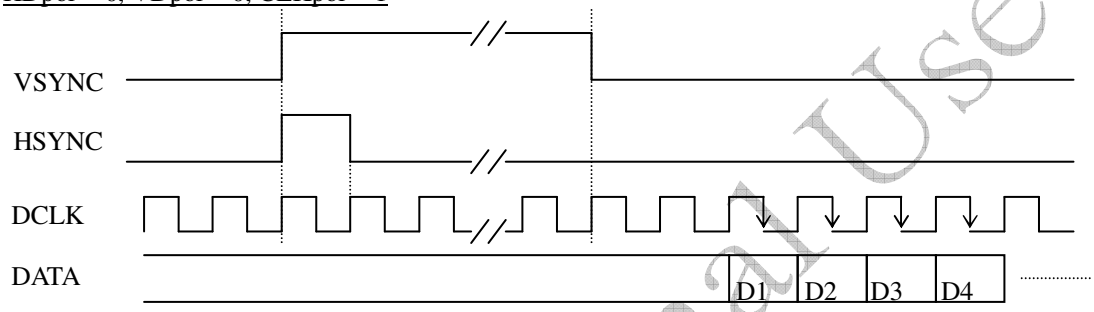
(20) VDpol: VSYNC polarity selection

VDpol	Function
0	Positive polarity
1	Negative polarity (Default)

HDpol = 1, VDpol = 1, CLKpol = 0



HDpol = 0, VDpol = 0, CLKpol = 1



(20) CSYNC: Separate SYNC or CSYNC input selection

CSYNC	Function
0	CSYNC input
1	Separate SYNC input (Default)

When CSYNC ='0', CSYNC input from HSYNC pin

(21) PAIR : Vertical start time of Odd / Even Frame

For RGB666 input mode (ParaSeri = "Low")

PAIR(1:0)		VBLK	Unit
		ODD/EVEN	
X	0	21/21 (Default)	H
X	1	20/20	

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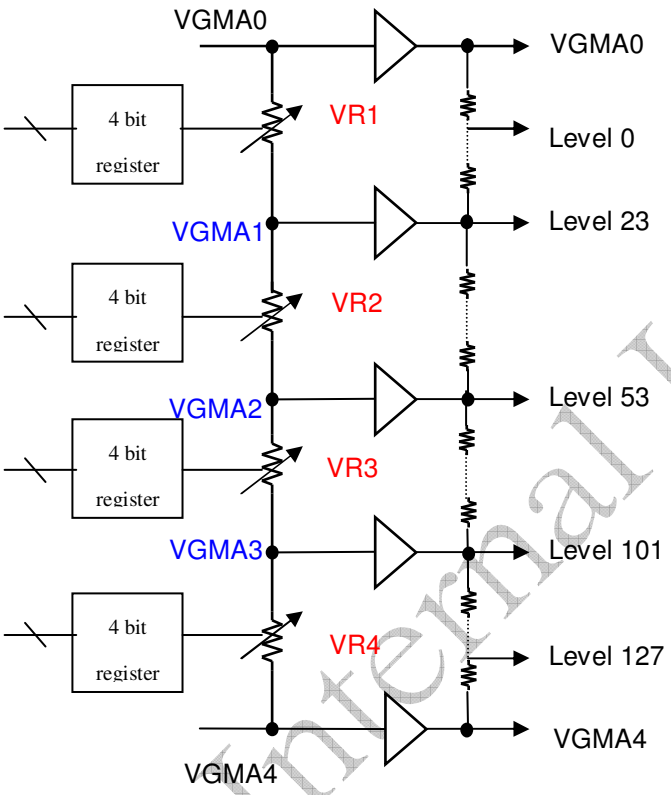
(22) Gamma_VR1, Gamma_VR2, Gamma_VR3, Gamma_VR4: resistor range 8K(0000)~23K(1111)

(MSB-LSB)	Function
0000	8K
1000	16K (Default)
1111	23K

Note: please see the detail description on the next page.



1. VGMA1, VGMA2, VGMA3 are generated within driver IC and adjustable through serial register setting
2. VR1, VR2, VR3, VR4 are adjustable through 4 bit registers
3. When FRP = L (Positive Polarity) VGMA0 = 3.7V, VGMA4 = 0V
4. When FRP = H (Negative Polarity) VGMA0 = 0V, VGMA4 = 3.7V

(22) CONTRAST: RGB Contrast level setting, the gain changes (1/64)/bit

(MSB-LSB)	Function
00h	0
40h	1 (Default)
FFh	3.984

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(23) SUB-CONTRAST: RB sub-contrast level setting, the gain changes (1/256) / bit

(MSB-LSB)	Function
00h	0.75
40h	1 (Default)
7Fh	1.246

(24) SUB-BRIGHTNESS: RB sub-bright level setting, setting accuracy: 1 step / bit

(MSB-LSB)	Function
00h	Dark (-64)
40h	Center (0) (Default)
7Fh	Bright (+63)

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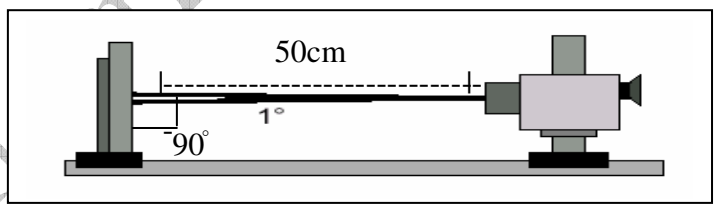
C. Optical specifications (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time Rise Fall	 Tr Tf	 θ =0°	 - -	 15 20	 25 30	 ms ms	Note 4
Contrast ratio	CR	At optimized viewing angle	200	300	-		Note 5,6
Viewing angle Top Bottom Left Right		CR≧10	 10 60 40 40	 20 70 50 50	 - - - -	deg.	Note 7
Brightness	Y_L	θ =0°	180	230	-	cd/m^2	Note 8
White chromaticity	X	θ =0°	0.28	0.33	0.38		
	y	θ =0°	0.30	0.35	0.40		
Luminance Uniformity			60			%	Note 9

Note 1. Ambient temperature =25℃. And backlight current I_L=20 mA

Note 2. To be measured in the dark room.

Note 3. To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation, distance: 500± 50mm.



Note 4. Definition of response time: The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to

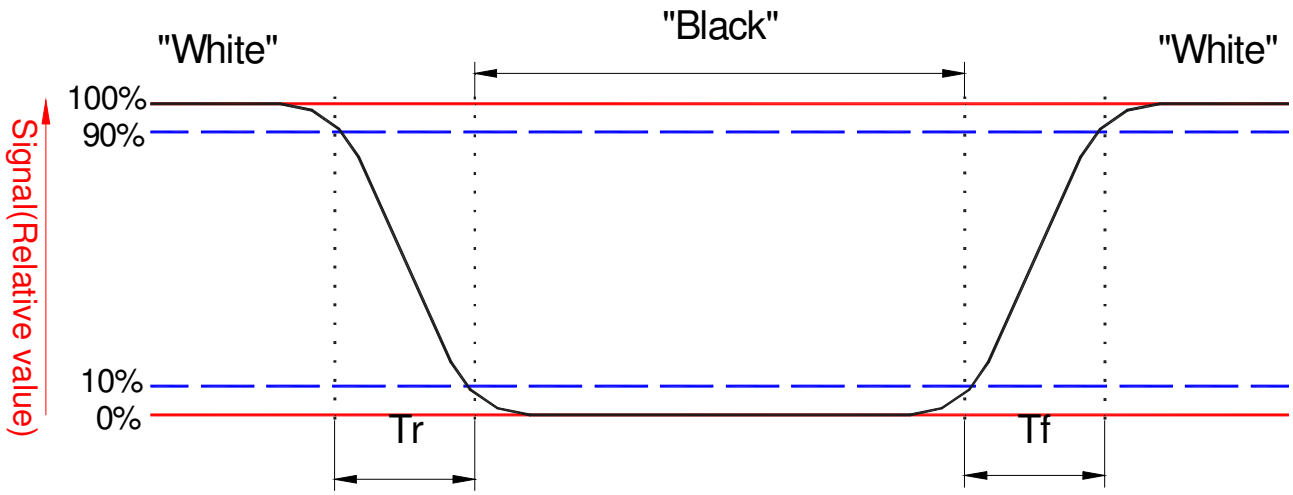


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figure as below.

Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \pm 1.5V$

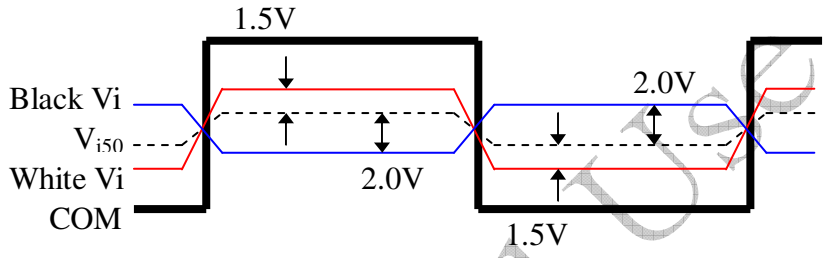
Black $Vi=V_{i50} \mp 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

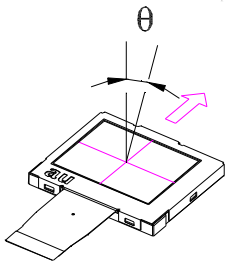
“∓” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.



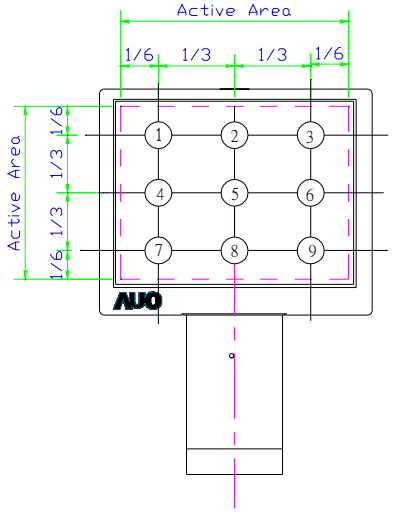
Note 7. Definition of viewing angle:



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Definition of luminance uniformity

$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine point}}{\text{Max. Brightness of nine point}}$$



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D. Reliability test items

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80℃ 240Hrs	
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~80℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient temperature.

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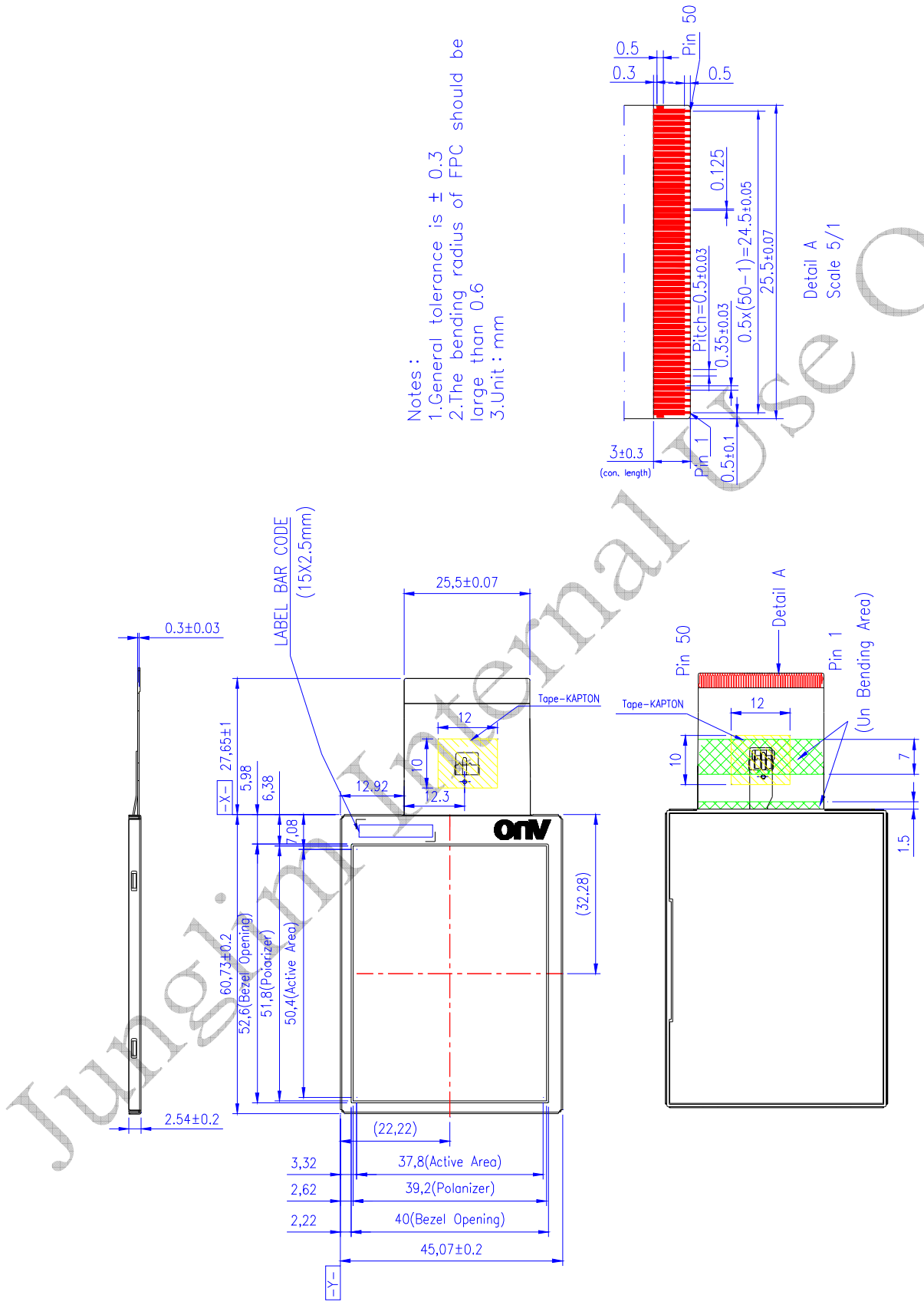
E. Outline dimension



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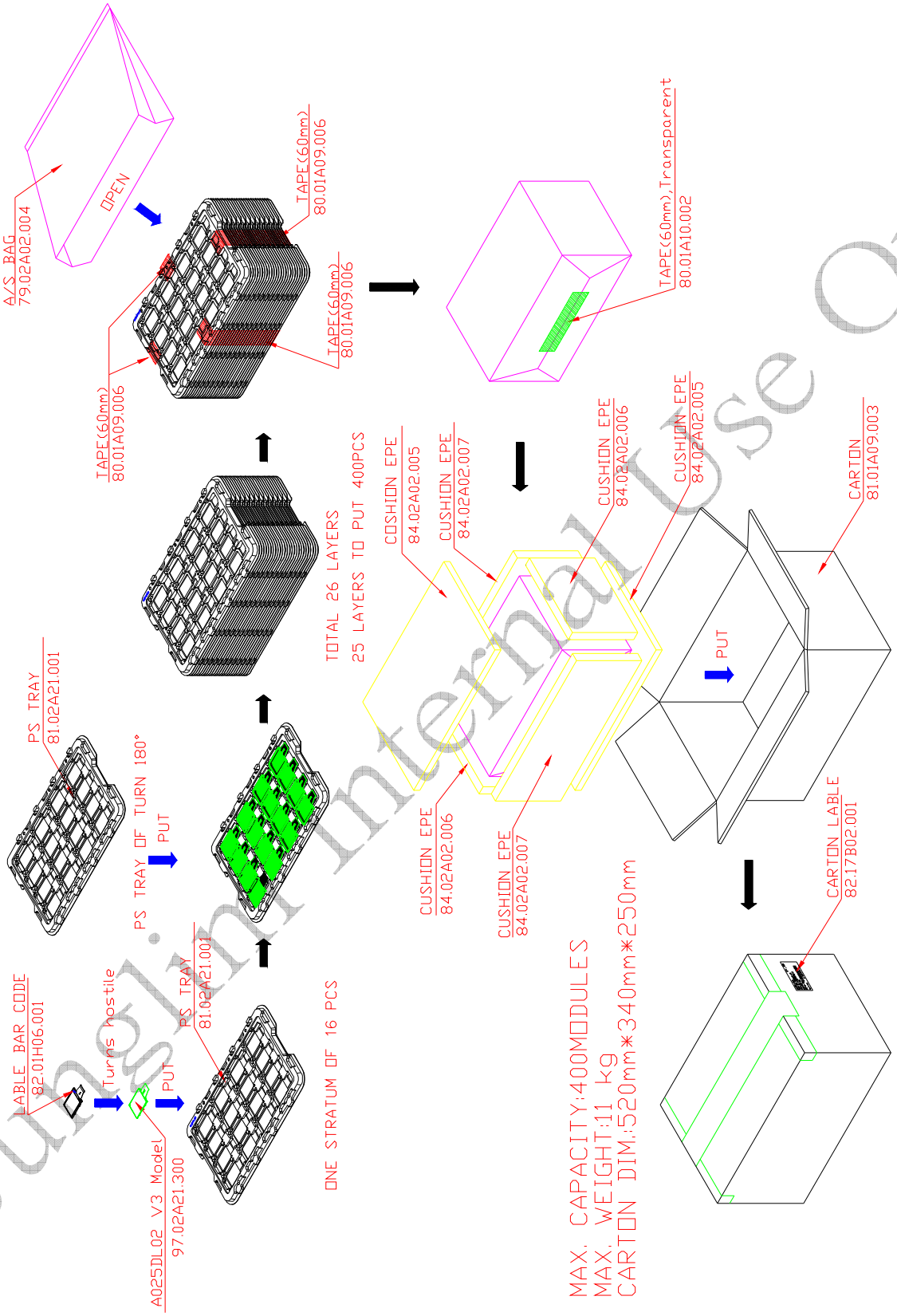
F. Packing form



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G. Application Notes

This LTPS TFT LCD module is designed for digital still camera application. A COG type LCD driver IC is integrated within this module, makes it much easier to design and cost-effective. The main features of integrated driver are:

- Accepting digital R, G, B 6-bit signal, fewer adjustment, fewer design effort, and lower power consumption compared to other analog LTPS solution.
- Integrated timing controller for RGB666 input timing formats. For RGB666 input timing, the input signal is always the same for different panel resolution.
- Integrated LED power converter controller, DC-DC charge pump, and Vcom driver. A design requires less peripheral components and reduces the total system cost.

1. Input Data Timing

In RGB666 input format, the mapping of incoming data to display dots is take cared by built in scaling function of driver IC.

There are only one input RGB data mode: 320xRGBx240. Input data is processed and mapped to display dots by integrated driver IC according to panel resolution and scan direction settings. RGB666 input format saves the effort of data scaling for users and keeps a consistent interface for different display resolutions, in the cost of higher input data rate and less image processing elasticity.

For vertical input timing, RGB666 accept odd / even field switching or single field only input. For detail timing spec., please refer to Fig 2.

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2. Typical Application Circuit

a. Internal LED booster circuit

The integrated driver IC provides build-in LED booster controller, DC-DC charge pump, and Vcom driver. See Fig. 6 for the application circuit.

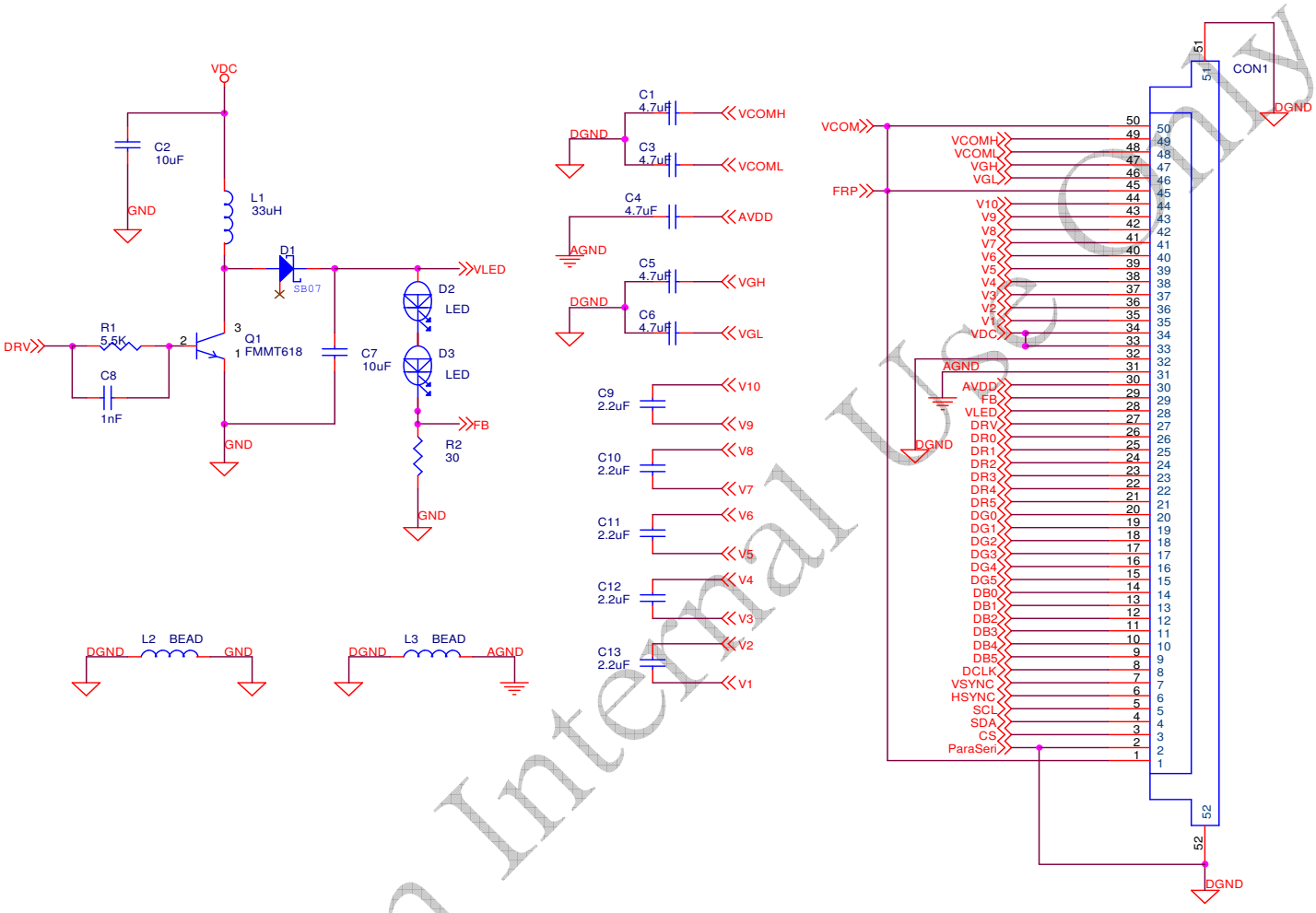

Fig. 6 Typical Application Circuit

<Note> : The charge pump frequency is about 7~8KHz, which can be heard by human. To prevent this signal from being amplified by microphone or other audio recoder, C9~C13 are suggested to be kept as far away as possible from these devices.

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b. External LED driver circuit

See Fig. 7 for the application circuit.

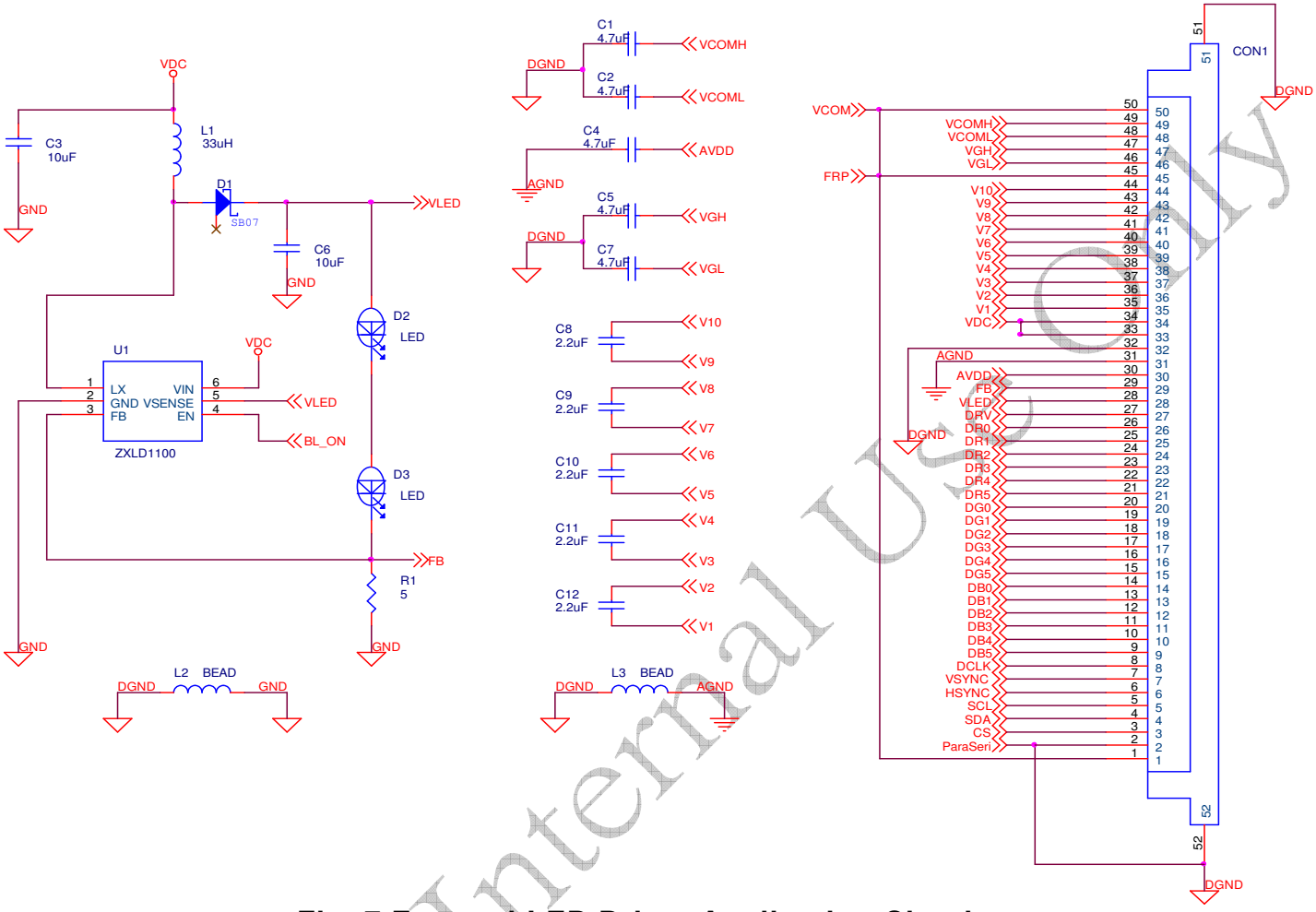

Fig. 7 External LED Driver Application Circuit

Single power VDC (Typical 3.3V) is required to provide driver IC power and generate all necessary voltages for LCD related circuits.

According to Fig. 7, the LED driver(ZXLD1100) and R1(5 ohm) with 0.1V feedback (FB) can provide a constant 20mA current for LED backlight unit. To control the back light on/off timing, user should create a control signal BL_ON (please refer to the ZXLD1100 date sheet). The LCD driver output DRV signal can also be used to drive BL_ON.

<Note> : The charge pump frequency is about 7~8KHz, which can be heard by human. To prevent this signal from being amplified by microphone or other audio recorder, C8~C12 are suggested to be kept as far away as possible from these devices.

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3. Power ON/OFF Sequence

The register setting of standby mode disabling / enabling is used to control the build-in power on / off sequence.

a. Power On (Global Reset and Standby Disabling)

After V_{DC} power on reset, VSYNC/HSYNC/DCLK/DATA can be input, and serial control interface is also operational. To ensure that panel can be lighted on successfully, the first step is setting global reset (register #5 "16(hex)") as the timing in Fig. 9. Then the LCD driver is in default standby mode after V_{DC} power-on, and setting register #5 bit #0 to high (STB=1) to disable the standby mode is required for normal operation. When the standby mode is disabled, a build-in power on sequence is started. The driver IC analog power AVDD is turned on first, and then the LCD positive and negative power supplies VGH/VGL are pumped, and followed by the LED power VLED. Since we recommend using external LED driver, the BL_ON signal (see Fig.8) should be provided at this time. Please refer to Fig.8 and Fig. 9 for the detail timing of power on/off sequence, especially the global reset timing in Fig. 9.

b. Power Off (Standby Enabling)

When the register #5 bit #0 is set to low (STB=0) to enable standby mode, a build-in power off sequence is started. Please refer to Fig.8 for the detail timing. No serial command programming is allowed right after standby mode is enabled, for a time period of minimum 5 fields.

c. Clock Stop Reset

The DCLK signal is required for normal operation. When the DCLK is stopped for more than 5.6μsec (or DCLK frequency < 140KHz) during normal operation, the driver IC will be reset and operated in standby mode. This DCLK stop reset does not affect the serial interface settings.

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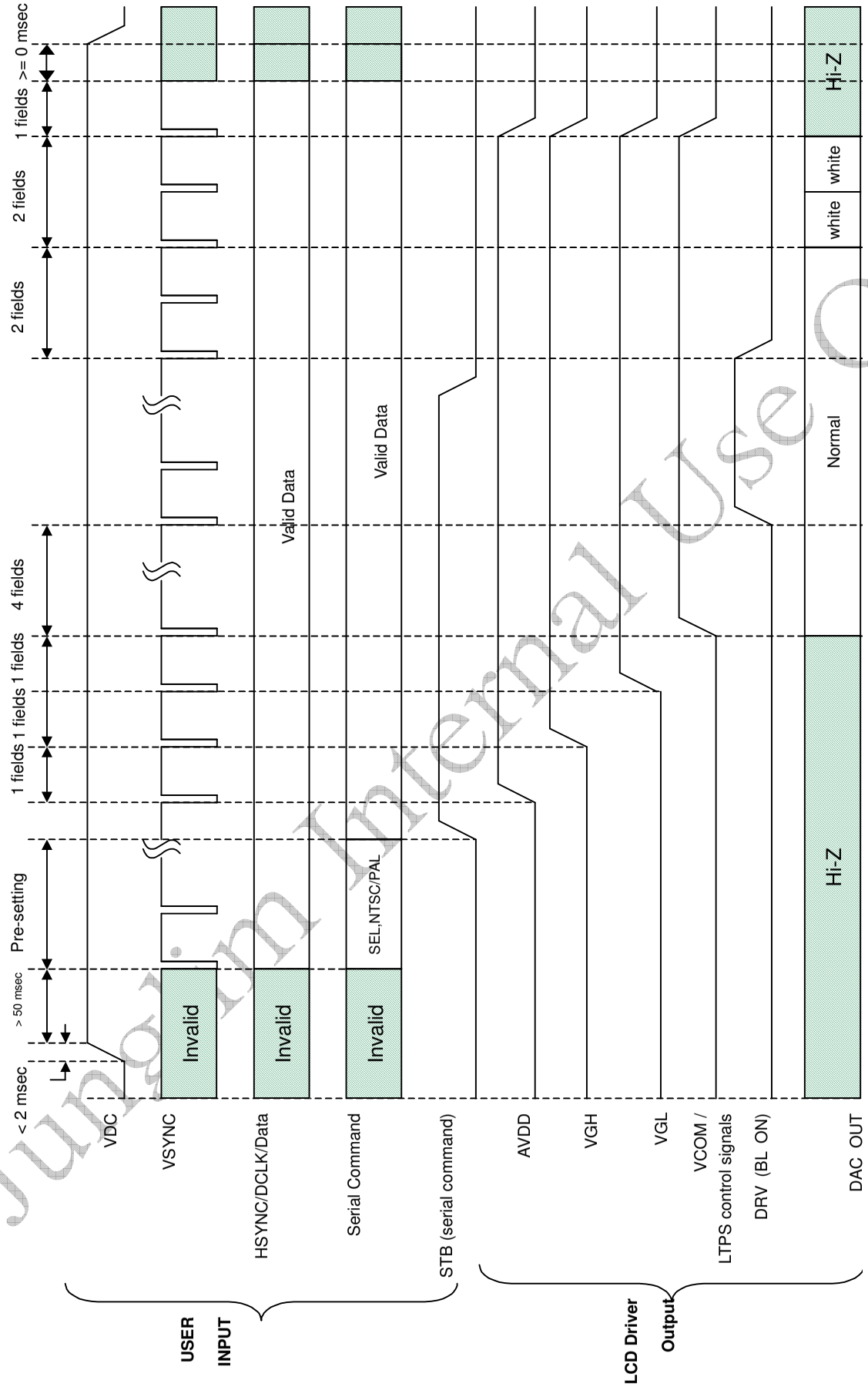

Fig. 8 Power ON / OFF Sequence

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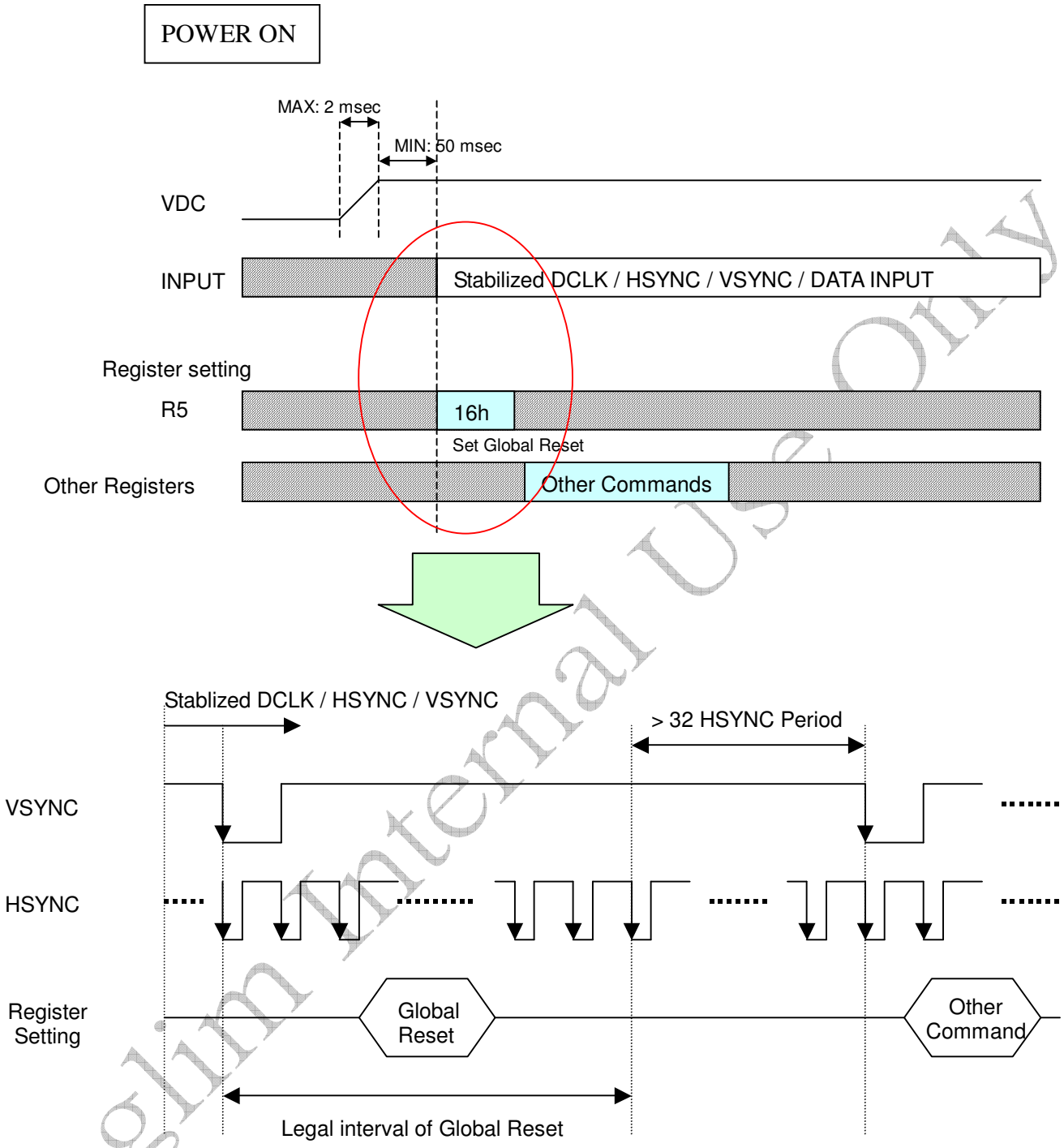

Fig. 9 Valid Timing of Global Reset

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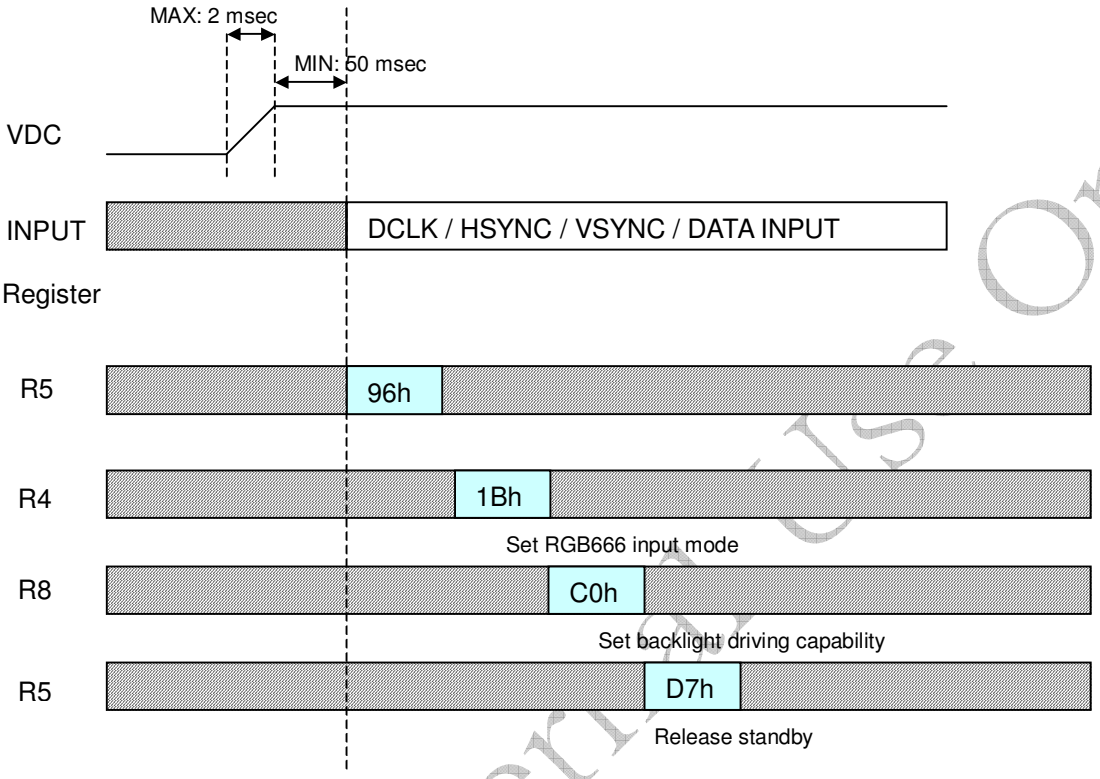
POWER ON



POWER OFF

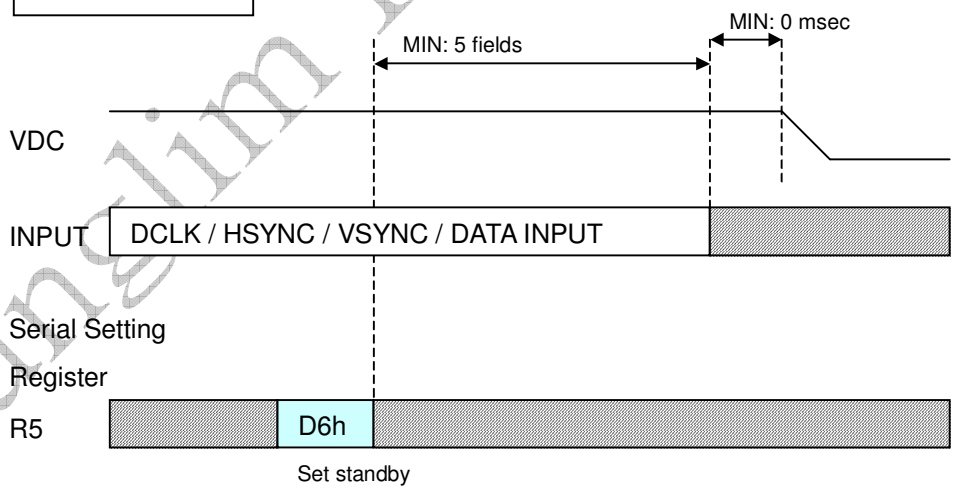


Fig. 10 Recommend serial command settings

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