CUSTOMER APPROVAL SHEET

Company Name

MODEL A027DW01 V1

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- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver.___)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.___)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.___)**
- ☐ **CUSTOMER REMARK :**

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Product Specification

2.7”COLOR TFT-LCD MODULE

Model Name： A027DW01 V1

Planned Lifetime:	From 2009/July. To 2010/July
Phase-out Control:	From 2010/July. To 2011/Jan.
EOL Schedule:	2011/Jan.

< > Preliminary Specification

< ◆ > Final Specification

Note: The content of this specification is subject to change without prior notice.

Record of Revision

Version	Revise Date	Page	Content
0.0	2009/07/27	-	First draft
0.1	2009/08/25	8	Modify I_{PVDD} and I_{IO} current value.
		20	Add R0 register bit1 and R10 register.
		21	Add R0 register bit1.
		23	Modify R4 bit2.
		25	Add R10 register.
		27~30	Update application circuit.
		38	Modify backlight drawing on time.
		40~42	Update power on serial command settings.
0.2	2009/10/20	32	Update the RGB color coordinate
		38	Update the Module outline drawing

Contents

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution（dot）	960(W) x 240(H)	
2	Active area（mm）	57.84 x 34.20	
3	Screen size（inch）	2.7 (Diagonal)	
4	Dot pitch（um）	60.25x142.5	
5	Color configuration	R, G, B delta	
6	Overall dimension（mm）	64.14 x 44.05 x 2.6	Note 1
7	Weight（g）	16	
8	Panel surface treatment	Hard Coating	

Note 1: Refer to F. Outline Dimension

B. Electrical specifications

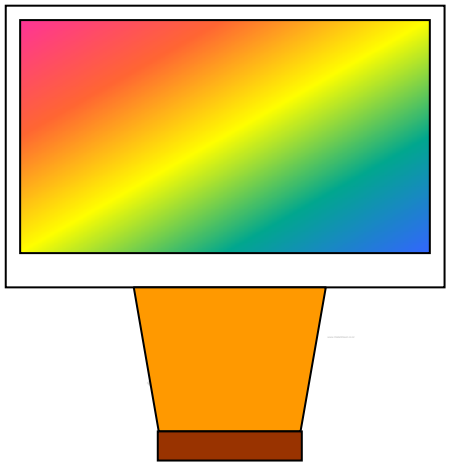
1. Pin assignment

Pin no	Symbol	I/O	Description	Remark
1	VCOM	I	VCOM	
2	VGL	C	Capacitor of charge pumping circuit	
3	VGH	C	Capacitor of charge pumping circuit	
4	C3P	C	Capacitor of charge pumping circuit	
5	C3M	C	Capacitor of charge pumping circuit	
6	V_10	C	Capacitor of charge pumping circuit	
7	V_5	C	Capacitor of charge pumping circuit	
8	VINT2	C	Capacitor of charge pumping circuit	
9	C2P	C	Capacitor of charge pumping circuit	
10	C2M	C	Capacitor of charge pumping circuit	
11	VCAC	C	Capacitor of VCOMAC circuity	
12	FRP	O	Frame polarity	
13	VINT1	C	Capacitor of charge pumping circuit	
14	C1BP	C	Capacitor of charge pumping circuit	
15	C1AP	C	Capacitor of charge pumping circuit	
16	C1BM	C	Capacitor of charge pumping circuit	
17	C1AM	C	Capacitor of charge pumping circuit	
18	GND	G	Ground	
19	PVDD	PI	Analog power input, 3.0~3.6V is recommended.	
20	GMA_H	C	Stabilizing capacitor for analog power	
21	VLED-	I	LED back light cathode	
22	VLED+	I	LED back light anode	
23	DRV	O	Gate signal for the power transistor of the boost converter.	
24	GND	G	Ground	
25	VCC	C	Digital power supply	
26	VIO	PI	Digital power input	
27	CS	I	Chip enable of serial interface	
28	SDA	IO	Serial data input and output of serial interface	
29	SCL	I	Clock of serial interface	
30	HSYNC	I	Horizontal synchronous signal	
31	VSYNC	I	Vertical synchronous signal	
32	DCLK	I	Dot clock	

33	DATA 7	I	Data of serial RGB input (MSB)	
34	DATA 6	I	Data of serial RGB input	
35	DATA 5	I	Data of serial RGB input	
36	DATA 4	I	Data of serial RGB input	
37	DATA 3	I	Data of serial RGB input	
38	DATA 2	I	Data of serial RGB input	
39	DATA 1	I	Data of serial RGB input	
40	DATA 0	I	Data of serial RGB input (LSB)	
41	VCOM	I	VCOM	

I：Input, O：Output, C：Capacitor, P：Power, D：Dummy

Note: Definition of scanning direction, Refer to figure as below：



2. Electrical characteristics

2.1 Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Analog Power Supply	PVDD	AGND=GND=0V	-0.5	7	V	
Digital Power Supply	VIO	AGND=GND=0V	-0.5	7	V	
Storage Temperature	Tstg	-	-55	100	℃	Ambient temperature
Operating Temperature	Topa	-	-30	85	℃	Ambient temperature

2.2 Recommended operating conditions (GND =0V)

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Analog Power Supply		PVDD	3.0	3.3	3.6	V	Note 1
Digital Power Supply		VIO	1.7	3.3	3.6	V	Note 1
Input Signal voltage	H Level	V_{IH}	0.7* VIO		VIO	V	
	L Level	V_{IL}	GND		0.3* VIO	V	

Note 1: A build-in power on reset circuit for PVDD and VIO is provided within the integrated LCD driver IC. The LCD module is in power save mode in default, and a standby releasing is required after VIO power on through serial control. Please refer to the register STB setting for detail.

2.3 Electrical characteristics (GND=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Input Current for V_{PVDD}	I_{PVDD}	V_{PVDD}=3.3V	-	8.5	10.5	mA	Note 1
	$I_{PVDD\ (STANDBY)}$		-	2.1	3	uA	Note 1
Input Current for V_{IO}	I_{IO}	V_{IO}=3.3V	-	80	100	uA	Note 1
	$I_{IO(STANDBY)}$		-	50	70	uA	Note 1
DC-DC voltage	V_{GH}	V_{PVDD}=3.3V	14.0	15.0	16.0	V	Note 2
	V_{GL}	V_{PVDD}=3.3V	-11.0	-10.0	-9.0	V	Note 2
VCOM voltage	V_{CAC}	-	3.5	4.2	5.0	Vp-p	AC component, Note 3
	V_{CDC}	-	0.52	0.62	0.72	V	DC component, Note 4

Note 1: Use UPS051 mode, PVDD=VIO=3.3V, and F_{DCLK}=27MHz,.other registers are default setting.

Note 2: VGH and VGL are output voltages of integrated LCD driver IC.

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: VCDC could be adjusted, so as to minimize flicker and maximum contrast on each module.

2.4 Recommended Capacitance Values of External Capacitor

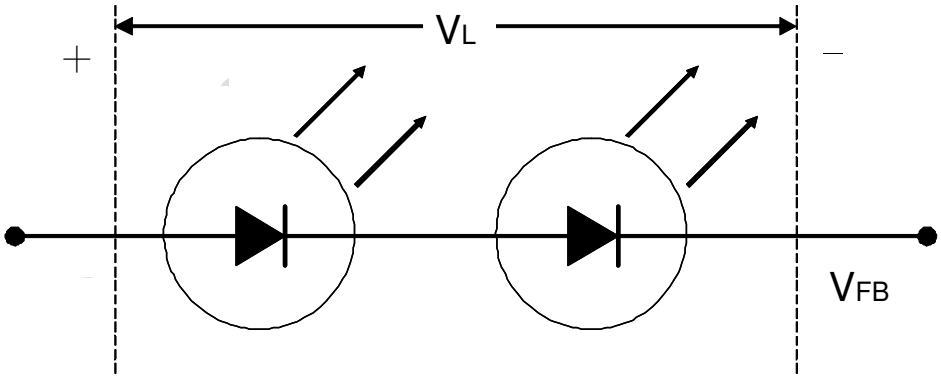
The recommended capacitance values of the external capacitor are shown below. These values should be finally determined only after performing sufficient evaluation on the module.

Pin name	Recommended value of capacitors (μF)	Withstanding voltage (V)
VGH	1 to 10	25
VGL	1 to 10	16
V_10	2.2 to 10	16
V_5	2.2 to 10	10
Vint2	2.2 to 10	16
Vint1	2.2 to 10	10
VCAC	1 to 10	10

2.5 Backlight driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current			25	27.5	mA	
LED voltage	V_L		6.5	7	V	2 LED's
Feedback voltage	V_{FB}	-	0.6	-	V	

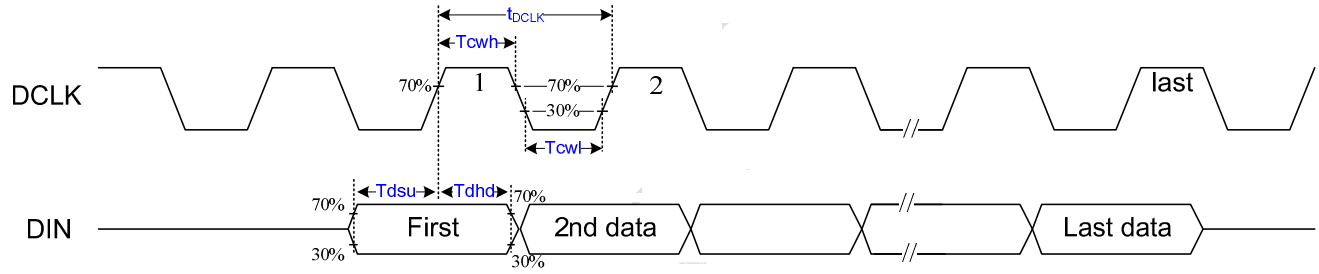
Note1: To consider Backlight driver and feedback resistor tolerance.

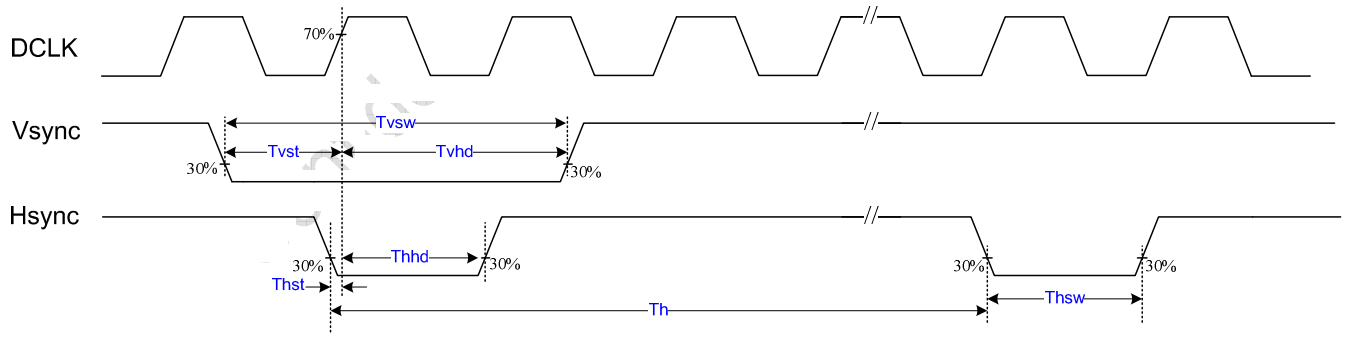


3. Input timing AC characteristic

3.1 Digital Signal AC Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit.
DCLK duty cycle	Tcwh/Tcwl	40	50	60	% t_{DCLK}
VSYNC setup time	Tvst	12	-	-	ns
VSYNC hold time	Tvhd	12	-	-	ns
HSYNC setup time	Thst	12	-	-	ns
HSYNC hold time	Thhd	12	-	-	ns
Data set-up time	Tdsu	12	-	-	ns
Data hold time	Tdhd	12	-	-	ns
HSYNC width	Thsw	1	1	254	t_{DCLK}
VSYNC width	Tvsw	1 t_{DCLK}	1 t_{DCLK}	6t	





3.2 UPS051 Timing conditions

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	13.5	27	27.19	MHz	
Hsync	Period		t_H	1024	1716	1728	t_{DCLK}	Note 1
	Display period		t_{hd}	960			t_{DCLK}	
	Back porch		t_{hbp}	57	70	255	t_{DCLK}	
	Front porch		t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	255.5	262.5	277.5	t	Note 2, 3, 4
		Even						
	Display period	Odd	t_{vd}	240			t	
		Even						
	Back porch	Odd	t_{vbp}	14	21	29	t_H	
		Even		14.5	21.5	29.5		
	Front porch	Odd	t_{vfp}	t			t_H	
		Even						
	Pulse width	Odd	t_{vsw}	1	1	-	t_{DCLK}	
		Even						

Note 1: UPS051 Horizontal back porch time (t) is adjustable by setting register DDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 2: UPS051 Vertical back porch time (t) is adjustable by setting register HDL; requirement of minimum back porch time and minimum front porch time must be satisfied.

Note 3: Both interlace and non-interlace mode can be accepted.

Note 4: AUO suggests frame rate at least 50 Hz to get the better display quality.

Fig.1 UPS051 Input Horizontal Timing Chat

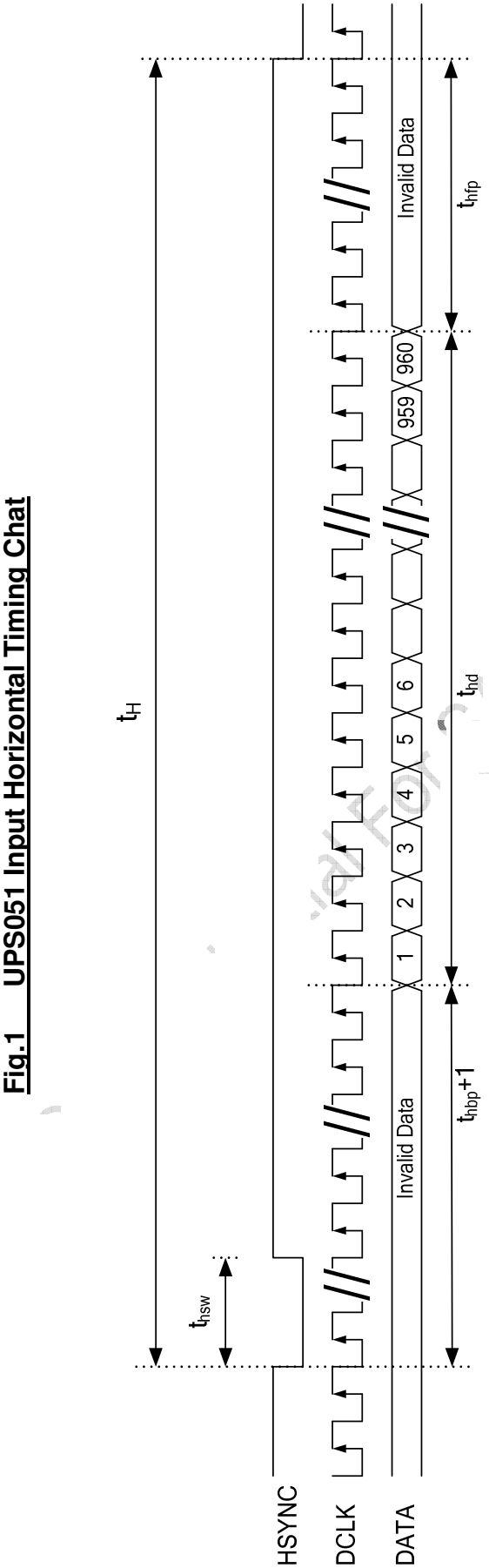


Fig.2 UPS051 Input Horizontal Data Sequence

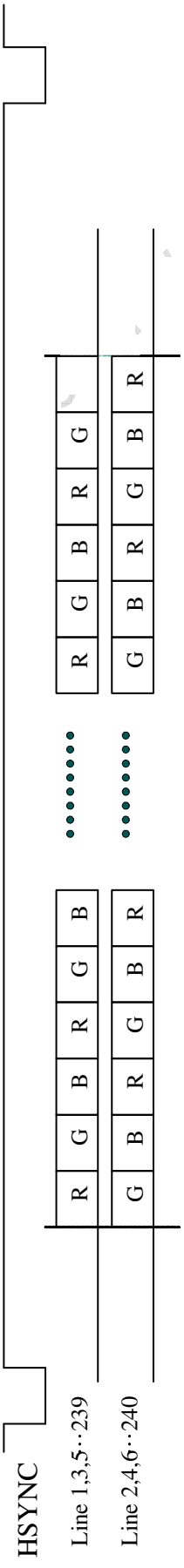
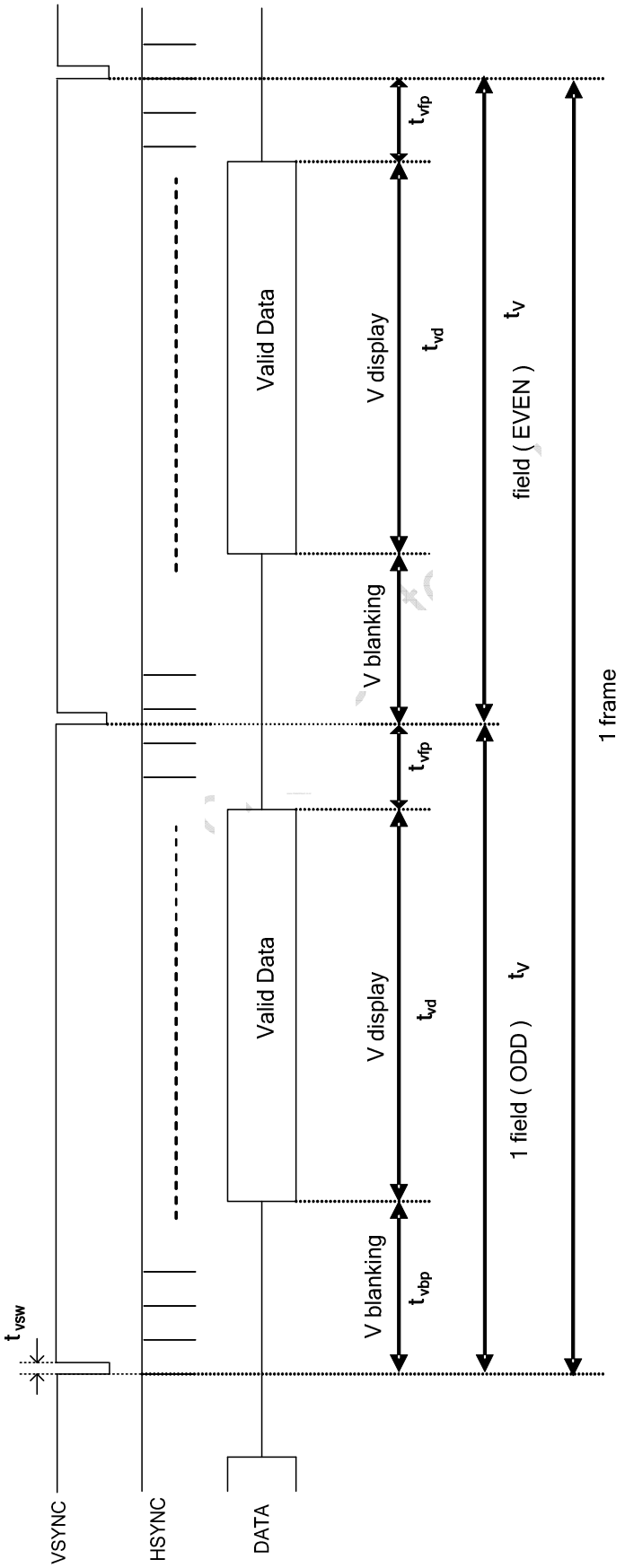


Fig.3 UPS051 Input Vertical Timing Chat



3.3 UPS052 Timing conditions

➢ 3.2.1 UPS052 (320 mode 24.54MHz) timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20	24.54	28	MHz	
Hsync	Period		t_H	1500	1560	1700	t_{DCLK}	
	Display period		t_{hd}	1280			t_{DCLK}	
	Back porch		t_{hbp}	64	241	319	t_{DCLK}	
	Front porch		t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	255.5	262.5	277.5	t	Note 1, 2
		Even						
	Display period	Odd	t_{vd}	240			t	
		Even						
	Back porch	Odd	t_{vbp}	14	21	29	t_H	
		Even		14.5	21.5	29.5		
	Front porch	Odd	t_{vfp}	$t_{vd} - t_{vbp}$			t_H	
		Even						
	Pulse width	Odd		1	1	-	t_{DCLK}	
		Even						

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

➢ 3.2.2 UPS052 (360 mode 27MHz) timing specifications

Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK Frequency			$1/t_{DCLK}$	20	27	28	MHz	
Hsync	Period		t_H	1660	1716	1900	t_{DCLK}	
	Display period		t_{hd}	1440			t_{DCLK}	
	Back porch		t_{hbp}	64	241	319	t_{DCLK}	
	Front porch		t_{hfp}	$t_H - t_{hd} - t_{hbp}$			t_{DCLK}	
	Pulse width		t_{hsw}	1	1	-	t_{DCLK}	
Vsync	Period	Odd	t_V	255.5	262.5	277.5	t_H	Note 1, 2
		Even						
	Display period	Odd	t_{vd}	240			t_H	
		Even						
	Back porch	Odd	t_{vbp}	14	21	29	t_H	
		Even		14.5	21.5	29.5		
	Front porch	Odd	t_{vfp}	$t_V - t_{vd} - t_{vbp}$			t_H	
		Even						
	Pulse width	Odd	t_{vsw}	1	1	-	t_{DCLK}	
		Even						

Note 1: AUO suggests frame rate at least 50 Hz to get the better display quality.

Note 2: Both interlace and non-interlace mode can be accepted.

Fig.4 UPS052 Input Horizontal Timing Chart

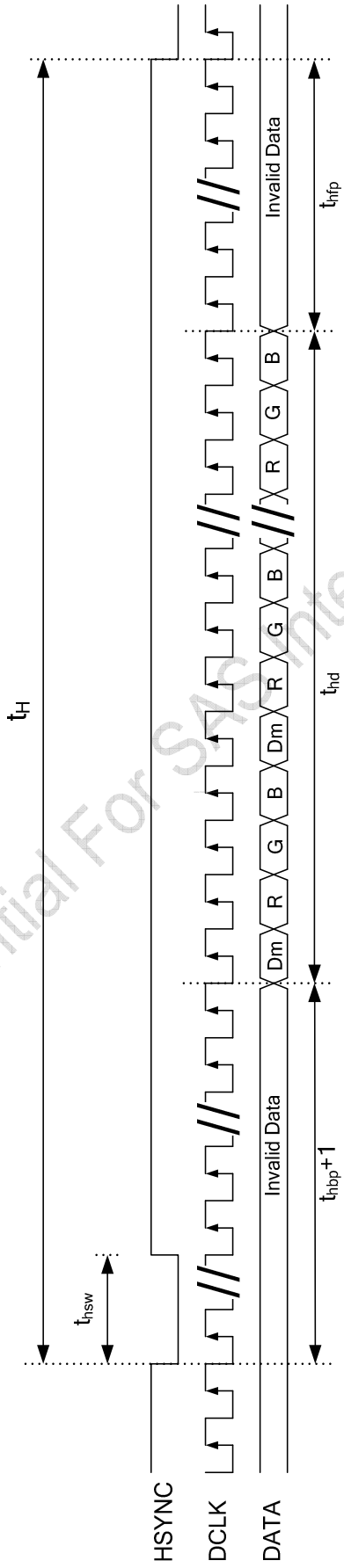
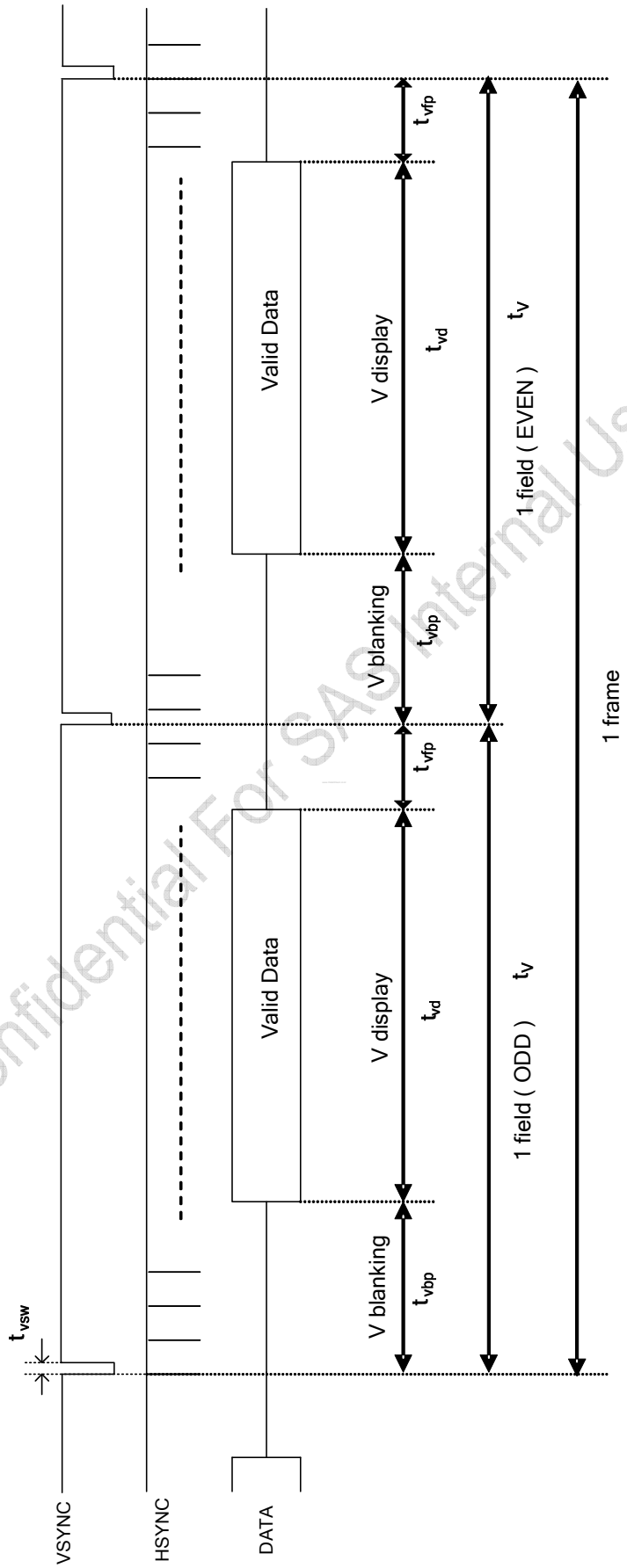


Fig.5 UPS052 Input Vertical Timing Chart



4. Command Register Map

4.1 Command Timing: Serial Peripheral Interface

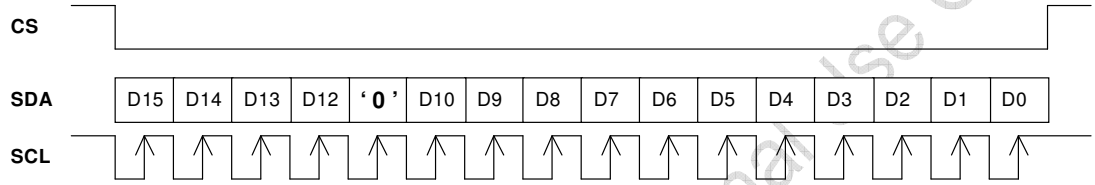
- **Configuration of serial data at SDA terminal**

MSB LSB

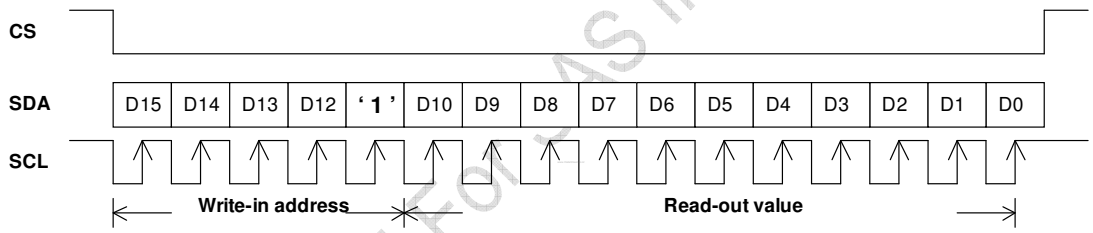
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address				R/W	DATA										

Note: R/W = '0' ➔ Write mode R/W = '1' ➔ Read mode

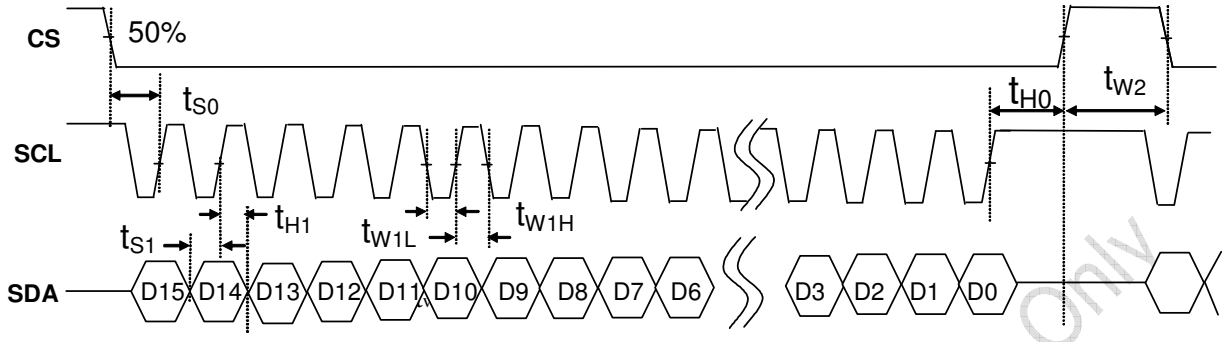
- **Write mode waveform**



- **Read mode waveform**



4.2 SPI timing diagram



Item	Symbol	Conditions	Min	Typical	Max	Unit
Data Setup Time	t_{S0}	SCL to CS	30			ns
	t_{S1}	SCL to SDA	30			ns
Data Hold Time	t_{H0}	SCL to CS	30			ns
	t_{H1}	SCL to SDA	30			ns
Pulse Width	t_{W1L}	SCL pulse width	30			ns
	t_{W1H}	SCL pulse width	30			ns
	t_{W2}	CS pulse width	500			ns

- Each serial command consists of 16 bits of data which is loaded one bit a time at the rising edge of serial clock SCL.
- Command loading operation starts from the falling edge of CS and is completed at the next rising edge of CS.
- The serial control block is operational after power on reset, but commands are established by the Vsync signal. If command is transferred multiple times for the same register, the last command before the Vsync signal is valid.
- If less than 16 bits of SCL are input while CS is low, the transferred data is ignored.
- If 16 bits or more of SCL are input while CS is low, the previous 5 bits of transferred data after the falling edge of CS pulse ,and the previous 11 bits of transferred data before the rising edge of CS pulse are valid data.
- Serial block operates with the SCL clock.
- Serial data can be accepted in the power save mode.

4.3 Serial Setting Map

Reg No	ADRESS				CONTENT											
	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	-	-	Reserved (00)		FPOL (0)	U/D (1)	SHL (1)	GRB (1)	STB (1)	SHDB (0)	SHCB (1)
R1	0	0	0	1	R/W	-	-	-	-	T051 (0)	Reserved (0)			SEL (001)		
R2	0	0	1	0	R/W	-	-	DDL_E (0)	DDL (46H)							
R3	0	0	1	1	R/W	-	-	-	-	-	Reserved (00)		HDL (7H)			
R4	0	1	0	0	R/W	-	-	-	-	AVG (1)	Reserved (010)			D/S (0)	DITH (1)	Reserved (0)
R5	0	1	0	1	R/W	-	-	-	-	-	-	-	CONTRAST (8H)			
R6	0	1	1	0	R/W	-	-	-	-	BRIGHTNESS (40H)						
R8	1	0	0	0	R/W	-	-	-	-	-	-	-	VCOM_AC (7H)			
R9	1	0	0	1	R/W	-	-	-	-	VDCE (1)	VCOM_DC (2DH)					
R10	1	0	1	0	R/W	-	-	-	-	DC_F (1)	CLK_Chp_M (10)		DC_MAX_DUTY (01)		DC_FB_LVL (10)	
R11	1	0	1	1	R/W	-	-	-	-	GMA_M (1)	GMA3_LVL (100)			GMA2_LVL (100)		
R12	1	1	0	0	R/W	-	-	-	-	-	GMA5_LVL (100)			GMA4_LVL (100)		
R13	1	1	0	1	R/W	-	-	-	-	-	GMA7_LVL (100)			GMA6_LVL (100)		

4.4 Description of serial control data

R0: System settings

Address	Bit	Description		Default
0000	[6..0]	Bit6(FPOL)	FRP source driver polarity inversion polarity inversion selection.	011_1101b
		Bit5(U/D)	Vertical shift direction selection.	
		Bit4(SHL)	Horizontal shift direction selection.	
		Bit3(GRB)	Global reset.	
		Bit2(STB)	Standby mode setting.	
		Bit1(SHDB)	DC-DC converter shutdown setting.	
		Bit0(SHCB)	Charge Pump shutdown setting.	

Bit6	FPOL function
0	Polarity between Source driver and VCOM follow Panel type. **(default)**
1	Polarity between Source driver and VCOM inverted from Panel type.

Bit5	UD function
0	Scan down: First line=G241 → G239 → … → G2 → Last line=G0.
1	Scan up: First line=G0→ G2 →…→ G239 → Last line=G241. **(default)**

Bit4	SHL function
0	Shift left; First data=S640 → S639 → …→ S2 → Last data=S1.
1	Shift right: First data=S1→ S2 → …→ S639→ Last data=S640. **(default)**

Bit3	GRB function
0	The controller is reset, the charge pump and DCDC are off. Reset all registers to default value.
1	Normal operation. **(default)**

Bit2	STB function
0	T-CON, source driver and DC-DC converter are off. All outputs are High-Z.
1	Normal operation. **(default)**

Bit1	SHDB function
0	DC-DC converter is off. **(default)**
1	DC-DC converter is on. DC-DC controlled by STB and power on/off sequence.

Bit0	SHCB function
0	Charge Pump converter is off.
1	Charge Pump converter is on. **(default)** Charge Pump controls by STB and power on/off sequence.

R1: Timings settings

Address	Bit	Description		Default
0001	[6..0]	Bit6(T051)	UPS051 output timing selection.	001_0001b
		Reserved	Reserved	
		Reserved	Reserved	
		Reserved	Reserved	
		Bit2-0(SEL)	Input data format selection.	

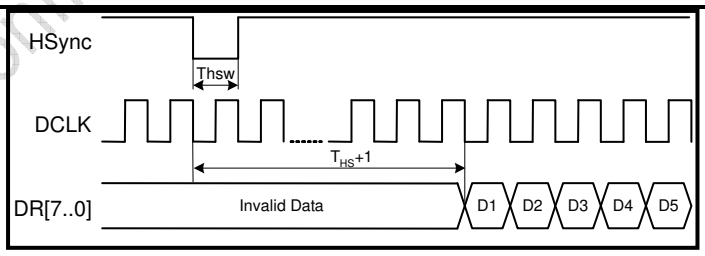
Bit6	T051 timing function
0	Use output timing for UPS051 based on DCLK 27 MHz frequency. **(default)**
1	Use output timing for UPS051 based on DCLK 13.5 MHz frequency

Bit2-0	SEL function
000	UPS051 mode.
001	UPS052 320 mode. **(default)**
010	UPS052 360 mode.

R2: Data delay settings

Address	Bit	Description		Default
0010	[8..0]	Bit8(DDL_E)	DDL setting selection.	0_0100_0110b
		Bit7-0(DDL)	Horizontal Data start delay selection.	

DDL_E	DDL	T_{HS}	Unit	Remark
X	00h	0	DCLK	UPS051
X	46h	70 (Default)	DCLK	
X	FFh	255	DCLK	
0	XXh	241(fixed)	DCLK	UPS052
1	00h~FFh	64~319	DCLK	



R3: Vertical delay settings

Address	Bit	Description		Default
0011	[3..0]	Bit3-0(HDL)	Vertical delay selection.	_0111b

Bit3-0	HDL function
0000	TSTV=TVStyp - 7 Hsync period
0111	TSTV=TVStyp - 0 Hsync period. **(default)**
1111	TSTV=TVStyp + 8 Hsync period

R4: Data settings

Address	Bit	Description		Default
0100	[6.0]	Bit6(AVG)	Dots average function	101_0011b
		Reserved	Reserved	
		Bit2(D/S)	Delta/Stripe matrix selection.	
		Bit1(DITH)	Dithering algorithm selection.	
		Reserved	Reserved	

Bit6	AVG function
0	Data alignment with orginal input data (R1, G1, B2…).
1	Data alignment with averaged input data (R1, (G1+3G2)/4, (3B2+B3)/4…). **(default)**

Bit2	D/S function
0	UPS051 mode. **(default)**
1	UPS052 mode.

*Note: Bit2 is “0”: Stripe mode. Bit2 is “1”: Delta mode.

Bit1	DITH function
0	Dithering off. 6-bit resolution (last 2 bits of input data truncated).
1	Dithering on. 8-bit resolution. **(default)**

R5: Contrast setting

Address	Bit	Description		Default
0101	[3..0]	Bit3-0(CONTRAST)	RGB contrast level adjustment. The contrast gain step is 0.125/LSB.	_1000b

Bit3-0	Contrast gain
0000	0
1000	1 **(default)**
1111	1.875

R6: Brightness settings

Address	Bit	Description		Default
0110	[6..0]	Bit6-0(BRIGHT)	Brightness level adjustment. The Brightness level step is 4/LSB.	100_0000b

Bit6-0	Brightness level
00h	-256
40h	0 **(default)**
7Fh	+252

*Display data= (RGB data) x CONTRAST + BRIGHT

R8: VCOM AC settings

Address	Bit	Description		Default
1000	[3..0]	Bit3-0(VCOM_AC)	VCAC level adjustment. Step 0.1V/LSB.	_0111b

Bit3-0	VCAC level
0000	3.6V
0111	4.2V **(default)**
1111	5.0V

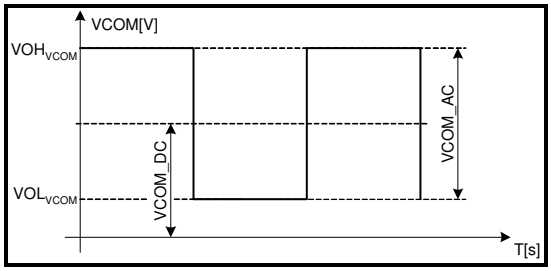
R9: VCOM DC settings

Address	Bit	Description		Default
1001	[6..0]	Bit6(VDCE)	VCOM DC Enable signal.	110_1101b
		Bit5-0(VCOM_DC)	VCOM DC level adjustment. Step 20mV/LSB.	

Bit6	VDCE function
0	VCOM DC function disables VCOM pin HighZ. VCOM_DC=VCOM_AC/2.
1	DC voltage of VCOM follows VCOM_DC settings.**(default)**

Bit5-0	VCOM DC level
00h	0.4V
0Bh	0.62V
2Dh	1.30V **(default)**
3Fh	1.66V

VOL_{VCOM}= VCOM_DC-VCOM_AC/2
VOH_{VCOM}= VCOM_DC+VCOM_AC/2



VCOM AC DC level definition

R10: Power supply settings

Address	Bit	Description		Default
1010	[6..0]	Bit6(DC_F)	DCDC frequency selection.	110_0110b
		Bit5-4(CLK_Chp_M)	Charge pump frequency selection.	
		Bit3-2(DC_MAX_DUTY)	DCDC maximum duty cycle selection.	
		Bit1-0(DC_FB_LEVEL)	DCDC feedback level adjustment.	

Bit6	DC_F function
0	DCDC operation based on 13.5MHz fDCDC = DCLK/32.
1	DCDC operation based on 27MHz fDCDC = DCLK/64. **(default)**

Bit5-4	CLK_Chp_M
00	F(Chp) = f(Hsync)/2
01	F(Chp) = f(Hsync)
10	F(Chp) = f(Hsync)*2 **(default)**
11	F(Chp) = f(Hsync)*4

Bit3-2	DC_MAX_DUTY
00	DCDC Max Duty = 68%.
01	DCDC Max Duty = 75%. **(default)**
10	DCDC Max Duty = 81%.
11	DCDC Max Duty = 88%.

Bit1-0	DC_FB_ LEVEL
00	0.3V
01	0.45V
10	0.6V **(default)**
11	0.75V

R11: Gamma settings 1

Address	Bit	Description		Default
1011	[6..0]	Bit6(GMA_M)	Gamma adjustment selection	110_0100b
		Bit5-3(GMA3_LVL)	GMA3 voltage adjustment	
		Bit2-0(GMA2_LVL)	GMA2 voltage adjustment t	

Bit6	GMA_M function
0	Manual set gamma by R11~R13.
1	Auto set to gamma 2.2 by LC type. **(default)**

R12: Gamma settings 2

Address	Bit	Description		Default
1100	[5..0]	Bit5-3(GMA5_LVL)	GMA5 voltage adjustment	10_0100b
		Bit2-0(GMA4_LVL)	GMA4 voltage adjustment t	

R13: Gamma settings 3

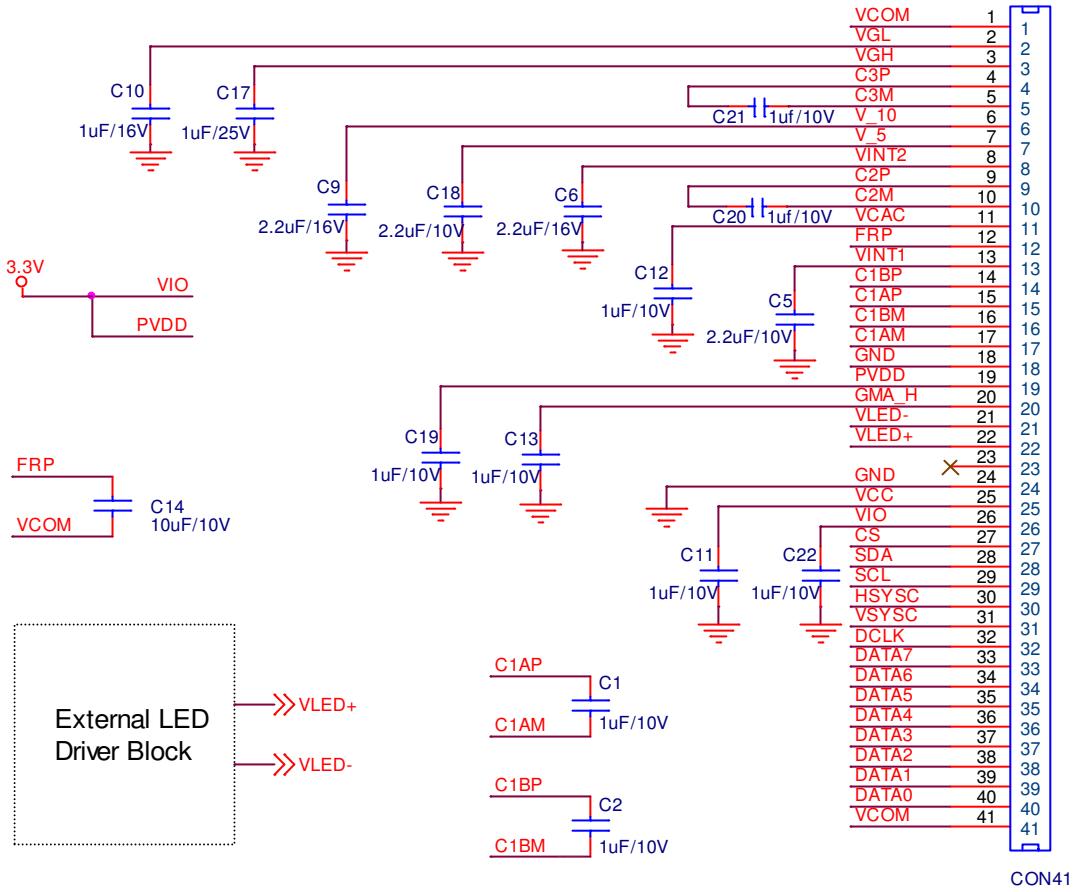
Address	Bit	Description		Default
1101	[5..0]	Bit5-3(GMA7_LVL)	GMA7 voltage adjustment	10_0100b
		Bit2-0(GMA6_LVL)	GMA6 voltage adjustment t	

	Reg	x00	x01	x10	x11
COM=L(1)	V0+	2.500			
	V8+	1.850	2.000	2.200	2.250
	V16+	1.570	1.700	2.000	2.050
	V50+	0.860	0.950	1.100	1.150
	V72+	0.680	0.840	0.900	0.970
	V110+	0.330	0.380	0.550	0.630
	V120+	0.150	0.180	0.330	0.400
	V127+	0.100			

	Reg	x00	x01	x10	x11
COM=H(1)	V0-	0.100			
	V8-	0.750	0.750	0.750	0.750
	V16-	1.030	1.030	1.030	1.030
	V50-	1.740	1.740	1.740	1.740
	V72-	1.920	1.920	1.920	1.920
	V110-	2.270	2.270	2.270	2.270
	V120-	2.450	2.450	2.450	2.450
	V127-	2.500			

5. Reference Circuit

➢ Internal VCOMDC + external LED driver application circuit

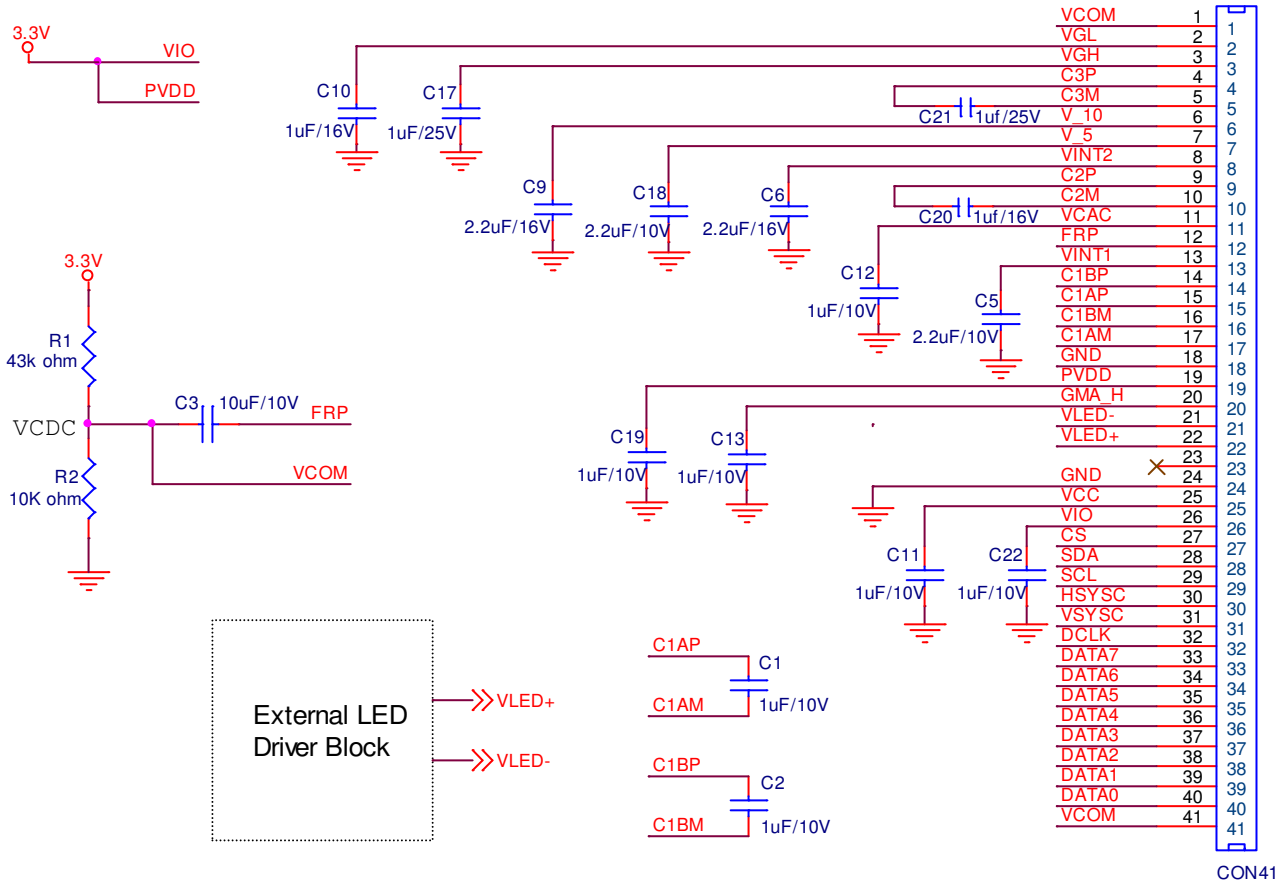


Note: (1) 3.3V is provided from system.

(2) External LED Driver Block is designed by customer.

(3) Use internal VCOMDC would make power on time too long.

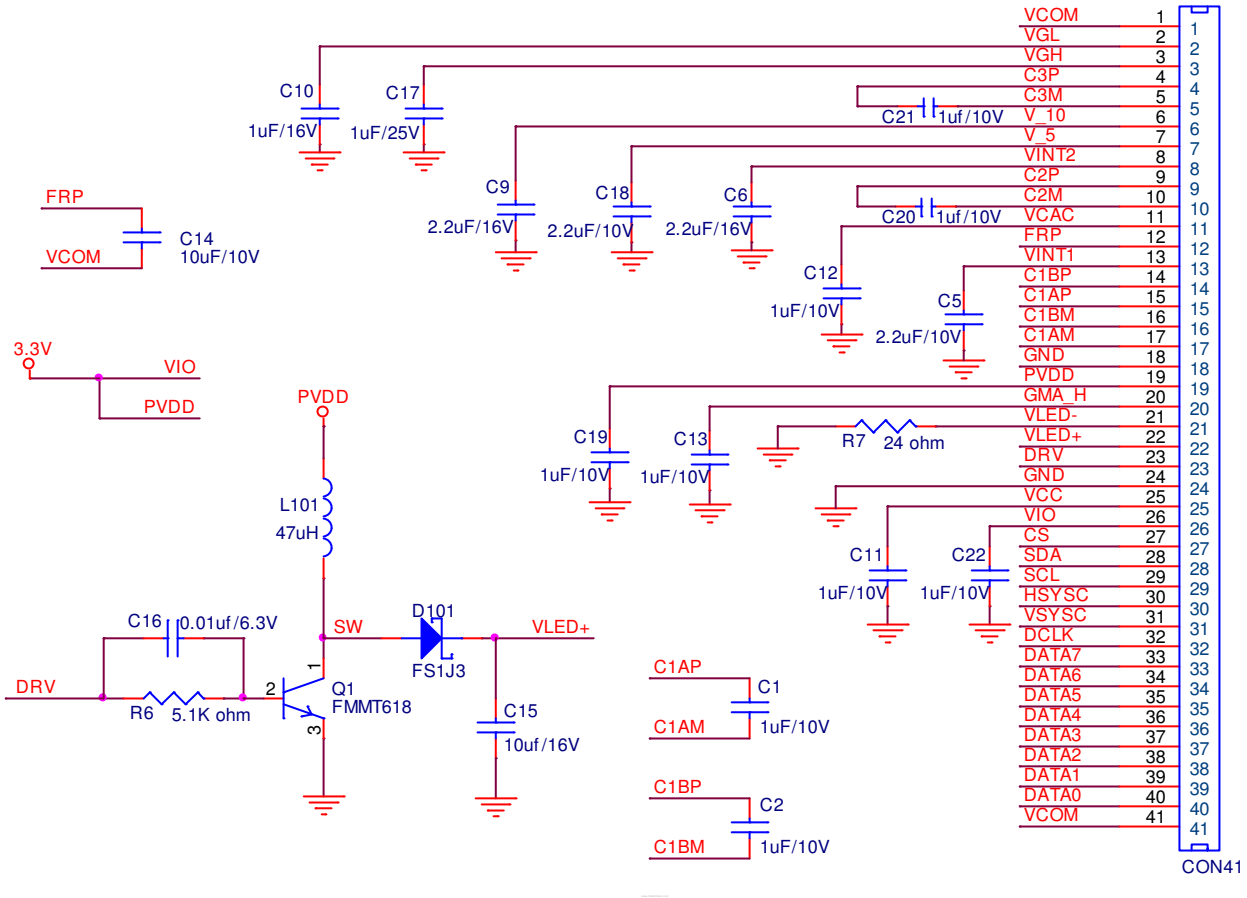
➢ External VCOMDC + external LED driver application circuit



Note: (1) 3.3V is provided from system.

(2) External LED Driver Block is designed by customer.

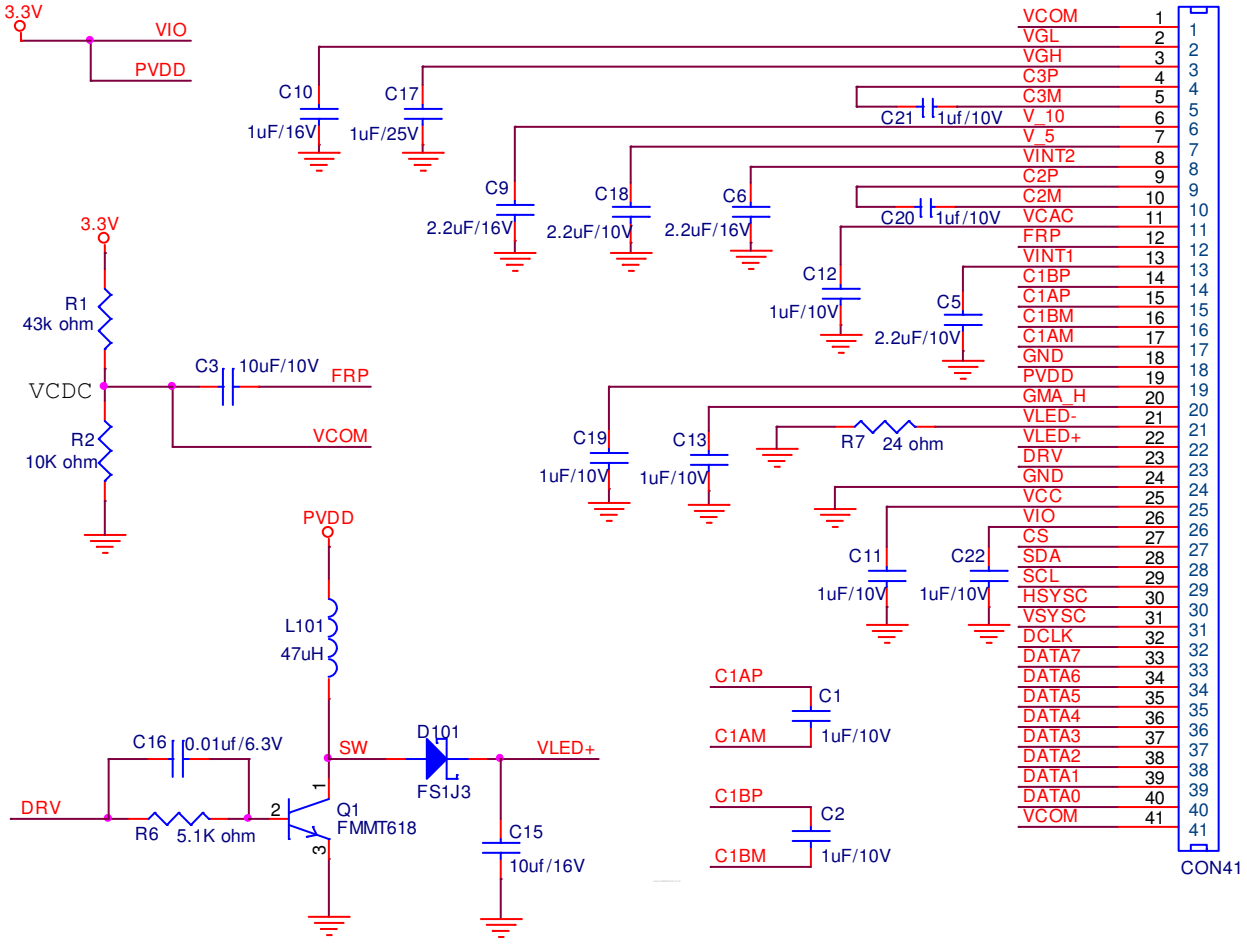
➢ Internal VCOMDC + internal LED driver application circuit



Note: (1) 3.3V is provided from system.

(2) Use internal VCOMDC would make power on time too long.

➢ External VCOMDC + internal LED driver application circuit



Note: (1) 3.3V is provided from system.

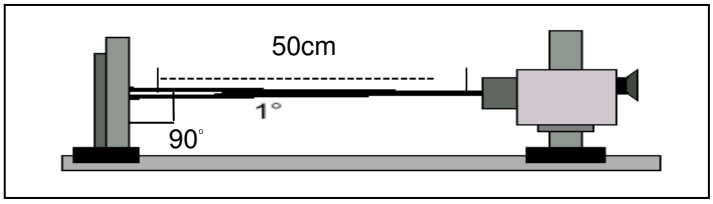
C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time							Note 4
Rise	Tr	θ =0°	-	10	20	ms	
Fall	Tf		-	25	35	ms	
Contrast ratio	CR	At optimized viewing angle	250	300	-		Note 5,6
Viewing angle						deg.	Note 7
Top	φ_T	CR≧10	50	60	-		
Bottom	φ_B		40	50	-		
Left	φ_L		50	60	-		
Right	φ_R		50	60	-		
Brightness *	Y_L	θ =0°	280	350	-	cd/m^2	Note 8,9
Luminance Uniformity			70	80		%	Note 10
Color Chromaticity	x	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.29	0.34	0.39		
	Rx	θ =0°	0.53	0.58	0.63		
	Ry	θ =0°	0.29	0.34	0.39		
	Gx	θ =0°	0.28	0.33	0.38		
	Gy	θ =0°	0.56	0.61	0.66		
	Bx	θ =0°	0.09	0.14	0.19		
	By	θ =0°	0.04	0.09	0.14		

Note 1. Ambient temperature =25℃.

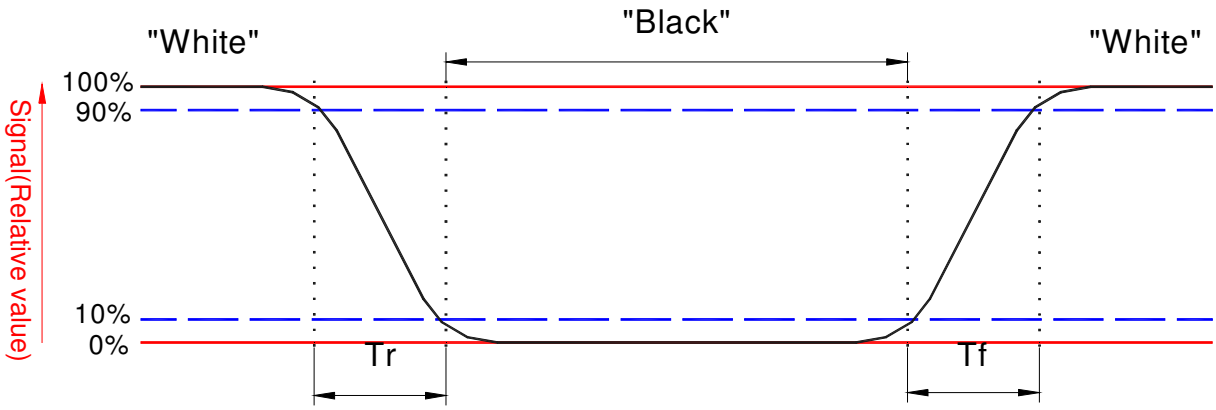
Note 2. To be measured in the dark room.

Note 3.To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-5A, after 10 minutes operation.



Note 4. Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. White $Vi=V_{i50} \mp 1.5V$

Black $Vi=V_{i50} \pm 2.0V$

“±” Means that the analog input signal swings in phase with COM signal.

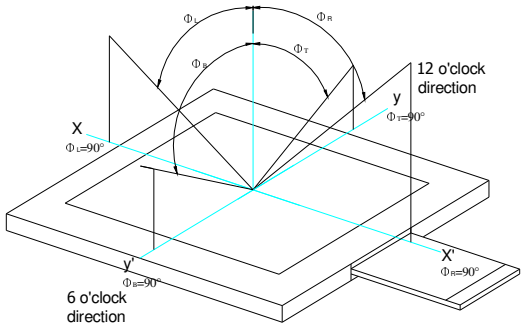
“$\mp$” Means that the analog input signal swings out of phase with COM signal.

V_{i50} : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

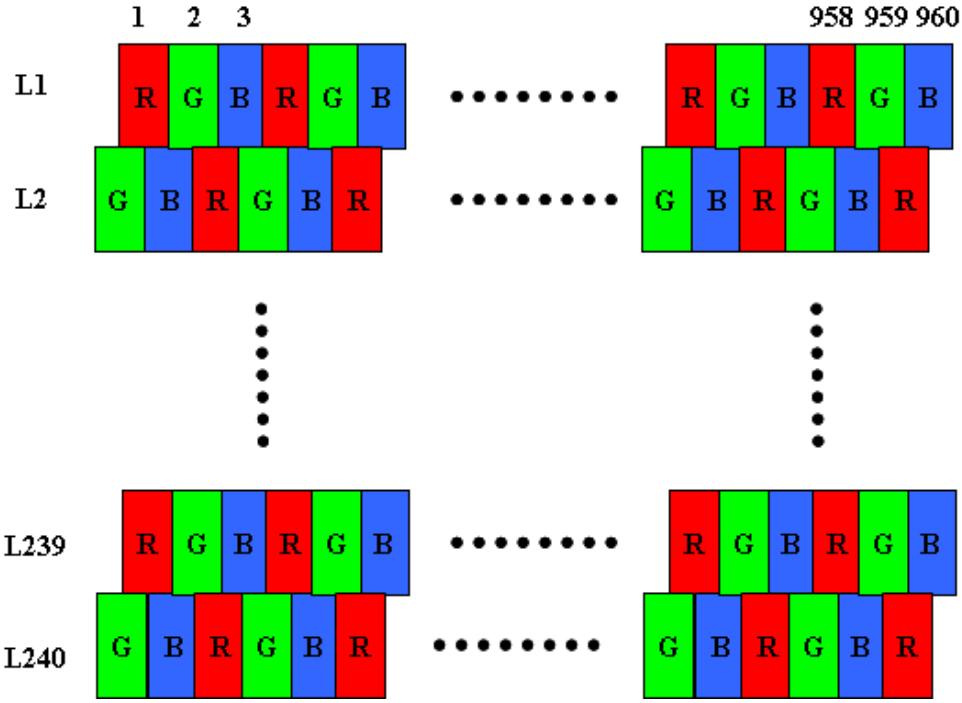
Note 7. Definition of viewing angle:

Refer to figure as below.



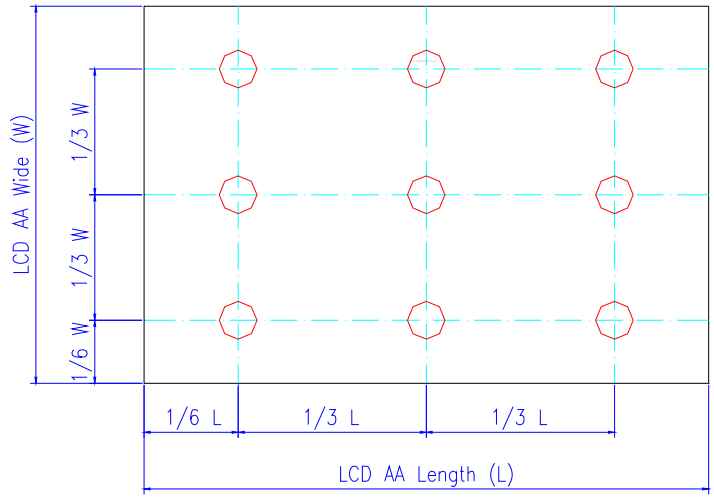
Note 8. Measured at the center area of the panel in gray level 255 with **backlight current 25mA**

Note 9. Color Filter Arrangement



Note 10. Definition of luminance uniformity

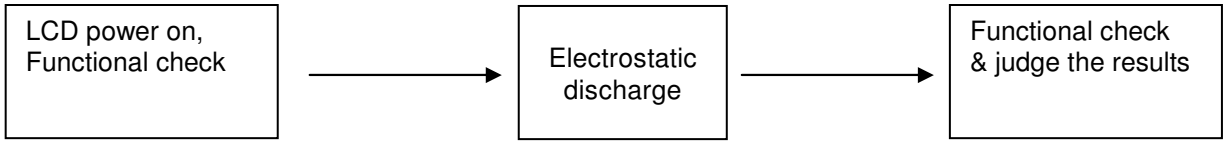
$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine point}}{\text{Max. Brightness of nine point}}$$



D. Reliability test items

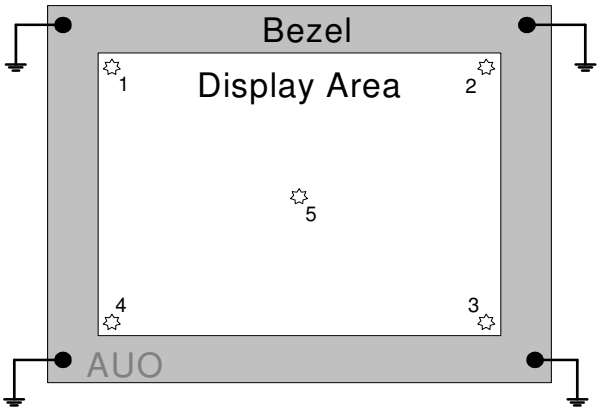
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	Note 1
2	Low temperature storage	Ta= -25℃ 240Hrs	
3	High temperature operation	Ta= 60℃ 240Hrs	
4	Low temperature operation	Ta= 0℃ 240Hrs	
5	High temperature and high humidity	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat shock	-25℃~60℃/50 cycle 2Hrs/cycle	Non-operation
7	Electrostatic discharge	Air-mode : +/- 8kV Contact-mode : +/- 4kV	Note.2, Note 3
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note1: Ta: Ambient temperature.
Note 2. ESD Testing Flow as the below



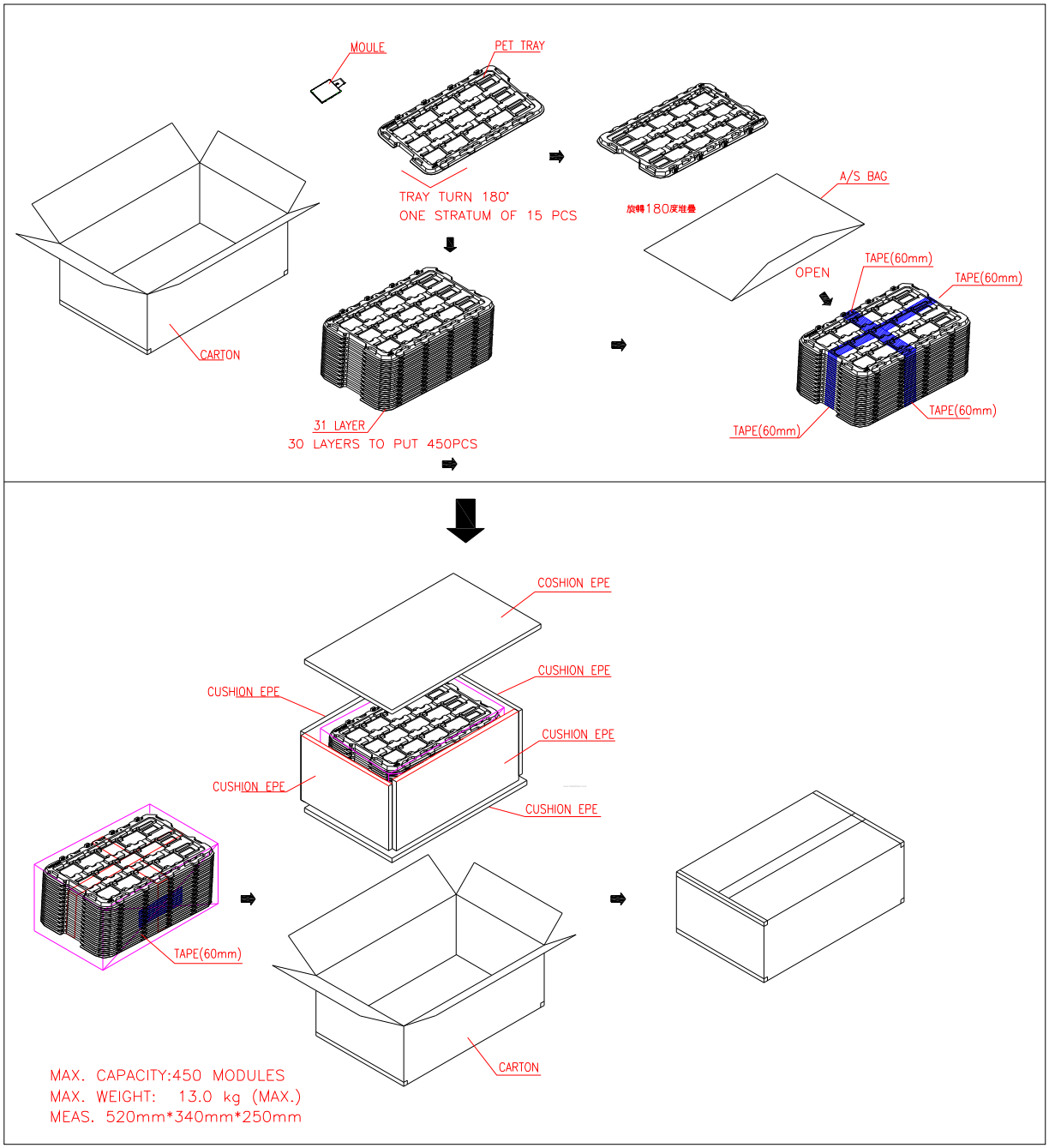
Note 3. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH
2. Instruments:NoisekenESS-2000,
3. Operation System: “CX40FL-B” and adapter “A027DW01 V1T0”
4. Test Mode: Operating mode, test pattern: colorbar+8Gray scale
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:

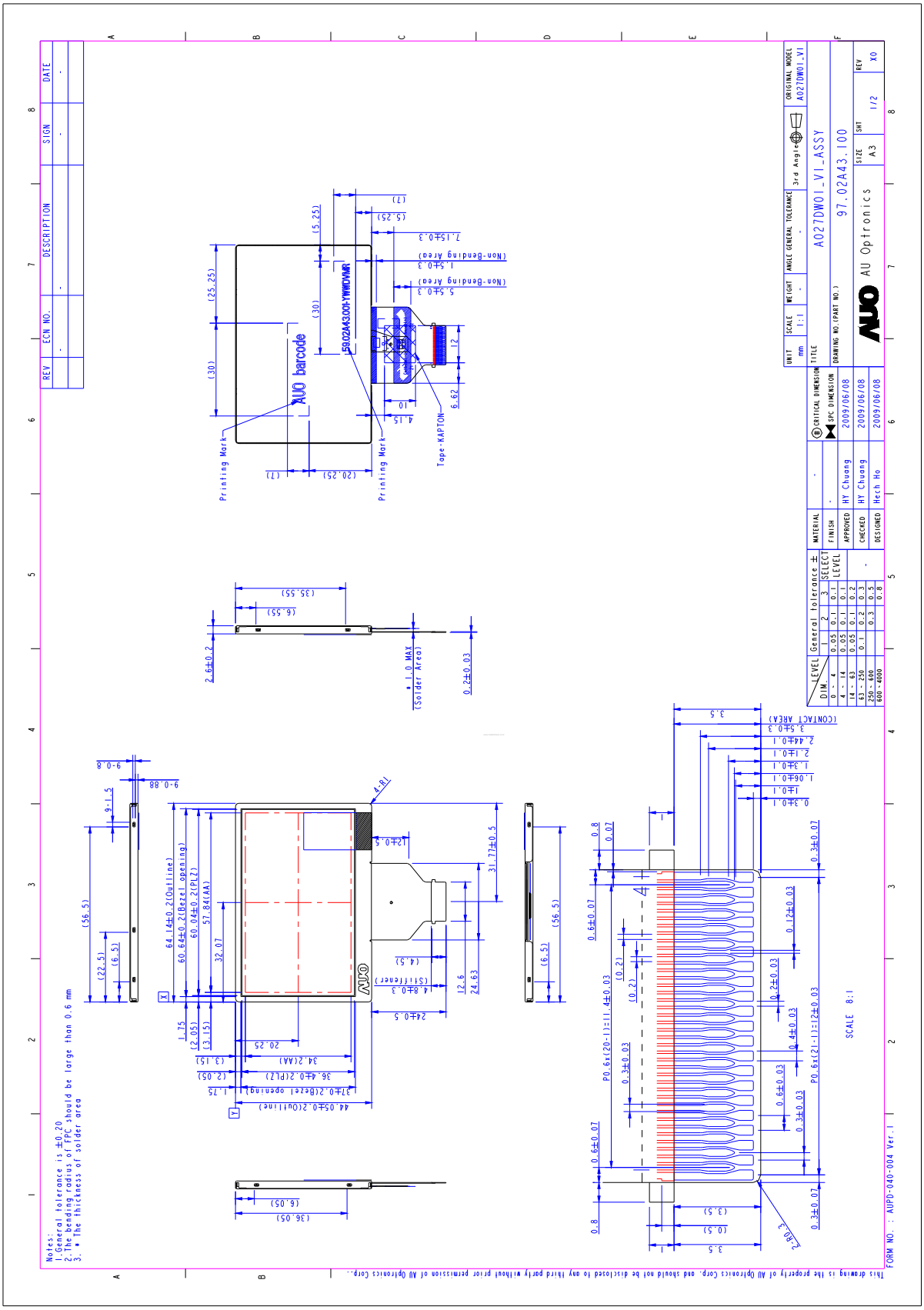


7. The metal casing is connected to power supply ground (0V) at four corners.
8. All register commands are repeating transfer.

E. Packing form



F. Outline dimension



G. Application note

1. Power on/off sequence

1.1 Power on sequence

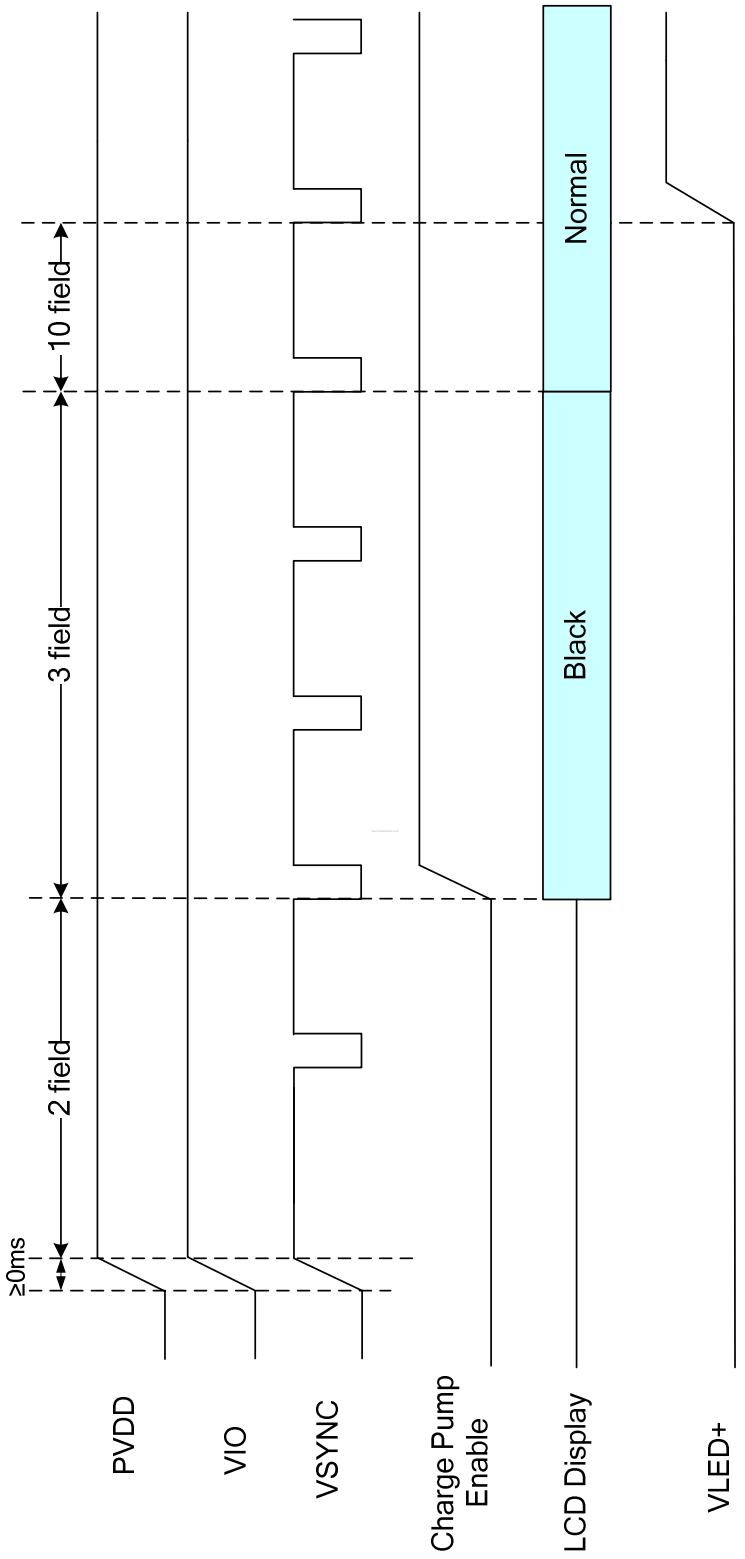


Fig.1 Power on sequence

1.2 Power off sequence

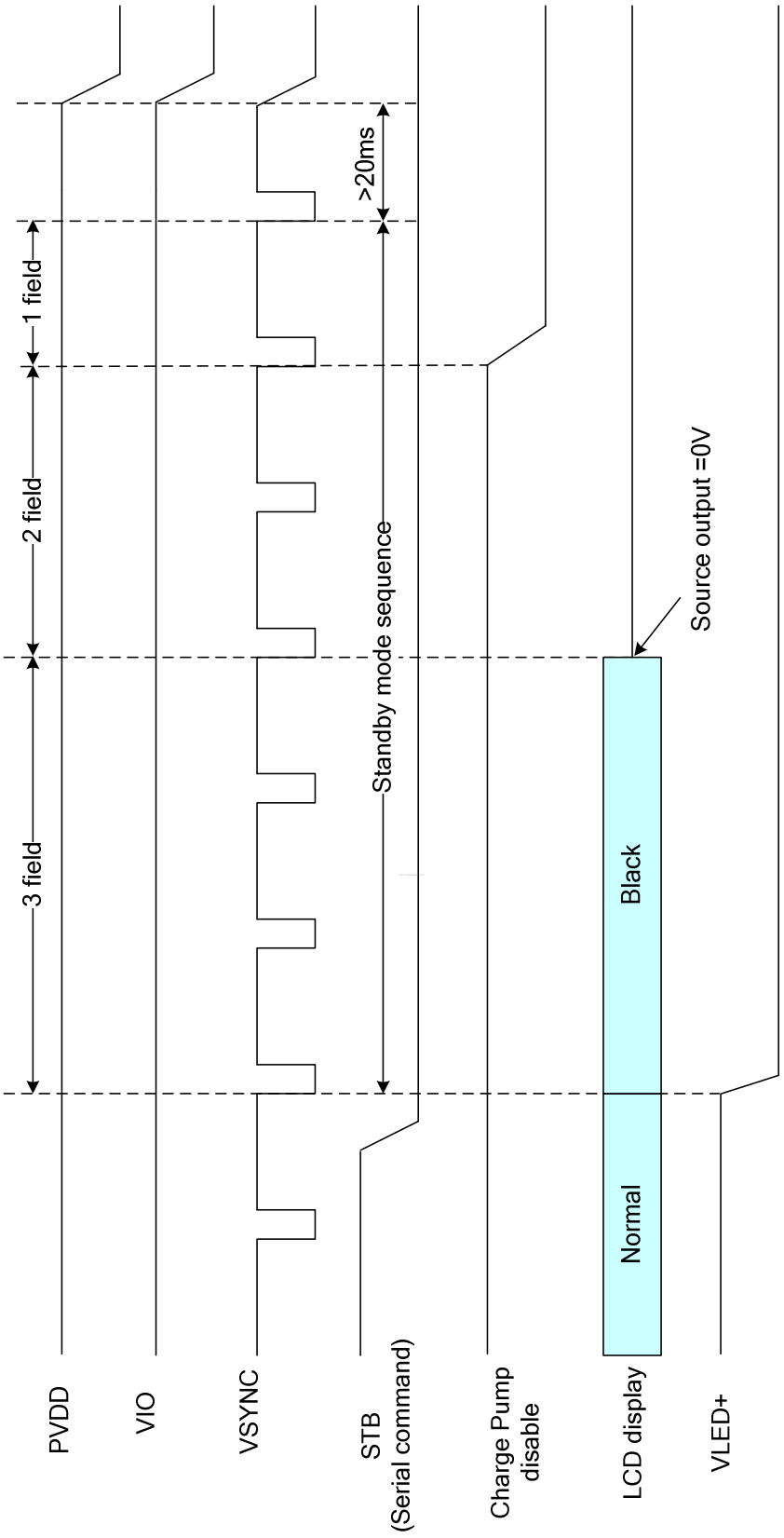
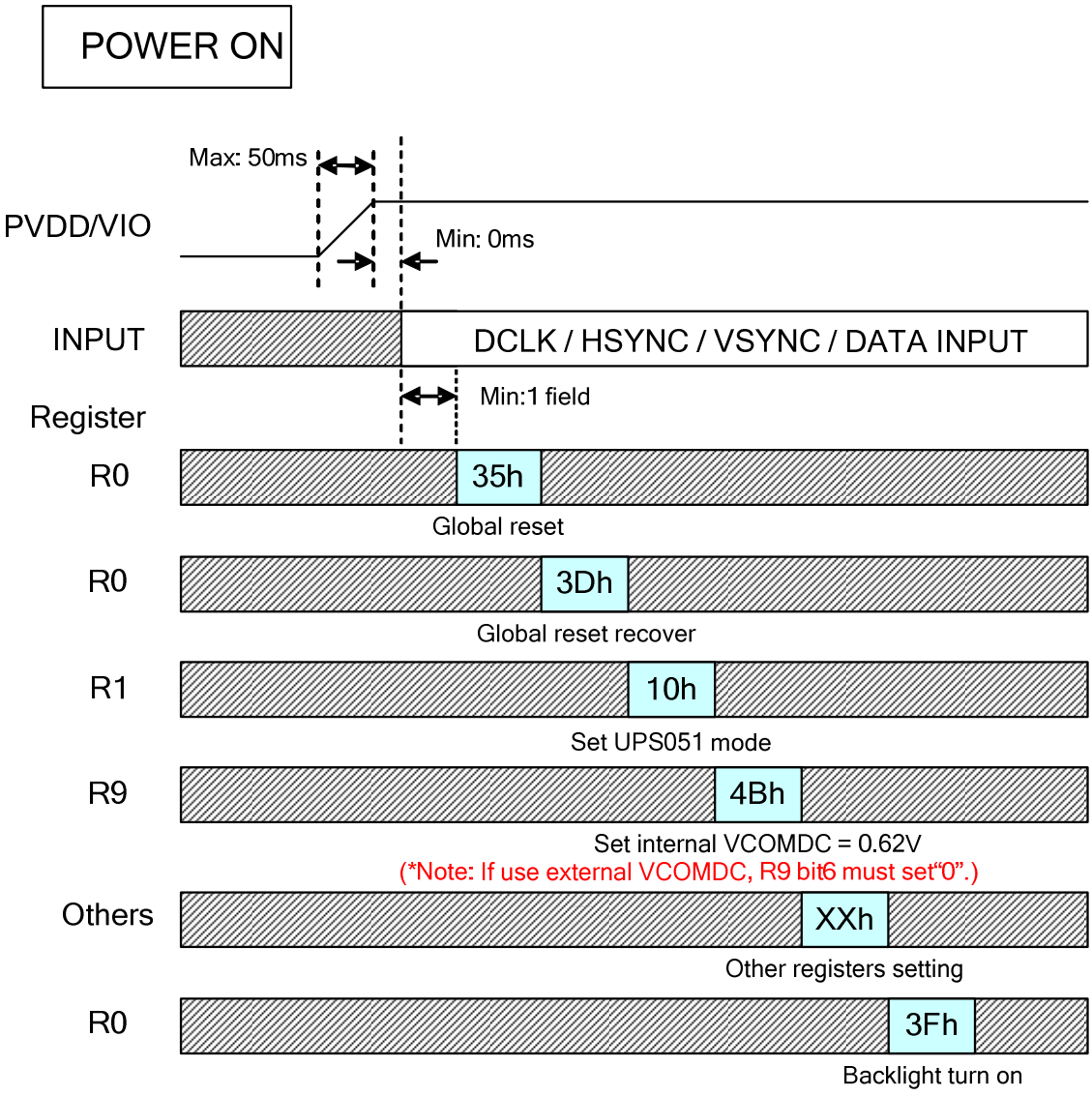
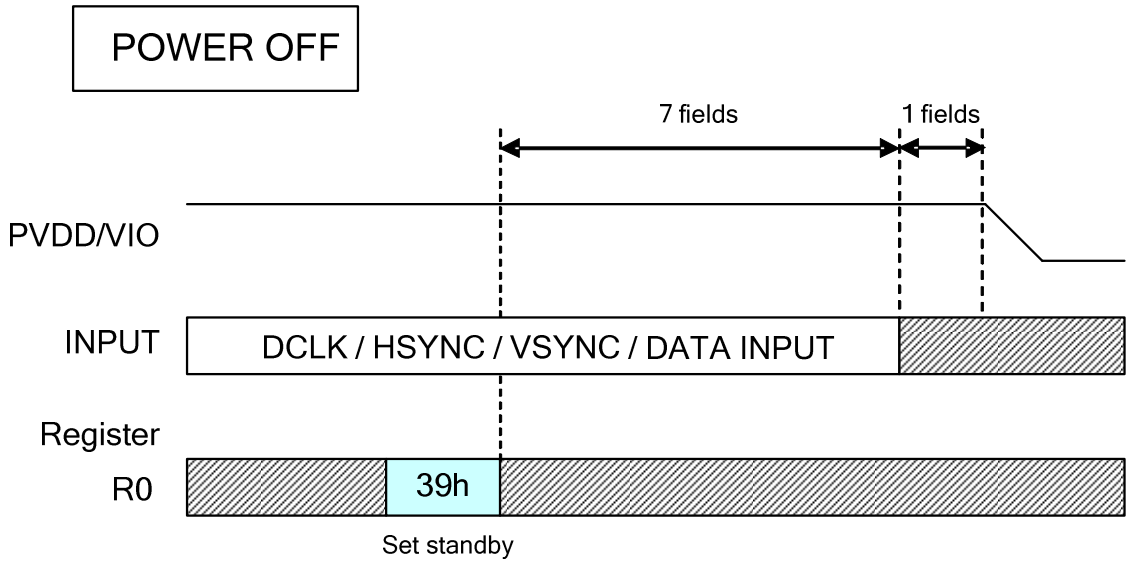


Fig. 2 Power off sequence

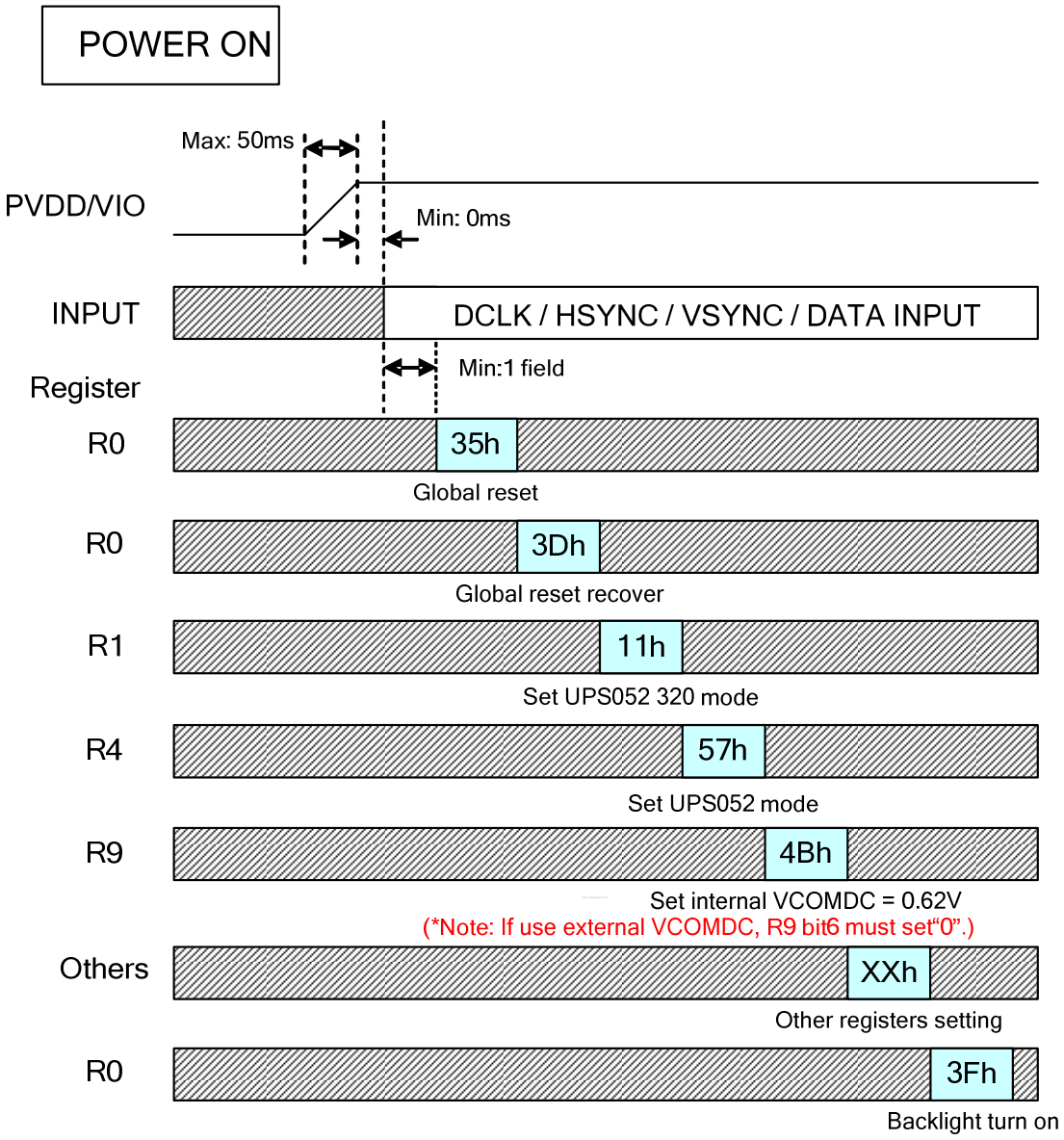
2 . Recommended power on/off serial command settings

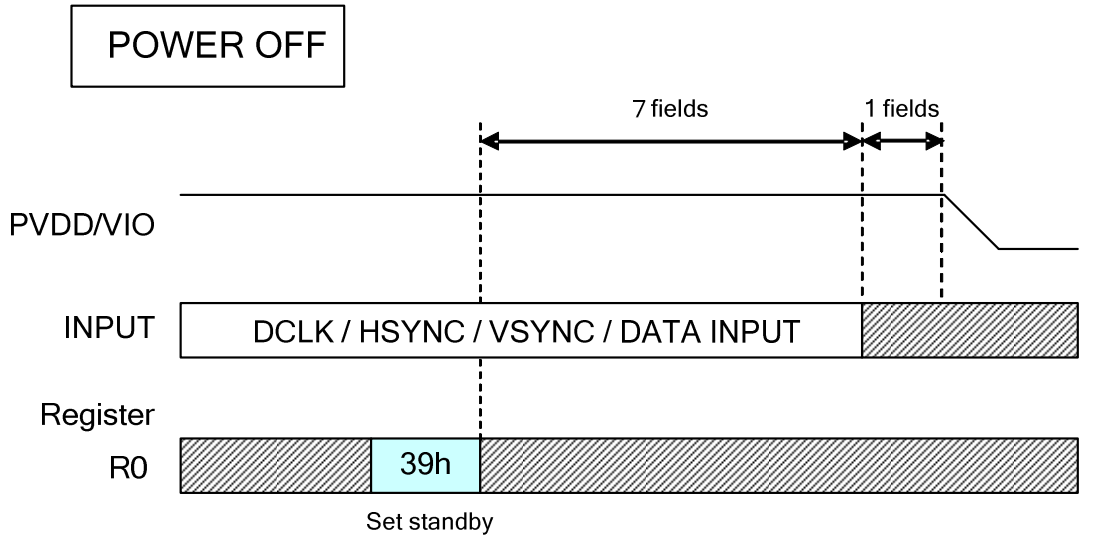
2.1 UPS051 mode





2.2 UPS052 320 mode





2.3 UPS052 360 mode