Doc. version :	1.0
Total pages :	27
Date :	2010/05/18

Product Specification

3.5" COLOR TFT-LCD MODULE/PANEL

MODEL NAME: A035QN02 VF

< >Preliminary Specification
<◆>Final Specification

Note: The content of this specification is subject to change.

Record of Revision

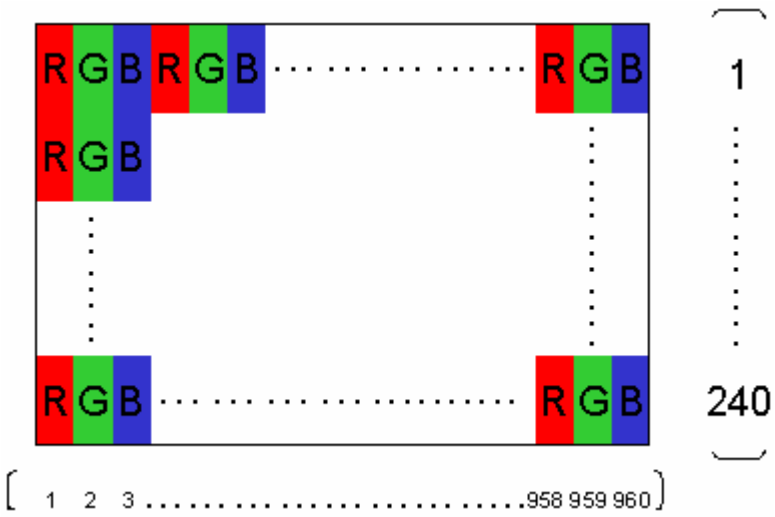
Version	Revise Date	Page	Content
0.0	2009/12/15		First Draft
0.1	2010/01/13	13	Update Serial Setting Map
1.0	2010/05/18	3	Update Weight
		21	Update Power On Sequence
		22	Update Power Off Sequence
		25	Update Vibration test condition

Contents

A. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.219(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 2.92(T)	Note 2
8	Weight	g	31	
9	Display Mode	--	Normally White	
10	Gray Level Inversion Direction		6 O'clock	

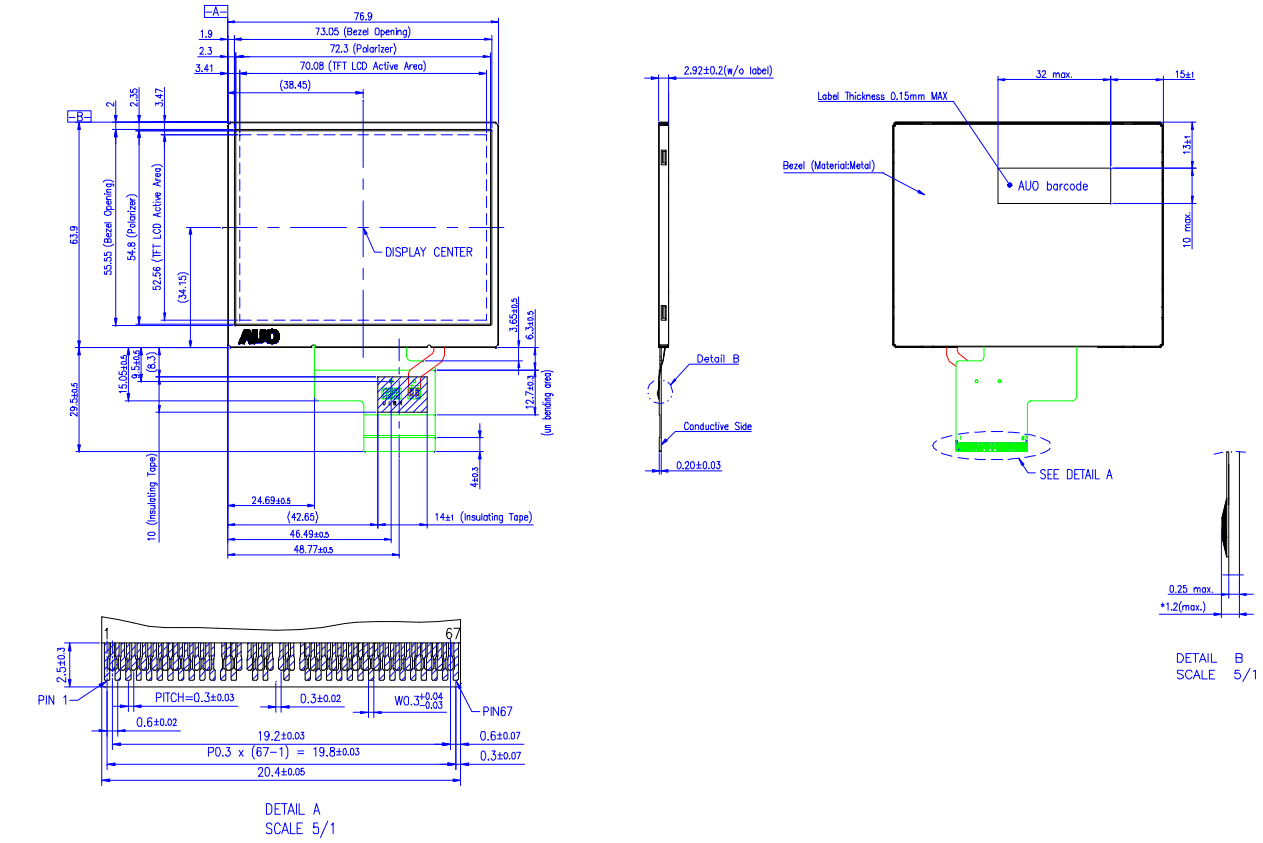
Note 1: Below figure shows dot stripe arrangement.



Note 2: Not including FPC. Refer to the drawing next page for further information.

B. Outline Dimension

NOTE:
1. Gerneral tolerance ±0.3mm
2. The bending radius of FPC should be larger than 0.6mm
3. * The thickness of solder area



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

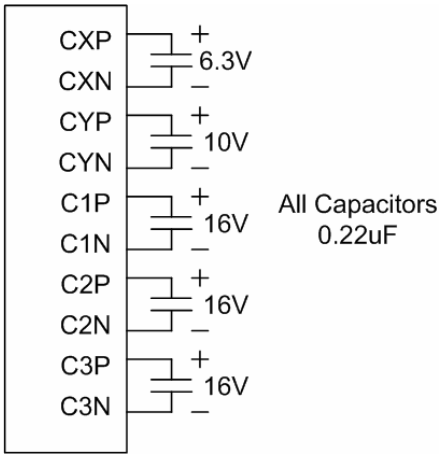
Recommended connector : FH26G 67pin 0.3mm pitch connector

Pin no	Symbol	I/O	Description	Remark
1	LED_C	I	Cathode for LED back-light	
2	LED_A	I	Ahode for LED back-light	
3	GND1	G	Power Grounding	
4	NC	N	Reserved for touch panel	Note 3
5	NC	N	Reserved for touch panel	Note 3
6	NC	N	Reserved for touch panel	Note 3
7	NC	N	Reserved for touch panel	Note 3
8	GND2	G	Power Grounding	
9	VGH	C	Stabilizing capacitor	Note 1
10	C2P	C	Booster capacitor	Note 2
11	C2N	C	Booster capacitor	Note 2
12	C1P	C	Booster capacitor	Note 2
13	C1N	C	Booster capacitor	Note 2
14	VGL	C	Stabilizing capacitor	Note 1
15	C3N	C	Booster capacitor	Note 2
16	C3P	C	Booster capacitor	Note 2
17	GND3	G	Power Grounding	
18	VCIX2	C	Stabilizing capacitor	Note 1
19	CYP	C	Booster capacitor	Note 2
20	CYN	C	Booster capacitor	Note 2
21	VCI	P	Booster input voltage pin	
22	NC	N	Not Connected	Note 3
23	GND4	G	Power Grounding	
24	VCIM	C	Stabilizing capacitor	Note 1
25	CXP	C	Booster capacitor	Note 2
26	CXN	C	Booster capacitor	Note 2
27	NC	N	Not Connected	Note 3
28	RESET	I	System reset pin	
29	GND5	G	Power Grounding	
30	VDDIO	P	Voltage input pin for logic I/O	
31	VCORE	C	Stabilizing capacitor	Note 1
32	GND6	G	Power Grounding	
33	NC	N	Not Connected	Note 3
34	CSB	I	Chip select pin of serial interface	
35	SDI	I	Data input pin in serial mode	

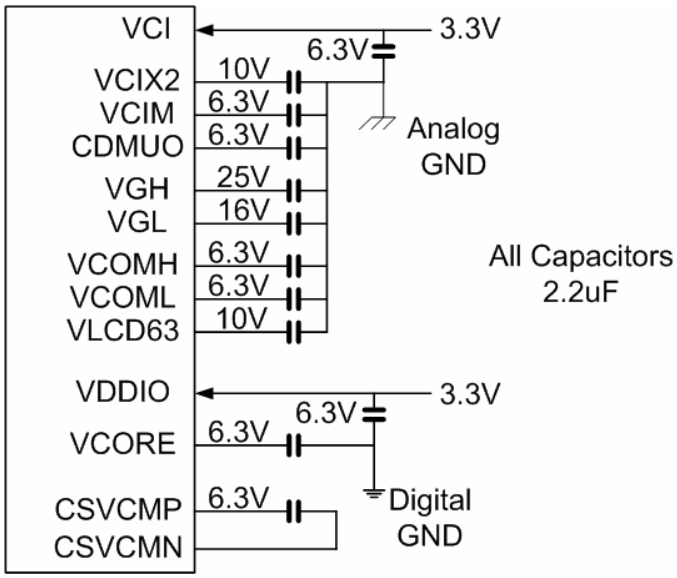
36	SCK	I	Clock input pin in serial mode	
37	NC	N	Not Connected	Note 3
38	DEN	I	Display enable pin from controller	Fixed to VDDIO if not used
39	BB5	I	Blue Data Bit 5	
40	BB4	I	Blue Data Bit 4	
41	BB3	I	Blue Data Bit 3	
42	BB2	I	Blue Data Bit 2	
43	BB1	I	Blue Data Bit 1	
44	BB0	I	Blue Data Bit 0	
45	GG5	I	Green Data Bit 5	
46	GG4	I	Green Data Bit 4	
47	GG3	I	Green Data Bit 3	
48	GG2	I	Green Data Bit 2	
49	GG1	I	Green Data Bit 1	
50	GG0	I	Green Data Bit 0	
51	RR5	I	RED Data Bit 5	
52	RR4	I	RED Data Bit 4	
53	RR3	I	RED Data Bit 3	
54	RR2	I	RED Data Bit 2	
55	RR1	I	RED Data Bit 1	
56	RR0	I	RED Data Bit 0	
58	VSYNC	I	Frame synchronization signal	Fixed to VCC or GND if not used.
58	HSYNC	I	Line synchronization signal	Fixed to VCC or GND if not used.
59	DOTCLK	I	Dot-clock and oscillator source	Fixed to VCC or GND if not used.
60	CDMUO	C	Stabilizing capacitor	Note 1
61	GND7	G	Power Grounding	
62	VLCD63	C	Stabilizing capacitor	Note 1
63	VCOMH	C	Stabilizing capacitor	Note 1
64	VCOML	C	Stabilizing capacitor	Note 1
65	GND7	G	Grounding for digital circuit	
66	CSVCMP	C	Stabilizing capacitor	Note 1
67	CSVCMN	C	Stabilizing capacitor	Note 1

I: Input pin; P: Power pin; G: Ground pin; C: Capacitor pin; N: Not connected

NOTE 1)



NOTE 2)



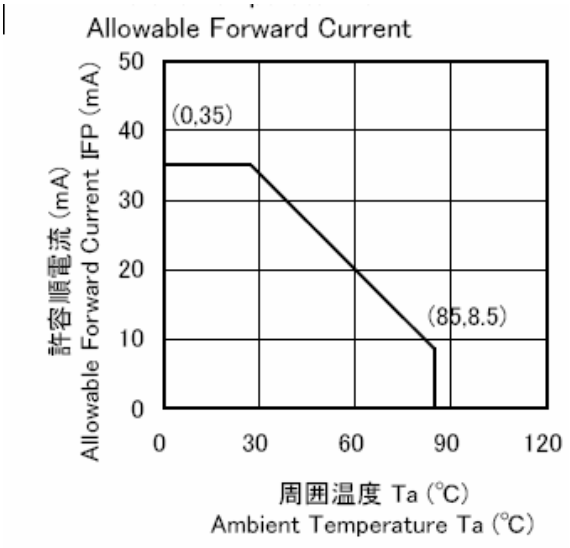
NOTE 3) The pin should be opened.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VCC	-0.3	3.5	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		22	mA	One LED, Note 2

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



3. Electrical DC Characteristics

The following items are measured under stable condition and suggested application circuit.

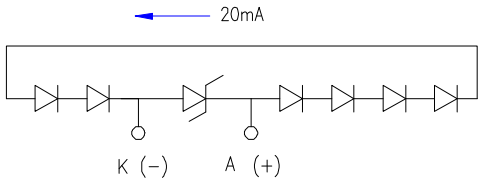
a.TFT- LCD Panel (GND=0V)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power Supply	VCC	2.8	3.2	3.6	V	
Frame Frequency	f_{Frame}		60		Hz	
Dot Data Clock	DCLK		5		MHz	
Input Signal Voltage	Vi	0		0.2 x VDDIO	V	
	VI	0.8 x VDDIO		VDDIO	V	
VCOM High Voltage	VCOMH	3.3		6	V	
VCOM Low Voltage	VCOML	-2.5			V	
Current Consumption	IVCC		7	10	mA	VCC=3.3V

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		20	22	mA	single serial
LED Supply Voltage	V_L		(19.2)	21	V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



Note 2: The ”LED Supply Voltage” is defined by the number of LED at Ta=25°C, I_L=20mA. In the case of 6 pcs LED, V_L=3.2*6=19.2V

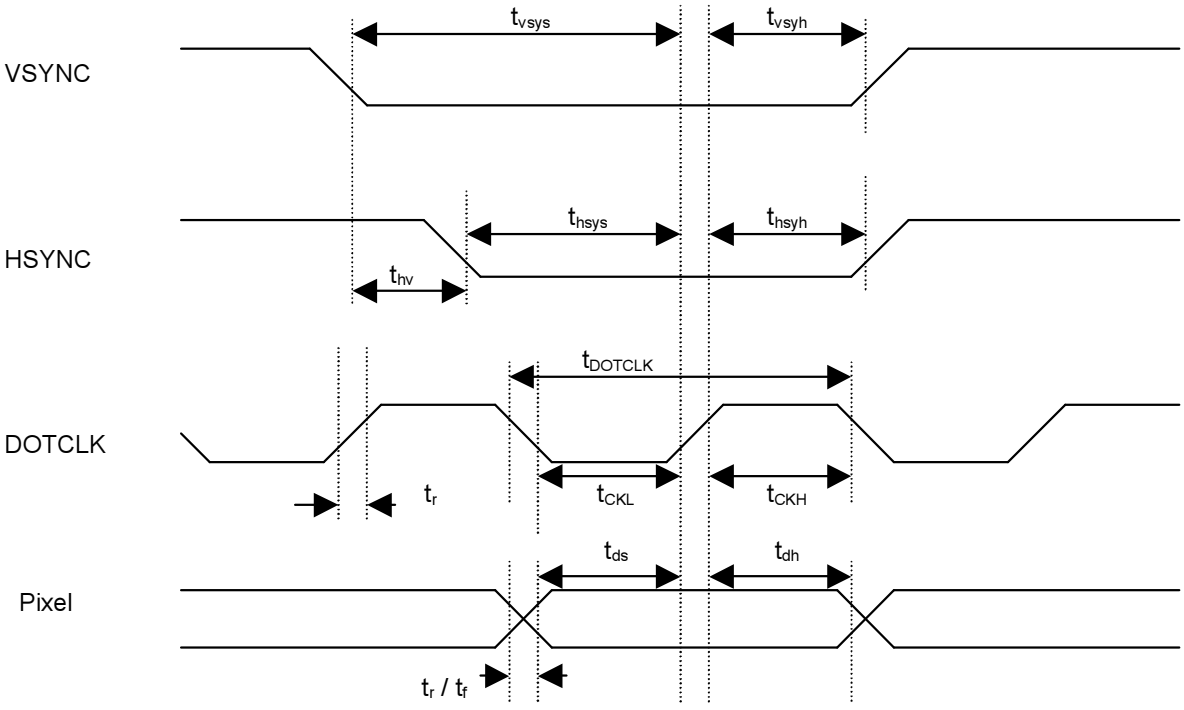
Note 3: The ”LED life time” is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, I_L=20mA

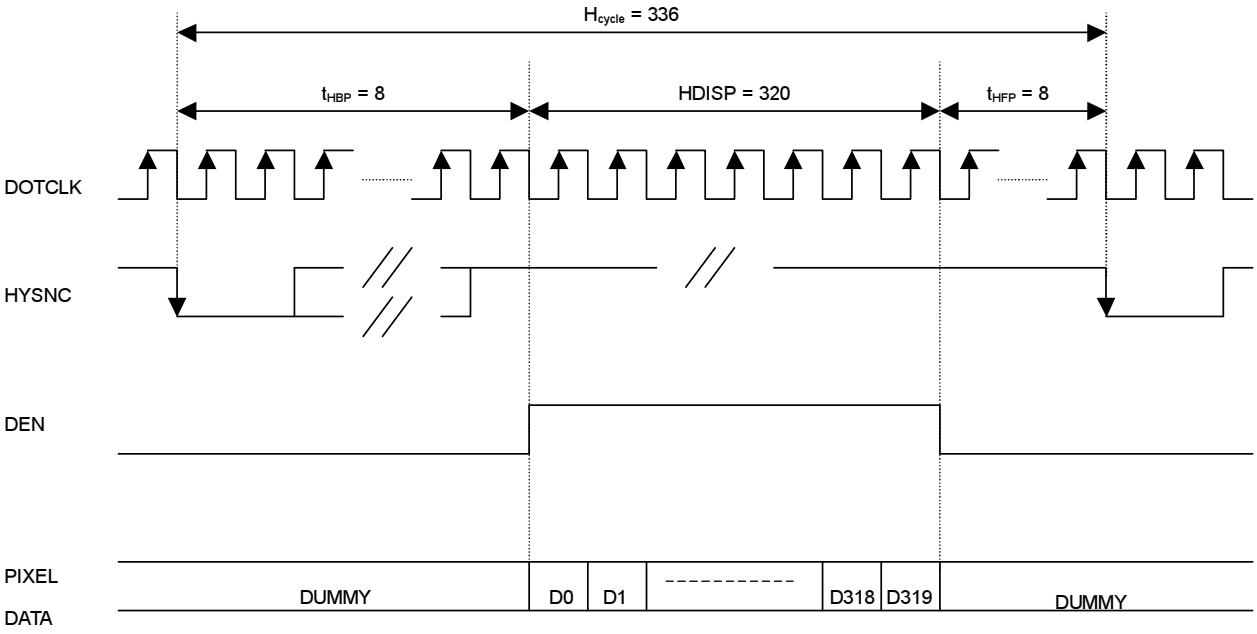
Note 4: The LED lifetime could be decreased if operating $I_L$is larger than 25mA

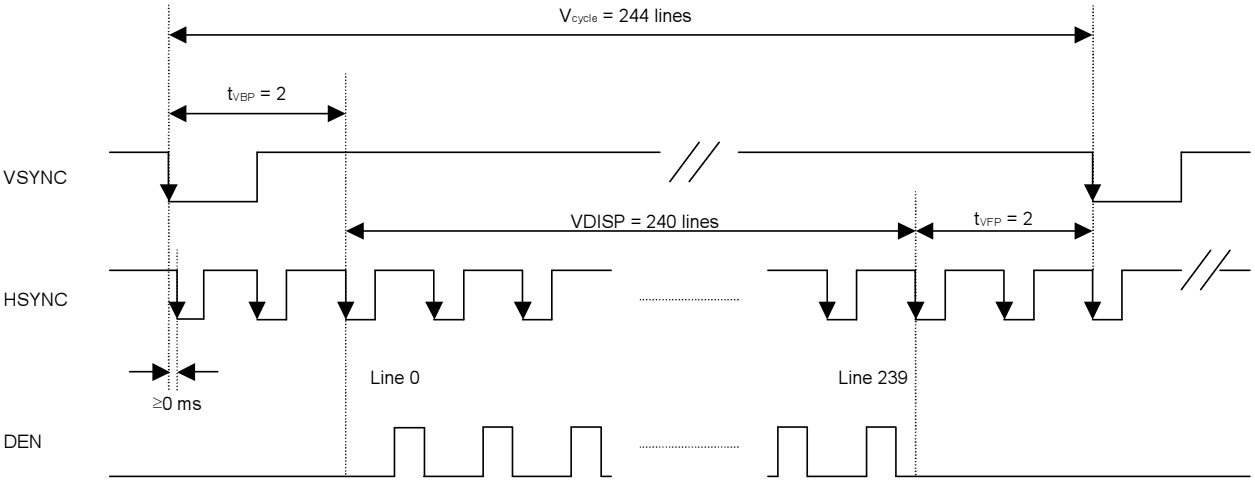
4. Electrical AC Characteristics

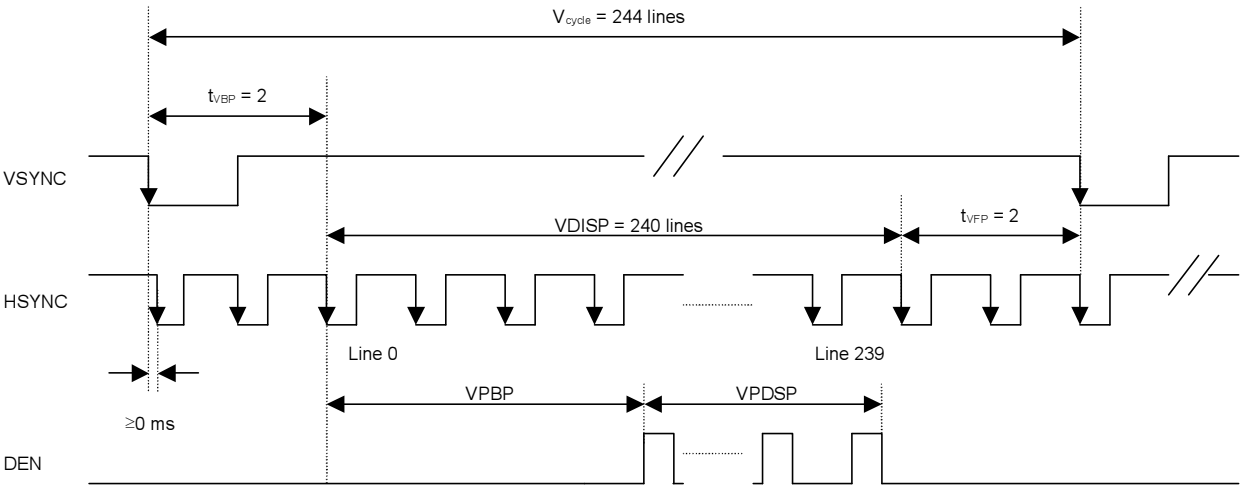
a. Signal AC Characteristics

Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f_{DOTCLK}		5.0	7.5	MHz
DOTCLK Period	t_{DOTCLK}	133	200		nSec
Vsync Setup Time	t_{vsys}	20			nSec
Vsync Hold Time	t_{vsyh}	20			nSec
Hsync Setup Time	t_{hsys}	20			nSec
Hsync Hold Time	t_{hsyh}	20			nSec
Phase Difference of Sync Signal Falling Edge	t_{hv}	0		320	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	66.5			nSec
DOTCLK High Period	t_{CKH}	66.5			nSec
Data Setup Time	t_{ds}	40			nSec
Data Hold Time	t_{dh}	40			nSec
Reset Pulse Width	t_{RES}	10			uSec
Rise / Fall Time	t_r/t_f	20		100	nSec



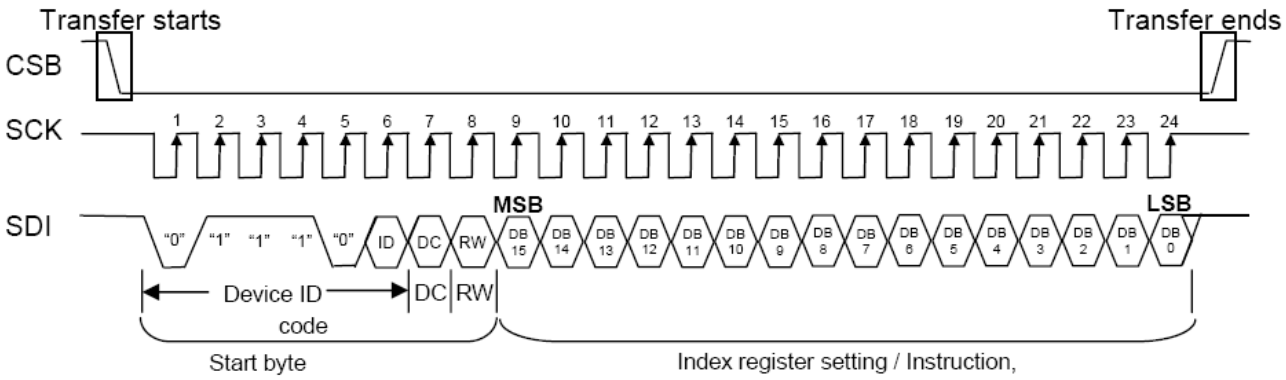






b. SPI Timing Diagram

Write Mode RW="0"



c.SPI Timing Specification

Item	Symbol	Conditions	Min	Typical	Max	Unit
Serial clock frequency	tfclk				15	M Hz
Serial clock cycle time	tclk		66.6			nsec
Clock low width	tsl		33.3			nsec
Clock high width	tsh		33.3			nsec
Chip select set up time	tcss		0			nsec
Chip select hold time	tcsh		10			nsec
Chip select high delay time	tcsd		20			nsec
Data set up time	tds		5			nsec
Data hold time	tdh		10			nsec

5. Command Register Map

a.Serial Setting Map

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output	0	1	0	0	*	*	*	*	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	1	0	1	0	1	0	1	1	1	0	1	1	1	1
R03h	Power control (1)	0	1	*	*	*	*	BT2	BT1	BT0	0	*	*	*	*	*	*	*	0
	(9490h)			1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
R10h	Uniformity	0	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	1	1	0	0
	(005Ch)			0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
R11h	Shut	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SHUT
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R12h	Entry Control	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	IFS	0	0
	(0064h)			0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R16h	Horizontal porch	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R34h	γ control (1)	0	1	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20

	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	γ control (1)	0	1	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R3Ah	γ control (2)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	γ control (2)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

NOTE:

1. "*" is for engineering reserved register setting, and please follow the default value.
2. The map shows the power-on default values of the LCM.
3. Please refer to our recommended register settings section for better performance.

b. Description of serial control data

R01h	Driver output	0	1	0	0	*	*	*	*	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	1	0	1	0	1	0	1	1	1	0	1	1	1	1

TB: Selects the vertical scanning direction of the display.

When TB = "1", the scanning direction is from top to bottom.

When TB = "0", the scanning direction is from bottom to top.

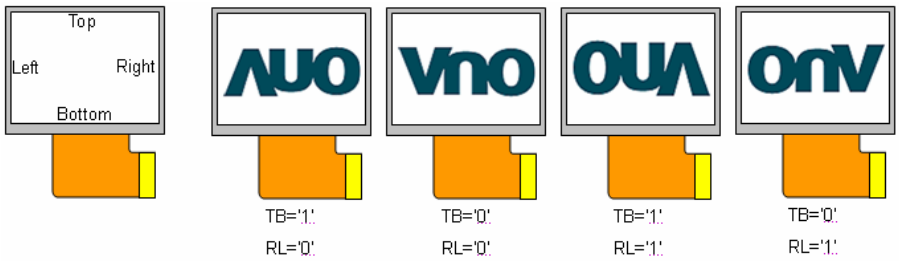
RL: Selects the horizontal scanning direction of the display.

When RL = "1", the scanning direction is from right to left.

When RL = "0", the scanning direction is from left to right.

Note:

1. When the display surface is upward and the FPC golden finger is toward the right, "top", "bottom", "left" and "right" are defined as in the picture below:



2. Please refer to our recommended register settings section for better performance.

R03h	Power control	0	1	*	*	*	*	BT2	BT1	BT0	0	*	*	*	*	*	*	*	0
	(9490h)			1	0	0	1	0	1	0	0	1	0	0	1	0	0	0	0

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply

voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	V_{CIX2}x3	- V_{GH} + VCI	6	-5
0	0	1	V_{CIX2}x3	- V_{GH} + V_{CIX2}	6	-4
0	1	0	V_{CIX2}x3	- V_{CIX2}	6	-2
0	1	1	V_{CIX2}x2+VCI	- V_{GH}	5	-5
1	0	0	V_{CIX2}x2+VCI	- V_{GH} + V_{CIX2}	5	-4
1	0	1	V_{CIX2}x2+VCI	- V_{GH} + V_{CIX2}x2	5	-3
1	1	0	V_{CIX2}x2	- V_{GH}	4	-4
1	1	1	VCIX2x2	- V_{GH} +VCI	4	-3

NOTE: Please refer to our recommended register settings section for better performance.

R0Ch	Power control	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	V_{CIX2} voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

NOTE: Please refer to our recommended register settings section for better performance.

R0Dh	Power control	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

VRH3-0: Set amplitude magnification of gamma reference voltage VLCD63. These bits amplify the VLCD63 voltage 1.78 to 3.00 times the Vref voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.815
0	0	0	1	Vref x 2.905
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020

0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

NOTE: Please refer to our recommended register settings section for better performance.

R0Eh	Power control	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV4-0) becomes available. When VCOMG = “0”, VCOML output is fixed to Hi-z level, VCI2 output for VCOML power supply stops, and the instruction (VDV4-0) becomes unavailable.

Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive.

These bits amplify VCOM amplitude 0.6 to 1.23 times the VLCD63 voltage.

When VCOMG = “0”, the settings become invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOMA
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
		:			Step = 0.03
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reserved
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		:			Step = 0.03
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

NOTE: Please refer to our recommended register settings section for better performance.

R10h	Uniformity	0	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	1	1	0	0
	(005Ch)			0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0

ENSVIN:

When ENSVIN = '1', uniformity improvement scheme is enabled.

When ENSVIN = '0', uniformity improvement scheme is disabled.

R11h	Shut	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SHUT
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SHUT:

When SHUT = 1, the driver enters into the sleep mode. In the sleep mode, the internal display operations are halted.

R12h	Entry Mode	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0	IFS	0	0
	(0064h)			0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0

IFS: Selection for HV SYNC and DEN modes.

IFS	Interface
0	18-bit digital RGB DEN Mode
1	18-bit digital RGB HV SYNC Mode

R16h	Horizontal	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

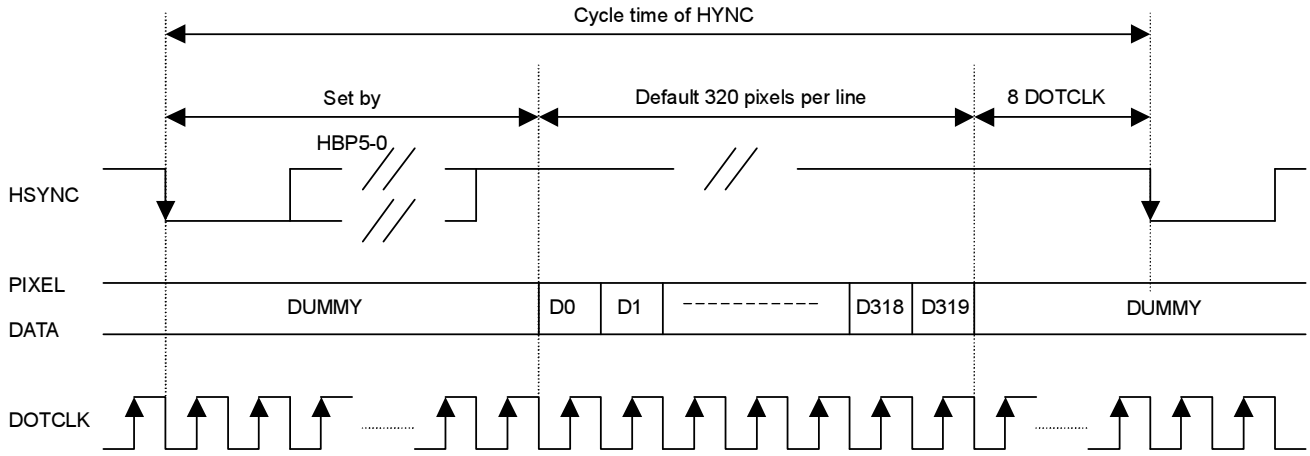
XL7-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	# of pixels per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					:
				:					step = 1
				:					:
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved

HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data.

The pixel data exceed the range set by XL8-0 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	# of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
			:			:
			:			step = 1
			:			:
1	1	1	1	1	0	64
1	1	1	1	1	1	65

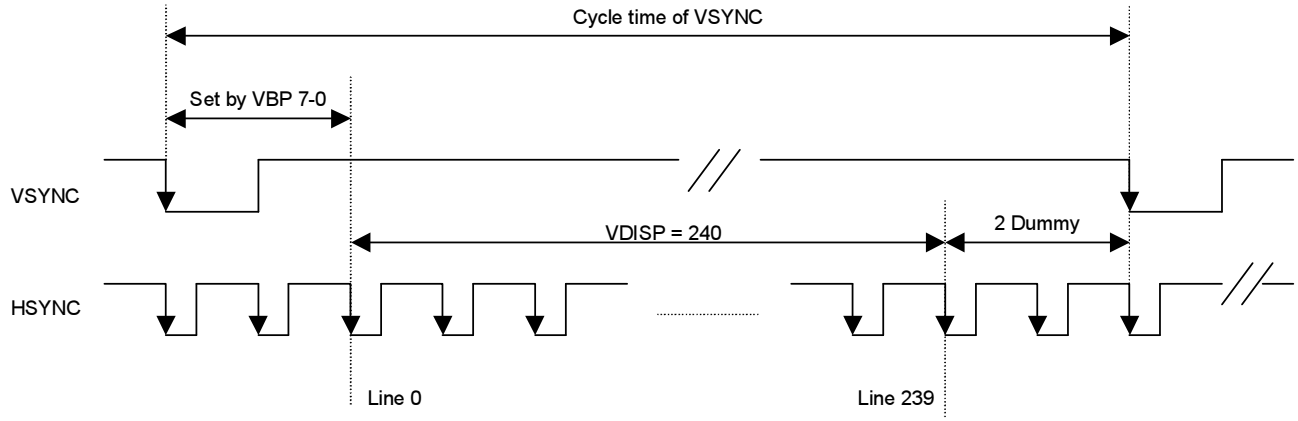


R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line.

The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	# of lines per frame
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1	2
				:				:
				:				step = 1
				:				:
1	1	1	0	1	1	1	1	239
1	1	1	1	0	0	0	0	240
1	1	1	1	*	*	*	*	reserved



R1Eh	Power	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value. When nOTP set to “1”, setting of VCM5-0 becomes valid and voltage of VCOMH can be adjusted.

VCM5-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.99 times the VLCD63 voltage by step = 0.01.

NOTE: Please refer to our recommended register settings section for better performance.

R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R34h	γ control (1)	0	1	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	γ control (1)	0	1	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

PKP52–00: Gamma micro adjustment register for the positive polarity output.

PRP12-00: Gradient adjustment register for the positive polarity output.

PKN52-00: Gamma micro adjustment register for the negative polarity output.

PRN12-00: Gradient adjustment register for the negative polarity output.

NOTE: Please refer to our recommended register settings section for better performance.

R3Ah	γ control	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	γ control	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output.

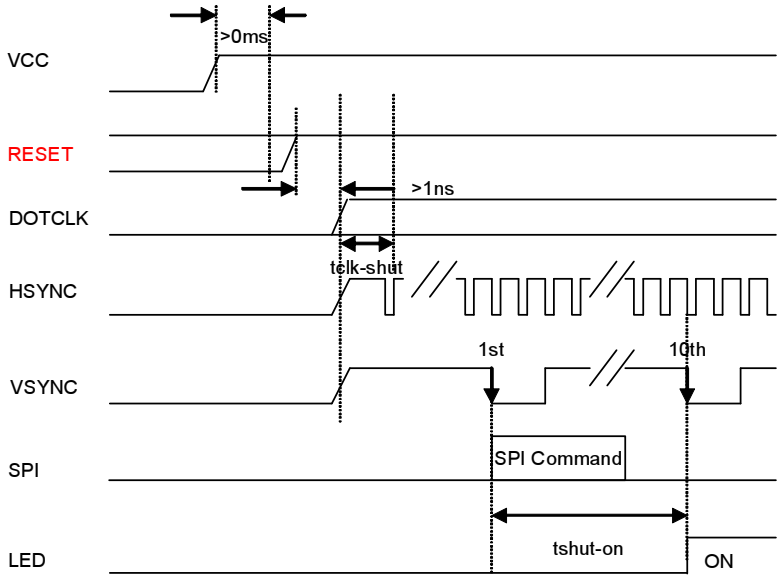
VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output.

NOTE: Please refer to our recommended register settings section for better performance.

6. Power On/Off Characteristics

a. Recommended Power On Sequence

Power On



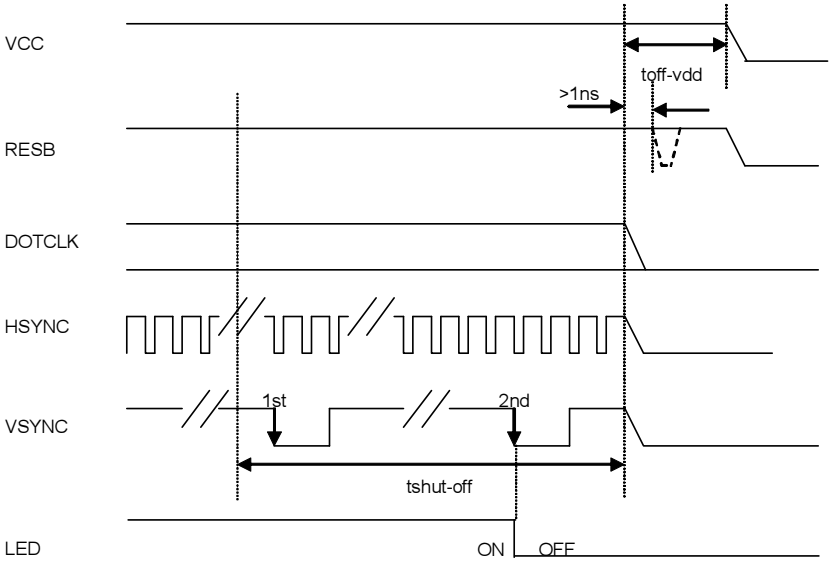
Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK	tclk-shut	1			clk
Rising edge of RESB to display on -- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz	tshut-on			10	frame
			164		mSec

Note1: It is necessary to input DOTCLK before the rising edge of RESB.

Note2: Display starts at 10th falling edge of VSYNC after the rising edge of RESB.

b. Recommended Power Off Sequence

Power Off



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off	tshut-off	2	-	-	frame
-- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz		32.8	-	-	mSec
Input-signal-off to V_{DDIO} off	toff-vdd	1	-	-	uSec

Note1: DOTCLK must be maintained at lease 2 frames after enter into sleep mode.

Note2: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

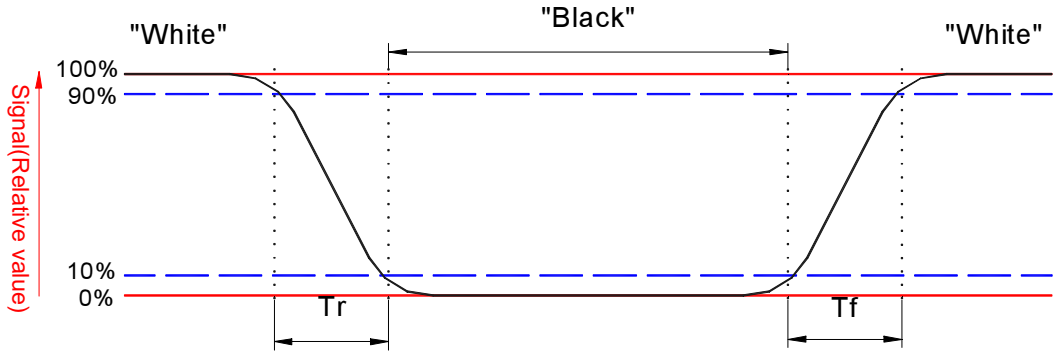
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ=0°	-	10	20	ms	Note 3
Fall	Tf		-	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ=0°	350	430	-	cd/m^2	Note 9
NTSC			50	60		%	
White Chromaticity	X	θ=0°	0.26	0.31	0.36		
	y	θ=0°	0.28	0.33	0.38		

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25°C.

Note 5. Contrast ratio is calculated with the following formula.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White Vi=Vi50 ± 1.5V

Black Vi=Vi50 ± 2.0V

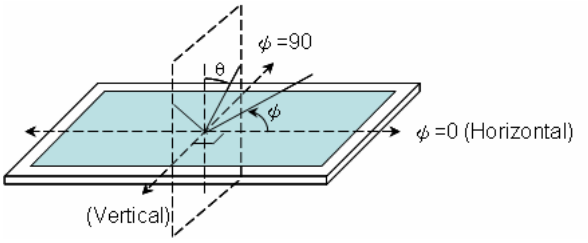
"±" means that the analog input signal swings in phase with COM signal.

"μ" means that the analog input signal swings out of phase with COM signal.

Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Brightness is measured at the center point of the display area.

E. Reliability Test Items

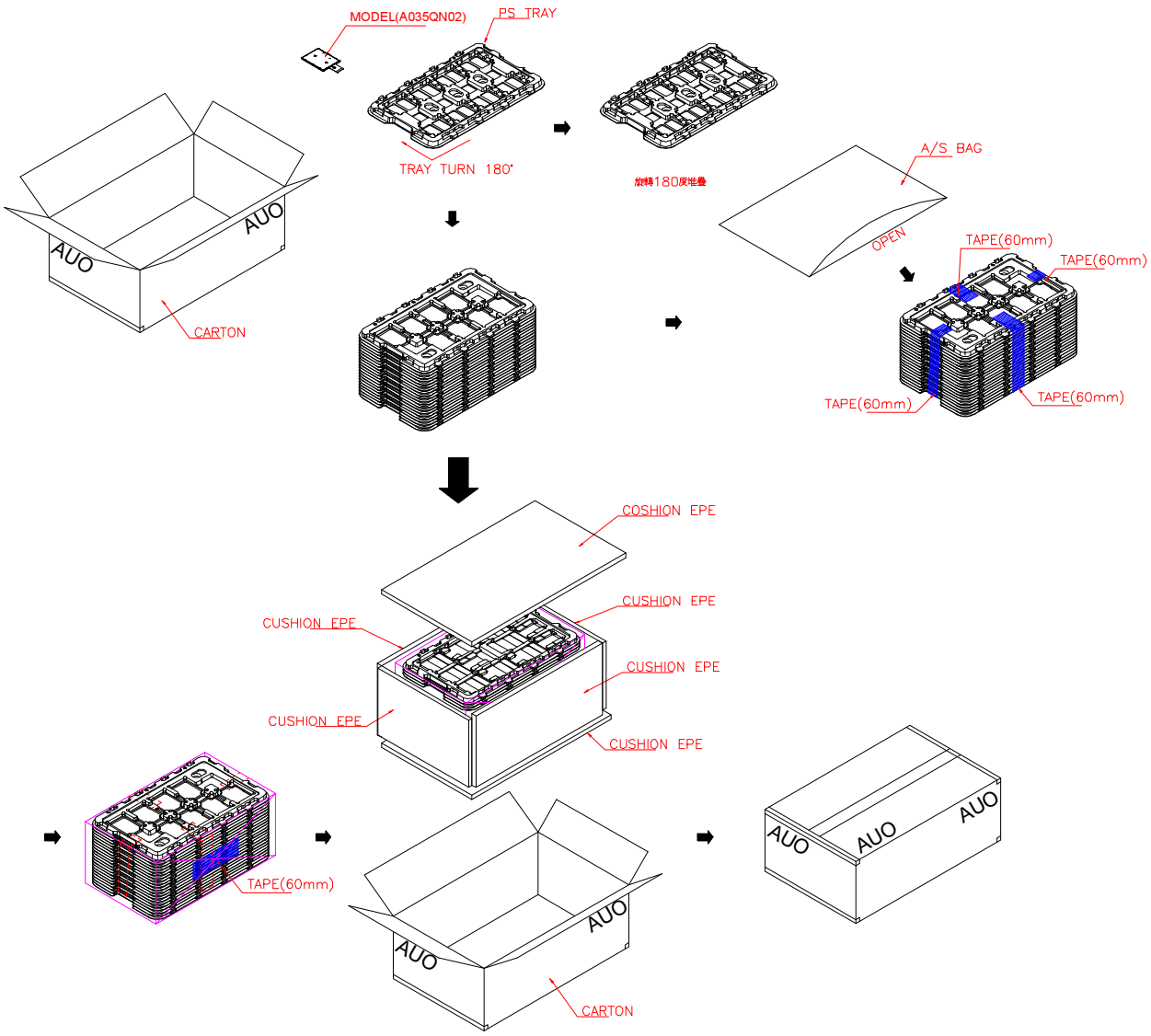
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80□ 240Hrs	
2	Low Temperature Storage	Ta= -40□ 240Hrs	
3	High Ttemperature Operation	Tp= 70□ 240Hrs	
4	Low Temperature Operation	Ta= -20□ 240Hrs	
5	High Temperature & High Humidity	Tp= 60□. 90% RH 240Hrs	Operation
6	Heat Shock	-25□~70□, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Vibration	Frequency range: 10Hz~55Hz Stoke: 1.5mm Sweep: 10Hz~55Hz~10Hz ±x, ±y, ±z 2 hours for each axis	Non-operation JIS C7021, A-10 condition A : 15 minutes
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7 condition C
10	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
12	Pressure	5kg, 5sec	Note 6

Note 1: In the standard conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2: Ta: Ambient temperature.

Note 3: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

F. Packing and Marking



MAX. CAPACITY:160 MODULES
MAX. WEIGHT: 12Kg
MEAS. 520mm*340mm*250mm

G. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.

H. Application Note

1. Recommended Register Settings

Register	Setting
R01	“2AEF”h
R03	“920E”h
R28	“0006”h
R0B	“D000”h
R26	“2780”h
R27	“0038”h
R0C	“0003”h
R0D	“000C”h
R0E	“3100”h
R1E	“00A9”h
R2Eh	“B945”h
R30	“0304”h
R31	“0507”h
R32	“0405”h
R33	“0007”h
R34	“0507”h
R35	“0004”h
R36	“0605”h
R37	“0103”h
R3A	“000F”h
R3B	“000F”h

NOTE:

1. The different sequence of registers setting would not affect the normal behavior of LCM.

2.Please refer to the POWER ON/OFF sequence section for register setting timing as power-on.