Doc. version :	0.1
Total pages :	28
Date :	2016/06/16

Product Specification

3.5" COLOR TFT-LCD MODULE/PANEL

MODEL NAME: A035QN02 VG

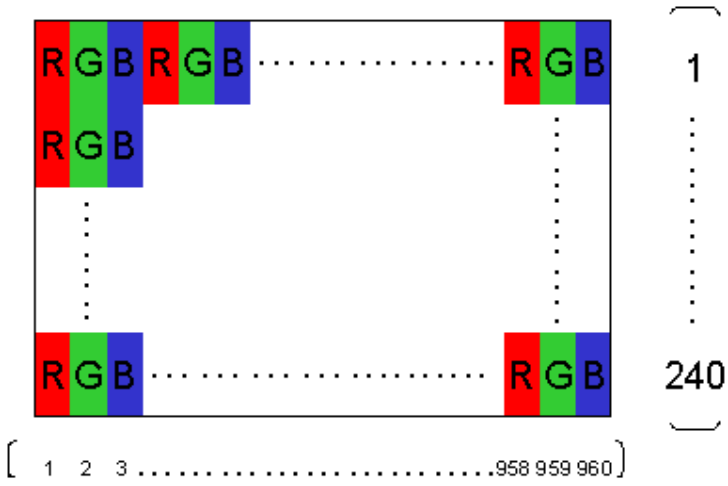
< ◆ >Preliminary Specification
< >Final Specification

Note:
The content of this specification is subject to change.
All changes to delivery specification shall be notified in advance

A. General Information

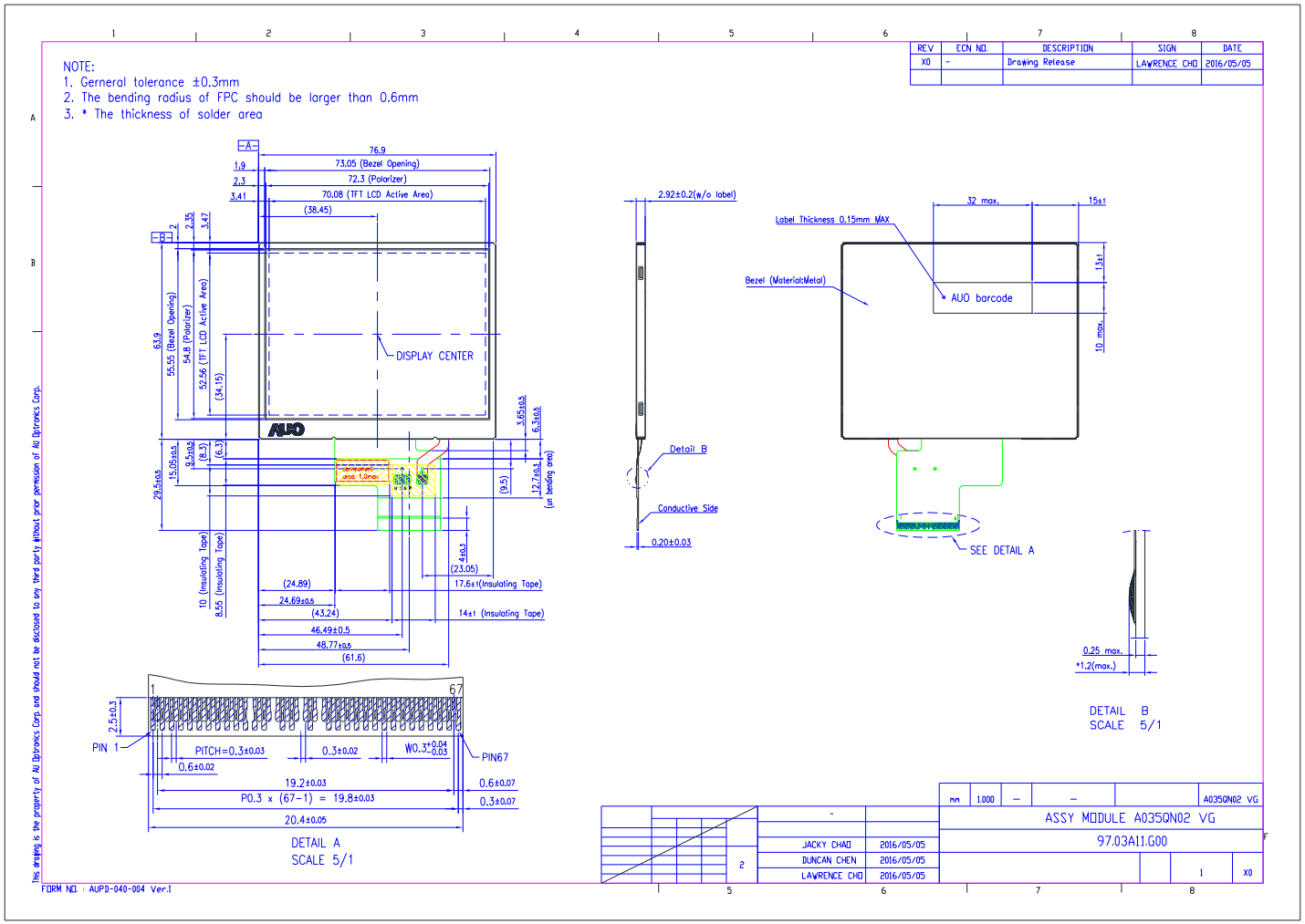
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.219(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 2.92(T)	Note 2
8	Weight	g	31	
9	Display Mode	--	Normally White	
10	Gray Level Inversion Direction		6 O'clock	

Note 1: Below figure shows dot stripe arrangement.



Note 2: Not including FPC. Refer to the drawing next page for further information.

B. Outline Dimension



C. Electrical Specifications

1. TFT LCD Panel Pin Assignment

Recommended connector : FH26G 67pin 0.3mm pitch connector

Pin no	Symbol	I/O	Description	Remark
1	LED_C	I	Cathode for LED back-light	--
2	LED_A	I	Ahode for LED back-light	--
3	GND1	G	Power Grounding	--
4	NC	N	Reserved for touch panel	--
5	NC	N	Reserved for touch panel	--
6	NC	N	Reserved for touch panel	--
7	NC	N	Reserved for touch panel	--
8	GND2	G	Power Grounding	--
9	VGH	C	Stabilizing capacitor	Note
10	C2P	C	Booster capacitor	Note
11	C2N	C	Booster capacitor	Note
12	C1P	C	Booster capacitor	Note
13	C1N	C	Booster capacitor	Note
14	VGL	C	Stabilizing capacitor	Note
15	C3N	C	Booster capacitor	Note
16	C3P	C	Booster capacitor	Note
17	GND3	G	Power Grounding	--
18	VCIX2	C	Stabilizing capacitor	Note
19	CYP	C	Booster capacitor	Note
20	CYN	C	Booster capacitor	Note
21	VCI	P	Booster input voltage pin	--
22	NC	N	Not Connected	--
23	GND4	G	Power Grounding	--
24	VCIM	C	Stabilizing capacitor	Note
25	CXP	C	Booster capacitor	Note
26	CXN	C	Booster capacitor	Note
27	NC	N	Not Connected	--
28	RESET	I	System reset pin	--
29	GND5	G	Power Grounding	--
30	VDDIO	P	Voltage input pin for logic I/O	--
31	VCORE	C	Stabilizing capacitor	Note
32	GND6	G	Power Grounding	--
33	NC	N	Not Connected	--
34	CSB	I	Chip select pin of serial interface	--
35	SDI	I	Data input pin in serial mode	--

36	SCK	I	Clock input pin in serial mode	--
37	NC	N	Not Connected	--
38	DEN	I	Display enable pin from controller	--
39	BB5	I	Blue Data Bit 5	--
40	BB4	I	Blue Data Bit 4	--
41	BB3	I	Blue Data Bit 3	--
42	BB2	I	Blue Data Bit 2	--
43	BB1	I	Blue Data Bit 1	--
44	BB0	I	Blue Data Bit 0	--
45	GG5	I	Green Data Bit 5	--
46	GG4	I	Green Data Bit 4	--
47	GG3	I	Green Data Bit 3	--
48	GG2	I	Green Data Bit 2	--
49	GG1	I	Green Data Bit 1	--
50	GG0	I	Green Data Bit 0	--
51	RR5	I	RED Data Bit 5	--
52	RR4	I	RED Data Bit 4	--
53	RR3	I	RED Data Bit 3	--
54	RR2	I	RED Data Bit 2	--
55	RR1	I	RED Data Bit 1	--
56	RR0	I	RED Data Bit 0	--
58	VSYNC	I	Frame synchronization signal	--
58	HSYNC	I	Line synchronization signal	--
59	DOTCLK	I	Dot-clock and oscillator source	--
60	CDMUO	C	Stabilizing capacitor	Note
61	GND7	G	Power Grounding	--
62	VLCD63	C	Stabilizing capacitor	Note
63	VCOMH	C	Stabilizing capacitor	Note
64	VCOML	C	Stabilizing capacitor	Note
65	GND7	G	Grounding for digital circuit	--
66	CSVCMP	C	Stabilizing capacitor	Note
67	CSVCMN	C	Stabilizing capacitor	Note

I: Input pin; P: Power pin; G: Ground pin; C: Capacitor pin; N: Not connected

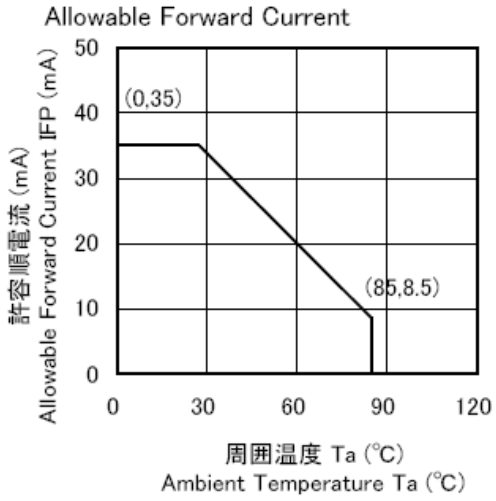
Note: IC pin connect to capacitor on FPCA. Open at FPC pin assignment.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VCI	-0.3	3.6	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		22	mA	One LED, Note 2

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



3. Electrical DC Characteristics

The following items are measured under stable condition and suggested application circuit.

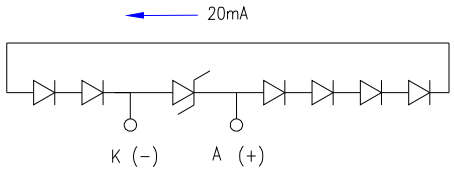
a.TFT- LCD Panel (GND=0V)

Parameter		Symbol	MIN	TYP	MAX	Unit	
Power Supply		VCI	3.0	3.3	3.6	V	
		VDDIO	3.0	3.3	3.6		
Frame Frequency		Hz		60		Hz	
Dot Data Clock		MH z	—	6.134	7.5	MH z	
Input Signal Voltage	VIH	V	0.8VDDIO	—	VDDIO	V	
	VIL	V	0	—	0.2VDDIO	V	
Current Consumption		mA	—	15	18	mA	

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		20	22	mA	single serial
LED Supply Voltage	V_L		(19.2)	21	V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



Note 2: The ”LED Supply Voltage” is defined by the number of LED at Ta=25˚C, I_L=20mA. In the case of 6 pcs LED, V_L=3.2*6=19.2V

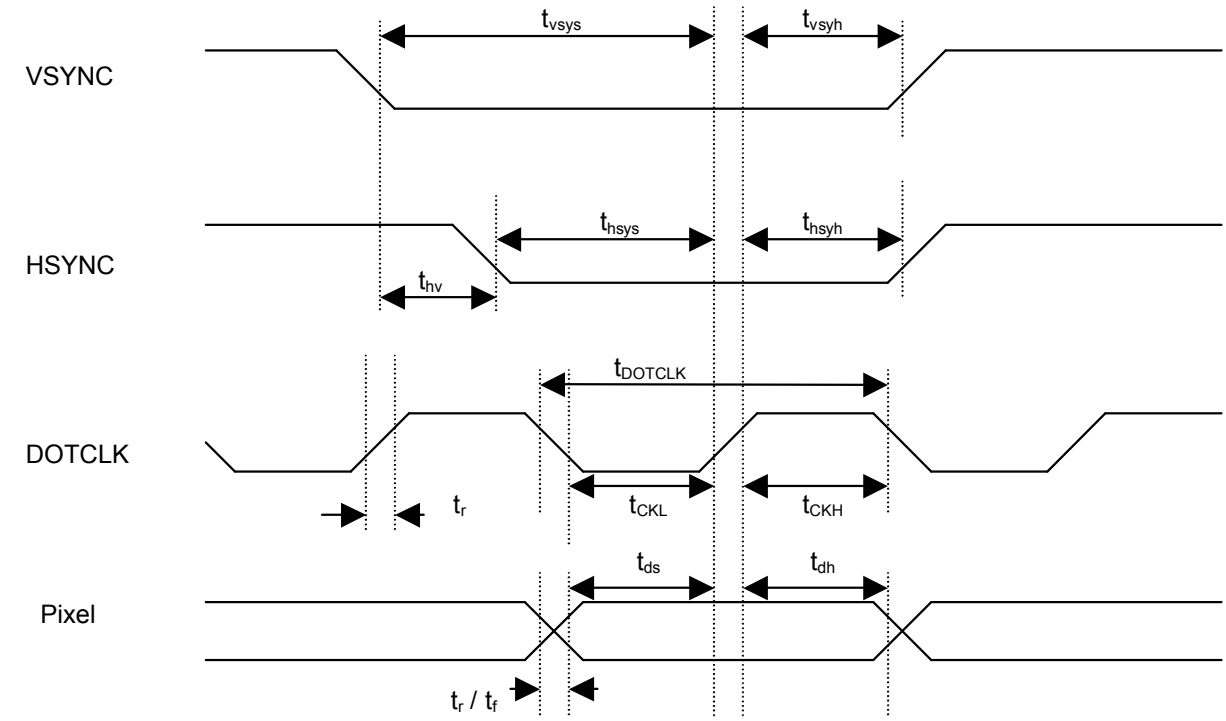
Note 3: The ”LED life time” is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25˚C, I_L=20mA

Note 4: The LED lifetime could be decreased if operating $I_L$is larger than 25mA

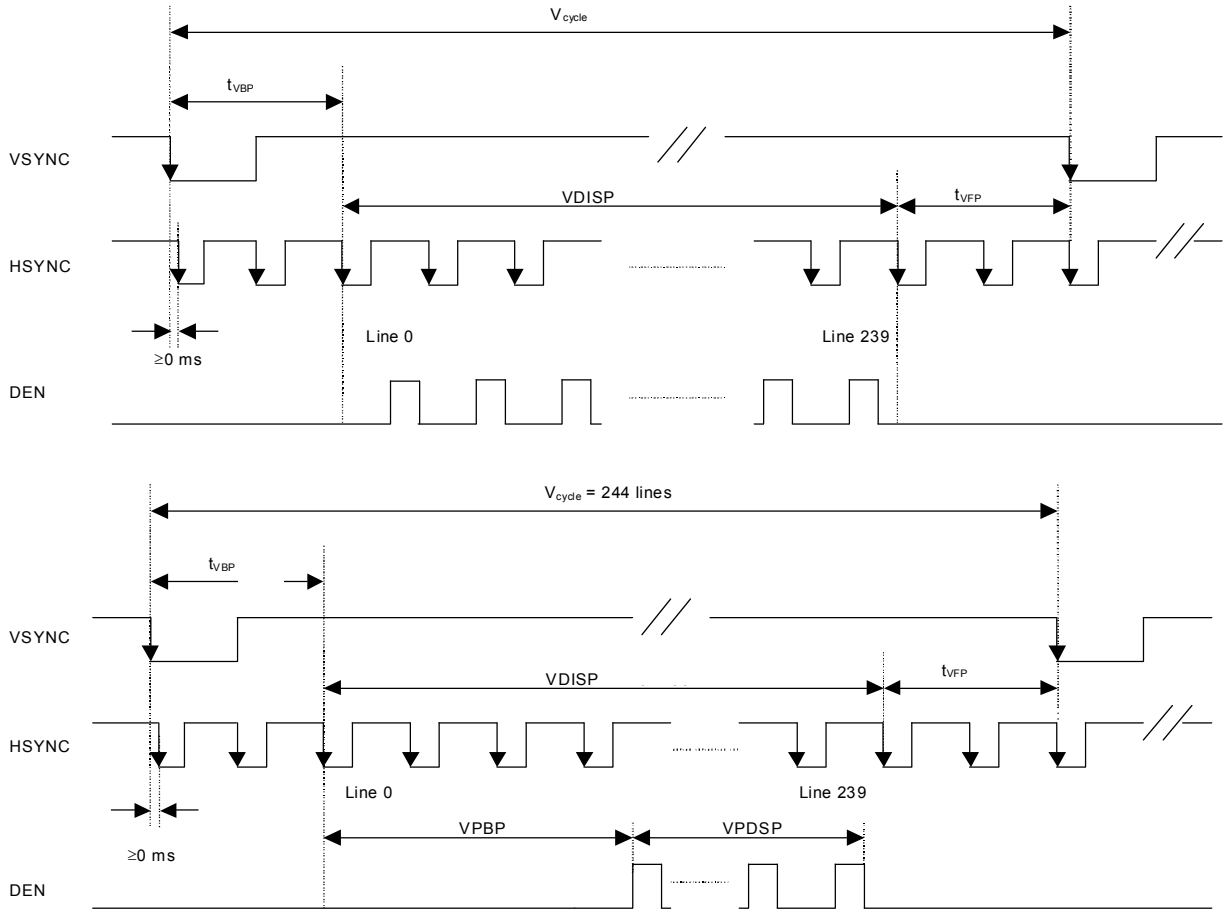
4. Electrical AC Characteristics

a. Signal AC Characteristics

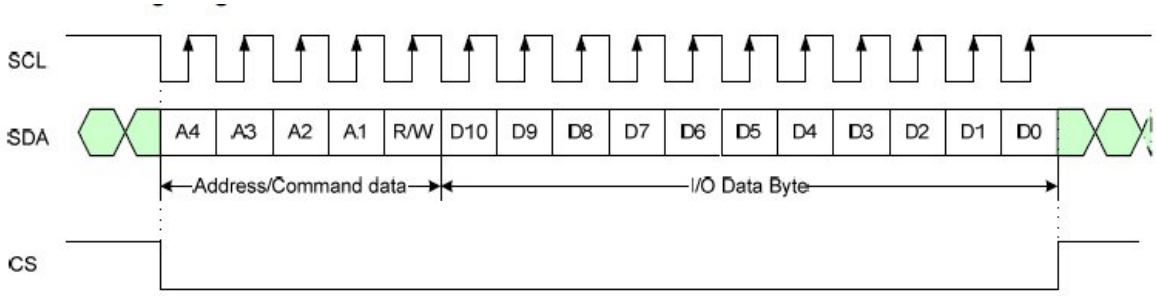
	Symbol	MIN	TYP	MAX	Unit	Note
DOTCLK Frequency	fDOTCLK	—	6.134	7.5	MHz	
DOTCLK Period	tDOTCLK	133.5	163	—	nSec	
Vsync Setup Time	tvsys	20	—	—	nSec	
Vsync Hold Time	tvsyh	20	—	—	nSec	
Hsync Setup Time	thsys	20	—	—	nSec	
Hsync Hold Time	thsyh	20	—	—	nSec	
DOTCLK Low Period Duty	tCKL	40	50	60	%	
DOTCLK High Period Duty	tCKH	40	50	60	%	
Data Setup Time	tds	30	—	—	nSec	
Data Hold Time	tdh	30	—	—	nSec	
Reset Pulse Width	tRES	50	—	—	uSec	



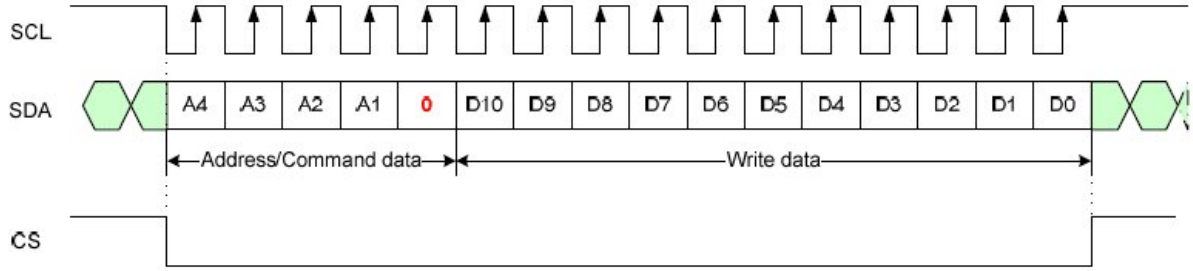
Parameter			Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK frequency			$1/t_{DCLK}$	5.3	6.134	7.5	MHz	
HSYNC	Period		t_H	377	390	476	t_{DCLK}	
	Display period		thd		320		t_{DCLK}	
	Back porch		thbp	50	61	63	t_{DCLK}	
	Front porch		thfp	7	9	93	t_{DCLK}	
	Pulse width		thsw	1	1	50	t_{DCLK}	
VSYNC	Period	Odd	t_V	247.5	262.5	276.5	t_H	
		Even						
	Display Period	Odd	tvd		240		t_H	
		Even						
	Back porch	Odd	tvbp	6	21	31	t_H	
		Even		6.5	21.5	31.5		
	Front porch	Odd	tvfp	1.5	1.5	-	t_H	
		Even		1	1	-		
	Pulse width		tvsw	1 t_{DCLK}	1 t_{DCLK}	$6t_H$		



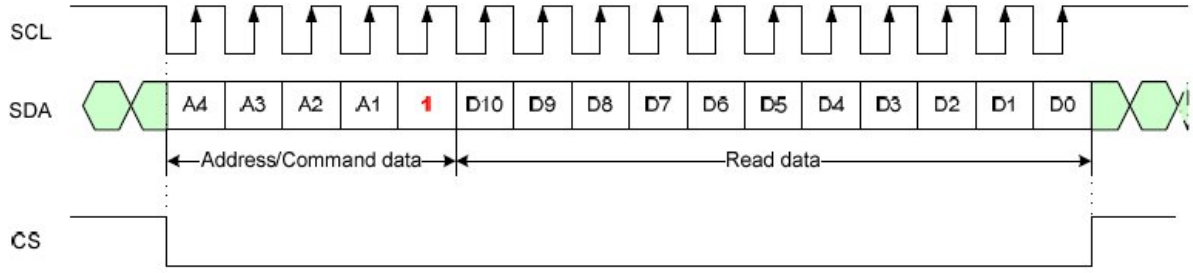
b. SPI Timing Diagram



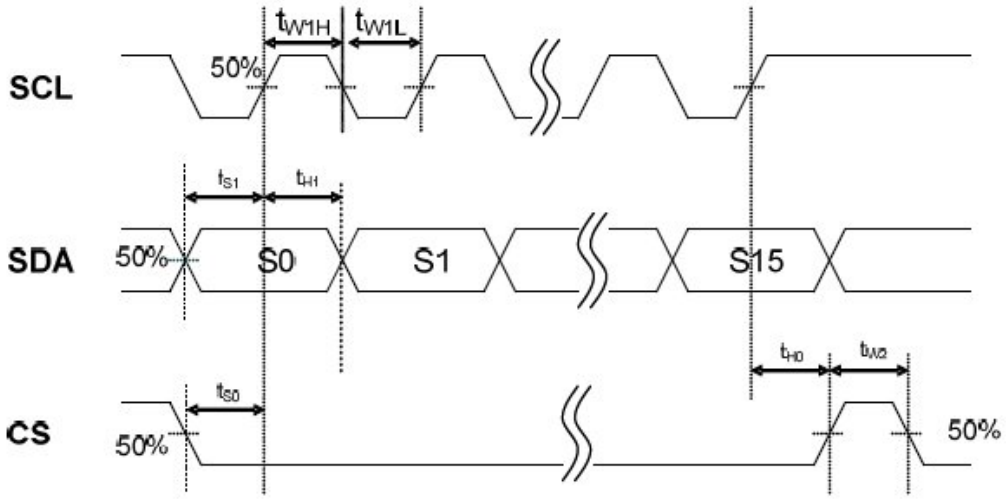
Write Mode:



Read Mode:



c.SPI Timing Specification



Item	Symbol	Min	Typical	Max	Unit
CS input setup Time	t_{S0}	50			ns
CS input hold Time	t_{H0}	50			ns
CS pulse high width	t_{W2}	1			us
Serial data input setup Time	t_{S1}	50			ns
Serial data input hold Time	t_{H1}	50			ns
SCL pulse low width	t_{W1L}	50			ns
SCL pulse high width	t_{W1H}	50			ns

5. Command Register Map

a. Serial Setting Map

- ( ) is suggested value

No.	Register address					MSB		Register data								LSB
	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	MODE (00)		0	0	0	UD (1)	SHL (1)	GRB (1)	STB (0)	SHDB (0)	SHCB (1)
R1	0	0	0	1	R/W	0	0	0	0	0	1	1	1	0	1	1
R2	0	0	1	0	R/W	0	0	0	HBLK (00111101)							
R3	0	0	1	1	R/W	0	0	0	0	0	0	VBLK (10101)				
R4	0	1	0	0	R/W	0	1	1	1	1	0	0	1	0	0	1
R5	0	1	0	1	R/W	0	0	0	0	0	0	0	1	0	0	0
R6	0	1	1	0	R/W	0	0	0	0	1	0	0	0	0	0	0
R7	0	1	1	1	R/W	0	0	0	0	0	0	0	VGL_SEL (11)		VGH_SEL (11)	
R8	1	0	0	0	R/W	0	0	0	1	VCOMH (0111011)						
R9	1	0	0	1	R/W	0	0	0	0	VCOML (0111100)						
R10	1	0	1	0	R/W	0	0	0	PWM_400K (0)	DC_F (1)	CLK_ChP_M (10)		0	1	1	0
R11	1	0	1	1	R/W	0	GMA_M (0)	GMA_V4 (010)			GMA_V1 (010)			GMA_V0 (011)		
R12	1	1	0	0	R/W	0	0	GMA_V48 (011)			GMA_V36 (011)			GMA_V16 (011)		
R13	1	1	0	1	R/W	0	0	0	0	0	GMA_V59 (011)			GMA_V55 (011)		
R14	1	1	1	0	R/W	0	0	0	0	0	GMA_V63 (010)			GMA_V62 (000)		
R15	1	1	1	1	R/W	0	0	0	0	0	VENDOR (00)		VERSION (0000)			

NOTE:

1. “0*”and “1*” is for engineering reserved register setting, and please follow the suggested value.
2. Please refer to our recommended register settings section for better performance.

b. Description of serial control data

R0 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	R/W	MODE (00)		0	0	0	UD (1)	SHL (1)	GRB (1)	STB (0)	SHDB (0)	SHCB (1)

MODE Vertical shift direction selection

UD	Function
D10~D9	
x0	HV Mode **(Default)**
x1	DE Mode

Note：If DE Mode, the minimun veritcal blanking number is 10.

UD: Vertical shift direction selection

UD	Function
D5	
0	Shift from down to up, Last line = G1←G2…G239←G240 = First line
1	Shift from up to down, First line = G1→G2…G239→G240 = Last line **(Default)**

SHL: Horizontal shift direction selection

SHL	Function
D4	
0	Shift from right to left, Last data = S1←S2…S959←S960 = First data
1	Shift from left to right, First data = S1→S2…S959→S960 = Last data **(Default)**

GRB: Global reset

GRB	Function
D3	
0	Reset all registers to default value
1	Normal operation **(Default)**

STB: Standby mode setting

STB	Function
D2	
0	Standby (Display OFF); timing control, DAC, and DC/DC converter are off, and register data should be kept **(Default)**
1	Normal operation (Display ON), with power on/off sequence

SHDB: DC-DC converter shutdown setting

SHDB	Function
D1	
0	DC-DC converter is off. **(Default)**
1	DC-DC converter is on. DC-DC controls by STB and power on/off sequence.

SHCB: Charge Pump shutdown setting

SHCB	Function
D0	
0	Charge Pump converter is off.
1	Charge Pump converter is on. **(Default)** Charge Pump controls by STB and power on/off sequence.

R2 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R2	0	0	1	0	R/W	0	0	1	HBLK (00111101)							

HBLK: Horizontal blanking setting.

HBLK(D7~D0)	HBLK	Unit	Remark
00110010	50	DCLK(*)	Parallel RGB
00111111	63		

R3 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R3	0	0	1	1	R/W	0	0	0	0	0	0	VBLK (10101)				

VBLK: Vertical blanking setting

VBLK(D4~D0)	VBLK	Unit
00001	1	t_H
11111	31	

R7 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R7	0	1	1	1	R/W	0	0	0	0	0	0	0	VGL_SEL (11)		VGH_SEL (11)	

VGL_SEL:VGL voltage selection

VGL_SEL	Function
D3~D2	
00	-8V
01	-9V
10	-10V**(Default)**
11	-11V

VGH_SEL:VGH voltage selection

VGH_SEL	Function
D1~D0	
00	12
01	13
10	14
11	15**(Default)**

R8 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R8	1	0	0	0	R/W	0	0	0	1	VCOMH (0111011)						

VCOMH: VCOMH level adjustment

VCOMH	Voltage(V)	
D6~D0	MVA/TN Normal	TN LV
00h	3.162	1.362
:	:	:
41h	4.332	2.532
:	:	:
7Fh	5.448	3.648

Note: Step is 18mV/step.

R9 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R9	1	0	0	1	R/W	0	0	0	0	VCOML (0111100)						

VCOML: VCOML level adjustment

VCOML	Voltage(V)	
D6~D0	MVA/TN Normal	TN LV
00h	-2.358	-2.628
:	:	:
41h	-1.188	-1.458
:	:	:
7Fh	-0.072	-0.342

Note: Step is 18mV/step.

R10 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R10	1	0	1	0	R/W	0	0	0	PWM_400K (0)	DC_F (1)	CLK_ChP_M (10)		0	1	1	0

PWM_400K: PWM frequency selection

PWM_400K	Function
D7	
0	Around 200KHz. **(Default)**
1	Around 400KHz.

DC_F: DCDC frequency selection

DC_F	Function
D6	
0	Operating frequency is base on 13.5MHz.
1	Operating frequency is base on 27MHz. **(Default)**

CLK_ChP_M: Charge pumping frequency selection

CLK_ChP_M	Function
D5~D4	
00	F(Chp)= f(Hsync)/2
01	F(Chp)= f(Hsync)
10	F(Chp)= f(Hsync)*2. **(Default)**
01	F(Chp)= f(Hsync)*4

R11~14 Register

No.	A4	A3	A2	A1	R/W	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R11	1	0	1	1	R/W	0	GMA_M (0)	GMA_V4 (010)			GMA_V1 (010)			GMA_V0 (011)		
R12	1	1	0	0	R/W	0	0	GMA_V48 (011)			GMA_V36 (011)			GMA_V16 (011)		
R13	1	1	0	1	R/W	0	0	0	0	0	GMA_V59 (011)			GMA_V55 (011)		
R14	1	1	1	0	R/W	0	0	0	0	0	GMA_V63 (010)			GMA_V62 (000)		

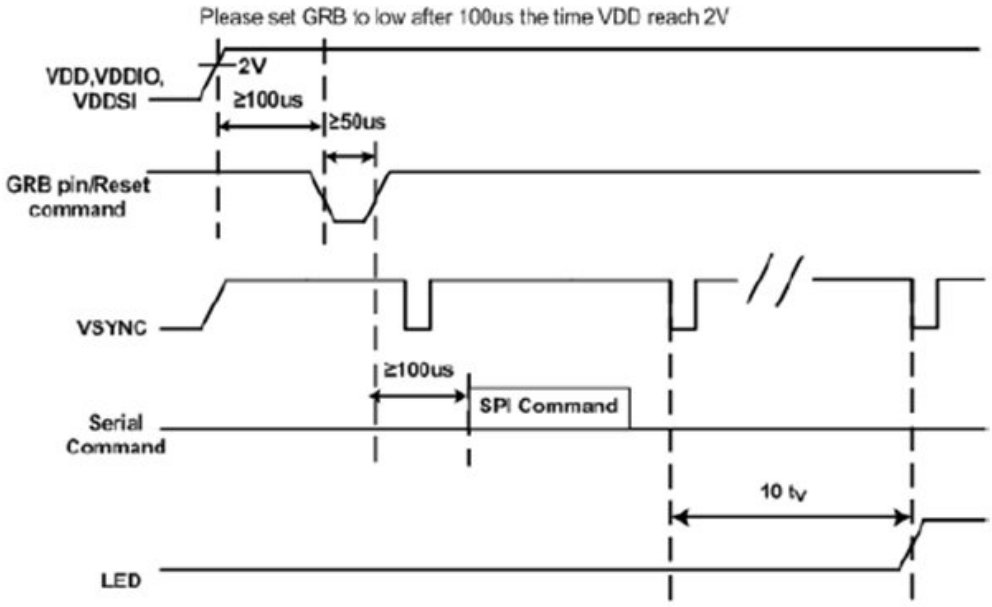
GMA_M: Gamma adjustment selection

GMA_M	Function
D9	
0	Manual adjust by registers R11~R14.
1	Auto set to gamma 2.2 by LC type. **(Default)**

6. Power On/Off Characteristics

a. Recommended Power On Sequence

Power On (Standby Enabling)

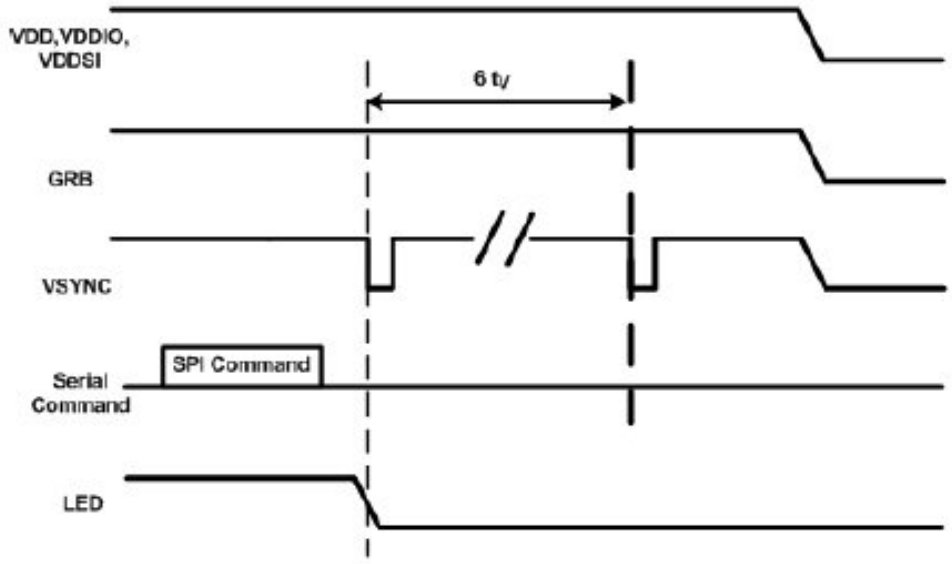


t_V: VSYNC Period

Note
1: After Setting Recommended Register, the driver enters intro the normal operating mode.
2: RESET signal is necessary for power on, Please refer to the POWER ON sequence.
You can use HW GRB PIN or SW Reset command to do this.
3: After the driver enters intro the normal operating mode, The minimum cycle time of LED ON is 10 frames.

b. Recommended Power Off Sequence

Power Off (Standy Enabling)



t_V: VSYNC Period

Note

1: After Setting Recommended Register, the driver enters intro standby mode.
2: Please Let LED OFF after the driver enters intro thestandby mode,
3: When enters intro standby mode, The minimum cycle time of VDD OFF is 6 frames.

D. Optical Specification

All optical specification is measured under typical condition (Note 1, 2)

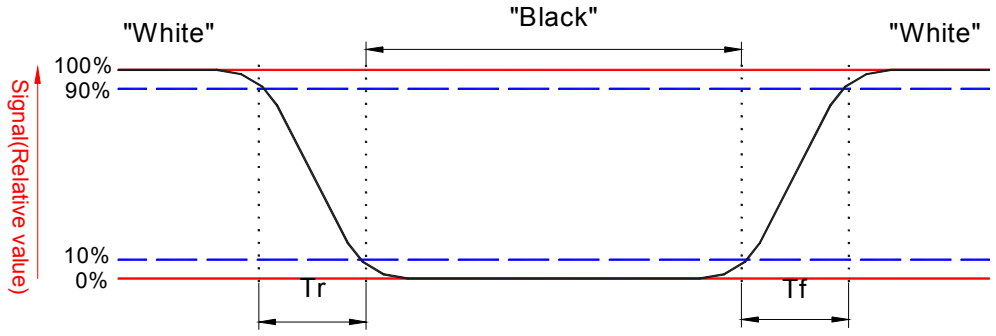
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ=0°	-	10	15	ms	Note 3
Fall	Tf		-	15	30	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ=0°	350	430	-	cd/m^2	Note 9
NTSC			50	60		%	
White Chromaticity	X	θ=0°	0.26	0.31	0.36		
	y	θ=0°	0.28	0.33	0.38		

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25˚C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25˚C.

Note 5. Contrast ratio is calculated with the following formula.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White Vi=Vi50 μ 1.5V

Black Vi=Vi50 ± 2.0V

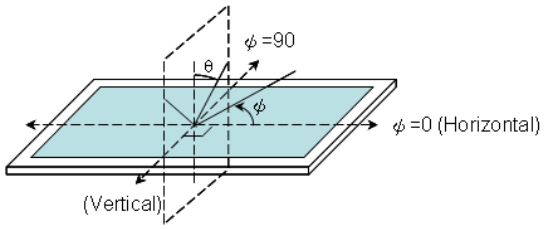
"±" means that the analog input signal swings in phase with COM signal.

"μ" means that the analog input signal swings out of phase with COM signal.

Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Brightness is measured at the center point of the display area.

E. Reliability Test Items

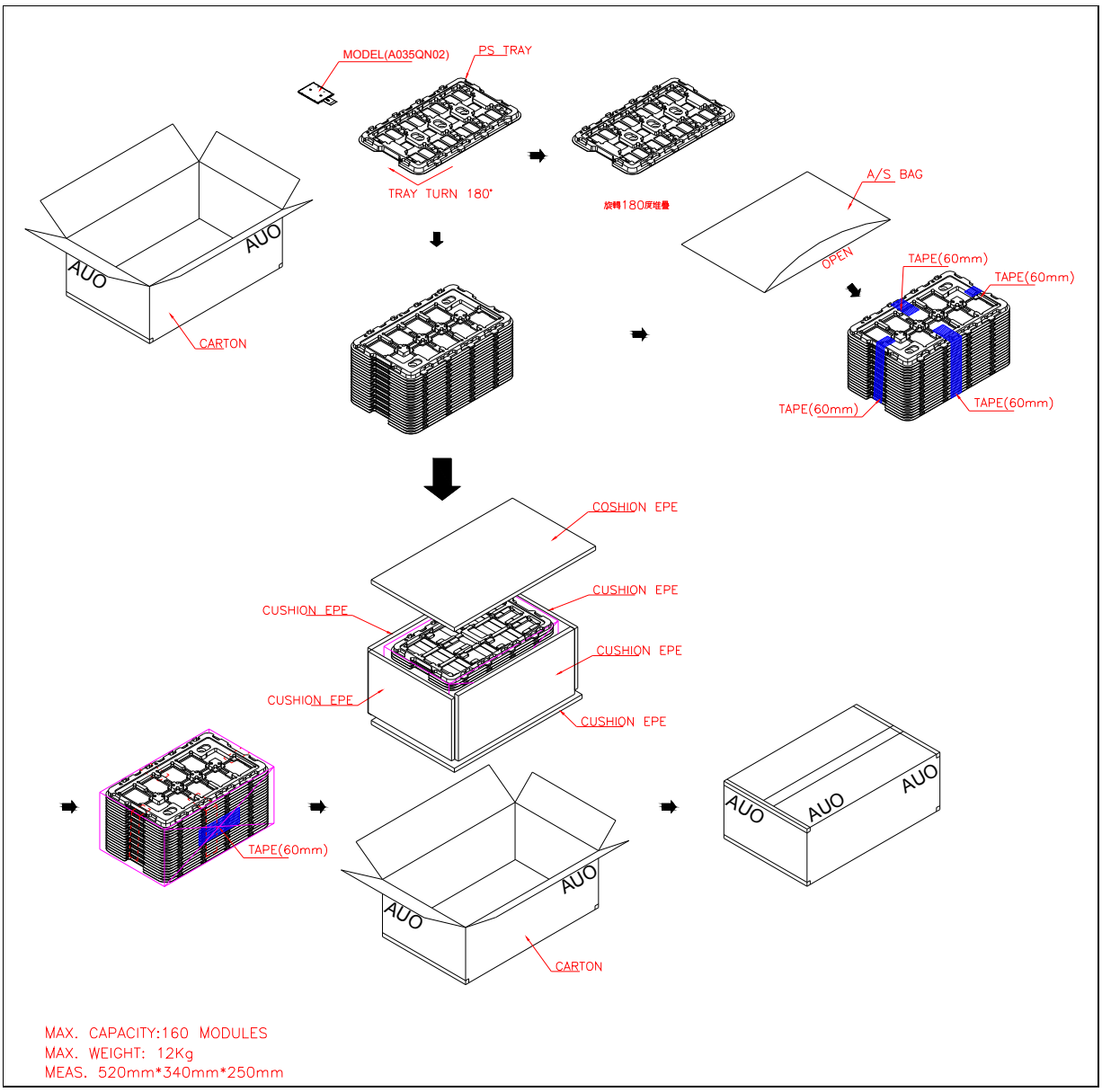
No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80℃ 240Hrs	
2	Low Temperature Storage	Ta= -40℃ 240Hrs	
3	High Ttemperature Operation	Tp= 70℃ 240Hrs	
4	Low Temperature Operation	Ta= -20℃ 240Hrs	
5	High Temperature & High Humidity	Tp= 60℃. 90%RH 240Hrs	Operation
6	Heat Shock	-25℃~70℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	Contact = ± 4 kV, class B Air = ± 8 kV, class B	Note 5
8	Vibration	Frequency range: 10Hz~55Hz Stoke: 1.5mm Sweep: 10Hz~55Hz~10Hz ±x, ±y, ±z 2 hours for each axis	Non-operation JIS C7021, A-10 condition A: 15 minutes
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021,A-7 condition C
10	Vibration (With Carton)	Random vibration: $0.015G^2$/Hz from 5~200Hz –6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	
12	Pressure	5kg, 5sec	Note 6

Note 1: In the standard conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2: Ta: Ambient temperature.

Note 3: According to EN61000-4-2, ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

F. Packing and Marking



G. Application note

1.Recommended Register Settings

8-bit Serial Interface HV Sync.

Power On

No.	Command		NOTE
	High byte	Low byte	
1	00h	31h	NOTE1
Whait 50 us			
2	00h	39h	
Whait 100 us			
3	10h	3Bh	NOTE2
4	20h	3Dh	
5	30h	15h	
6	43h	C9h	
7	50h	08h	
8	60h	40h	
9	70h	0Fh	
10	80h	BCh	
11	90h	3Dh	
12	A0h	66h	
13	B0h	93h	
14	C0h	DBh	
15	D0h	1Bh	
16	E0h	10h	
17	00h	3Dh	

Power Off

No.	Command		NOTE
	High byte	Low byte	
1	00h	39h	NOTE3

NOTE 1. Please add these commands if you don't use the HW Reset.

NOTE 2. Please refer to the POWER ON sequence section for register setting timing as power-on.

NOTE 3. Please refer to the POWER OFF sequence section for register setting timing as power-off.

H. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.
8. Be sure to turn off the power when connecting or disconnecting the circuit.
9. Polarizer scratches easily, please handle it carefully.
10. Display surface never likes dirt or stains.
11. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
12. Sudden temperature changes cause condensation, and it will cause polarizer damaged.
13. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
14. Acetic acid or chlorine compounds are not friends with TFT display module.
15. Static electricity will damage the module, please do not touch the module without any grounded device.
16. Do not disassemble and reassemble the module by self.
17. Be careful do not touch the rear side directly.
18. No strong vibration or shock. It will cause module broken.
19. Storage the modules in suitable environment with regular packing.
20. Be careful of injury from a broken display module.
21. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.