



Doc. Version	0.8
Total Page	33
Date	2007/03/20

# Product Specification

## 3.5" COLOR TFT-LCD MODULE

**MODEL NAME: A035QN02 V0**

< ◆ > Preliminary Specification

< > Final Specification

Note: The content of this specification is subject to change.

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## Record of Revision

Version	Revise Date	Page	Content																								
0.0	2006/10/20		First draft.																								
0.1	2006/10/24	11	E-4-a. Update AC timing condition																								
		14	E-5-d. Update SPI I/F timing condition																								
		23	J-1. Add application circuit																								
		24	J-1. Add component BOM list for the application circuit																								
0.2	2006/11/14	4	Update module thickness to 4.0mm (original 4.1mm)																								
		4	Add description of gray level inversion																								
		5	Update mechanical drawing																								
		6, 7	Pin assignment revised from 61 pins to 67 pins																								
		10, 11	Update power On/Off sequence																								
		19	Add panel FPC bending test, touch panel FPC peeling test & touch panel impact resistance criteria																								
		22	Update the cushion area illustration																								
		24	Update application circuit																								
0.3	2006/11/15	6	Correct the pin description, Pin 8 DGND2 → AGND1																								
		8	Update the LED curve																								
0.4	2006/11/27	5	Update the drawing																								
0.5	2006/12/04	5	Update the drawing																								
			<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 60%;">Item</th> <th style="width: 20%;">Original</th> <th style="width: 20%;">Updated</th> </tr> </thead> <tbody> <tr> <td>FPC thickness</td> <td>0.360.05mm</td> <td>0.260.03mm</td> </tr> <tr> <td>Module Left edge to suggested bezel open area left edge</td> <td>2.76mm</td> <td>2.71mm</td> </tr> <tr> <td>Module left edge to TP A/A left edge</td> <td>3.16mm</td> <td>3.11mm</td> </tr> <tr> <td>Module left edge to LCD A/A left edge</td> <td>3.46mm</td> <td>3.41mm</td> </tr> <tr> <td>Module upper edge to suggested bezel open area upper edge</td> <td>2.82mm</td> <td>2.77mm</td> </tr> <tr> <td>Module upper edge to TP A/A upper edge</td> <td>3.22mm</td> <td>3.17mm</td> </tr> <tr> <td>Module upper edge to LCD A/A upper edge</td> <td>3.52mm</td> <td>3.47mm</td> </tr> </tbody> </table>	Item	Original	Updated	FPC thickness	0.360.05mm	0.260.03mm	Module Left edge to suggested bezel open area left edge	2.76mm	2.71mm	Module left edge to TP A/A left edge	3.16mm	3.11mm	Module left edge to LCD A/A left edge	3.46mm	3.41mm	Module upper edge to suggested bezel open area upper edge	2.82mm	2.77mm	Module upper edge to TP A/A upper edge	3.22mm	3.17mm	Module upper edge to LCD A/A upper edge	3.52mm	3.47mm
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Update drawing, add label location, size and thickness																											
0.6	2006/12/15	5	Update drawing, add label location, size and thickness																								
0.7	2007/01/29	4	Update module dimension (Thickness 4mm → 4.32mm)																								
		5	Update drawing, modify thickness																								
		14	Update command register map, add detailed descriptions																								
0.8	2007/03/20	5	Update the module weight																								

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## A. General Description

A035QN02 V0 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, a driver, an FPC (flexible printed circuit), a backlight unit and a touch panel.

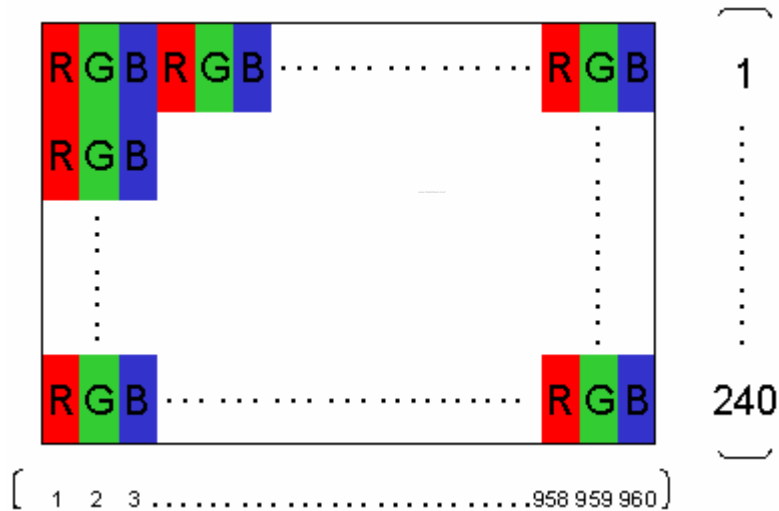
## B. Features

- 3.5-inch display with touch panel
- QVGA resolution in RGB stripe dot arrangement
- DC/DC integrated
- High brightness
- 3-wire register setting
- Interfaces: parallel RGB 18-bit
- Wide viewing angle
- Integrated touch screen panel (resistive type)
- 3-in-1 FPC for LCD signals, backlight LED power and touch panel
- Green design

### C. Physical Specifications

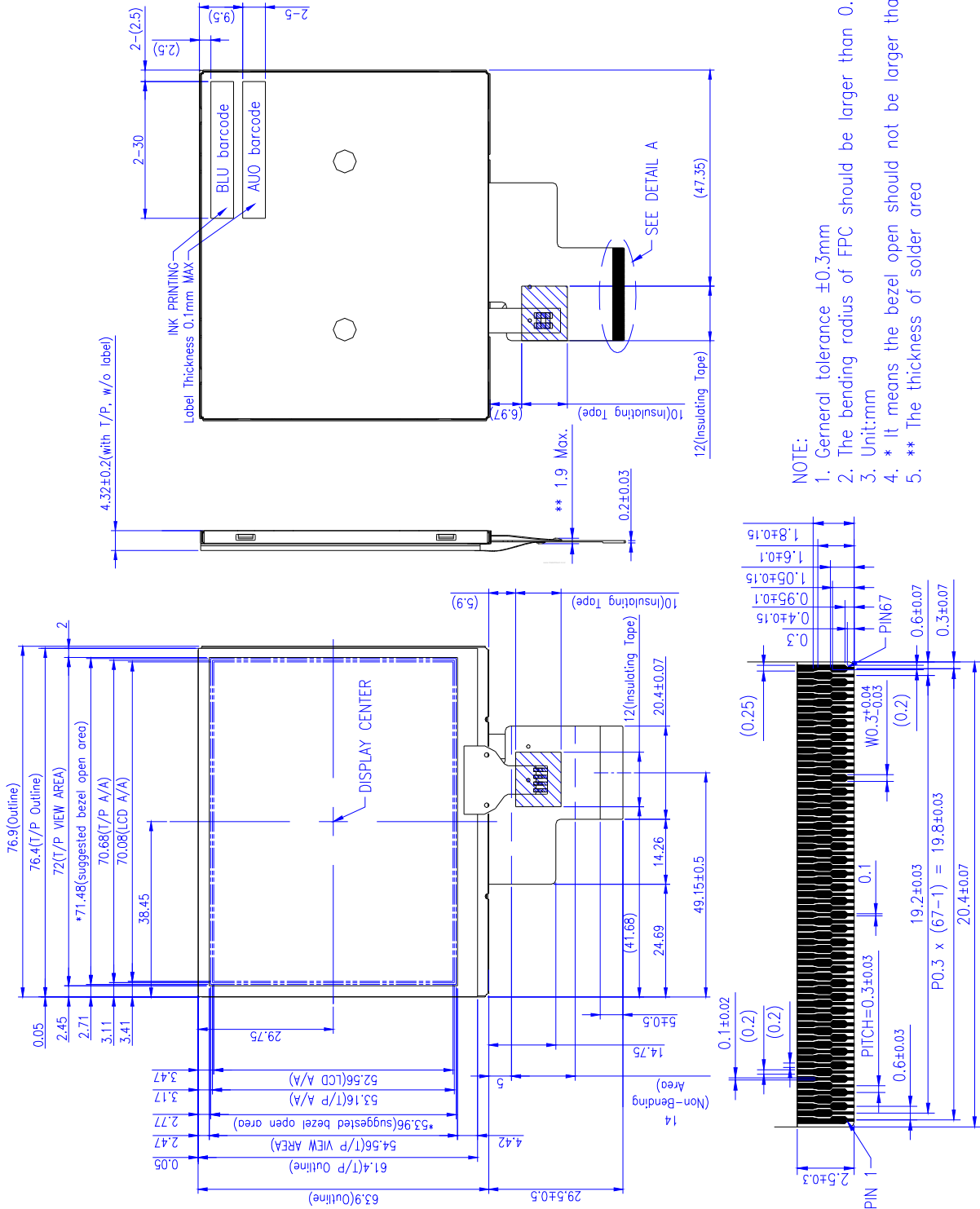
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 4.32(T)	Note 2
8	Weight	g	40	
9	Panel surface treatment	--	Hard coating 3H	
10	Display Mode	--	Normally White	
11	Gray Level Inversion Direction		6 O'clock	

Note 1: Below figure shows dot stripe arrangement.



Note 2: Not including FPC. Refer to the drawing next page for further information.

### D. Outline Dimension



## E. Electrical Specifications

### 1. Pin Assignment

Connector type: FH26G 67pin 0.3mm pitch connector

No.	Pin Name	I/O	Description	Remarks
1	LED_C	PI	Cathode for LED back-light	
2	LED_A	PI	Anode for LED back-light	
3	DGND1	G	Grounding for digital circuit	
4	X1	O	Touch Panel Right Electrode	
5	Y2	O	Touch Panel Bottom Electrode	
6	X2	O	Touch Panel Left Electrode	
7	Y1	O	Touch Panel Top Electrode	
8	AGND1	G	Grounding for digital circuit	
9	VGH	C	Stabilizing capacitor	
10	C2P	C	Booster capacitor	
11	C2N	C	Booster capacitor	
12	C1P	C	Booster capacitor	
13	C1N	C	Booster capacitor	
14	VGL	C	Stabilizing capacitor	
15	C3N	C	Booster capacitor	
16	C3P	C	Booster capacitor	
17	AGND2	G	Grounding for analog circuit	
18	VCIX2	C	Stabilizing capacitor	
19	CYP	C	Booster capacitor	
20	CYN	C	Booster capacitor	
21	VCI	PI	Booster input voltage pin	
22	NC	N	Not Connected	
23	AGND3	G	Grounding for analog circuit	
24	VCIM	C	Booster capacitor	
25	CXP	C	Booster capacitor	
26	CXN	C	Booster capacitor	
27	CM	I	Input pinto select 262k- or 8-color mode	
28	RESET	I	System reset pin	
29	DGND2	G	Grounding for digital circuit	
30	VDDIO	PI	Voltage input pin for logic I/O	
31	VCORE	C	Stabilizing capacitor	
32	DGND3	G	Grounding for logic I/O	

33	SHUT	I	Display shut-down pin for sleep-mode	
34	CSB	I	Chip select pin of serial interface	
35	SDI	I	Data input pin in serial mode	
36	SCK	I	Clock input pin in serial mode	
37	VDROP	C	Stabilizing capacitor	
38	DEN	I	Display enable pin from controller	
39	BB5	I	Blue data	
40	BB4	I	Blue data	
41	BB3	I	Blue data	
42	BB2	I	Blue data	
43	BB1	I	Blue data	
44	BB0	I	Blue data	
45	GG5	I	Green data	
46	GG4	I	Green data	
47	GG3	I	Green data	
48	GG2	I	Green data	
49	GG1	I	Green data	
50	GG0	I	Green data	
51	RR5	I	Red data	
52	RR4	I	Red data	
53	RR3	I	Red data	
54	RR2	I	Red data	
55	RR1	I	Red data	
56	RR0	I	Red data	
57	VSYNC	I	Frame synchronization signal	
58	HSYNC	I	Line synchronization signal	
59	DOTCLK	I	Dot-clock and oscillator source	
60	CDMUO	C	Stabilizing capacitor	
61	DGND4	G	Grounding for digital circuit	
62	VLCD63	C	Stabilizing capacitor	
63	VCOMH	C	Stabilizing capacitor	
64	VCOML	C	Stabilizing capacitor	
65	DGND5	G	Grounding for digital circuit	
66	CSVCMPI	C	Stabilizing capacitor	
67	CSVCMNI	C	Stabilizing capacitor	

I: Digital signal input, O: Digital signal output, G: GND, PI: Power input, C: Capacitor

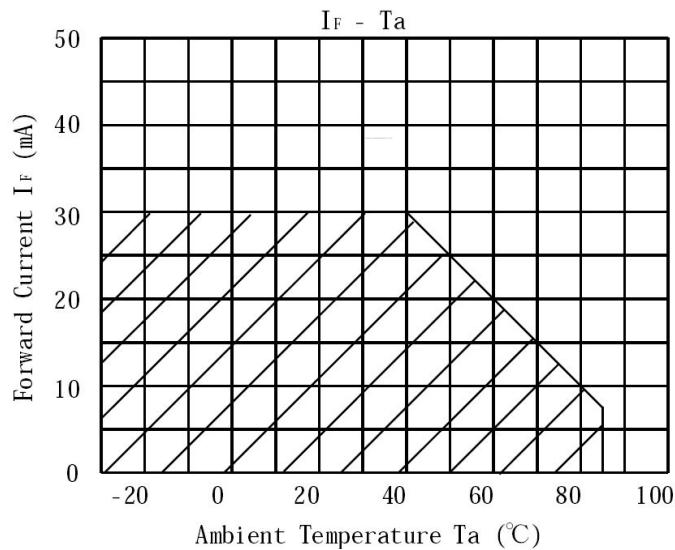


## 2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VDDIO	1.8	3.6	V	
	VCI	2.5	3.6	V	
Input Signal Voltage	Vi	0	0.2 x VDDIO	V	
	VI	0.8 x VDDIO	VDDIO	V	
LED Reverse Voltage	Vr		2	V	One LED
LED Forward Current	If		30	mA	One LED, Note 2
Operating Temperature (Ta)	T <sub>OP</sub>	-20	70	°C	Note 3
Storage Temperature	T <sub>ST</sub>	-30	85	°C	Note 3

Note 1. If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



Note 3. 90% RH maximum humidity when temp. ≤60°C.

If temp. >60°C, the absolute humidity maximum shall be less than 90% RH.

### 3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

#### a. TFT- LCD Panel (GND=0V)

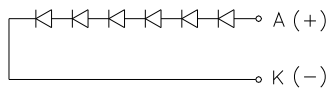
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VDDIO	1.8	3.3	3.6	V	
Analog Power Supply	VCI	2.5	3.3	3.6	V	
Frame Frequency	$f_{Frame}$		60		Hz	
Dot Data Clock	DCLK		5		MHz	

Note 1. Panel surface temperature should be kept less than content of section 3.2. "Absolute maximum ratings"

#### b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	$I_L$		20		mA	single serial
LED Supply Voltage	$V_L$		19.2		V	single serial
LED Life Time	$L_L$	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



Note 2: The "LED Supply Voltage" is defined by the number of LED at  $T_a=25^{\circ}C$ ,  $I_L=20mA$ . In the case of 6 pcs LED,  $V_L=3.2*6=19.2V$

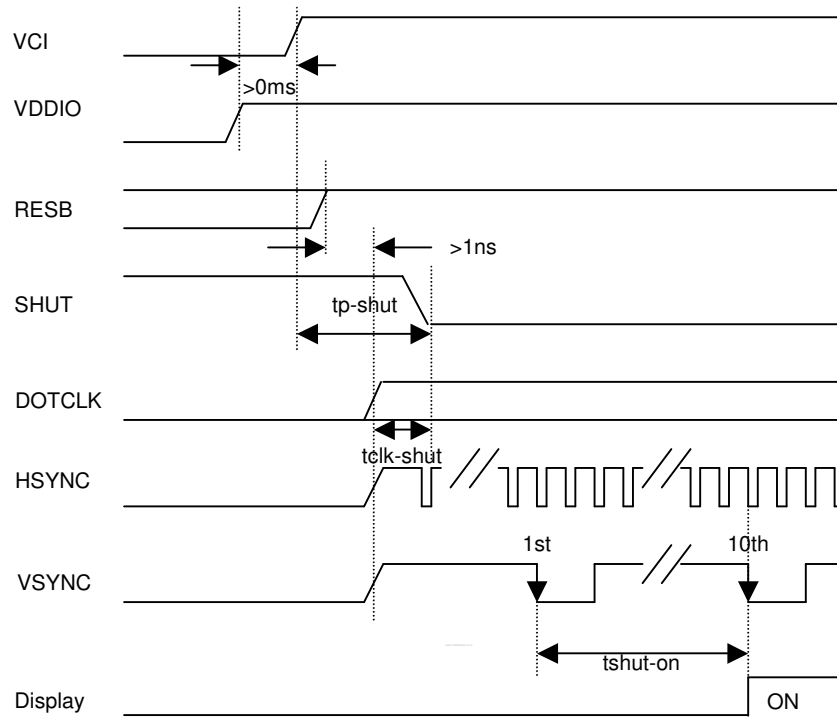
Note 3: The "LED life time" is defined as the time for the module brightness to decrease to 50% of the initial value at  $T_a=25^{\circ}C$ ,  $I_L=20mA$

Note 4: The LED lifetime could be decreased if operating  $I_L$  is larger than 25mA

## 4. AC Timing

### a. Power on/off sequence

#### Power On

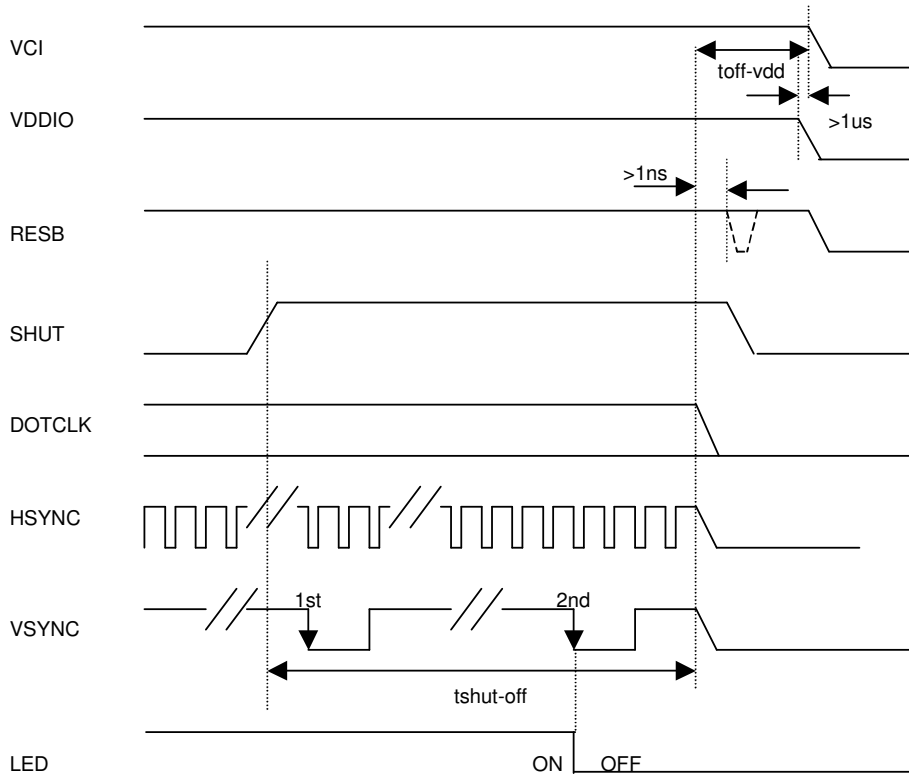


Characteristics	Symbol	Min	Typ	Max	Unit
VDDIO on to falling edge of SHUT	tp-shut	1			uSec
DOTCLK	tclk-shut	1			clk
Falling edge of SHUT to display on	tshut-on			10	frame
-- 1 line: 336 clk					
-- 1frame: 244 line			164		mSec
-- DOTCLK = 5.0 MHz					

**Note1:** It is necessary to input DOTCLK before the falling edge of SHUT.

**Note2:** Display starts at 10<sup>th</sup> falling edge of VSTNC after the falling edge of SHUT

**Power Off**



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off	tshut-off	2		10	frame
-- 1 line: 336 clk		32.8			mSec
-- 1frame: 244 line					
-- DOTCLK = 5.0 MHz					
Input-signal-off to V <sub>DDEXT</sub> / V <sub>DDIO</sub> off	toff-vdd	1			uSec

**Note1:** DOTCLK must be maintained at least 2 frames after the rising edge of SHUT.

**Note2:** Display become off at the 2<sup>nd</sup> falling edge of VSTNC after the falling edge of SHUT.

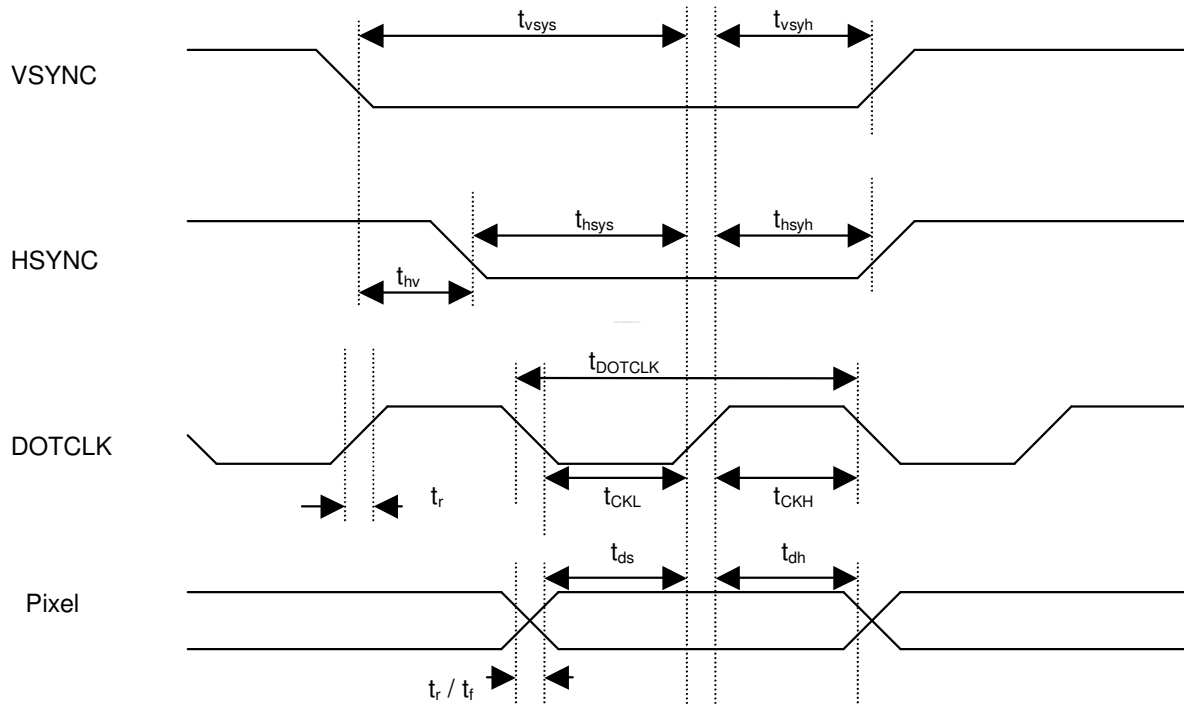
**Note3:** If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

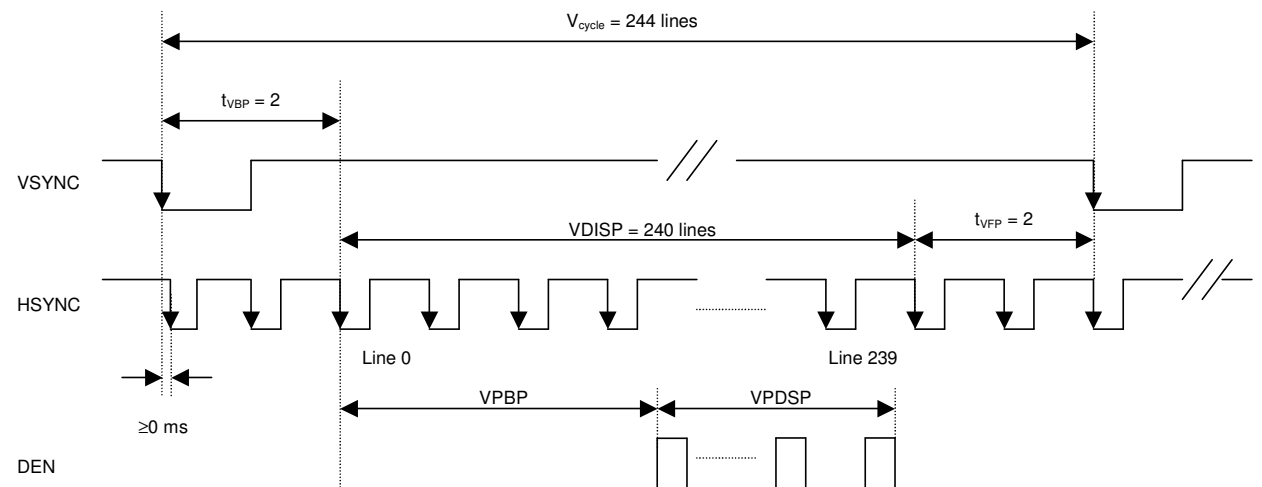
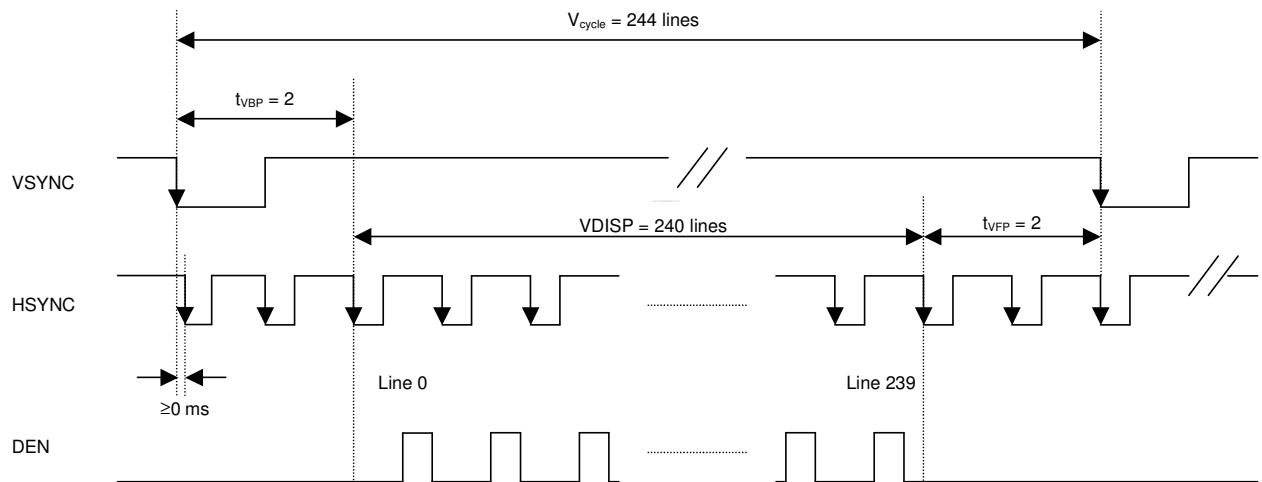
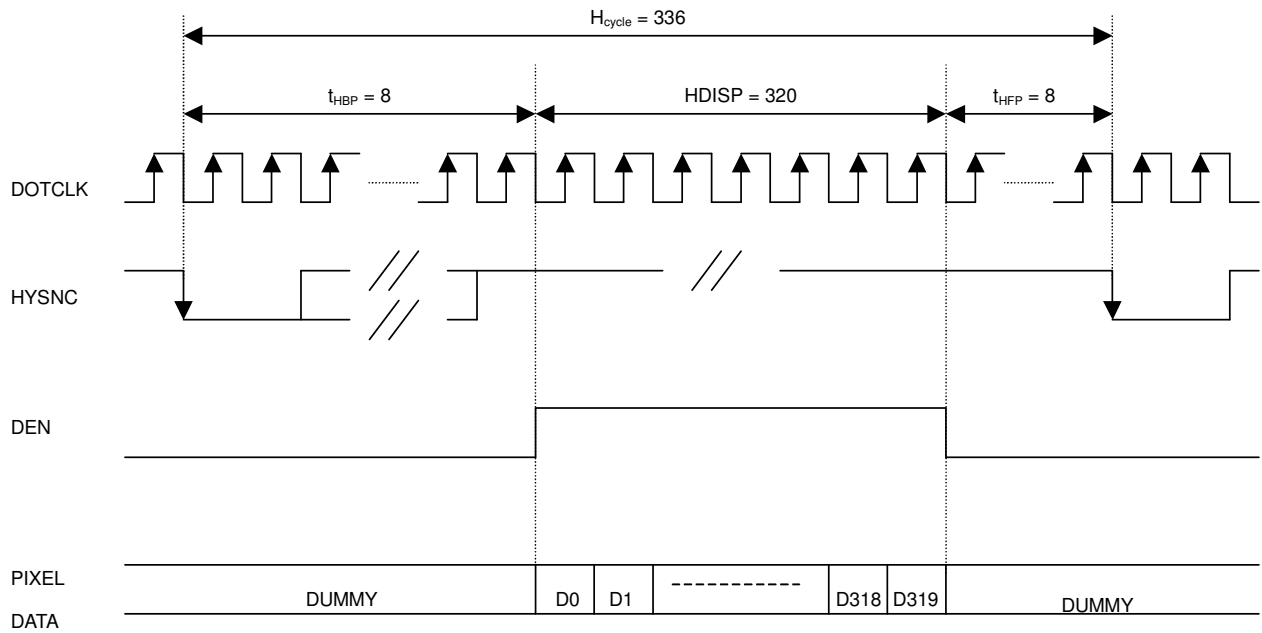
**b. Timing Condition**

Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f <sub>DOTCLK</sub>		5.0	7.5	MHz
DOTCLK Period	t <sub>DOTCLK</sub>	133	200		nSec
Vsync Setup Time	t <sub>vsys</sub>	20			nSec
Vsync Hold Time	t <sub>vsyh</sub>	20			nSec
Hsync Setup Time	t <sub>hsys</sub>	20			nSec

Hsync Hold Time	$t_{hsyh}$	20			nSec
Phase Difference of Sync Signal Falling Edge	$t_{hv}$	0		320	$t_{DOTCLK}$
DOTCLK Low Period	$t_{CKL}$	66.5			nSec
DOTCLK High Period	$t_{CKH}$	66.5			nSec
Data Setup Time	$t_{ds}$	40			nSec
Data Hold Time	$t_{dh}$	40			nSec
Reset Pulse Width	$t_{RES}$	10			nSec
Rise / Fall Time	$t_r/t_f$	20		100	nSec

**c. Timing Diagram**





NOTE: The falling edge of HSYNC belongs to blanking period is always behind or equal to the one of VSYNC.

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## 5. Command Register Map

### a. Serial setting map

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output control	0	1	0	0	REV	CAD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	X	X	X	0	X	X	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	0	0	0	B/C	ERO	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0300h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(7272h)			0	1	1	1	0	0	1	0	0	1	1	1	0	0	1	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	0	0	0	0	0	0	0	0
	(DC00h)			1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
R0Fh	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R16h	Horizontal porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
R2Eh	3 Gamma	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	OLO
	(B945h)			1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1
R30h	y control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	y control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	y control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	y control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

R34h	y control (1)	0	1	0	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	y control (1)	0	1	0	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20
	(0202h)			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	y control (1)	0	1	0	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	y control (1)	0	1	0	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R3Ah	y control (2)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	
R3Bh	y control (2)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	

**b. Description of serial control data**

R01h	Driver output control	0	1	0	0	REV	CAD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	X	X	X	0	X	X	1	1	1	0	1	1	1	1

**REV:** Displays all character and graphic display sections with reversal when REV = "1".

Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Source output level is indicated below.

REV	RGB data	Source Output level	
		VCOM = "H"	VCOM = "L"
1	000000B	V63	V0
	111111B	V0	V63
0	000000B	V0	V63
	111111B	V63	V0

**CAD:** Set up based on retention capacitor configuration of the TFT panel.

CAD	Retention capacitor configuration
0	Cs on Common
1	Cs on Gate

**BGR:** Selects the <R><G><B> arrangement.

When BGR = "0" <R><G><B> color is assigned from S0. When BGR = "1" <B><G><R> color is assigned from S0.

**SM:** Change the division of gate driver.



When SM = "0", odd/even division (interlace mode) is selected. When SM = "1", upper/lower division is selected.

Select the division mode according to the mounting method.

**TB:** Selects the output shift direction of the gate driver.

When TB = "1", G0 shifts to G239. When TB = "0", G239 shifts to G0.

**RL:** Selects the output shift direction of the source driver.

When RL = "1", S0 shifts to S959 and <R><G><B> color is assigned from S1.

When RL = "0", S959 shifts to S0 and <R><G><B> color is assigned from S959.

Set RL bit and BGR bit when changing the dot order of R, G and B.

**Note:** The default setting of register bits *REV*, *CAD*, *BGR*, *TB* and *RL* are defined by the logic stage of corresponding hardware pins.

These bits will override the hardware setting once software command was sent to set the bits.

R02h	LCD drive AC control	0	1	0	0	0	0	0	0	0	B/C	ERO	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0300h)			0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

**B/C:** Select the liquid crystal drive waveform VCOM.

When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

**EOR:** When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive.

EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

**NW6-0:** Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW6-0 alternate for every set value + 1 lines.

R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(7272h)			0	1	1	1	0	0	1	0	0	1	1	1	0	0	1	0

**DCT3-0:** Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO).

When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too.

Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2

1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96
1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

**BT2-0:** Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V <sub>GH</sub> output	V <sub>GL</sub> output	V <sub>GH</sub> booster ratio	V <sub>GL</sub> booster ratio
0	0	0	V <sub>CIX2</sub> ×3	-( V <sub>CIX2</sub> ×3)+V <sub>CI</sub>	6	-5
0	0	1	V <sub>CIX2</sub> ×3	-( V <sub>CIX2</sub> ×2)	6	-4
0	1	0	V <sub>CIX2</sub> ×3	-( V <sub>CIX2</sub> ×3)	6	-6
0	1	1	V <sub>CIX2</sub> ×2+V <sub>CI</sub>	-( V <sub>CIX2</sub> ×3)+V <sub>CI</sub>	5	-5
1	0	0	V <sub>CIX2</sub> ×2+V <sub>CI</sub>	-( V <sub>CIX2</sub> ×2)	5	-4
1	0	1	V <sub>CIX2</sub> ×2+V <sub>CI</sub>	-( V <sub>CIX2</sub> ×2)+V <sub>CI</sub>	5	-3
1	1	0	V <sub>CIX2</sub> ×2	-( V <sub>CIX2</sub> ×2)	4	-4
1	1	1	V <sub>CIX2</sub> ×2	-( V <sub>CIX2</sub> ×2)+V <sub>CI</sub>	4	-3

**DC3-0:** Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS).

When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too.

Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96

1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

**AP2-0:** Adjust the amount of current from the stable-current source in the internal operational amplifier circuit.

When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase.

Adjust the current taking into account the power consumption.

During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	0	0	0	0	0	0	0
	(DC00h)			1	1	0	1	1	1	0	0	0	0	0	0	0	0	0

**NO1-0:** Sets amount of non-overlap of the gate output.

**SDT1-0:** Set delay amount from the gate output signal falling edge of the source outputs.

**EQ1-0:** Sets the equalizing period on source

R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

**VRC[2:0]:** Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	V <sub>Clx2</sub> voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

**VRH3-0:** Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 1.78 to 3.00 times the Vref voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	VLCD63 Voltage
0	0	0	0	Vref x 2.815
0	0	0	1	Vref x 2.905
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

**VCOMG:** When VCOMG = "1", it is possible to set output voltage of VCOML to any level, and the instruction (VDV4-0) becomes available.

When VCOMG = "0", VCOML output is fixed to Hi-z level, VCI2 output for VCOML power supply stops, and the instruction (VDV4-0) becomes unavailable.

Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

**VDV4-0:** Set the alternating amplitudes of VCOM at the VCOM alternating drive.

These bits amplify VCOM amplitude 0.6 to 1.23 times the VLCD63 voltage.

When VCOMG = "0", the settings become invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOMA
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
:					Step = 0.03
:					

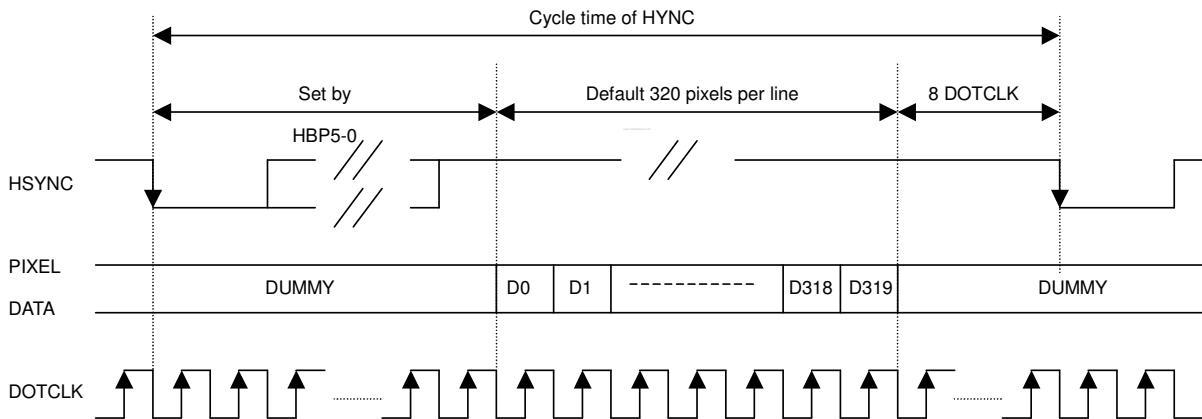


1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved

**HBP5-0:** Set the delay period from falling edge of HSYNC signal to first valid data.

The pixel data exceed the range set by XL8-0 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	# of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
:						:
:						step = 1
:						:
1	1	1	1	1	0	64
1	1	1	1	1	1	65



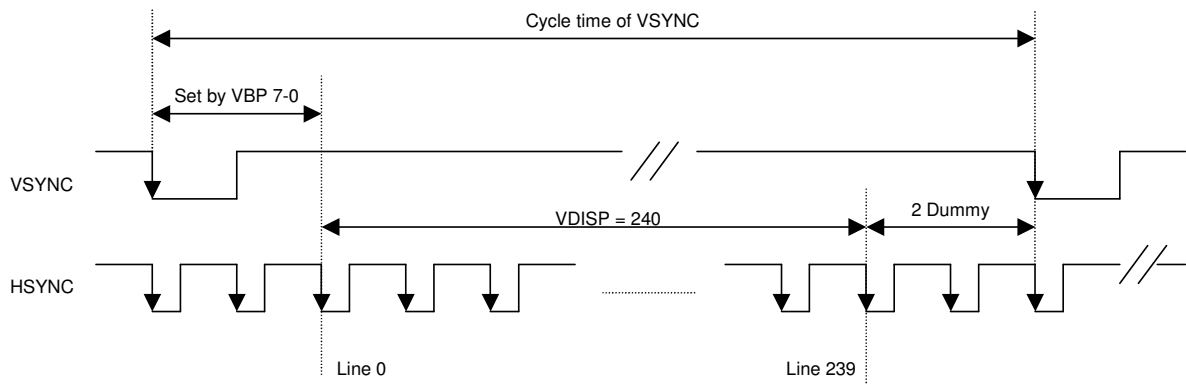
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

**VBP7-0:** Set the delay period from falling edge of VSYNC to first valid line.

The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	VBP7	# of pixels per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3

:									:
:									step = 1
:									:
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1		320
1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved



R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1

**nOTP:** nOTP equals to "0" after power on reset and VCOMH voltage equals to programmed OTP value.

When nOTP set to "1", setting of VCM5-0 becomes valid and voltage of VCOMH can be adjusted.

**VCM5-0:** Set the VCOMH voltage if nOTP = "1". These bits amplify the VCOMH voltage 0.36 to 0.99 times the VLCD63 voltage.

R2Eh	3 Gamma	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	OLO
	(B945h)			1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1

**OLO:** When OLO = "1", all R,G and B gamma registers are set by one set of gamma control, R30h to R3Bh.

When OLO = "0", R, G and B gamma registers are set separately by registers R30h to R3Bh, R40h to R4Bh and R50h to R5Bh.

R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0



R34h	y control (1)	0	1	0	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	y control (1)	0	1	0	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20
	(0202h)			0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	y control (1)	0	1	0	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	y control (1)	0	1	0	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

When OLO = "0", R30h-R3Bh are registers to adjust the gamma register values on the output of source S(3n), where n = 0 to 319. S(3n) are the red color source output when BGR = "0".

When OLO = "1", R30h-R3Bh are registers to adjust the gamma register values on the output of all source S0 to S959.

**PKP52-00:** Gamma micro adjustment register for the positive polarity output.

**PRP12-00:** Gradient adjustment register for the positive polarity output.

**PKN52-00:** Gamma micro adjustment register for the negative polarity output.

**PRN12-00:** Gradient adjustment register for the negative polarity output.

R3Ah	y control (2)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	y control (2)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

**VRP14-00:** Adjustment register for amplification adjustment of the positive polarity output.

**VRN14-00:** Adjustment register for the amplification adjustment of the negative polarity output.



### F. Optical specifications (Note 1, 2)

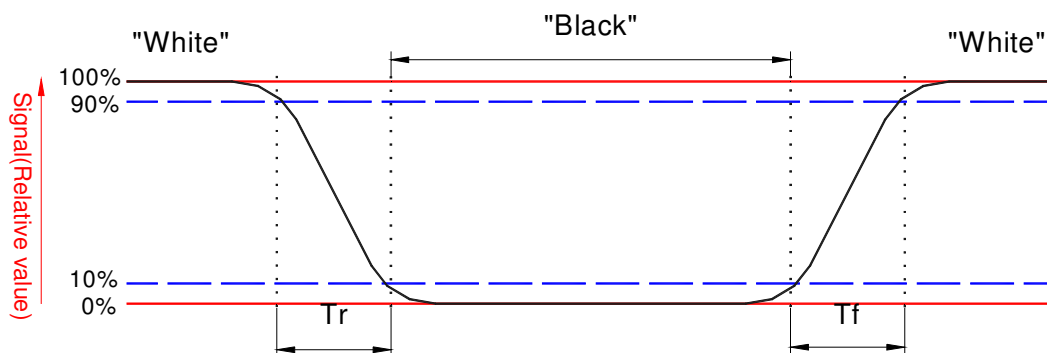
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	$\theta = 0^\circ$	-	10	20	ms	Note 3
Fall	Tf		-	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top		CR $\geq 10$	35	50	-	deg.	Note 7, 8
Bottom			40	55	-		
Left			45	60	-		
Right			45	60	-		
Brightness	YL	$\theta = 0^\circ$	280	330	-	cd/m <sup>2</sup>	Note 9
NTSC			50	60		%	
White Chromaticity	X	$\theta = 0^\circ$	0.26	0.31	0.36		
	y	$\theta = 0^\circ$	0.28	0.33	0.38		
Luminance Uniformity			75	80		%	Note 9

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current  $I_L=20$  mA

Note 2: To be measured on the center area of panel with a field angle of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25°C .

Note 5. Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White  $V_i = V_{i50} \pm 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

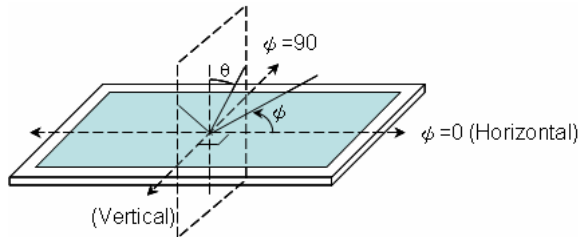
“±” means that the analog input signal swings in phase with COM signal.

“μ” means that the analog input signal swings out of phase with COM signal.

$V_{i50}$  :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.

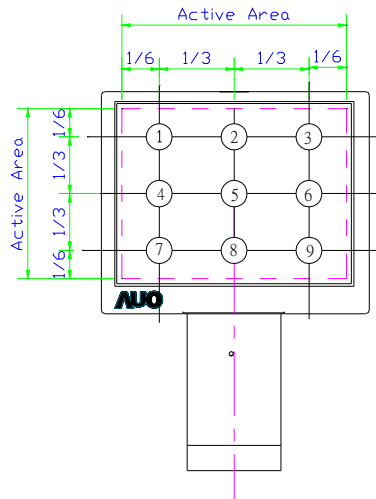


Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9. Definition of brightness and luminance uniformity:

Brightness = average brightness of nine points illustrated below

$$\text{Luminance Uniformity} = \frac{\text{Min. Brightness of nine points}}{\text{Max. Brightness of nine points}}$$



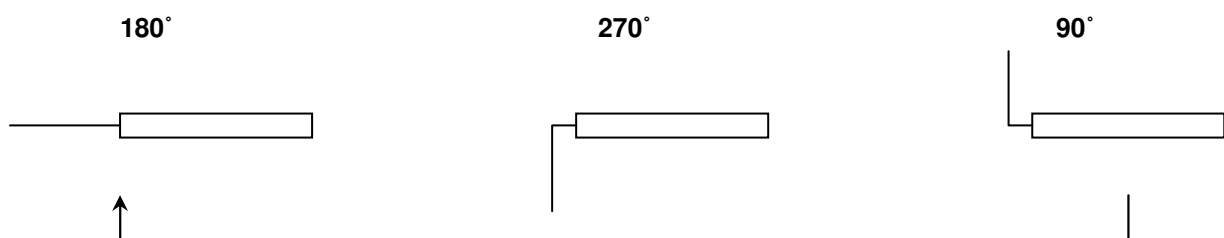
### G. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 85°C	240Hrs	
2	Low Temperature Storage	Ta= -30°C	240Hrs	
3	High Temperature Operation	Ta= 70°C	240Hrs	
4	Low Temperature Operation	Ta= -20°C	240Hrs	
5	High Temperature & High Humidity	Ta= 60°C . 90% RH	240Hrs	Operation
6	Heat Shock	-25°C~70°C, 50 cycle, 2Hrs/cycle		Non-operation
7	Electrostatic Discharge	Contact 64kV, Air +/-12kV Display surface		Non-operation
8	Vibration (With Carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/Octave from 200~500Hz		IEC 68-34
9	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		
10	FPC Bending Test	Curved radius: 2mm Pulling force: 250g Bending angle: 180°→270°→90°→180° 50 cycles (Note 10)		
11	Touch Panel FPC Peeling Test	5N Min Peeling upward by 90°		
12	Touch Panel Impact Resistance	φ11mm(5g) steel ball Distance: 70cm Measured at the center of touch panel (Touch panel is supported around its four edges with 10mm thick and 10 mm wide PVC board)		

Note 1: In the standard conditions, there is not display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2: Ta: Ambient temperature.

Note 3: Bending test condition:



## H. Touch Screen Panel Specifications

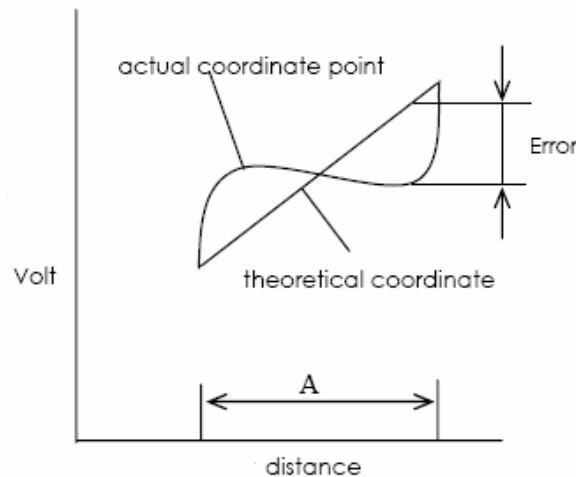
### 1. FPC Pin Assignment

Pin No.	Symbol	I/O
4	R	O
5	B	O
6	L	O
7	U	O

### 2. Electrical Characteristics

Item	Min.	Max.	Unit	Remark
Rate DC Voltage		7	V	
Resistance	X (Film)	350	Ω	At connector
	Y (Glass)	150		
Linearity	-1.5%	1.5%	--	Note 1, test by 250 gf
Chattering		10	ms	At connector pin
Insulation Resistance	10M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



### 3. Mechanical Characteristics

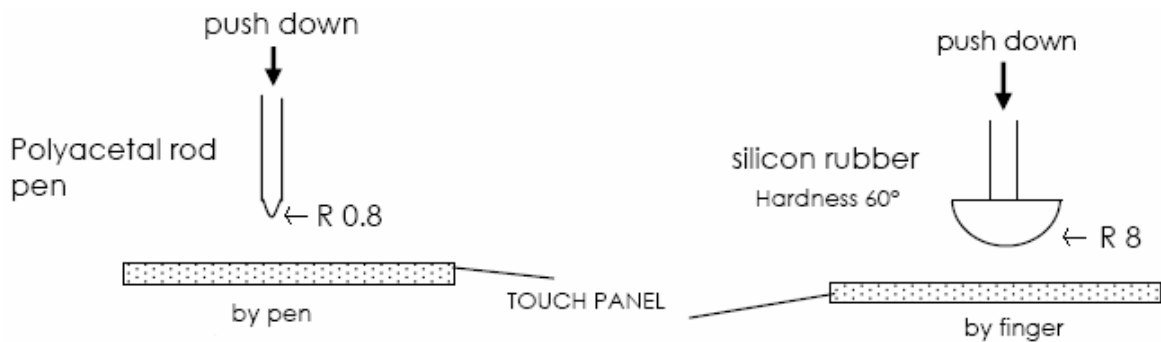
Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Operation Force (Pen or Finger)	--	50	gf	Note 1

Note 1: Within "guaranteed active area", but not on the edge and dot-spacer.

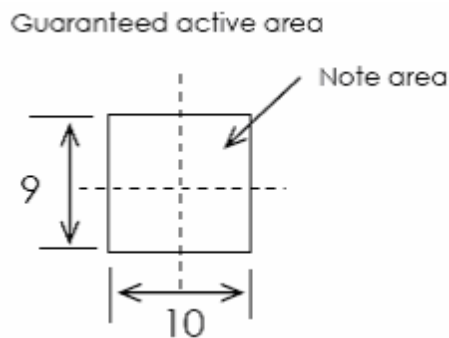
#### 4. Life test Condition

Item	Min.	Max.	Unit	Remark
Notes Life	10 <sup>5</sup>	--	words	Note 1, 2
Input Life	10 <sup>6</sup>	--	times	Note 1, 3

Note 1: Measurement condition of Operation Force: Within "guaranteed active area". Resistance, Insulation resistance, and operation force should be under 5.2 & 5.3 condition. When user pushes down on the film, resistance between X & Y axis must be equal or lower than 2kΩ. Below is test figure.



Note 2: Notes Life test condition (by pen): Notes area for pen notes life test is 10×9 mm. Size of word is 7.5×6.75mm. Word is any A.B.C..... letter. Writing speed is 60mm/s. Center of each word is changed at random in notes area.



Note 3: Input Life test condition( by finger): By silicone rubber tapping at same point. Tapping Load is 200g, and tapping frequency is 5Hz.

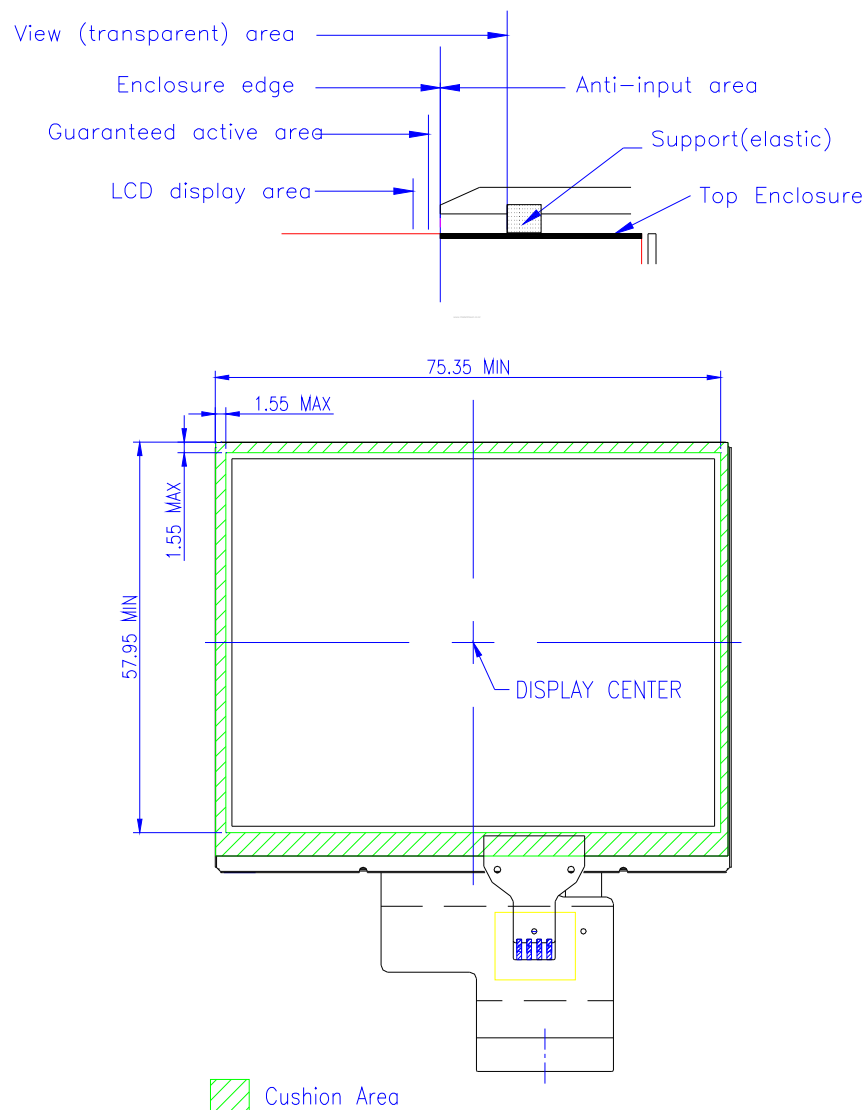
#### 5. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

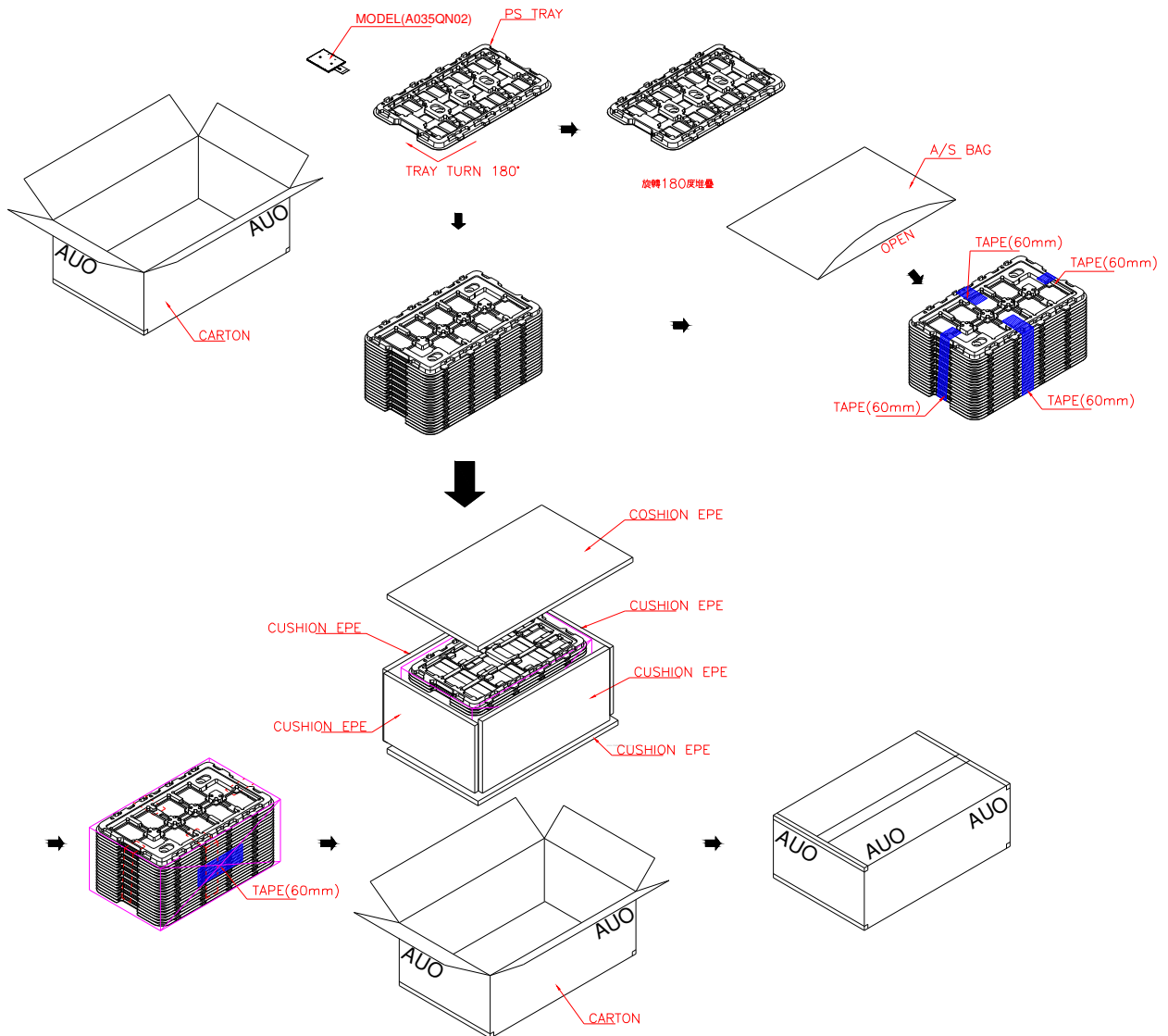
1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.

4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm<sup>2</sup> below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.
7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.
8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.

Recommendation of the cushion area:



## I. Packing Form

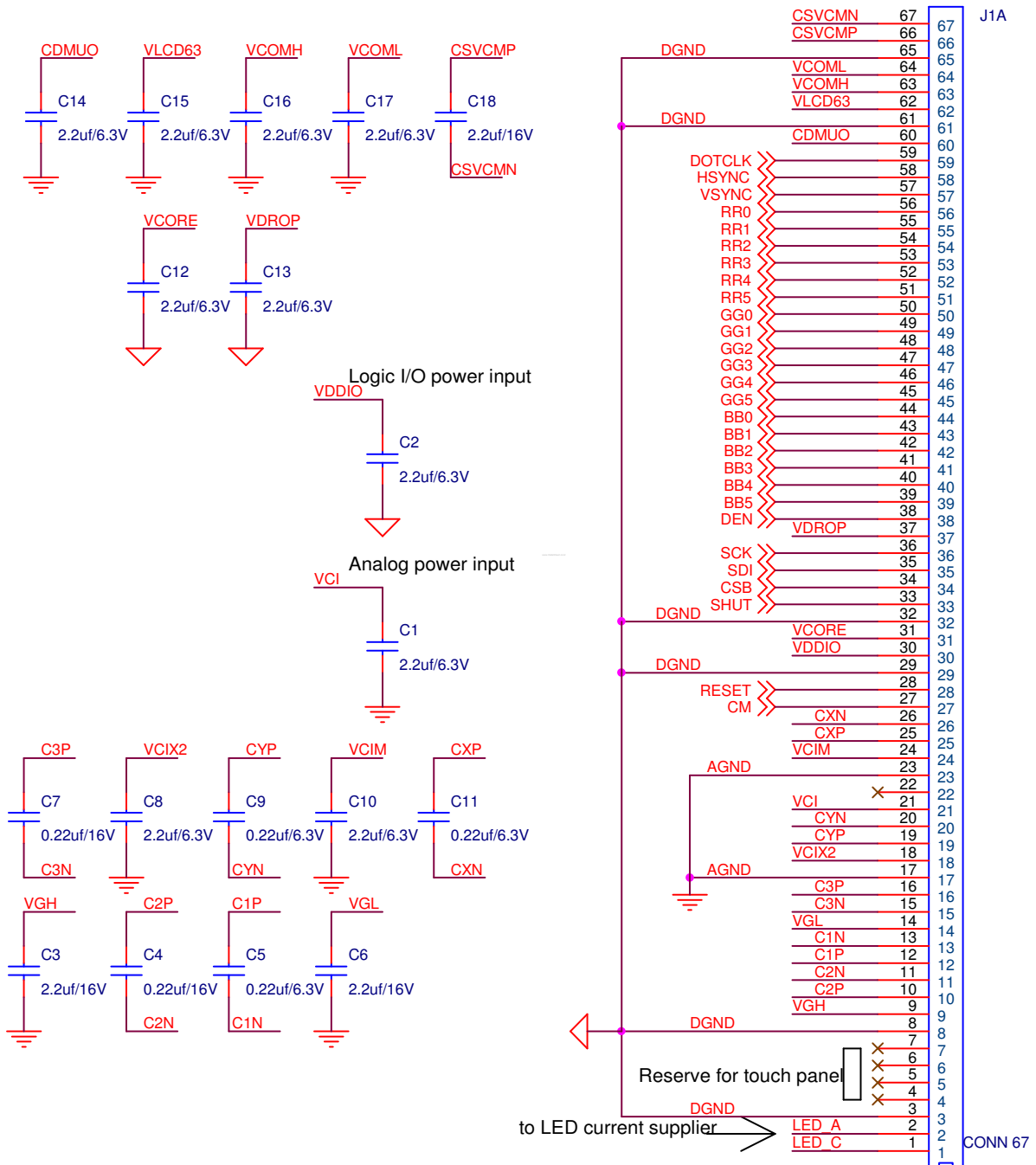


MAX. CAPACITY:160 MODULES  
 MAX. WEIGHT: 12Kg  
 MEAS. 520mm\*340mm\*250mm

## J. Application Note

### 1. Application circuit

The following drawing is the application circuit recommended.





The BOM list is as follows.

Name	Component	Value	Description	Remark
J1A	61 pins connector			
C1	Capacitor	2.2uF	6.3V / X5R	
C2	Capacitor	2.2uF	6.3V / X5R	
C3	Capacitor	2.2uF	16V / X5R	
C4	Capacitor	0.22uF	16V / X5R	
C5	Capacitor	0.22uF	6.3V / X5R	
C6	Capacitor	2.2uF	16V / X5R	
C7	Capacitor	0.22uF	16V / X5R	
C8	Capacitor	2.2uF	6.3V / X5R	
C9	Capacitor	0.22uF	6.3V / X5R	
C10	Capacitor	2.2uF	6.3V / X5R	
C11	Capacitor	0.22uF	6.3V / X5R	
C12	Capacitor	2.2uF	6.3V / X5R	
C13	Capacitor	2.2uF	6.3V / X5R	
C14	Capacitor	2.2uF	6.3V / X5R	
C15	Capacitor	2.2uF	6.3V / X5R	
C16	Capacitor	2.2uF	6.3V / X5R	
C17	Capacitor	2.2uF	6.3V / X5R	
C18	Capacitor	2.2uF	6.3V / X5R	