Doc. Version	0.1
Total Page	29
Date	2008/09/11

Product Specification

3.5" COLOR TFT-LCD MODULE

MODEL NAME: A035QN02 V6

< □ >Preliminary Specification

< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/03/19		First draft.
0.1	2008/09/11	7	Add Pin assignment description

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A. General Description

A035QN02 V6 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD and a driver IC.

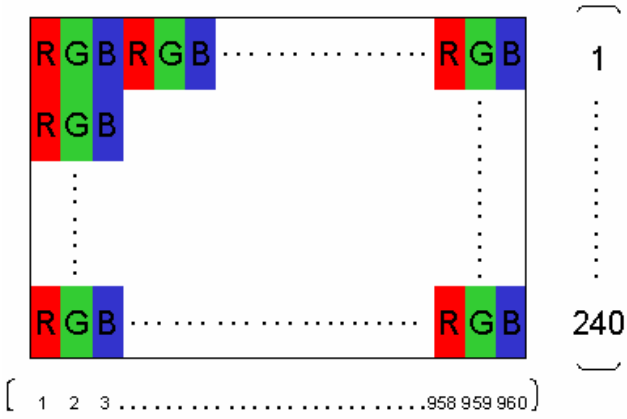
B. Features

- 3.5-inch display
- QVGA resolution in RGB stripe dot arrangement
- DC/DC integrated
- 3-wire register setting
- Interfaces: parallel RGB 18-bit
- Wide viewing angle
- Green design

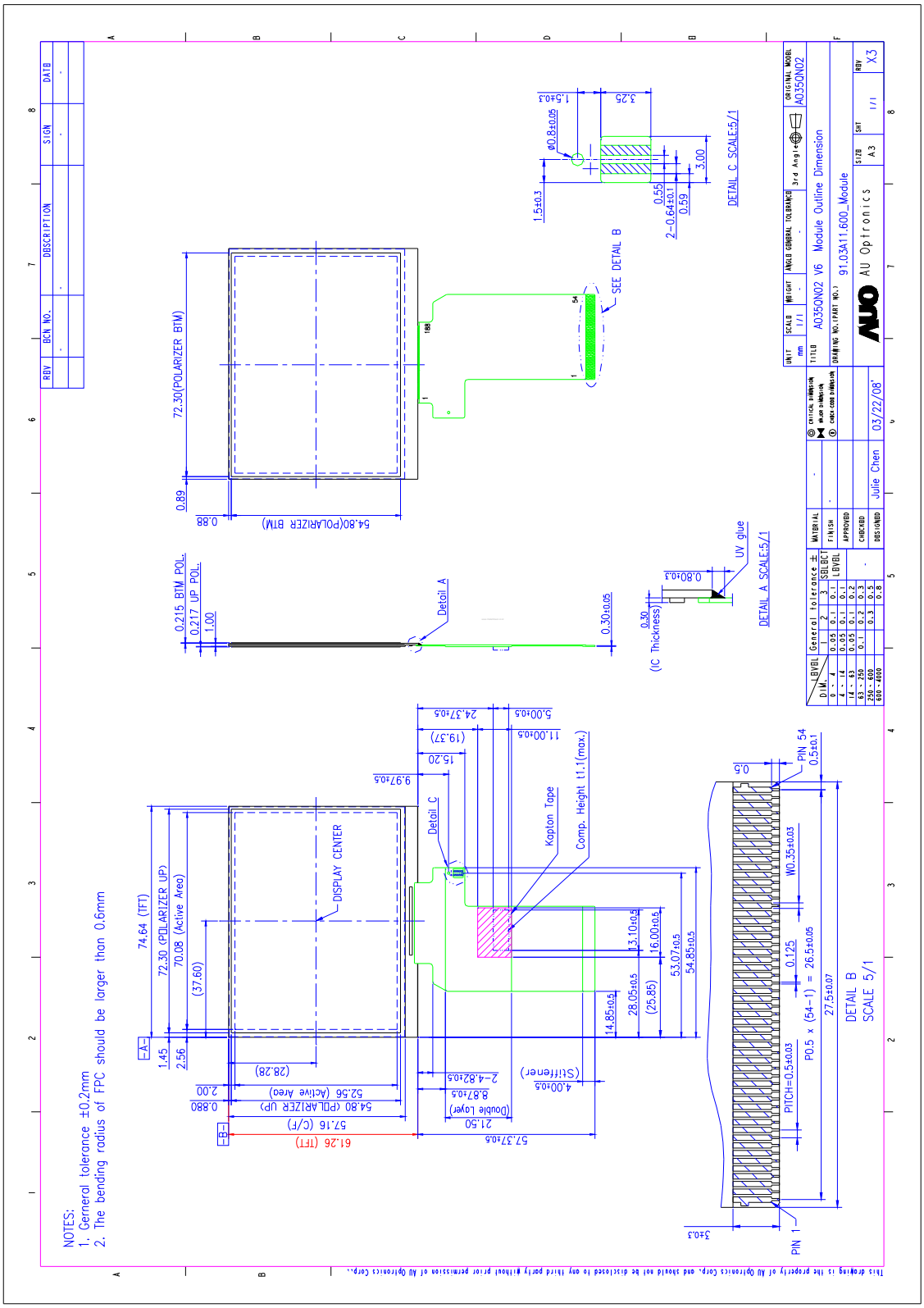
C. Physical Specifications

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	262K Colors	
7	Overall Dimension	mm	74.64(H)×61.26(V)x1.432(T)	
8	Weight	g	13	
9	Panel surface treatment	--	Hard coating 3H	
10	Display Mode	--	Normally White	
11	Gray Level Inversion Direction		6 O'clock	

Note 1: Below figure shows dot stripe arrangement.



D. Outline Dimension



E. Electrical Specifications

1. Pin Assignment

No.	Pin Name	I/O	Description	Remarks
1	LED-	-	Power supply for LED	
2	LED-	-	Power supply for LED	
3	LED+	-	Power supply for LED	
4	LED+	-	Power supply for LED	
5	NC	-	Non connection	Note 1
6	NC	-	Non connection	Note 1
7	NC	-	Non connection	Note 1
8	RESET	I	System reset	
9	CS	I	Chip select	
10	SCL	I	Clock input pin in serial mode	
11	SDI	I	Data input pin serial mode	
12	NC	-	Non connection	Note 1
13	NC	-	Non connection	Note 1
14	B0	I	BLUE data signal (LSB)	
15	B1	I	BLUE data signal	
16	B2	I	BLUE data signal	
17	B3	I	BLUE data signal	
18	B4	I	BLUE data signal	
19	B5	I	BLUE data signal (MSB)	
20	NC	-	Non connection	Note 1
21	NC	-	Non connection	Note 1
22	G0	I	GREEN data signal (LSB)	
23	G1	I	GREEN data signal	
24	G2	I	GREEN data signal	
25	G3	I	GREEN data signal	
26	G4	I	GREEN data signal	
27	G5	I	GREEN data signal (MSB)	
28	NC	-	Non connection	Note 1
29	NC	-	Non connection	Note 1
30	R0	I	RED data signal (LSB)	
31	R1	I	RED data signal	
32	R2	I	RED data signal	

33	R3	I	RED data signal	
34	R4	I	RED data signal	
35	R5	I	RED data signal (MSB)	
36	HSYNC	I	Line synchronization signal	
37	VSYNC	I	Frame synchronization signal	
38	DOTCLK	I	Dot-clock signal	
39	AVDD	-	Voltage input pin for analog	
40	AVDD	-	Voltage input pin for analog	
41	VDD	-	Voltage input pin for logic I/O	
42	VDD	-	Voltage input pin for logic I/O	
43	NC	-	Non connection	Note 1
44	VGL	-	Voltage input VGOFF	Note 2
45	VGL	-	Voltage input VGOFF	Note 2
46	NC	-	Non connection	Note 1
47	VGH	-	Voltage input VGON	Note 2
48	NC	-	Non connection	Note 1
49	NC	-	Non connection	Note 1
50	NC	-	Non connection	Note 1
51	NC	-	Non connection	Note 1
52	ENABLE	-	Data enable signal.	Note 3
53	GND	-	Ground	
54	GND	-	Ground	

Note 1 : An NC Pins OPEN in FPC.

Note 2 : No use.

Note 3 : In sync mode, “ENABLE” pin must be fixed to high.

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VDDIO	-0.3	4	V	
	VCI	-0.3	5	V	

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

3. Electrical Characteristics

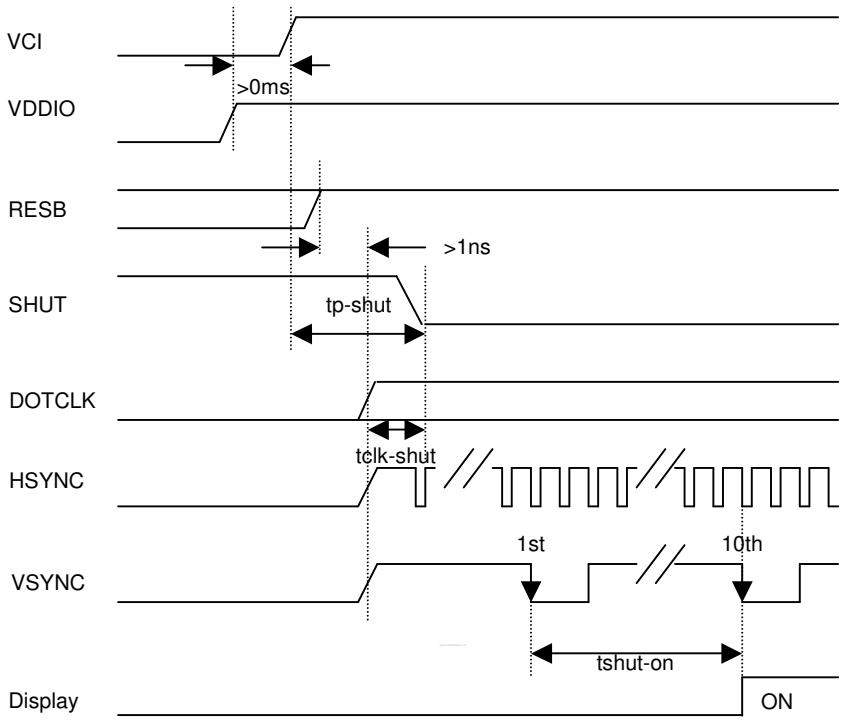
The following items are measured under stable condition and suggested application circuit.

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Digital Power Supply	VDDIO	2.5	3.3	3.6	V	
Analog Power Supply	VCI	2.5	3.3	3.6	V	
Frame Frequency	f_{Frame}		60		Hz	
Dot Data Clock	DCLK		5		MHz	
Input Signal Voltage	Vi	0		0.2 x VDDIO	V	
	VI	0.8 x VDDIO		VDDIO	V	

4. AC Timing

a. Power on/off sequence

Power On

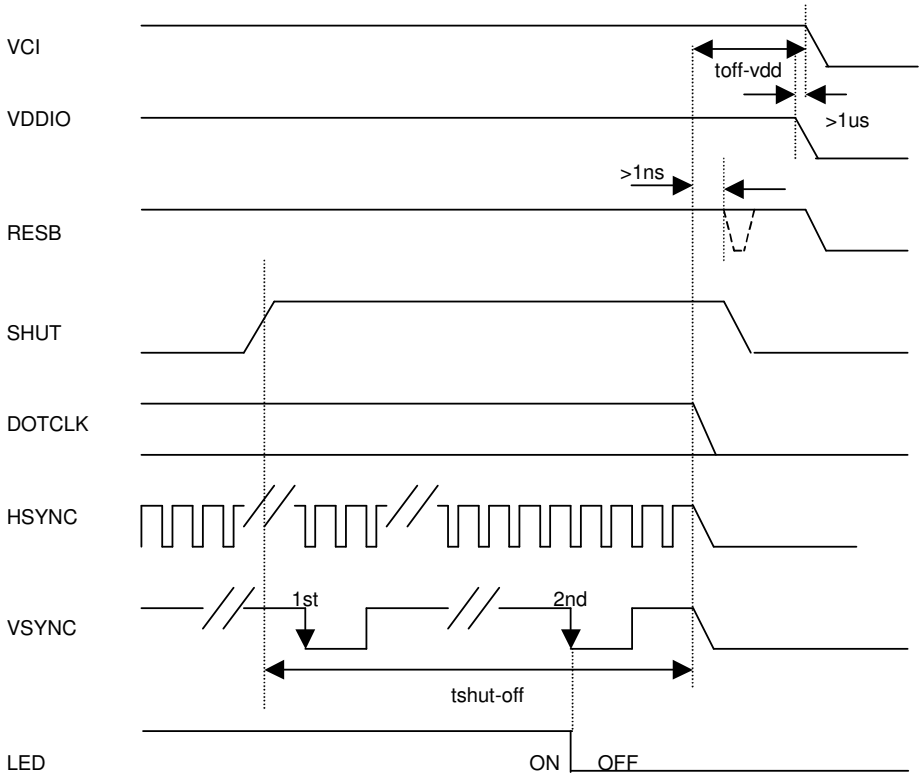


Characteristics	Symbol	Min	Typ	Max	Unit
VDDIO on to falling edge of SHUT	tp-shut	1			uSec
DOTCLK	tclk-shut	1			clk
Falling edge of SHUT to display on	tshut-on			10	frame
-- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz			164		mSec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT

Power Off



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off	tshut-off	2		10	frame
-- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz		32.8			mSec
Input-signal-off to V_{DDEXT} / V_{DDIO} off	toff-vdd	1			uSec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

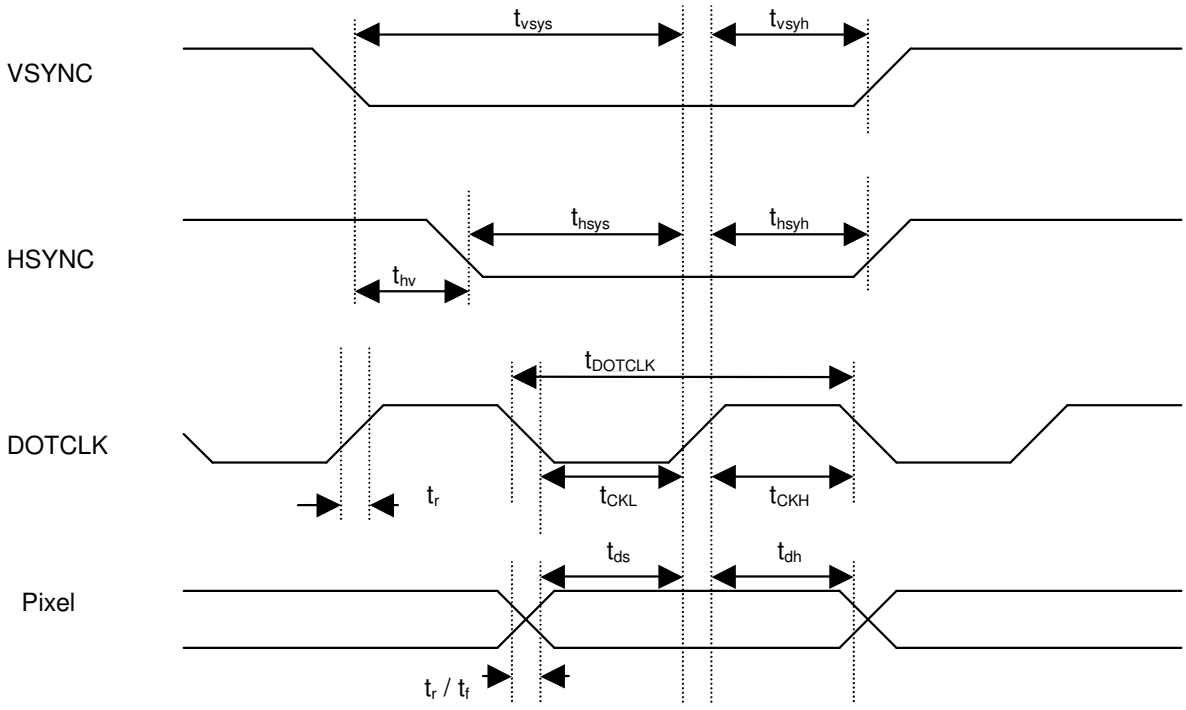
Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

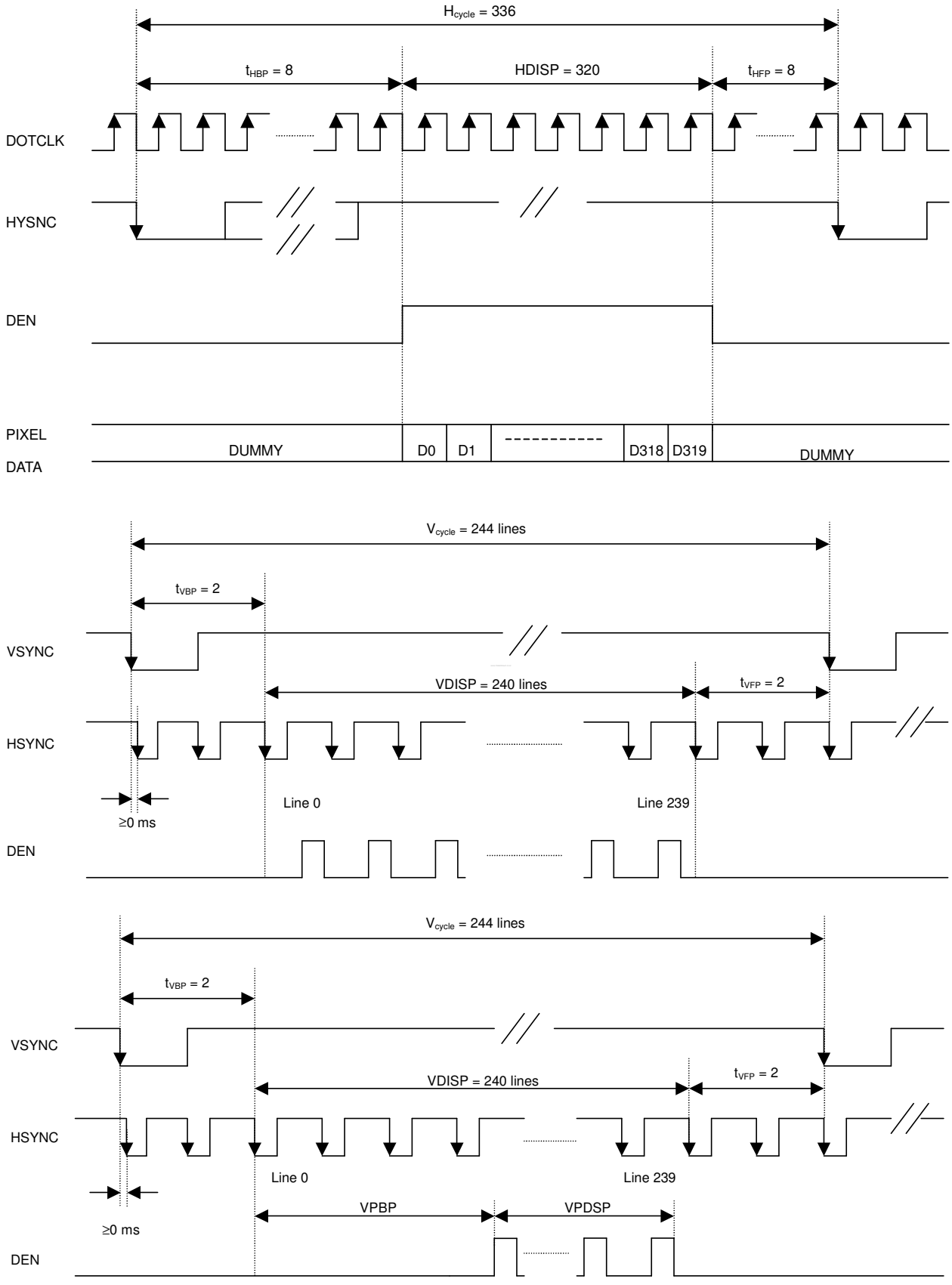
b. Timing Condition

Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK Frequency	f_{DOTCLK}		5.0	7.5	MHz
DOTCLK Period	t_{DOTCLK}	133	200		nSec
Vsync Setup Time	t_{vsys}	20			nSec
Vsync Hold Time	t_{vsyh}	20			nSec
Hsync Setup Time	t_{hsys}	20			nSec
Hsync Hold Time	t_{hsyh}	20			nSec

Phase Difference of Sync Signal Falling Edge	t_{hv}	0		320	t_{DOTCLK}
DOTCLK Low Period	t_{CKL}	66.5			nSec
DOTCLK High Period	t_{CKH}	66.5			nSec
Data Setup Time	t_{ds}	40			nSec
Data Hold Time	t_{dh}	40			nSec
Reset Pulse Width	t_{RES}	10			nSec
Rise / Fall Time	t_r/t_f	20		100	nSec

c. Timing Diagram





NOTE: The falling edge of HSYNC belongs to blanking period is always behind or equal to the one of VSYNC.

5. Command Register Map

a. Serial setting map

Reg#	Register	R/W	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output control	0	1	0	0	REV	CAD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	X	X	X	0	X	X	1	1	1	0	1	1	1	1
R02h	LCD drive AC control	0	1	0	0	0	0	0	0	B/C	ERO	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0300h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(7272h)			0	1	1	1	0	0	1	0	0	1	1	1	0	0	1	0
R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	0	0	0	0	0	0	0	0
	(DC00h)			1	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
R0Fh	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R16h	Horizontal porch	0	1	XLIM8	XLIM7	XLIM6	XLIM5	XLIM4	XLIM3	XLIM2	XLIM1	XLIM0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1
R2Eh	3 Gamma	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	OLO
	(B945h)			1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1
R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

R34h	γ control (1)	0	1	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	γ control (1)	0	1	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R3Ah	γ control (2)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	γ control (2)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

b. Description of serial control data

R01h	Driver output control	0	1	0	0	REV	CAD	BGR	SM	TB	RL	1	1	1	0	1	1	1	1
	[00XX][X0XX]EF			0	0	X	X	X	0	X	X	1	1	1	0	1	1	1	1

REV: Displays all character and graphic display sections with reversal when REV = “1”.

Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

Source output level is indicated below.

REV	RGB data	Source Output level	
		VCOM = ”H”	VCOM = ”L”
1	000000B	V63	V0
	:	:	:
	111111B	V0	V63
0	000000B	V0	V63
	:	:	:
	111111B	V63	V0

CAD: Set up based on retention capacitor configuration of the TFT panel.

CAD	Retention capacitor configuration
0	Cs on Common
1	Cs on Gate

BGR: Selects the <R><G><B> arrangement.

When BGR = “0” <R><G><B> color is assigned from S0. When BGR = “1” <B><G><R> color is assigned from S0.

SM: Change the division of gate driver.

When SM = “0”, odd/even division (interlace mode) is selected. When SM = “1”, upper/lower division is selected.

Select the division mode according to the mounting method.

TB: Selects the output shift direction of the gate driver.

When TB = “1”, G0 shifts to G239. When TB = “0”, G239 shifts to G0.

RL: Selects the output shift direction of the source driver.

When RL = “1”, S0 shifts to S959 and <R><G><B> color is assigned from S1.

When RL = “0”, S959 shifts to S0 and <R><G><B> color is assigned from S959.

Set RL bit and BGR bit when changing the dot order of R, G and B.

Note: The default setting of register bits *REV*, *CAD*, *BGR*, *TB* and *RL* are defined by the logic stage of corresponding hardware pins.

These bits will override the hardware setting once software command was sent to set the bits.

R02h	LCD drive AC control	0	1	0	0	0	0	0	0	B/C	ERO	0	NW6	NW5	NW4	NW3	NW2	NW1	NW0
	(0300h)			0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0

B/C: Select the liquid crystal drive waveform VCOM.

When B/C = 0, frame inversion of the LCD driving signal is enabled.

When B/C = 1, a N-line inversion waveform is generated and alternates in a N-line equals to NW[7:0]+1.

EOR: When B/C = 1 and EOR = 1, the odd/even frame-select signals and the N-line inversion signals are EORed for alternating drive.

EOR is used when the LCD is not alternated by combining the set values of the lines of the LCD driven and the N-lines.

NW6-0: Specify the number of lines that will alternate at the N-line inversion setting (B/C = 1). NW6-0 alternate for every set value + 1 lines.

R03h	Power control (1)	0	1	DCT3	DCT2	DCT1	DCT0	BT2	BT1	BT0	0	DC3	DC2	DC1	DC0	AP2	AP1	AP0	0
	(7272h)			0	1	1	1	0	0	1	0	0	1	1	1	0	0	1	0

DCT3-0: Set the step-up cycle of the step-up circuit for 8-color mode (CM = VDDIO).

When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too.

Adjust the cycle taking into account the display quality and power consumption.

DCT3	DCT2	DCT1	DCT0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2

1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96
1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	V_{CIX2}x3	-(V_{CIX2}x3)+VCI	6	-5
0	0	1	V_{CIX2}x3	-(V_{CIX2}x2)	6	-4
0	1	0	V_{CIX2}x3	-(V_{CIX2}x3)	6	-6
0	1	1	V_{CIX2}x2+VCI	-(V_{CIX2}x3)+VCI	5	-5
1	0	0	V_{CIX2}x2+VCI	-(V_{CIX2}x2)	5	-4
1	0	1	V_{CIX2}x2+VCI	-(V_{CIX2}x2)+VCI	5	-3
1	1	0	V_{CIX2}x2	-(V_{CIX2}x2)	4	-4
1	1	1	VCIX2x2	-(V_{CIX2}x2)+VCI	4	-3

DC3-0: Set the step-up cycle of the step-up circuit for 262k-color mode (CM = VSS).

When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too.

Adjust the cycle taking into account the display quality and power consumption.

DC3	DC2	DC1	DC0	Step-up cycle
0	0	0	0	Fline × 14
0	0	0	1	Fline × 12
0	0	1	0	Fline × 8
0	0	1	1	Fline × 7
0	1	0	0	Fline × 6
0	1	0	1	Fline × 5
0	1	1	0	Fline × 4
0	1	1	1	Fline × 3
1	0	0	0	Fline × 2
1	0	0	1	Fline × 1
1	0	1	0	fosc / 64
1	0	1	1	fosc / 80
1	1	0	0	fosc / 96

1	1	0	1	fosc / 128
1	1	1	0	fosc / 160
1	1	1	1	fosc / 256

AP2-0: Adjust the amount of current from the stable-current source in the internal operational amplifier circuit.

When the amount of current becomes large, the driving ability of the operational-amplifier circuits increase.

Adjust the current taking into account the power consumption.

During times when there is no display, such as when the system is in a sleep mode.

AP2	AP1	AP0	Op-amp power
0	0	0	Least
0	0	1	Small
0	1	0	Small to medium
0	1	1	Medium
1	0	0	Medium to large
1	0	1	Large
1	1	0	Large to Maximum
1	1	1	Maximum

R0Bh	Frame cycle control	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	0	0	0	0	0	0	0	0	0
	(DC00h)			1	1	0	1	1	1	0	0	0	0	0	0	0	0	0

NO1-0: Sets amount of non-overlap of the gate output.

SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

EQ1-0: Sets the equalizing period on source

R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	V_{CIX2} voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ah)			0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1

VRH3-0: Set amplitude magnification of VLCD63. These bits amplify the VLCD63 voltage 1.78 to 3.00 times the Vref voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.815
0	0	0	1	Vref x 2.905
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3200h)			0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV4-0) becomes available.

When VCOMG = “0”, VCOML output is fixed to Hi-z level, VCI2 output for VCOML power supply stops, and the instruction (VDV4-0) becomes unavailable.

Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive.

These bits amplify VCOM amplitude 0.6 to 1.23 times the VLCD63 voltage.

When VCOMG = “0”, the settings become invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOMA
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
:					Step = 0.03
:					

:					
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reserved
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
: : :					Step = 0.03
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

VCOMAS: Set the equation of VCOML.

$V_{COML} = \alpha \times V_{COMH} - V_{COMA}$

VCOMAS	α
0	0.94
1	0.5

R0Fh	Gate scan starting position	0	1	0	0	0	0	0	0	0	0	SCN7	SCN6	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SCN7-0: Set the scanning starting position of the gate driver.

R16h	Horizontal porch	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

XL7-0: Set the number of valid pixel per line.

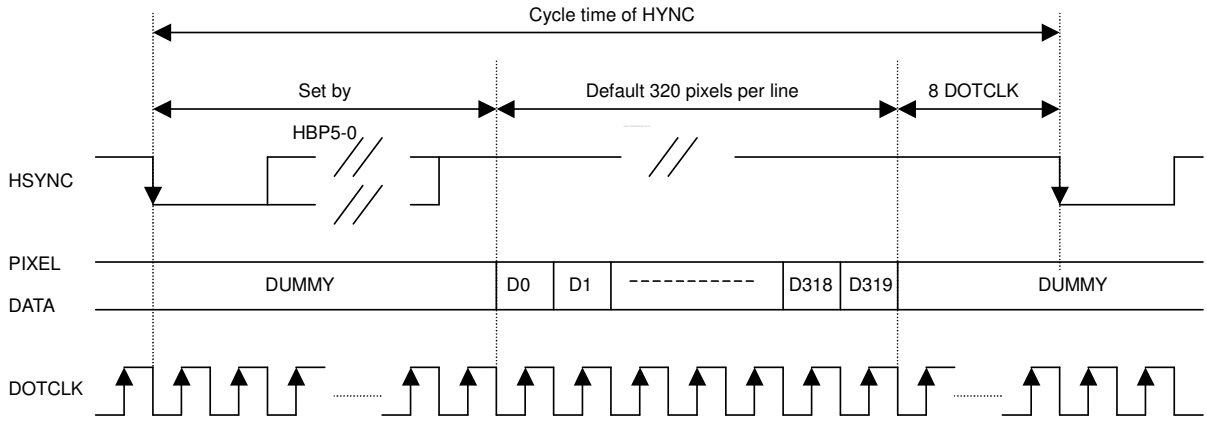
XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	# of pixels per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
: : :									: step = 1 :
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1		320

1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved

HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data.

The pixel data exceed the range set by XL8-0 and before the first valid data will be treated as dummy data.

HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	# of clock cycle of DOTCLK
0	0	0	0	0	0	2
0	0	0	0	0	1	3
0	0	0	0	1	0	4
:	:	:	:	:	:	: step = 1 :
1	1	1	1	1	0	64
1	1	1	1	1	1	65



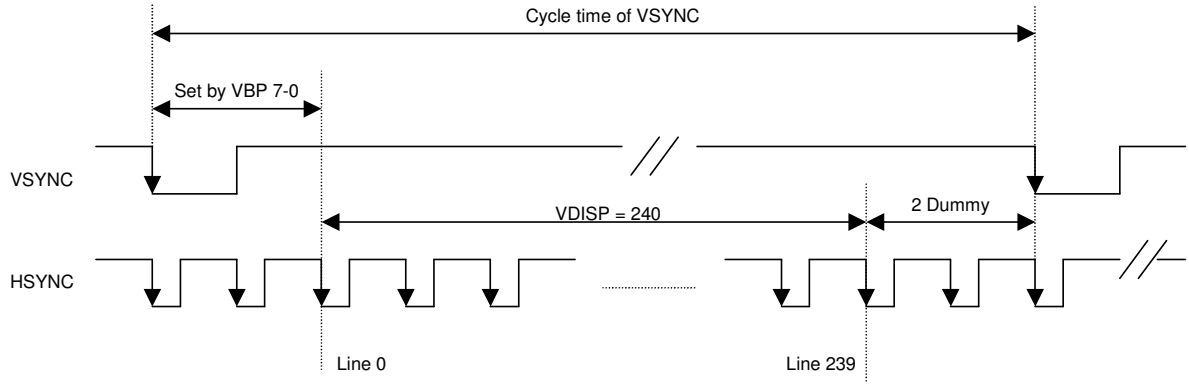
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line.

The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	VBP7	# of pixels per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3

				:					:
				:					step = 1
				:					:
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1		320
1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved



R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(002Dh)			0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	1

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value.

When nOTP set to “1”, setting of VCM5-0 becomes valid and voltage of VCOMH can be adjusted.

VCM5-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.99 times the VLCD63 voltage.

R2Eh	3 Gamma	0	1	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	OLO
	(B945h)			1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1

OLO: When OLO = “1”, all R,G and B gamma registers are set by one set of gamma control, R30h to R3Bh.

When OLO = “0”, R, G and B gamma registers are set separately by registers R30h to R3Bh, R40h to R4Bh and R50h to R5Bh.

R30h	γ control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP12	0	0	0	0	0	PKP02	PKP01	PKP00
	(0000h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R31h	γ control (1)	0	1	0	0	0	0	0	PKP32	PKP31	PKP32	0	0	0	0	0	PKP22	PKP21	PKP20
	(0200h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R32h	γ control (1)	0	1	0	0	0	0	0	PKP52	PKP51	PKP52	0	0	0	0	0	PKP42	PKP41	PKP40
	(0001h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R33h	γ control (1)	0	1	0	0	0	0	0	PRP12	PRP11	PRP12	0	0	0	0	0	PRP02	PRP01	PRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0

R34h	γ control (1)	0	1	0	0	0	0	0	PKN12	PKN11	PKN12	0	0	0	0	0	PKN02	PKN01	PKN00
	(0405h)			0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	1
R35h	γ control (1)	0	1	0	0	0	0	0	PKN32	PKN31	PKN32	0	0	0	0	0	PKN22	PKN21	PKN20
	(0202h)			0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
R36h	γ control (1)	0	1	0	0	0	0	0	PKN52	PKN51	PKN52	0	0	0	0	0	PKN42	PKN41	PKN40
	(0707h)			0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1
R37h	γ control (1)	0	1	0	0	0	0	0	PRN12	PRN11	PRN12	0	0	0	0	0	PRN02	PRN01	PRN00
	(0006h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

When OLO = “0”, R30h-R3Bh are registers to adjust the gamma register values on the output of source S(3n), where n = 0 to 319. S(3n) are the red color source output when BGR = “0”.

When OLO = “1”, R30h-R3Bh are registers to adjust the gamma register values on the output of all source S0 to S959.

PKP52–00: Gamma micro adjustment register for the positive polarity output.

PRP12-00: Gradient adjustment register for the positive polarity output.

PKN52-00: Gamma micro adjustment register for the negative polarity output.

PRN12-00: Gradient adjustment register for the negative polarity output.

R3Ah	γ control (2)	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
	(0700h)			0	0	0	0	0	1	1	1	0	0	0	0	0	0	0	0
R3Bh	γ control (2)	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00
	(0003h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

VRP14-00: Adjustment register for amplification adjustment of the positive polarity output.

VRN14-00: Adjustment register for the amplification adjustment of the negative polarity output.

F. Optical specifications (Note 1, 2)

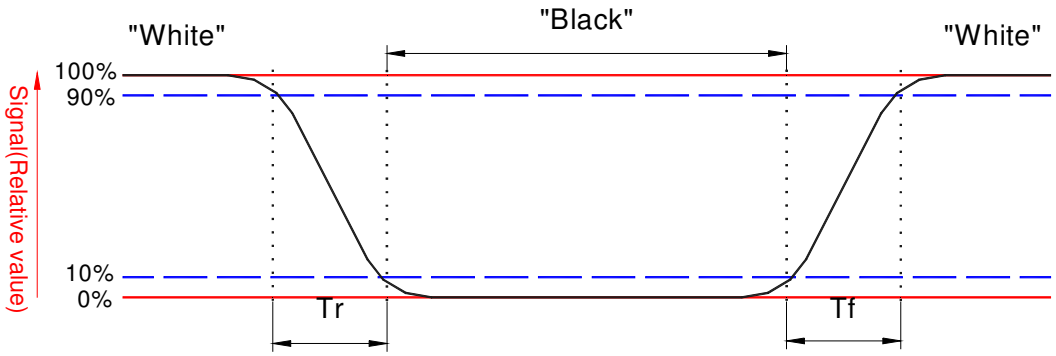
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	10	20	ms	Note 3
Fall	Tf		-	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Transmittance	Tr	θ =0°		7.2		%	
NTSC			50	60		%	
White Chromaticity	X	θ =0°		0.31			Note 9
	y	θ =0°		0.33			

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 5. Contrast ratio is calculated with the following formula.

Note 6. White Vi=Vi50 μ 1.5V

Black Vi=Vi50 ± 2.0V

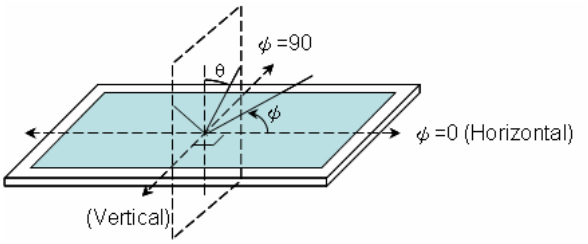
"±" means that the analog input signal swings in phase with COM signal.

"μ" means that the analog input signal swings out of phase with COM signal.

Vi50 :The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

Note 9.Color Filter white chromaticity is for reference. Actual panel white chromaticity varies based on different light sources.

G. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 85□	240Hrs	
2	Low Temperature Storage	Ta= -30□	240Hrs	
3	High Temperature Operation	Ta= 70□	240Hrs	
4	Low Temperature Operation	Ta= -20□	240Hrs	
5	High Temperature & High Humidity	Ta= 60□. 90% RH	240Hrs	Operation
6	Heat Shock	-25□~70□, 50 cycle, 2Hrs/cycle		Non-operation
7	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz		IEC 68-34
8	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces		

Note 1: In the standard conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2: Ta: Ambient temperature.

H. Packing Form

TBD

I. Application Note

1. Recommended Register Settings

Register	Setting
R01	“2AEF”h
R03	“7872”h
R0C	“0002”h
R0D	“000C”h
R0E	“3100”h
R1E	“00A9”h
R2Eh	“B945”h
R30	“0304”h
R31	“0507”h
R32	“0405”h
R33	“0007”h
R34	“0507”h
R35	“0004”h
R36	“0605”h
R37	“0103”h
R3A	“000F”h
R3B	“000F”h

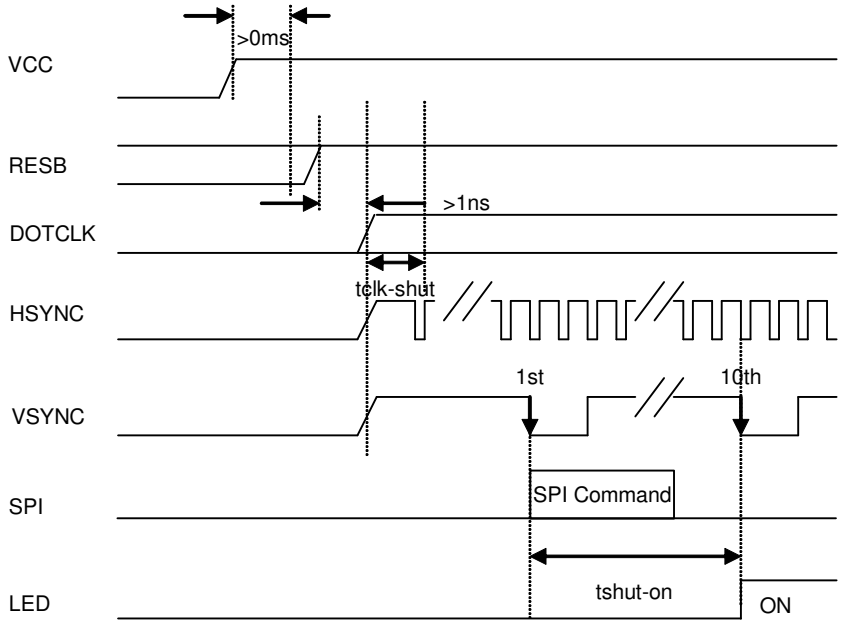
NOTE:

1. The different sequence of registers setting would not affect the normal behavior of LCM.

2.Please refer to the POWER ON/OFF sequence section for register setting timing as power-on.

2. Power on/off Sequence

Power On



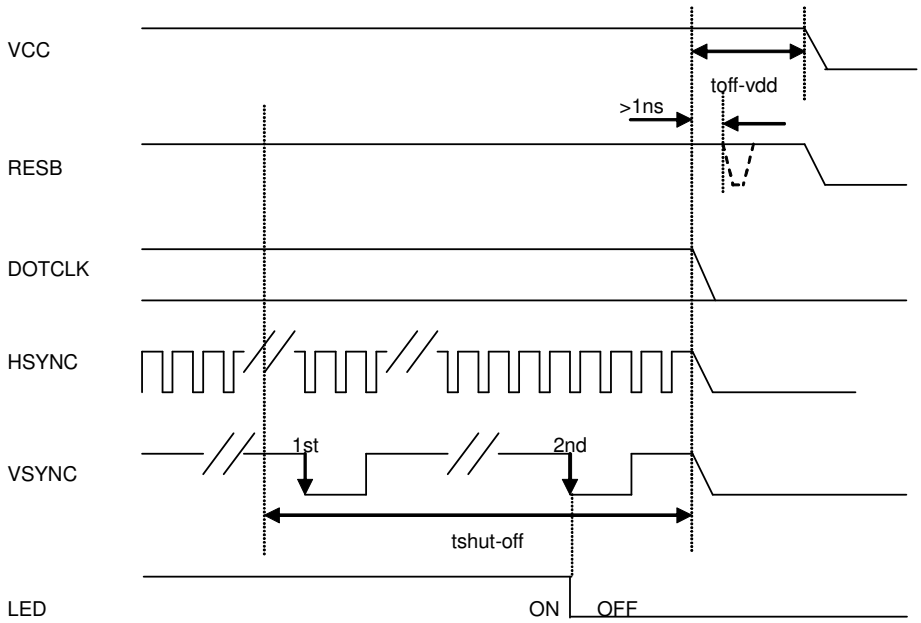
Characteristics	Symbol	Min	Typ	Max	Unit
DOTCLK	tclk-shut	1			clk
Rising edge of RESB to display on -- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz	tshut-on			10	frame
			164		mSec

Note:

1. It is necessary to input DOTCLK before the rising edge of RESB.

2. Display starts at 10th falling edge of VSYNC after the rising edge of RESB.

Power Off



Characteristics	Symbol	Min	Typ	Max	Unit
Falling edge of RESB to display off -- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz	tshut-off	2		10	frame
		32.8			mSec
Input-signal-off to V_{CC} off	toff-vdd	1			uSec

Note:

1. DOTCLK must be maintained at lease 2 frames before the falling edge of RESB.

2. If RESB signal is necessary for power down, provide it after the 2-frames-cycle of the power-off period.

3. There is no SPI setting during POWER-OFF sequence.