CUSTOMER APPROVAL SHEET

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MODEL	
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☐ APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.7)

☐ APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver.0.7)

☐ APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver.0.7)

P/N : 97.03A11.900-S06

Comment :

Product Specification

3.5" COLOR TFT-LCD MODULE

MODEL NAME: A035QN02 V9

< >Preliminary Specification

< □ >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0.0	2008/04/29		First draft.
0.1	2008/07/02	5	Modify module dimension (Thickness 4.32mm → 4.07mm)
		6	Update drawing
		19	Modify the command register settings (R12 : 0050h)
		29	Add packing form
		30	Update Recommend Register Settings (R12 : 0050h)
0.2	2008/10/06	30	Update Recommend Register Settings (R0C : 0004h)
0.3	2008/11/03	30	Update Recommend Register Settings (R0C : 0005h / R1E : 00A4h)
0.4	2008/12/05	7	Update Pin assignment
		9	Update LED Forward Current
		10	Update Backlight Driving Conditions
		15~23	Update Command Register Settings
		31	Update Recommended Register Settings
		32~33	Update Power on/off Sequence
0.5	2009/01/21	9	Update LED Forward Current (MAX 25mA)
		10	Update LED Supply Current (Max 22mA)
0.6	2009/06/02	22	Update Command Register Settings
		33,34	Add SHUT in power on sequence
		35	Update Suggested Circuit
0.7	2009/06/17	12	Update Thv and add design note
		13~15	Add Max and Min value in the timing format
		19	Add R0B description
		33	Add R08 register (DC80h) in the recommended register setting

Contents:

A. General Description

A035QN02 V9 is an amorphous transmissive type Thin Film Transistor Liquid crystal Display (TFT-LCD). This model is composed of a TFT-LCD, a driver, an FPC (flexible printed circuit), a backlight unit and a touch panel.

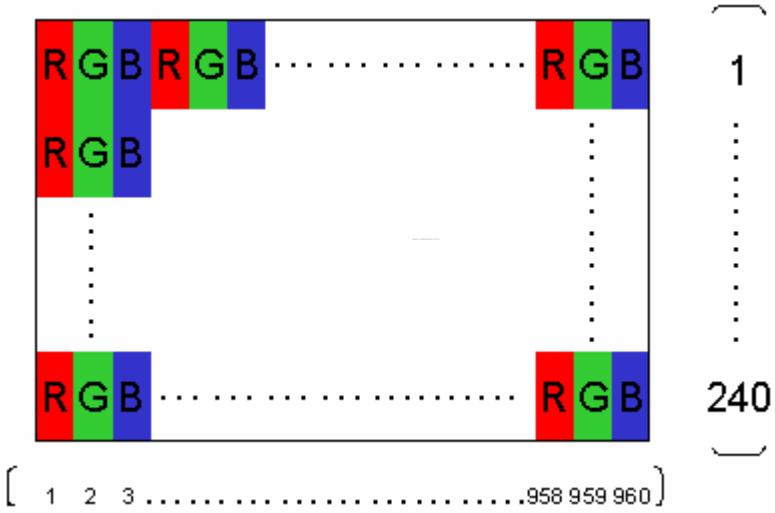
B. Features

- 3.5-inch display with integrated resistive type touch panel
- QVGA resolution in RGB stripe dot arrangement
- Single power, DC/DC integrated
- High brightness
- 3-wire register setting
- Interfaces: serial RGB 8-bit
- Wide viewing angle
- 3-in-1 FPC for LCD signals, backlight LED power and touch panel
- Green design

C. Physical Specifications

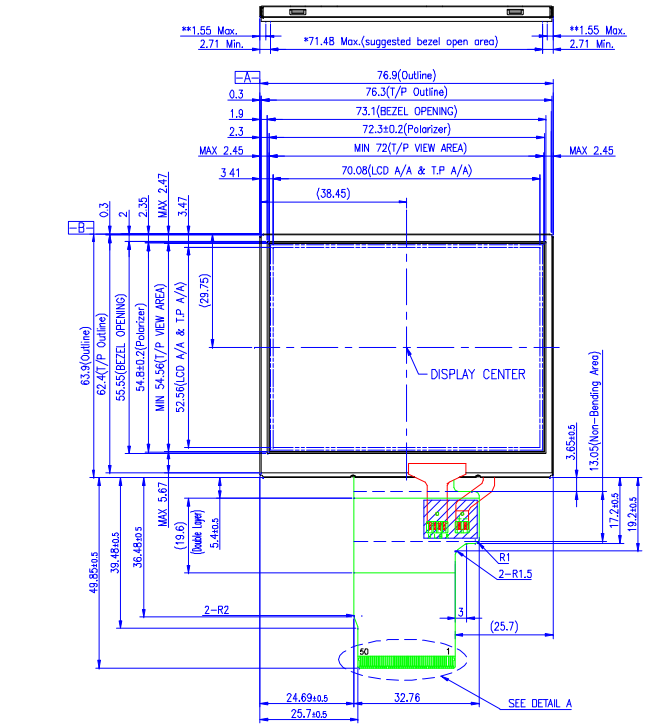
NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	320 RGB (H)×240(V)	
2	Active Area	mm	70.08(H)×52.56(V)	
3	Screen Size	inch	3.5(Diagonal)	
4	Dot Pitch	mm	0.073(H)×0.219(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	
7	Overall Dimension	mm	76.9(H) × 63.9(V) × 4.07(T)	Note 2
8	Weight	g	40	
9	Display Mode	--	Normally White	
10	Gray Level Inversion Direction		6 O'clock	

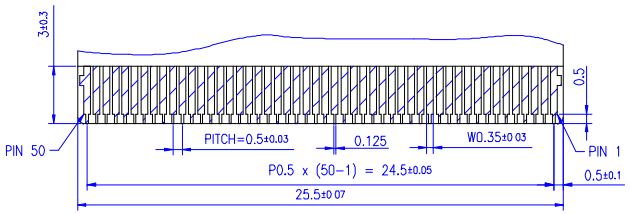
Note 1: Below figure shows dot stripe arrangement.



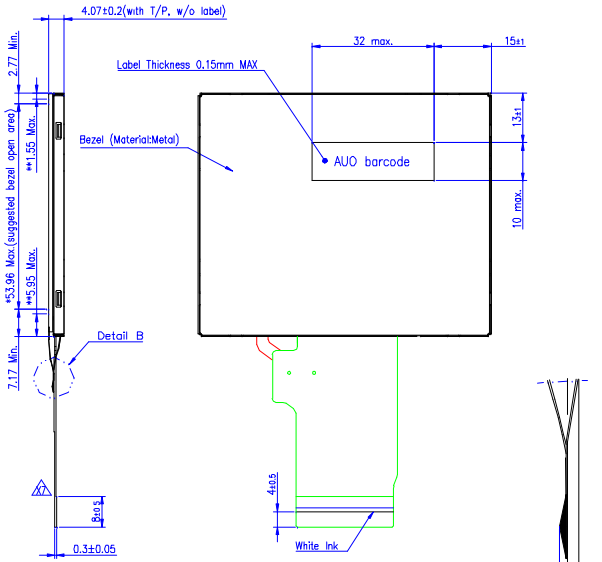
Note 2: Not including FPC. Refer to the drawing next page for further information.

D. Outline Dimension

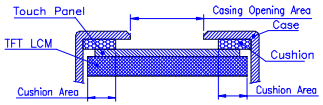




DETAIL A
SCALE 5/1



NOTES:
1. Gerneral tolerance ±0.3mm
2. The bending radius of FPC should be larger than 0.6mm
3. Unit : mm
4. * It means the case open should not be larger than this area .
   ** Suggested gasket (cushion) area



5. *** The thickness of solder area .

DETAIL B
SCALE 5/1

E. Electrical Specifications

1. Pin Assignment

No.	Pin Name	I/O	Description	Remarks
1	LED_C	P	Cathode foe LED back-light	
2	LED_A	P	Anode for LED back-light	
3	NC		No connection. Please leave it open	
4	Y1	O	Touch Panel Top Electrode	
5	X1	O	Touch Panel Right Electrode	
6	Y2	O	Touch Panel Bottom Electrode	
7	X2	O	Touch Panel Left Electrode	
8	NC		No connection. Please leave it open	
9	VGH	C	Stabilizing capacitor	
10	C2P	C	Booster capacitor	
11	C2N	C	Booster capacitor	
12	C1P	C	Booster capacitor	
13	C1N	C	Booster capacitor	
14	VGL	C	Stabilizing capacitor	
15	C3N	C	Booster capacitor	
16	C3P	C	Booster capacitor	
17	VCIX2	C	Stabilizing capacitor	
18	CYP	C	Booster capacitor	
19	CYN	C	Booster capacitor	
20	VCI	P	Booster input voltage pin	
21	GND	C	Power Grounding	
22	VCIM	C	Booster capacitor	
23	CXP	C	Booster capacitor	
24	CXN	C	Booster capacitor	
25	RESET	I	System reset pin	
26	VDDIO	P	Voltage input pin for logic I/O	
27	VCORE	C	Stabilizing capacitor	
28	GND	G	Power Grounding	
29	CSB	I	Chip select pin of serial interface	
30	SDI	I	Data input pin in serial mode	
31	SCK	I	Clock input pin in serial mode	

32	DEN	I	Data enable pin from controller	Fixed to VDDIO if not used.
33	DB7	I	Serial data (MSB)	
34	DB6	I	Serial data	
35	DB5	I	Serial data	
36	DB4	I	Serial data	
37	DB3	I	Serial data	
38	DB2	I	Serial data	
39	DB1	I	Serial data	
40	DB0	I	Serial data	
41	HSYNC	I	Line synchronization signal	Fixed to VDDIO or VSS if not used.
42	VSYNC	I	Frame synchronization signal	Fixed to VDDIO or VSS if not used
43	DOTCLK	I	Dot-clock and oscillator source	
44	NC		No connection. Please leave it open	
45	VLCD63	C	Stabilizing capacitor	
46	VCOMH	C	Stabilizing capacitor	
47	VCOML	C	Stabilizing capacitor	
48	CDMUO	C	Stabilizing capacitor	
49	CSVCMP	C	Stabilizing capacitor	
50	CSVCMN	C	Stabilizing capacitor	

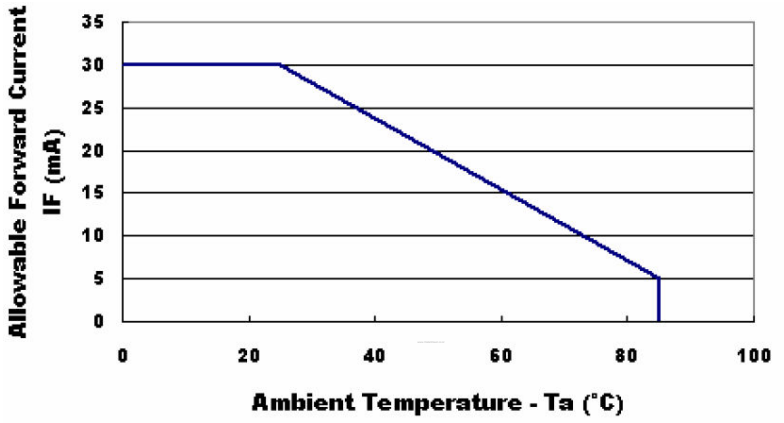
I: Input pin; P: Power pin; G: Ground pin; C: capacitor pin

2. Absolute Maximum Ratings

Items	Symbol	Values		Unit	Condition
		Min.	Max.		
Power Voltage	VCC	-0.3	4	V	
LED Reverse Voltage	Vr		5	V	One LED
LED Forward Current	If		25	mA	One LED, Note 2

Note 1.If the operating condition exceeds the absolute maximum ratings, the TFT-LCD module may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop.

Note 2. If LED current exceeds the limit curve, the lifetime will drop dramatically.



3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

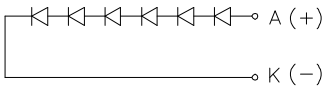
a. TFT- LCD Panel (GND=0V)

Parameter		Symbol	Min	Typ	Max	Unit	Notes
Power Supply		VCC	2.8	3.3	3.6	V	
Frame Frequency		f_{Frame}		60		Hz	
Dot Data Clock	8 bits serial without dummy	DCLK		15	24	MHz	
	8 bits serial with dummy			20	32		
Input Signal Voltage		Vi	0		0.2 x VDDIO	V	
		VI	0.8 x VDDIO		VDDIO	V	
VCOM High Voltage		VCOMH	3.3		6	V	
VCOM Low Voltage		VCOML	-2.5			V	
Current Consumption		IVCC		7	10	mA	VCC= 3.3V

b. Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Supply Current	I_L		20	22	mA	single serial
LED Supply Voltage	V_L	18		21.6	V	single serial
LED Life Time	L_L	10,000	---	---	Hr	Note 2, 3

Note 1: LED backlight is six LEDs serial type.



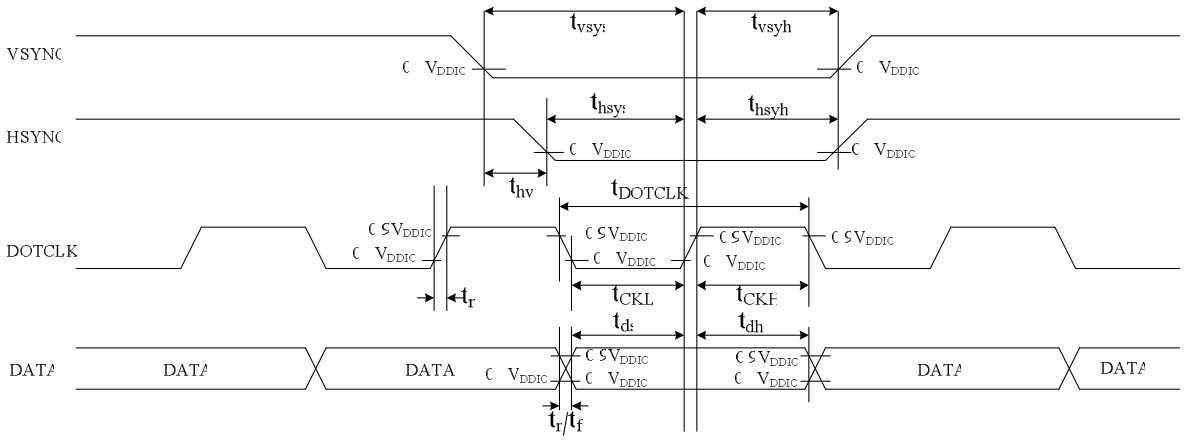
Note 2: The "LED Supply Voltage" is defined by the number of LED at Ta=25°C, I_L=20mA. In the case of 6 pcs LED, V_L=3.2*6=19.2V

Note 3: The "LED life time" is defined as the time for the module brightness to decrease to 50% of the initial value at Ta=25°C, I_L=20mA

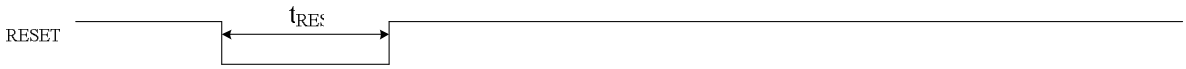
Note 4: The LED lifetime could be decreased if operating $I_L$is larger than 20mA

4. AC Timing

a. Display General Information



Reset Pulse Width:



Characteristics		Symbol	Target Min	Target Typ	Target Max	Units
DOTCLK Frequency	8 bits serial without Dummy	f_{DOTCLK}	-	15	24	MHz
	8 bits serial with Dummy		-	20	32	
DOTCLK Period	8 bits serial without Dummy	t_{DOTCLK}	42	67	-	nSec
	8 bits serial with Dummy		31	50	-	
Vertical Sync. Setup Time		t_{vsys}	5	-	-	nSec
Vertical Sync. Hold Time		t_{vsyh}	5	-	-	nSec
Horizontal Sync. Setup Time		t_{hsys}	5	-	-	nSec
Horizontal Sync. Hold Time		t_{hsyh}	5	-	-	nSec
Phase Difference of Sync. Signal Falling Edge	8 bits serial without Dummy	t_{hv}	0	-	960	t_{DOTCLK}
	8 bits serial with Dummy	t_{hv}	0		1280	t_{DOTCLK}
DOTCLK Low Period		t_{CKL}	16	-	-	nSec
DOTCLK High Period		t_{CKH}	16	-	-	nSec
Data Setup Time		t_{ds}	10	-	-	nSec
Data Hold Time		t_{dh}	10	-	-	nSec
Reset Pulse Width		t_{RES}	2.5	-	-	uSec
Rise/Fall Time		t_r/t_f	5	-	25	nSec

Note: HSYNC's falling and CLK's rising cannot be conflicted.

Note: Amplitude of input single is assumed to be equal to VDDIO (Input digital voltage).

b. 8-bit Serial Interface

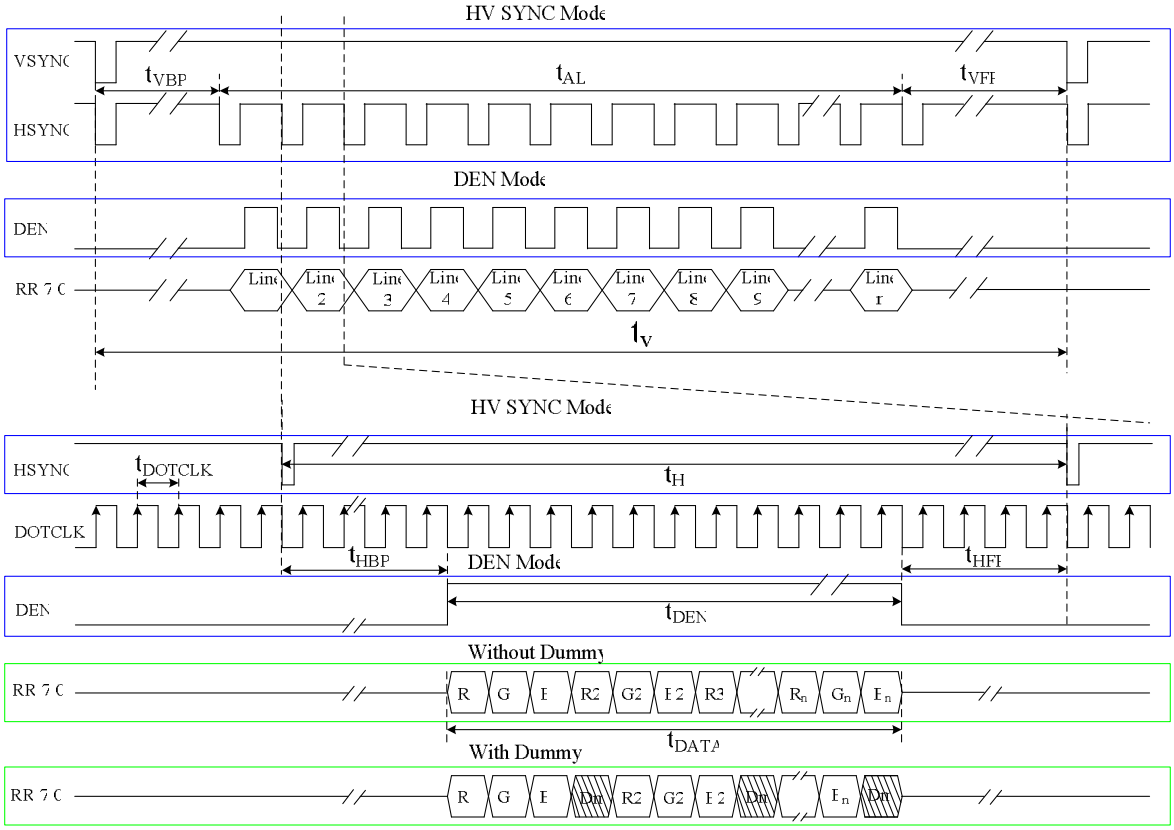


Table: 8-bit Serial Interface HV Sync. Mode without Dummy Timing Characteristics

Characteristics		Symbol	HV SYNC Mode Without Dummy			Units
			Min.	Typical	Max.	
Serial Clock Frequency		$1/t_{DOTCLK}$	13	15	24	MHz
Horizontal	One Line Period	t_H	975	1008	1023	t_{DOTCLK}
	Active Data Period	t_{DATA}	960	960	960	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	10	24	24	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	5	24	39	t_{DOTCLK}
	Hsyn. low polarity width		3			t_{DOTCLK}
Vertical	One Field Period	t_V	244	244	391	t_H
	Active Line Period	t_{AL}	240	240	240	t_H
	Vertical Back Porch	t_{VBP}	2	2	2	t_H
	Vertical Front Porch	t_{VFP}	2	2	149	t_H
	Vsyn. low polarity width		3			t_{DOTCLK}
Frame Rate Frequency			55	60	65	Hz

Table: 8-bit Serial Interface HV Sync. Mode with Dummy Timing Characteristics

Characteristics		Symbol	HV SYNC Mode With Dummy			Units
			Min.	Typical	Max.	
Serial Clock Frequency		$1/t_{DOTCLK}$	18	20	24	MHz
Horizontal	One Line Period	t_H	1344	1344	1344	t_{DOTCLK}
	Active Data Period	t_{DATA}	1280	1280	1280	t_{DOTCLK}
	Horizontal Back Porch	t_{HBP}	32	32	32	t_{DOTCLK}
	Horizontal Front Porch	t_{HFP}	32	32	32	t_{DOTCLK}
	Hsyn. low polarity width		3			t_{DOTCLK}
Vertical	One Field Period	t_V	244	244	275	t_H
	Active Line Period	t_{AL}	240	240	240	t_H
	Vertical Back Porch	t_{VBP}	2	2	2	t_H
	Vertical Front Porch	t_{VFP}	2	2	33	t_H
	Vsyn. low polarity width		3			t_{DOTCLK}
Frame Rate Frequency			55	60	65	Hz

Table: 8-bit Serial Interface DEN Mode without Dummy Timing Characteristics

Characteristics		Symbol	DEN Mode Without Dummy			Units
			Min.	Typical	Max.	
Serial Clock Frequency		$1/t_{DOTCLK}$	13	15	24	MHz
Horizontal	One Line Period	t_H	975	1008	1023	t_{DOTCLK}
	Active Data Period	t_{DATA}	960	960	960	t_{DOTCLK}
	Data Enable Period	t_{DEN}	960	960	960	t_{DOTCLK}
Vertical	One Field Period	t_V	244	244	391	t_H
	Active Line Period	t_{AL}	240	240	240	t_H
Frame Rate Frequency			55	60	65	Hz

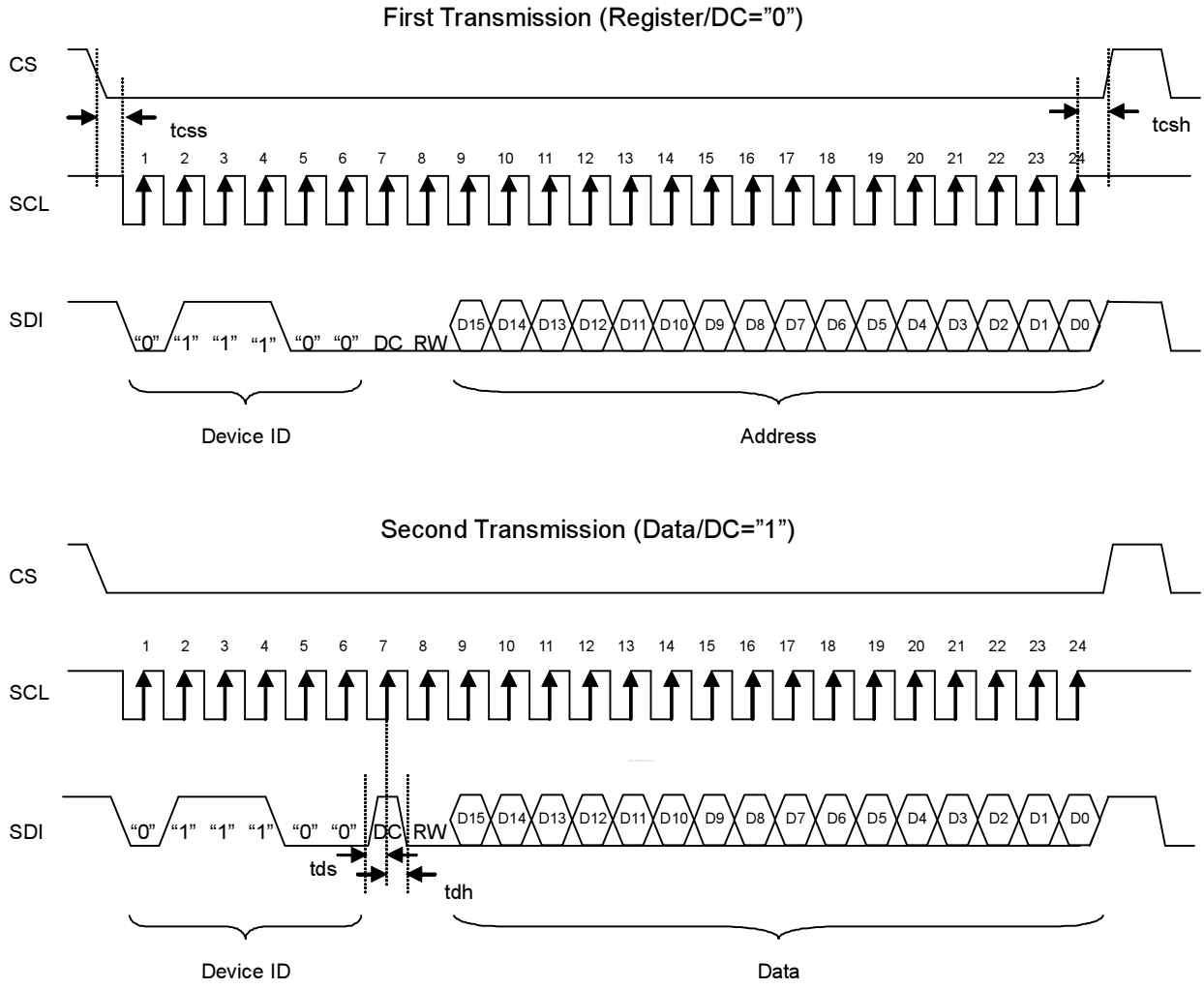
Table: 8-bit Serial Interface DEN Mode with Dummy Timing Characteristics

Characteristics		Symbol	DEN Mode With Dummy			Units
			Min.	Typical	Max.	
Serial Clock Frequency		$1/t_{DOTCLK}$	18	20	24	MHz
Horizontal	One Line Period	t_H	1344	1344	1344	t_{DOTCLK}
	Active Data Period	t_{DATA}	1280	1280	1280	t_{DOTCLK}

	Data Enable Period	t_{DEN}	1280	1280	1280	t_{DOTCLK}
Vertical	One Field Period	t_V	244	244	275	t_H
	Active Line Period	t_{AL}	240	240	240	t_H
Frame Rate Frequency			55	60	65	Hz

c. SPI Timing Diagram

Write Mode RW="0"



d. SPI Timing Specification

Item	Symbol	Conditions	Min	Typical	Max	Unit
Serial clock frequency	tfclk				20	MHz
Serial clock cycle time	tclk		50			nsec
Clock low width	tsl		25			nsec
Clock high width	tsh		25			nsec
Chip select set up time	tcss		0			nsec
Chip select hold time	tcsh		10			nsec
Chip select high delay time	tcsd		20			nsec
Data set up time	tds		5			nsec
Data hold time	tdh		10			nsec

5. Command Register Settings

a. Serial setting map

Reg#	Register	*	D/C	IB15	IB14	IB13	IB12	IB11	IB10	IB09	IB08	IB07	IB06	IB05	IB04	IB03	IB02	IB01	IB00
R	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0
R01h	Driver output	0	1	0	0	*	*	*	*	TB	RL	1	1	1	0	1	1	1	1
	(2AEFh)			0	0	1	0	1	0	1	0	1	1	1	0	1	1	1	1
R03h	Power control (1)	0	1	*	*	*	*	BT2	BT1	BT0	0	*	*	*	*	*	*	*	0
	(920Eh)			1	0	0	1	0	0	1	0	0	0	0	0	1	1	1	0
R0Ch	Power control (2)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0005h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R0Dh	Power control (3)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ch)			0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R0Eh	Power control (4)	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3100h)			0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
R10h	Uniformity	0	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	1	1	0	0
	(00DCh)			0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0
R12h	Entry Control	0	1	0	0	0	0	0	0	0	0	0	*	*	*	IFS1	IFS0	0	0
	(0050h)			0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0
R16h	Horizontal porch	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0
R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R1Eh	Power control (5)	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(00A4h)			0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0
R30h	γ control (1)	0	1	The register setting of R30h ~ R3Bh is adjusted after optical measurement under gamma 2.2 criteria. Please refer to our recommended register settings for better performance.															
	(0304h)																		
R31h	γ control (1)	0	1																
	(0507h)																		
R32h	γ control (1)	0	1																
	(0405h)																		
R33h	γ control (1)	0	1																
	(0007h)																		
R34h	γ control (1)	0	1																
	(0507h)																		
R35h	γ control (1)	0	1																
	(0004h)																		

R36h	γ control (1)	0	1
	(0605h)		
R37h	γ control (1)	0	1
	(0103h)		
R3Ah	γ control (2)	0	1
	(000Fh)		
R3Bh	γ control (2)	0	1
	(000Fh)		

NOTE:

1. "*" is for engineering reserved register setting, and please follow the suggested value.
2. The map shows the recommended values of the LCM, which should be written into the ASIC. However, R16h and R17h are showed default value.
3. Please refer to our recommended register settings section for better performance.

b. Description of serial control data

R01h	Driver output	0	1	0	0	*	*	*	*	TB	RL	1	1	1	0	1	1	1	1
	2AEF			0	0	1	0	1	0	1	0	1	1	1	0	1	1	1	1

TB: Selects the vertical scanning direction of the display.

When TB = "1", the scanning direction is from top to bottom.

When TB = "0", the scanning direction is from bottom to top.

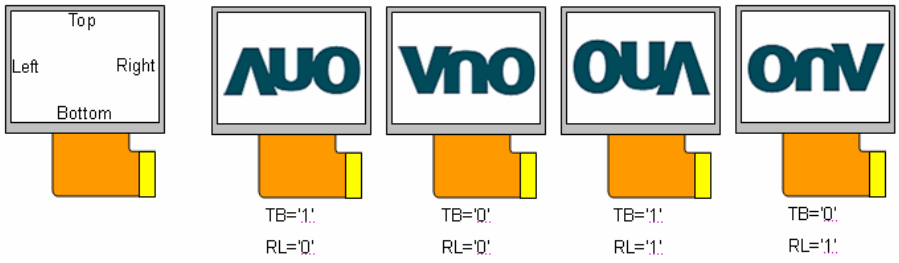
RL: Selects the horizontal scanning direction of the display.

When RL = "1", the scanning direction is from right to left.

When RL = "0", the scanning direction is from left to right.

Note:

1. When the display surface is upward and the FPC golden finger is toward the right, "top", "bottom", "left" and "right" are defined as in the picture below:



2. Please refer to our recommended register settings section for better performance.

R03h	Power control	0	1	*	*	*	*	BT2	BT1	BT0	0	*	*	*	*	*	*	*	0
	(920Eh)			1	0	0	1	0	0	1	0	0	0	0	0	1	1	1	0

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used.

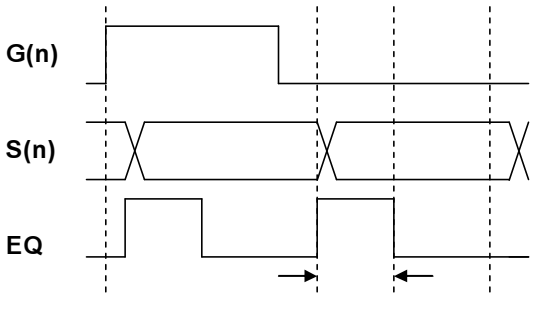
BT2	BT1	BT0	V_{GH} output	V_{GL} output	V_{GH} booster ratio	V_{GL} booster ratio
0	0	0	V_{CIX2}x3	- V_{GH} + VCI	6	-5
0	0	1	V_{CIX2}x3	- V_{GH} + V_{CIX2}	6	-4
0	1	0	V_{CIX2}x3	- V_{CIX2}	6	-2
0	1	1	V_{CIX2}x2+VCI	- V_{GH}	5	-5
1	0	0	V_{CIX2}x2+VCI	- V_{GH} + V_{CIX2}	5	-4
1	0	1	V_{CIX2}x2+VCI	- V_{GH} + V_{CIX2}x2	5	-3
1	1	0	V_{CIX2}x2	- V_{GH}	4	-4
1	1	1	VCIX2x2	- V_{GH} +VCI	4	-3

NOTE: Please refer to our recommended register settings section for better performance.

R0Bh	Frame control	0	1	0	0	0	0	EQ1	EQ0	0	0	EQ2	0	0	0	0	0	0	0
	(D800h)			1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0

EQ[2:0]: Sets the equalizing period on source

EQ2	EQ1	EQ0	EQ period
0	0	0	No EQ
0	0	1	24 pixel clock
0	1	0	42 pixel clock
0	1	1	After VCOM charge sharing + 12 Pixel clock cycle
1	0	0	64 pixel clock
1	0	1	80 pixel clock
1	1	0	96 pixel clock
1	1	1	106 pixel clock



Equalizing period

R0Ch	Power control	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VRC2	VRC1	VRC0
	(0005h)			0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

VRC[2:0]: Adjust VCIX2 output voltage. The adjusted level is indicated in the chart below VRC2-0 setting.

VRC2	VRC1	VRC0	V_{CIX2} voltage
0	0	0	5.1V
0	0	1	5.3V
0	1	0	5.5V
0	1	1	5.7V
1	0	0	5.9V
1	0	1	6.1V
1	1	0	Reserved
1	1	1	Reserved

NOTE: Please refer to our recommended register settings section for better performance.

R0Dh	Power control	0	1	0	0	0	0	0	0	0	0	0	0	0	0	VRH3	VRH2	VRH1	VRH0
	(000Ch)			0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0

VRH3-0: Set amplitude magnification of gamma reference voltage VLCD63. These bits amplify the VLCD63 voltage 1.78 to 3.00 times the Vref voltage set by VRH3-0.

VRH3	VRH2	VRH1	VRH0	V_{LCD63} Voltage
0	0	0	0	Vref x 2.815
0	0	0	1	Vref x 2.905
0	0	1	0	Vref x 3.000
0	0	1	1	Vref x 1.780
0	1	0	0	Vref x 1.850
0	1	0	1	Vref x 1.930
0	1	1	0	Vref x 2.020
0	1	1	1	Vref x 2.090
1	0	0	0	Vref x 2.165
1	0	0	1	Vref x 2.245
1	0	1	0	Vref x 2.335
1	0	1	1	Vref x 2.400
1	1	0	0	Vref x 2.500
1	1	0	1	Vref x 2.570
1	1	1	0	Vref x 2.645
1	1	1	1	Vref x 2.725

NOTE: Please refer to our recommended register settings section for better performance.

R0Eh	Power control	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	0	0	0	0	0
	(3100h)			0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0

VCOMG: When VCOMG = “1”, it is possible to set output voltage of VCOML to any level, and the instruction (VDV4-0) becomes available. When VCOMG = “0”, VCOML output is fixed to Hi-z level, VCI2 output for VCOML power supply stops, and the instruction (VDV4-0) becomes unavailable.

Set VCOMG according to the sequence of power supply setting flow as it relates with power supply operating sequence.

VDV4-0: Set the alternating amplitudes of VCOM at the VCOM alternating drive.

These bits amplify VCOM amplitude 0.6 to 1.23 times the VLCD63 voltage.

When VCOMG = “0”, the settings become invalid.

VDV4	VDV3	VDV2	VDV1	VDV0	VCOMA
0	0	0	0	0	VLCD63 x 0.60
0	0	0	0	1	VLCD63 x 0.63
		:			Step = 0.03
0	1	1	0	1	VLCD63 x 0.99
0	1	1	1	0	VLCD63 x 1.02
0	1	1	1	1	Reserved
1	0	0	0	0	VLCD63 x 1.05
1	0	0	0	1	VLCD63 x 1.08
		:			Step = 0.03
1	0	1	0	1	VLCD63 x 1.20
1	0	1	1	0	VLCD63 x 1.23
1	0	1	1	1	Reserved
1	1	*	*	*	Reserved

NOTE: Please refer to our recommended register settings section for better performance.

R10h	Uniformity	0	1	0	0	0	0	0	0	0	0	ENSVIN	1	0	1	1	1	0	0
	(00DCh)			0	0	0	0	0	0	0	0	1	1	0	1	1	1	0	0

ENSVIN:

When ENSVIN = ‘1’, uniformity improvement scheme is enabled.

When ENSVIN = ’0’, uniformity improvement scheme is disabled.

R12h	Entry Mode	0	1	0	0	0	0	0	0	0	0	0	*	*	*	IFS1	IFS0	0	0
	(0050h)			0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0

IFS1-0: Selection for HV SYNC, DEN, with and without dummy modes.

IF1	IF0	Interface
0	0	8-bit serial RGB DEN Mode (Without Dummy)
0	1	8-bit serial RGB DEN Mode (With Dummy)
1	0	8-bit serial RGB HV SYNC Mode (Without Dummy)
1	1	8-bit serial RGB HV SYNC Mode (With Dummy)

R16h	Horizontal	0	1	XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	0	HBP5	HBP4	HBP3	HBP2	HBP1	HBP0
	(9F86h)			1	0	0	1	1	1	1	1	1	0	0	0	0	1	1	0

XL7-0: Set the number of valid pixel per line.

XL8	XL7	XL6	XL5	XL4	XL3	XL2	XL1	XL0	# of pixels per line
0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	1	2
0	0	0	0	0	0	0	1	0	3
				:					:
				:					step = 1
				:					:
1	0	0	1	1	1	1	1	0	319
1	0	0	1	1	1	1	1	1	320
1	0	1	*	*	*	*	*	*	reserved
1	1	*	*	*	*	*	*	*	reserved

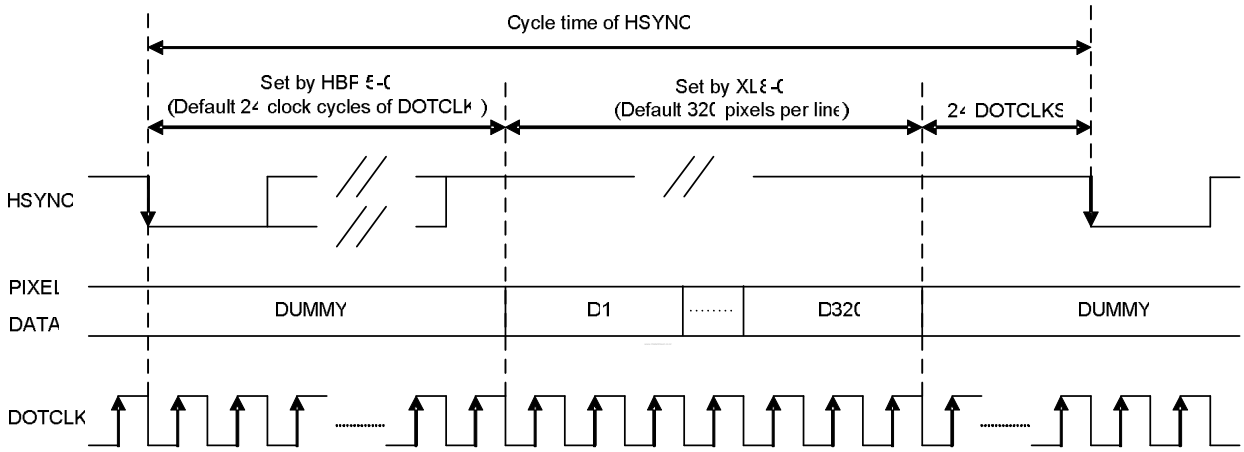
HBP5-0: Set the delay period from falling edge of HSYNC signal to first valid data.

The pixel data exceed the range set by XL8-0 and before the first valid data will be treated as dummy data.

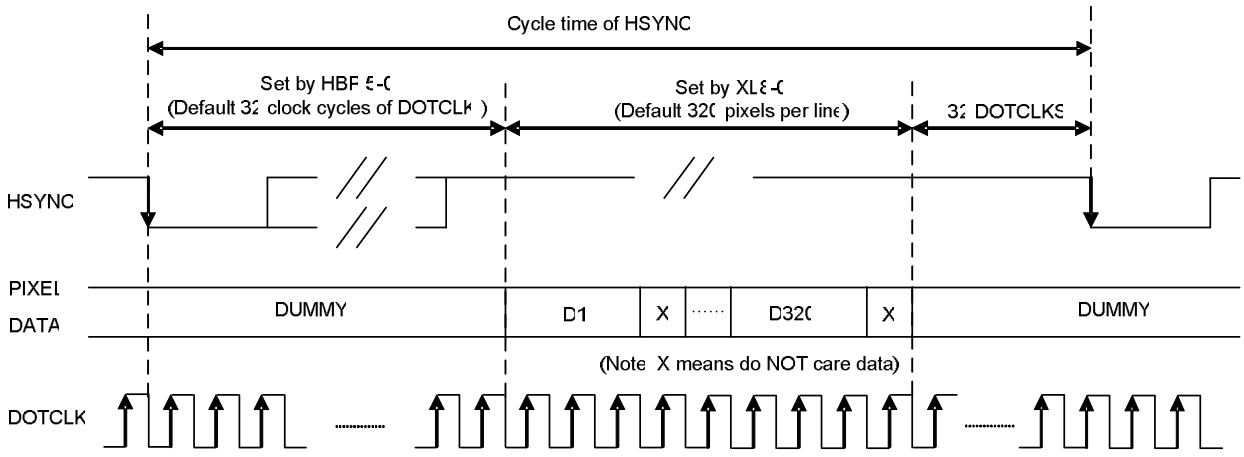
HBP5	HBP4	HBP3	HBP2	HBP1	HBP0	# of clock cycle of DOTCLK	
						8-bit RGB (without dummy)	8-bit RGB (with dummy)
0	0	0	0	0	0	6	8
0	0	0	0	0	1	9	12
0	0	0	0	1	0	12	16

0	0	0	0	1	1	15	20
0	0	0	1	0	0	18	24
0	0	0	1	0	1	21	28
0	0	0	1	1	0	24	32
:						: step = 3 :	: step = 4 :
1	1	1	1	1	0	192	256
1	1	1	1	1	1	195	260

Example for 8-bit RGB Interface (without dummy):



Example for 8-bit RGB Interface (with dummy):

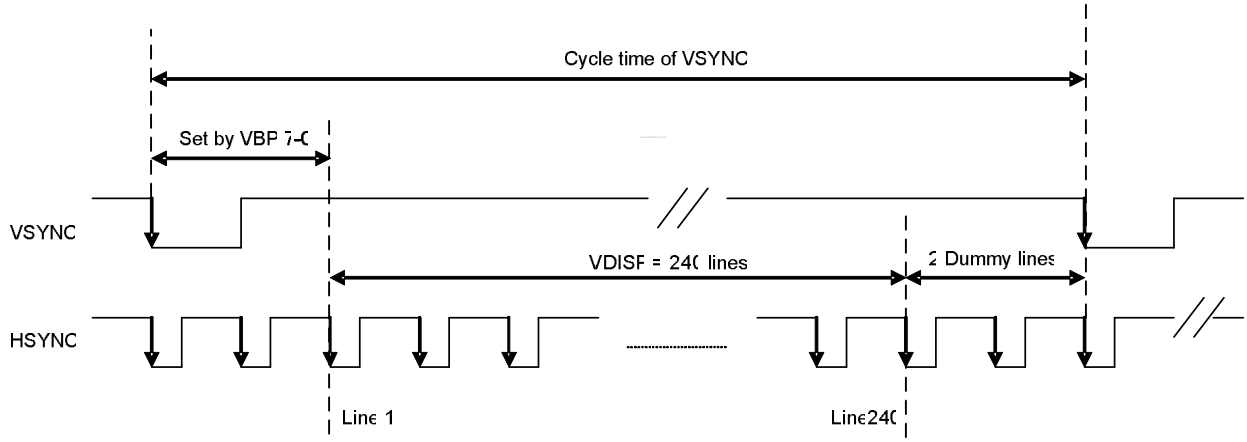


R17h	Vertical porch	0	1	0	0	0	0	0	0	0	0	VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0
	(0002h)			0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

VBP7-0: Set the delay period from falling edge of VSYNC to first valid line.

The line data within this delay period will be treated as dummy line.

VBP7	VBP6	VBP5	VBP4	VBP3	VBP2	VBP1	VBP0	# of lines per frame
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	0	2
				:				:
				:				step = 1
				:				:
1	1	1	0	1	1	1	1	239
1	1	1	1	0	0	0	0	240
1	1	1	1	*	*	*	*	reserved



R1Eh	Power	0	1	0	0	0	0	0	0	0	0	nOTP	0	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0
	(00A4h)			0	0	0	0	0	0	0	0	1	0	1	0	0	1	0	0

nOTP: nOTP equals to “0” after power on reset and VCOMH voltage equals to programmed OTP value.

When nOTP set to “1”, setting of VCM5-0 becomes valid and voltage of VCOMH can be adjusted.

VCM5-0: Set the VCOMH voltage if nOTP = “1”. These bits amplify the VCOMH voltage 0.36 to 0.99 times the VLCD63 voltage by step = 0.01.

NOTE: Please refer to our recommended register settings section for better performance.

R30h	γ control (1) (0000h)	The register setting of R30h ~ R3Bh is adjusted after optical measurement under gamma 2.2 criteria. Please refer to our recommended register settings for better performance.
R31h	γ control (1)	

	(0200h)	
R32h	γ control (1)	
	(0001h)	
R33h	γ control (1)	
	(0700h)	
R34h	γ control (1)	
	(0405h)	
R35h	γ control (1)	
	(0202h)	
R36h	γ control (1)	
	(0707h)	
R37h	γ control (1)	
	(0006h)	
R3Ah	γ control (2)	
	(0700h)	
R3Bh	γ control (2)	
	(0003h)	

F. Optical specifications (Note 1, 2)

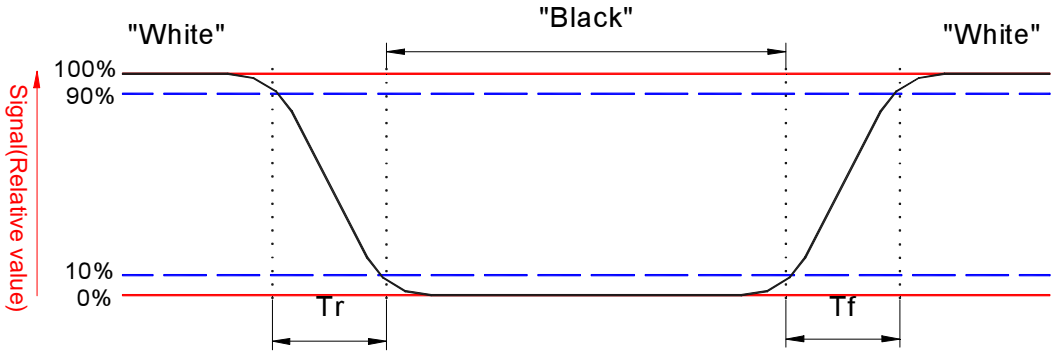
Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	10	20	ms	Note 3
Fall	Tf		-	15	25	ms	
Contrast ratio	CR	At optimized viewing angle	150	300	-		Note 5, 6
Viewing Angle							
Top			35	50	-		
Bottom		CR≧10	40	55	-	deg.	Note 7, 8
Left			45	60	-		
Right			45	60	-		
Brightness	Y_L	θ =0°	280	350	-	cd/m^2	Note 9
NTSC			50	60		%	
White Chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.28	0.33	0.38		

Note 1: Measurement should be performed in the dark room, optical ambient temperature =25°C, and backlight current I_L=20 mA

Note 2: To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.



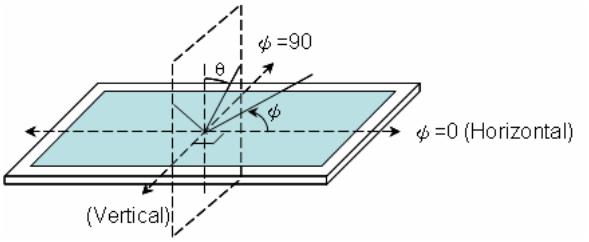
Note 4. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25°C.

Note 5. Contrast ratio is calculated with the following formula.

$$\text{Contrastratio} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White Vi=Vi50 μ 1.5V
Black Vi=Vi50 ± 2.0V
"±" means that the analog input signal swings in phase with COM signal.
"μ" means that the analog input signal swings out of phase with COM signal.
Vi50 :The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: refer to figure as below.



Note 8. The viewing angles are measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

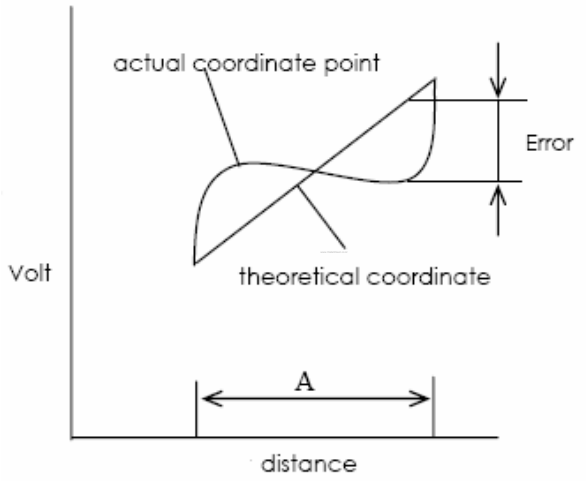
Note 9. Brightness is measured at the center point of the display area.

G. Touch Screen Panel Specifications

1. Electrical Characteristics

Item		Min.	Max.	Unit	Remark
Rate DC Voltage			7	V	
Resistance	X (Film)	350	950	Ω	At connector
	Y (Glass)	150	800		
Linearity		-1.5%	1.5%	--	Note 1, test by 250 gf
Chattering			10	ms	At connector pin
Insulation Resistance		10M		Ω	DC 25V

Note 1: Measurement condition of Linearity: difference between actual voltage & theoretical voltage is an error at any points. Linearity is the value max. error voltage divided by voltage difference on active area.



2. Mechanical Characteristics

Item	Min.	Max.	Unit	Remark
Hardness of Surface	3	--	H	JIS K-5400
Operation Force (Pen or Finger)	--	100	gf	Note 1

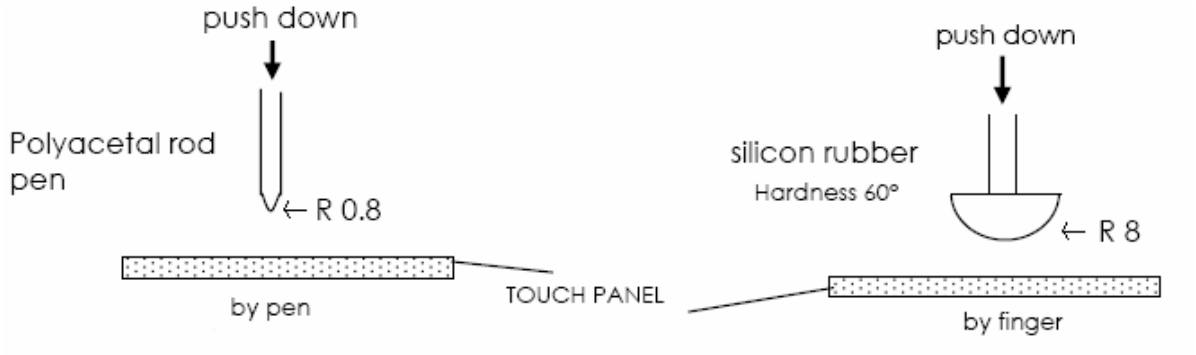
Note 1: Within ”guaranteed active area”, but not on the edge and dot-spacer.

3. Life test Condition

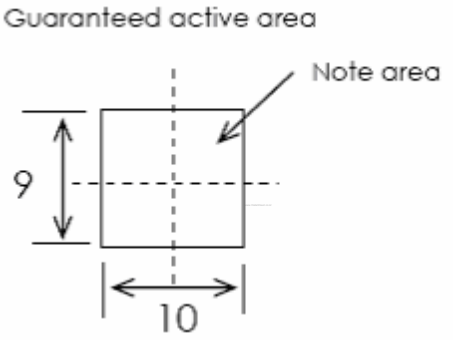
Item	Min.	Max.	Unit	Remark
Notes Life	10^5	--	words	Note 1, 2
Input Life	10^6	--	times	Note 1, 3

Note 1: Measurement condition of Operation Force: Within ”guaranteed active area”. Resistance,

Insulation resistance, and operation force should be under 5.2 & 5.3 condition. When user pushes down on the film, resistance between X & Y axis must be equal or lower than 2kΩ. Below is test figure.



Note 2: Notes Life test condition (by pen): Notes area for pen notes life test is 10×9 mm. Size of word is 7.5×6.75mm. Word is any A.B.C….. letter. Writing speed is 60mm/s. Center of each word is changed at random in notes area.



Note 3: Input Life test condition(by finger): By silicone rubber tapping at same point. Tapping Load is 200g, and tapping frequency is 5Hz.

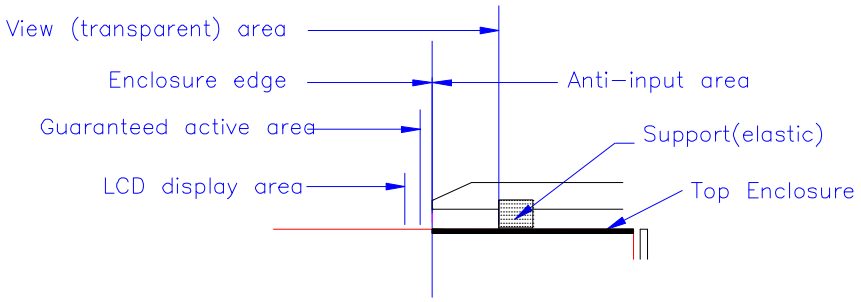
4. Attention

Please pay attention for below matters at mounting design of touch panel of LCD module.

1. Do not design enclosure pressing the view area to prevent from miss input.
2. Enclosure support must not touch with view area.
3. Use elastic or non-conductive material to enclosure touch panel.
4. Do not bond film of touch panel with enclosure.
5. The touch panel edge is conductive. Do not touch it with any conductive part after mounting.
6. If user wants to cleaning touch panel by air gun, pressure 2kg/cm2 below is suggested. Not to blow glass from FPC site to prevent FPC peeled off.
7. Do not put a heavy shock or stress on touch panel and film surface. Ex. Don't lift the panel by film face with vacuum.

8. Do not lift LCD module by FPC.
9. Please use dry cloth or soft cloth with neutral detergent (after wring dry) or one with ethanol at cleaning. Do not use any organic solvent, acid or alkali liquor.
10. Do not pile touch panel. Do not put heavy goods on touch panel.

Recommendation of the cushion area:



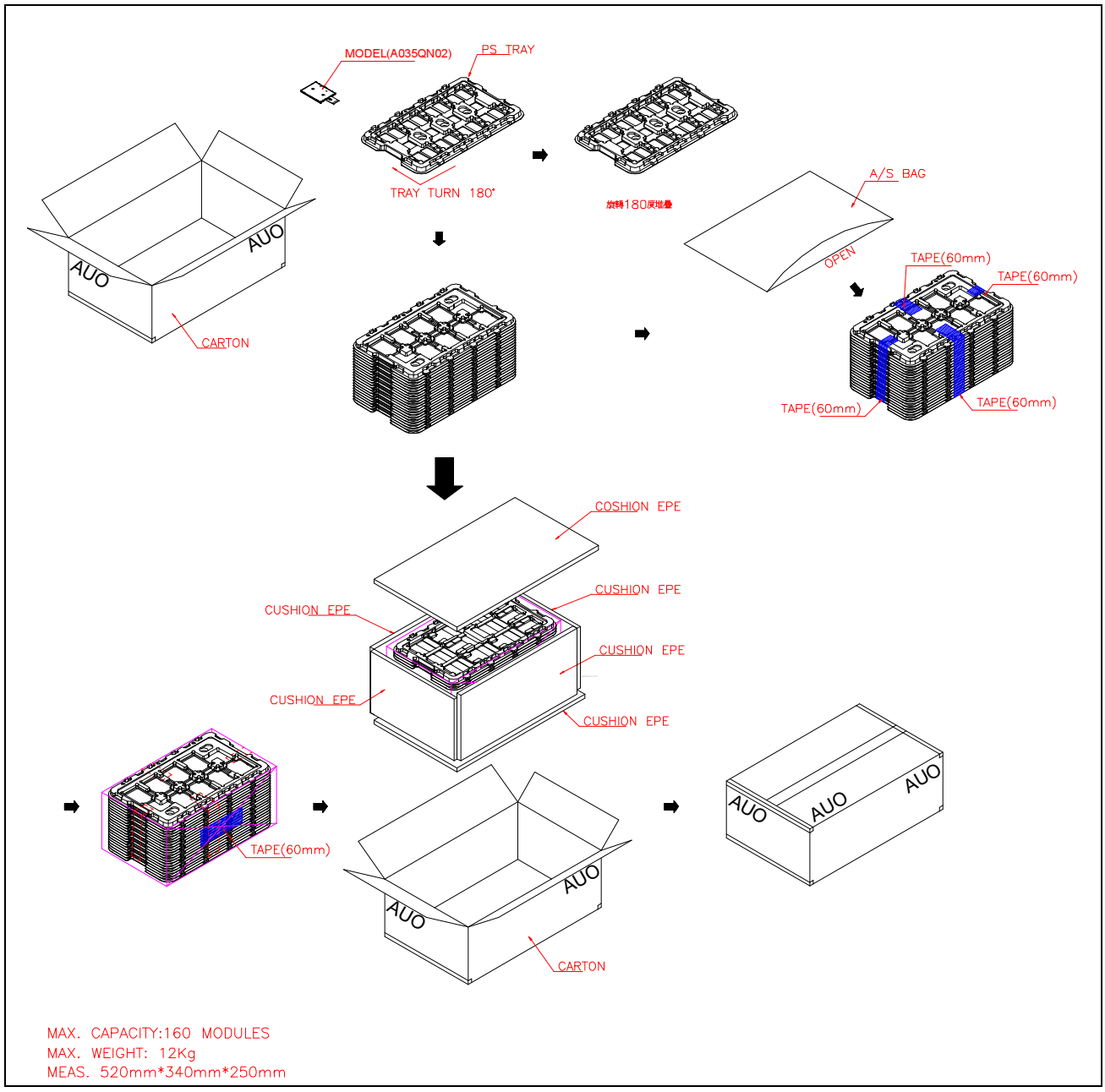
H. Reliability Test Items

No.	Test items	Conditions		Remark
1	High Temperature Storage	Ta= 85°C	240Hrs	
2	Low Temperature Storage	Ta= -30°C	240Hrs	
3	High Temperature Operation	Ta= 70°C	240Hrs	
4	Low Temperature Operation	Ta= -20°C	240Hrs	
5	High Temperature & High Humidity	Ta= 60°C. 90% RH	240Hrs	Operation
6	Heat Shock	-25°C~70°C, 50 cycle, 2Hrs/cycle		Non-operation
7	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/Octave from 200~500Hz		IEC 68-34
8	Drop (With Carton)	Height: 66cm 1 corner, 3 edges, 6 surfaces		

Note 1: In the standard conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2: Ta: Ambient temperature.

I. Packing Form



J. Application Note

1. Recommended Register Settings

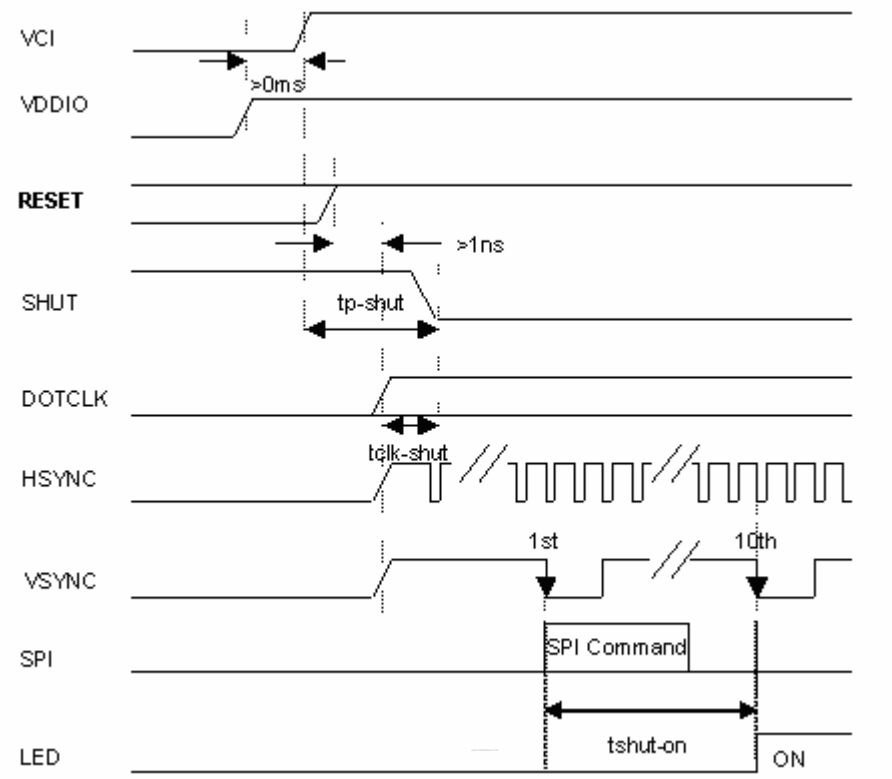
Register	Setting
R01	“2AEF”h
R03	“920E”h
R0B	“DC80”h
R0C	“0005”h
R0D	“000C”h
R0E	“3100”h
R10	“00DC”h
R12	“0050”h, which is set to be DEN mode and RGB without dummy data
R16	H/V blanking setting if necessary.
R17	
R1E	“00A4”h
R30	“0304”h
R31	“0507”h
R32	“0405”h
R33	“0007”h
R34	“0507”h
R35	“0004”h
R36	“0605”h
R37	“0103”h
R3A	“000F”h
R3B	“000F”h

NOTE:

1. The different sequence of registers setting would not affect the normal behavior of LCM.
2. Please refer to the POWER ON/OFF sequence section for register setting timing as power-on.

2. Power on/off Sequence

Power On

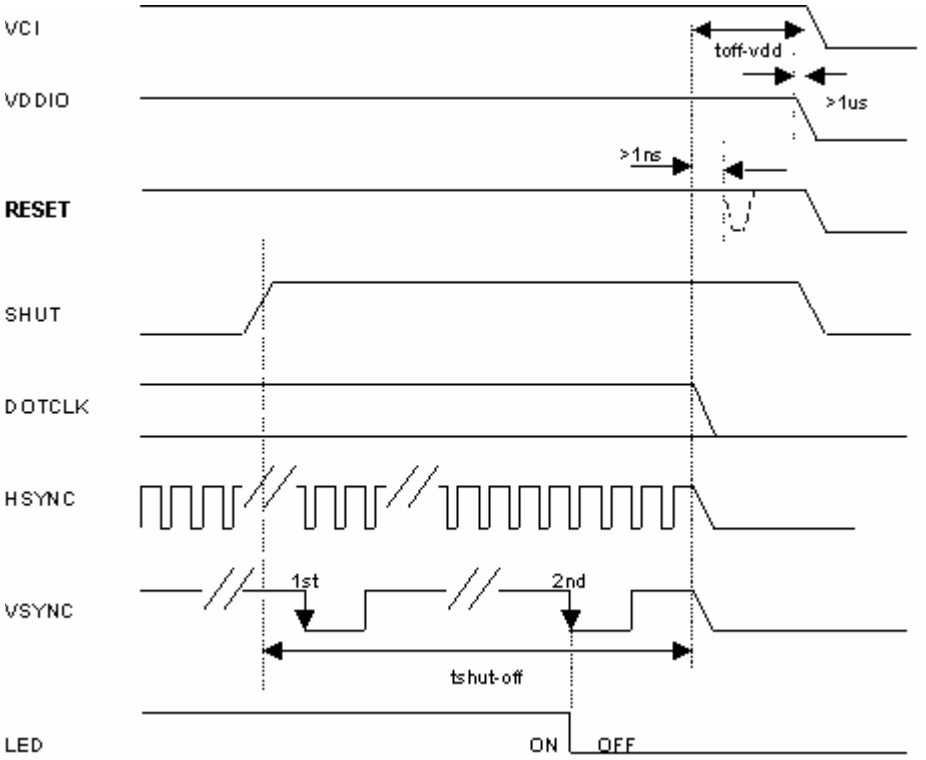


Characteristics	Symbol	Min	Typ	Max	Unit
VDDIO on to falling edge of SHUT	tp-shut	1	-	-	uSec
DOTCLK	tclk-shut	1	-	-	clk
Falling edge of SHUT to display on	tshut-on	-	-	10	frame
-- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz		-	164	-	mSec

Note1: It is necessary to input DOTCLK before the falling edge of SHUT.

Note2: Display starts at 10th falling edge of VSTNC after the falling edge of SHUT

Power Off



Characteristics	Symbol	Min	Typ	Max	Unit
Rising edge of SHUT to display off	tshut-off	2	-	10	frame
-- 1 line: 336 clk -- 1frame: 244 line -- DOTCLK = 5.0 MHz		32.8	-	-	mSec
Input-signal-off to V_{DDIO} off	toff-vdd	1	-	-	uSec

Note1: DOTCLK must be maintained at lease 2 frames after the rising edge of SHUT.

Note2: Display become off at the 2nd falling edge of VSTNC after the falling edge of SHUT.

Note3: If RESET signal is necessary for power down, provide it after the 2-frames-cycle of the SHUT period.

3. Suggested Circuit

The suggested circuit and recommended capacitor sepcification are both showed as follows. Please refer to the design for better display quality.