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Doc. Version	1.0
Total Pages	26
Date	2004/12/15

Product Specification
3.6″ COLOR TFT-LCD MODULE

MODEL NAME: A036QN01 V0

<◆>Preliminary Specification
< >Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
0	12/Feb/2004		First draft.
0.1	25/Feb/2004	11	Add a note “DCLK Tr and Tf is defined at 10%~90%” and a refer figure
0.2	1/Mar/2004	7	Correct Note4 text from “SEL0=Low, SEL1=High, SEL0=Low” to “SEL0=Low, SEL1=High, SEL2=Low”
0.3	4/May/2004	5-6 23-25	1) Point out optional VGH and LED backlight driving circuit in FPC pin assignment. 2) Provide suggested application circuit for private power supply of V_{GH}, V_{GL} and LED backlight driving
0.4	19/May/2004	4 7	1) Correct dot pitch. 2) Provide definition and suggestion of select pin in Note 4 and Note 5.
0.5	18/Jun/2004	7 10 23-26	1) Modify “SEL2” setting in Note 4, from “Low (or 0)” to N/C 2) Modify “Current consumption” table. 3) Modify application circuits.
0.6	26/Jul/2004	10 23-26	1) Confirm VCDC Value. 2) Modify application circuits.
0.7	05/Aug/2004	4 13 13 23-26	1) Add item “color depth”. 2) Modify response time. 3) Define white chromaticity. 4) Modify application circuits.
0.8	07/Sep/2004	9 10 14	1) Update “Equivalent circuit of I/O”. 2) Update AVDD & VCDC 3) Update “Current Consumption”. 4) Update left and right viewing angle.
0.9	29/Oct/2004	23-26	Modify application circuit.
1.0	22/Nov/2004		Re-edit spec.
1.1	15/Dec/2004	8 9 13-16 20 22	Modify description of Note 1. Modify V_{CDC} setting. Modify 3.5 suggested application circuit. Modify parameter of “Delay from HSYNC to 1st data” and “Delay from VSYNC to 1st data”, and note 2. Add “Power-on Sequence” figure

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General Description

A036QN01 V0 is a amorphous transmissive type TFT (Thin Film Transistor) LCD (Liquid crystal Display). This model is composed of TFT-LCD, drive IC, FPC (flexible printed circuit), and backlight unit.

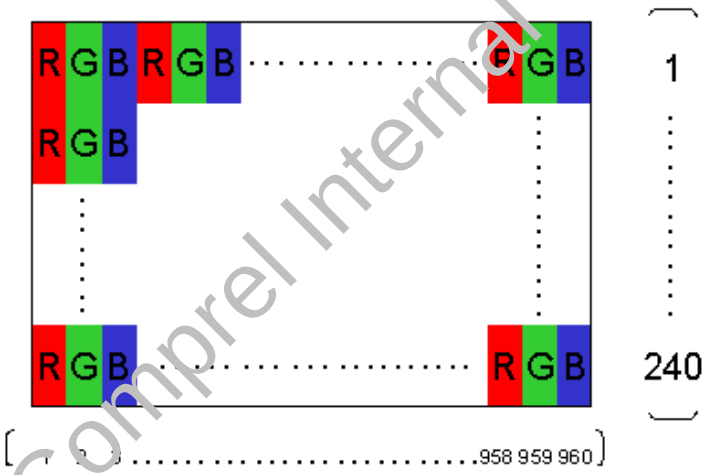
Features

- 3.6-inch display size
- QVGA resolution and stripe dot arrangement
- Small Integration Advanced: built in timing controller and two DC-DC controller
- Single 3.3V power supply
- Standby mode supported
- VCOM amplitude selected
- Low power consumption
- 8-bit digital signal Interface
- NTSC and PAL standard supported
- 2-in-1 FPC
- Slim 3.2mm thickness design
- Green design

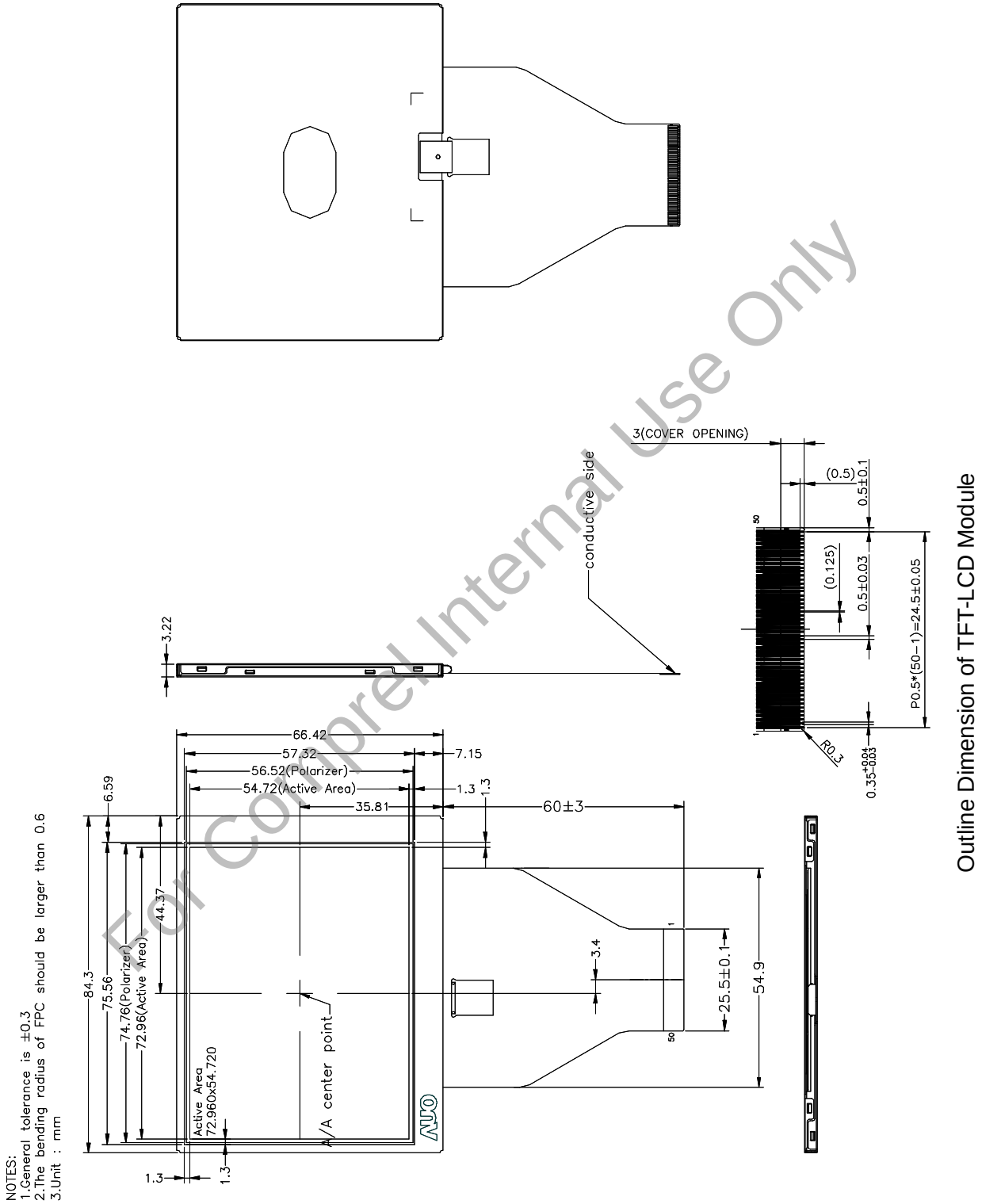
1. General Information

NO.	Item	Unit	Specification	Remark
1	Display Resolution	dot	960(H)x240(V)	
2	Active Area	mm	72.96(H)x54.72(V)	
3	Screen Size	inch	3.59(Diagonal)	
4	Dot Pitch	mm	0.076(H)x0.228(V)	
5	Color Configuration	--	R. G. B. Stripe	Note 1
6	Color Depth	--	16.7M Colors	Note 2
7	Overall Dimension	mm	84.3(H) × 66.42(V) × 3.2(T)	Note 3
8	Weight ()	g	38 (Typical)	
9	Panel surface treatment	--	Anti-Glare	
10	Display Mode	--	Normally White	

Note 1: Below figure shows dot stripe arrangement.



Note 2: The full color display depends on 8-bit data signal (pin35~42).
Note 3: Not include FPC. Refer next page to get further information.



Outline Dimension of TFT-LCD Module

2. Electrical Specifications

2.1 FPC Pin Assignment

Pin No.	Symbol	I/O	Description	Remark
1	VCSL2	I	VCAC level selection	Note 1
2	VCSL1	I	VCAC level selection	Note 1
3	VCSL0	I	VCAC level selection	Note 1
4	GND	G	Digital ground for gate driver	
5	VCC	PI	Digital power for gate driver (+3.3V)	
6	VCAC	PS	VCOM level supply	
7	VGoff_H	PS	Negative power supply (High) for gate driver	
8	VCOM	SO	Frame polarity output for panel VCOM	
9	VGoff_L	PS	Negative power supply (Low) for gate driver	
10	C3M	C	Power setting capacitor connect pin	
11	C3P	C	Power setting capacitor connect pin	
12	VGH	PI	Positive power supply for gate driver (+15V)	Option Note 2
13	GND	G	Ground	
14	FB_G	FI	Main boost regulator feedback input. FB threshold is 0.6V	
15	GND	G	Ground	
16	DRV_G	O	Power transistor gate signal for the boost converter	
17	GLED1	PI	LED module 1 cathode	
18	VLED1	-	LED module 1 anode	Option Note 2
19	VLED2	-	LED module 2 anode	Option Note 2
20	GLED2	PI	LED module 2 cathode	
21	DRV_S	O	Power transistor gate signal for the boost converter	
22	FB_S	FI	Main boost regulator feedback input. FB threshold is 0.6V	
23	GND	G	Digital ground for source driver	

24	SHL	I	Selects left or right shift (Default=”H”)	Note 3
25	STB	I	Standby mode (Default=”H”, Normal operation)	Note 4
26	VCC	PI	Digital power supply for source driver (+3.3V)	
27	SHDB	I	Shutdown input (SHDB=“L” DRV_S is off, Default=”L”)	Note 5
28	AVDD	PI	Analog power supply (+3.3V)	
29	AGND	G	Analog ground	
30	VSYNC	I	Vertical sync input (Negative polarity)	
31	HSYNC	I	Horizontal sync input (Negative polarity)	
32	GND	-	Ground	
33	DCLK	I	Clock signal	
34	GND	-	Ground	
35	D07	I	Data input (MSB)	
36	D06	I	Data input	
37	D05	I	Data input	
38	D04	I	Data input	
39	D03	I	Data input	
40	D02	I	Data input	
41	D01	I	Data input	
42	D00	I	Data input (LSB)	
43	GND	-	Ground	
44	RSTB	I	Global reset pin (Default=”H”, Normal operation)	Note 6
45	SEL0	I	Data format selection (Default=”L”)	Note 7
46	SEL1	I	Data format selection (Default=”L”)	Note 7
47	NC	-		
48	U/D	I	Shift up or down control. (Default=H”)	Note 3
49	NC	-		
50	VCOM_O	SI	VCOM Input	

I: Digital signal input, O: Digital signal output, G: GND, PI: Power input

C: Power set capacitor connect pin, FI: Feedback input, PS: Power setting,

SO: VCOM signal output, SI: VCOM_O signal input,

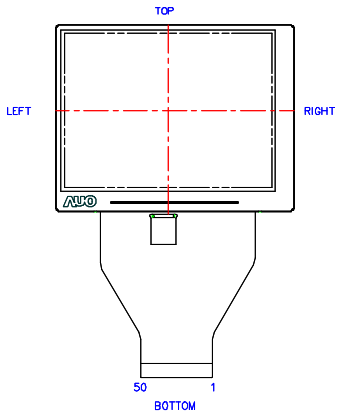
Note 1: Selection of VCAC level.

VCAC Input Pin Setting			VCAC Level (unit: V)		
VCSL2	VCSL1	VCSL0	Min.	Typ.	Max
0	0	0	4.0	4.4	4.6
0	0	1	4.2	4.6	4.8
0	1	0	4.4	4.8	5.0
0	1	1	4.6	5.0	5.2
1	0	0	4.8	5.2	5.4
1	0	1	5.0	5.4	5.6
1	1	0	5.2	5.6(Default)	5.8
1	1	1	5.4	5.8	6.0

Note 2: SIA (Smart Integration Advanced) platform provides internal PWM driving circuit (for VGH, VGL and LED backlight), application circuit as 3.5.1. Customer can optionally adapt these internal driving circuit or provides private power supply as 3.5.2~3.5.4.

Note 3: Selection of scanning mode

Mode	Setting of scan control input		Scanning direction
	U/D	SHL	
Normal Mode	L	H	From up to down, and from left to right.
Reserve Mode	H	L	From down to up, and from right to left.



Note 4: If STB is high, it is normal operation. If it is low, it is standby mode. Normally pulled high.

Note 5: If SHDB is high, DC-DC converter lights on backlight. If it is low, DC-DC converter and backlight is off. Normally pulled low.

Note 6: If RSTB is low, the controller is reset. If it is connected to VCC and set high, it is normal operation. Normally pulled high.

Note 7:Interface select pin, set “SEL0=Low, SEL1=High” for A036QN01 V0.

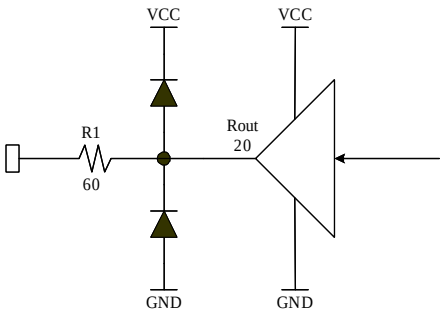
SEL1	SEL0	Data Input Format	Operating Frequency
1	0	Data format : D00~D07 , 8-bits (Pin35~42)	19.4MHz (NTSC)
1	1	Data format : D00~D07 , 8-bits (Pin35~42)	19.4MHz (PAL)

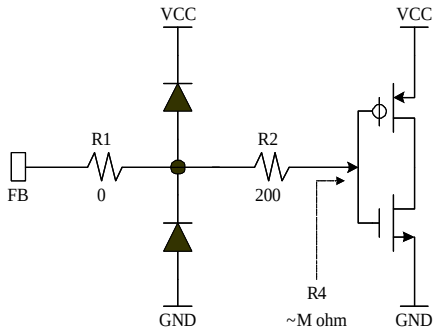
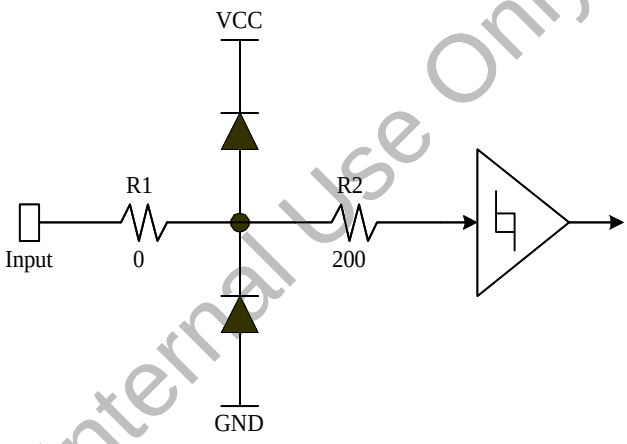
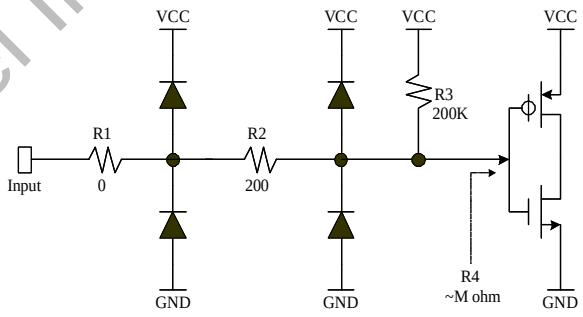
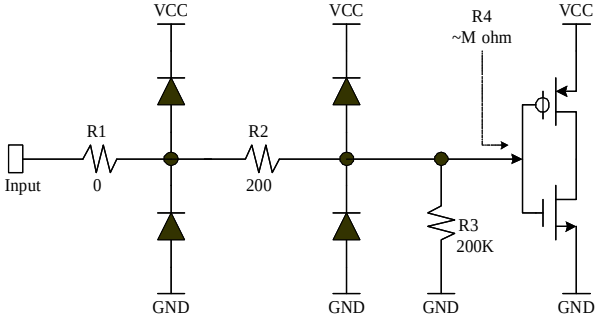
2.2 Absolute Maximum Ratings

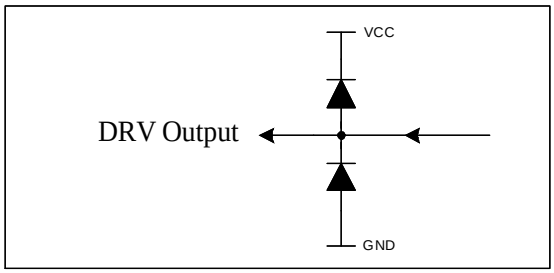
Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	VCC	GND=0	-0.5	5	V	Note 1
	AVDD	AGND=0	-0.5	7	V	Note 1
	VGH	GND=0	13	20	V	Note 1
Operating temperature	Topa	--	0	60	℃	Ambient Temperature
Storage temperature	Tstg	--	-25	80	℃	Ambient Temperature

Note 1: Functional operation should be restricted under normal ambient temperature.

2.3 Equivalent Circuit of I/O

Pin No. & Pin Name	Schematics
Pin08: VCOM	

Pin14: FB_G Pin22: FB_S	
Pin30: Vsync Pin31: Hsync Pin33: DCLK Pin35: D07 Pin36: D06 Pin37: D05 Pin38: D04 Pin39: D03 Pin40: D02 Pin41: D01 Pin42: D00	
Pin01: VCSL2 Pin02: VCSL1 Pin24: SHL Pin25: STB Pin44: RSTB Pin48: U/D	
Pin03: VCSL0 Pin27: SHDB Pin45: SEL0 Pin46: SEL1	

Pin21: DRV_S Pin16: DRV_G	

3. Electrical Characteristics

The following items are measured under stable condition and suggested application circuit.

3.1 TFT-LCD Typical Operation Condition

Item		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply		VCC	3.0	3.3	3.6	V	
		AVDD	3.0	3.3	3.6	V	
		VGH	13	15	17	V	
		VGoff_H	VGoff_L+VCAC			V	
		VGoff_L	-11	-10	-8.5	V	
VCOM		VCAC	4.4	---	5.8	Vp-p	Note 1
		VCDC	0.25	0.33	0.41	V	Note 2
Output Signal	H Level	V_{OH}	VCC-0.4	---	---	V	
	L Level	V_{OL}	GND	---	GND+0.4	V	
Input Signal Voltage	H Level	V_{IH}	0.8VCC	---	VCC	V	
	L Level	V_{IL}	GND	---	0.2VCC	V	
DRV Output Voltage		DRV_S	0	---	VCC	V	
		DRV_G	0	---	VCC	V	
DRV Output Current		DRV_S	---	---	10	mA	
		DRV_G	---	---	10	mA	
Feedback Voltage		FB_S	0..55	0.6	0.65	V	
		FB_G	0.55	0.6	0.65	V	

Note 1: The contrast of LCD panel could be adjusted by VCAC.

Note 2: VCDC could be adjusted so as to minimize flicker on each panel.

Note 3: Above every operation range is based on stable operation from suggested application circuit 3.5.1.

Note 4: GND=AGND=0V

3.2 TFT-LCD Current Consumption

Pin Name	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit	Remark
Current for Source Driver	ICC	26	VCC=3.3V	---	3.7	4.5	mA	Black Pattern
	IDD	28	AVDD=3.3V	---	2.8	3.5	mA	Black Pattern
Current for Gate Driver	IGH	12	VGH=15V	---	3.0	4.0	mA	Black Pattern
	ICC	5	VCC=3.3V	---	0.5	0.7	mA	Black Pattern
Total Power Consumption	(ICC+IDD)*3.3V+IGH*15V			---	68.1	88.7	mW	Black Pattern

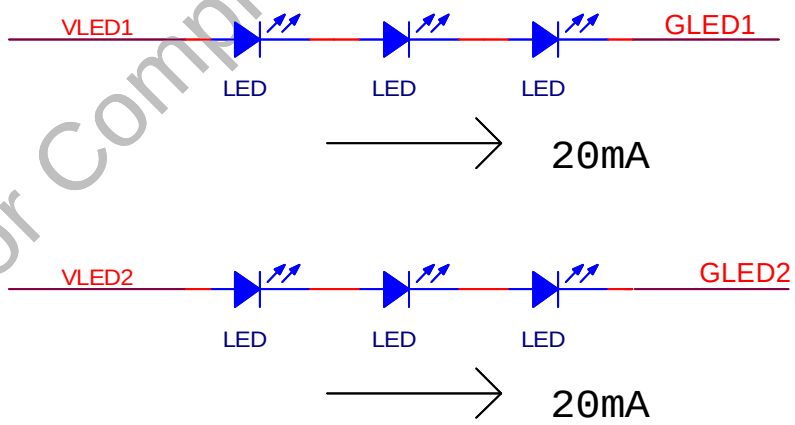
Note 1: GND=AGND=0

Note 2: Above current results are measured from suggested application circuit 3.5.1.

3.3 Backlight Driving Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED Current	I_L	---	20	---	mA	single seral
LED Voltage	V_L	---	9.9	12	V	single seral
LED Life Time	L_L	10000	---	---	Hr	Note 2, 3

Note 1: LED backlight is two parallel types and three LEDs serial type as below figure.

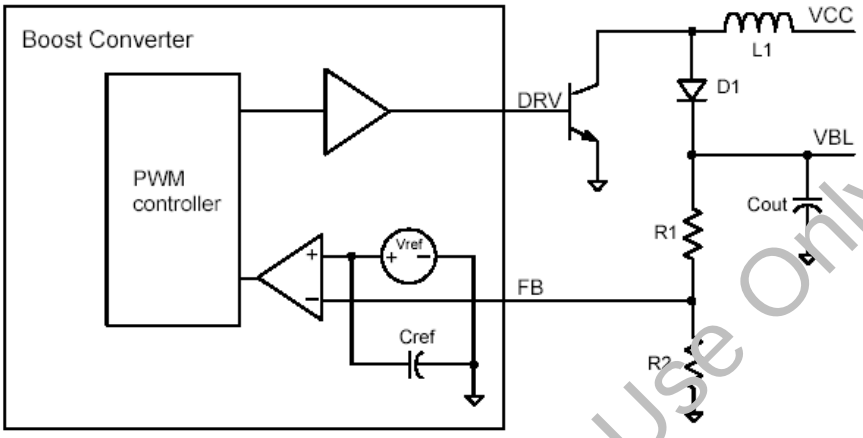


Note 2 :Define “LED Lifetime”: brightness is decreased to 50% of the initial value. LED Lifetime is restricted under normal condition, ambient temperature = 25℃ and LED current = 20mA.

Note 3: If it uses larger LED current I_L more than 20mA, it maybe decreases the LED lifetime.

3.4 Boost Converter

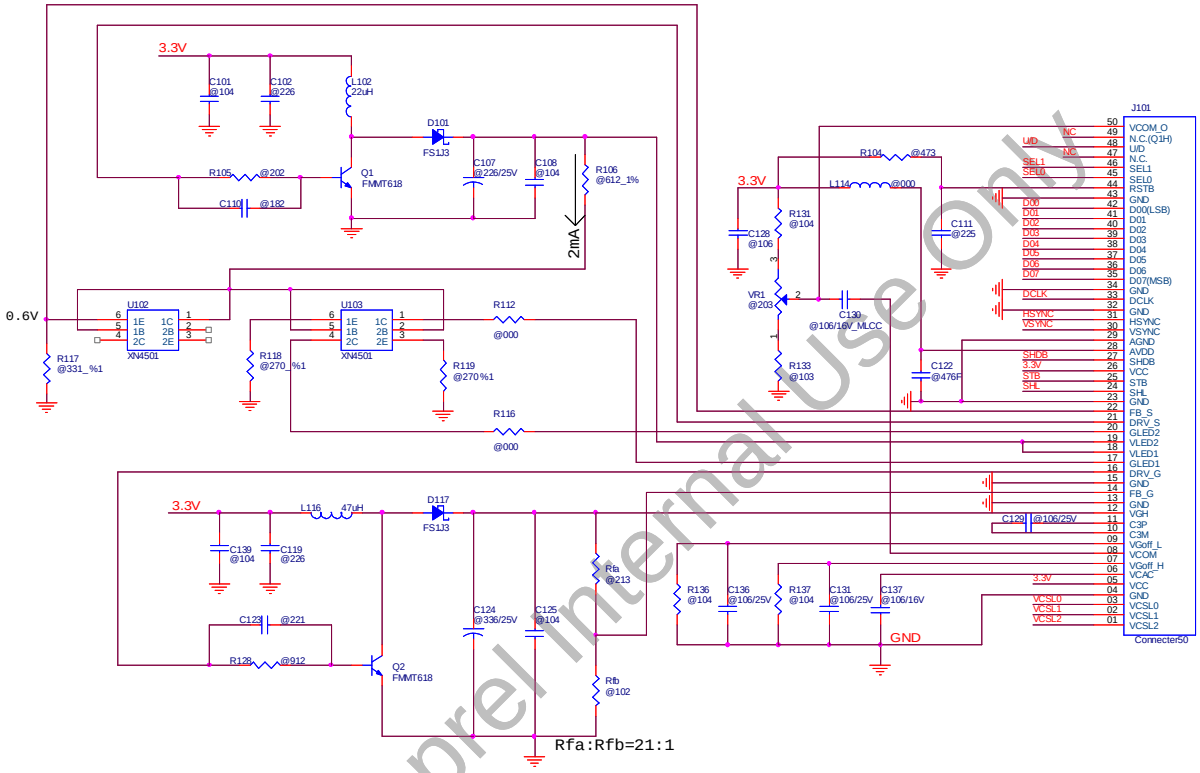
A036QN01 V0 main boost converter uses a boost PWM architecture to produce a positive regulated voltage, refer to the below figuresto see the block diagram.



3.5 Suggested Application Circuit

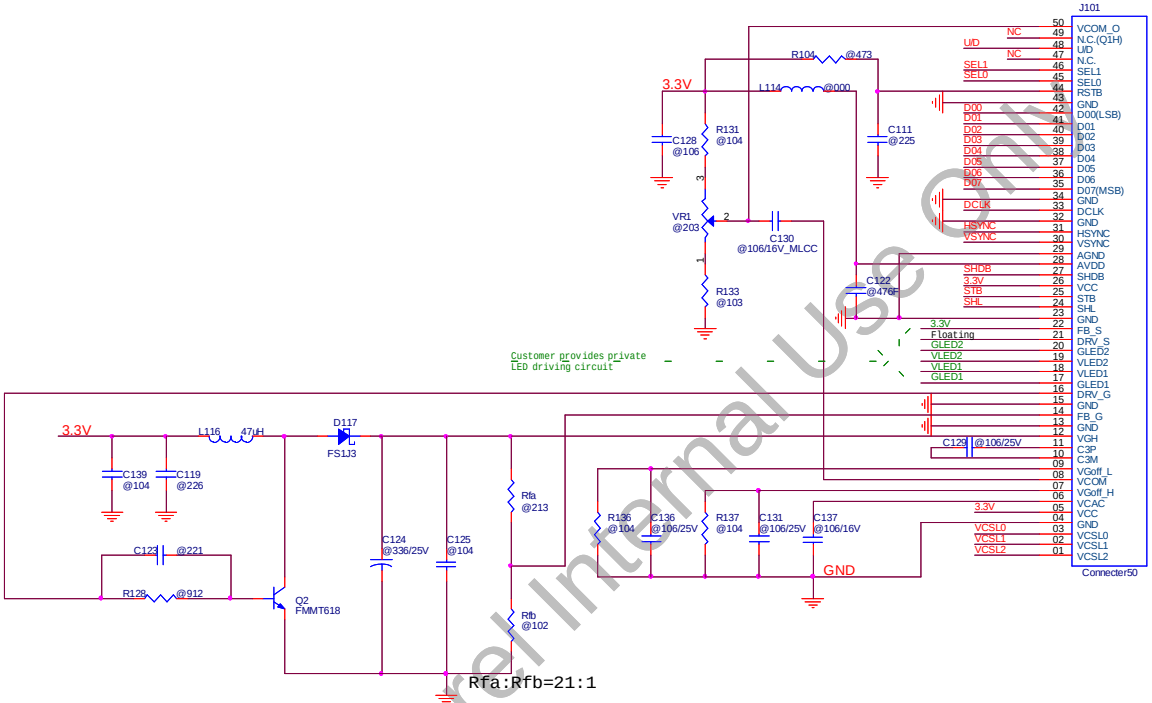
3.5.1 Typical Application Circuit

This application circuit uses internal VGH, LED backlight DC/DC converting function of drive IC. VGoff_L & VGoff_H are generated from VGH through driver.



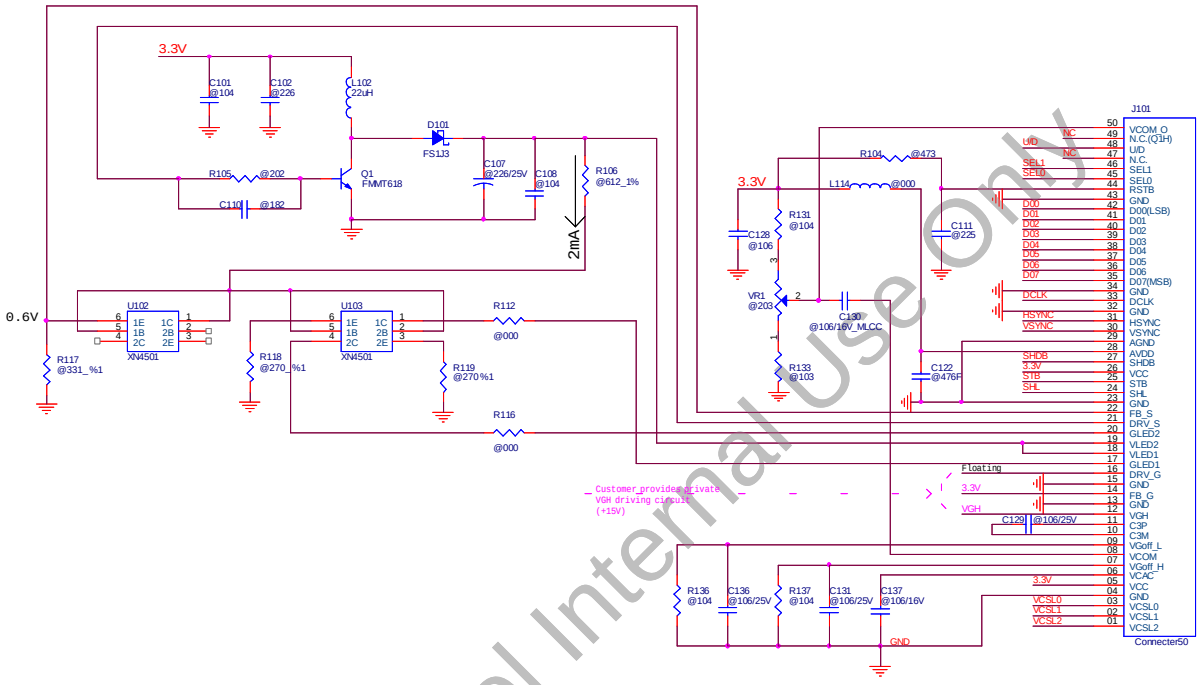
3.5.2 Application Circuit for Using External LED Driving

This application circuit uses only internal VGH DC/DC converting function of drive IC. Customer provides private LED backlight driving circuit. VGoff_L & VGoff_H are generated from VGH through driver.



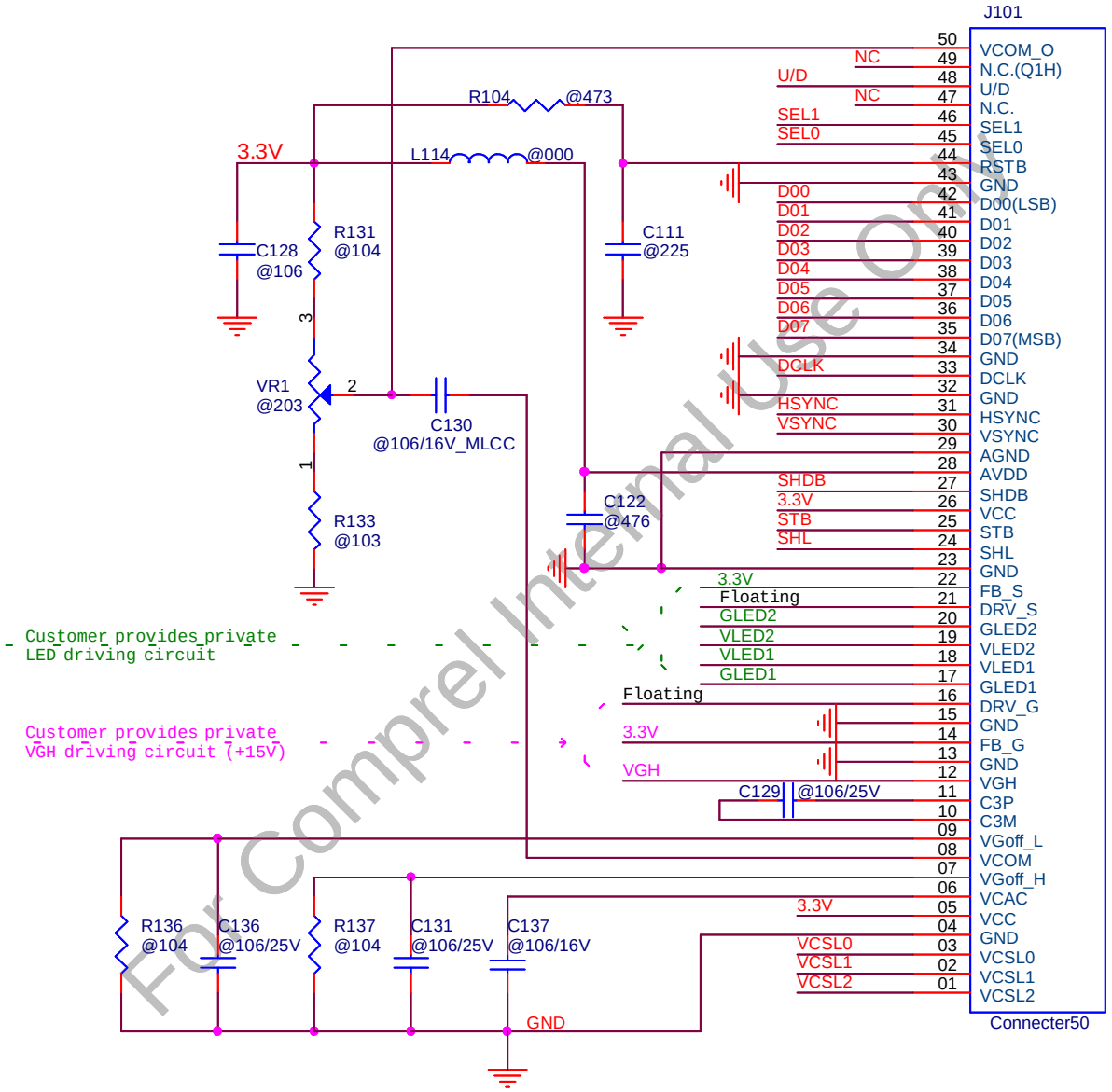
3.5.3 Application Circuit for Using External VGH Driving

This application circuit uses only internal LED backlight DC/DC converting function of drive IC. Customer provides private VGH driving circuit. VGoff_L & VGoff_H are generated from VGH through driver.



3.5.4 Application Circuit for Using External VGH & LED Backlight Driving

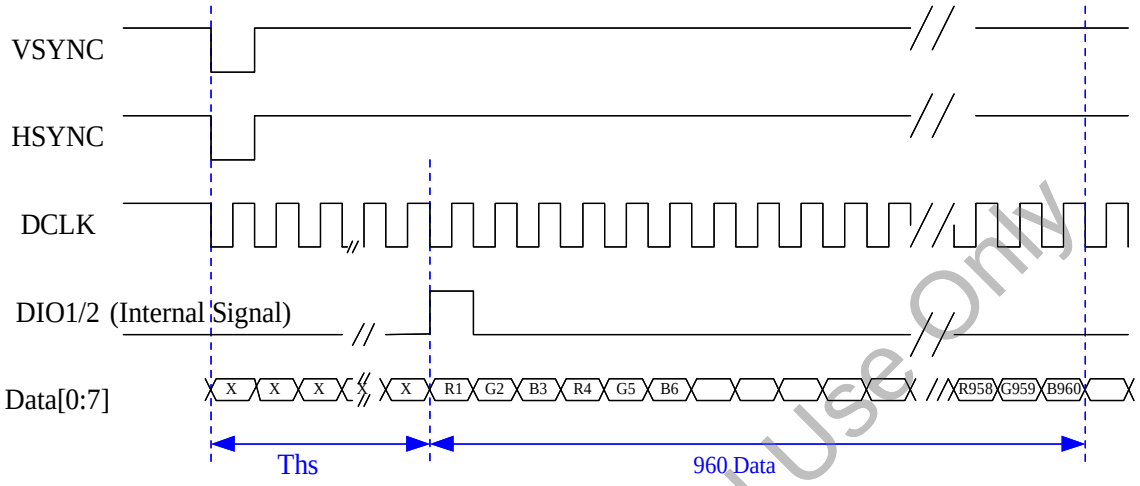
This application circuit uses external LED backlight & VGH driving circuit. VGoff_L & VGoff_H are generated from VGH through driver.



3.6 AC Timing

3.6.1 Timing Diagram

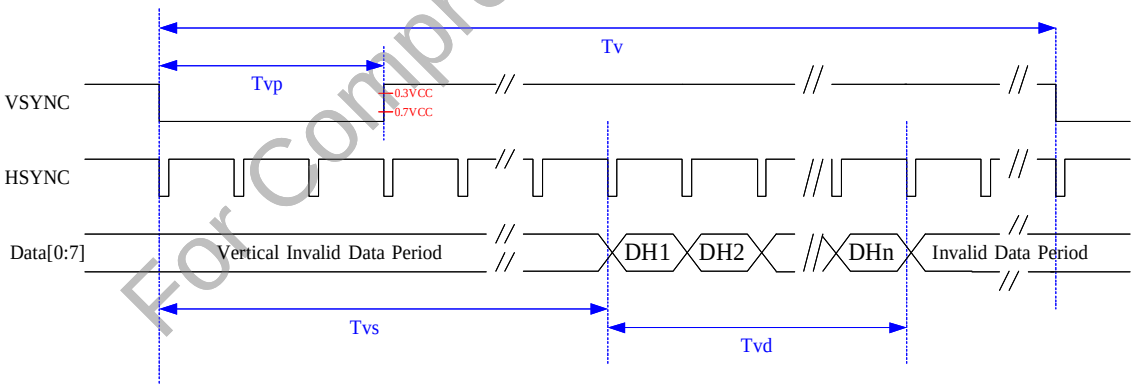
3.6.1.1 Relationship of HSYNC, VSYNC, DCLK, and Data



Note 1: DIO1/2 is “internal start pulse” to latch data.

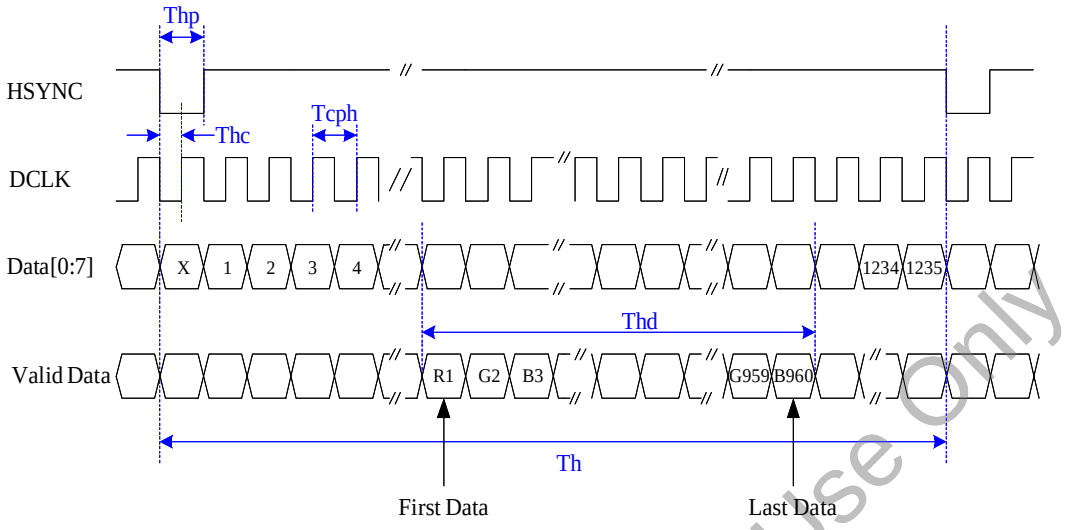
Note 2: “Ths” is the blanking area of HSYNC. The first data is at 195th CLK.

3.6.1.2 Vertical Timing of Input

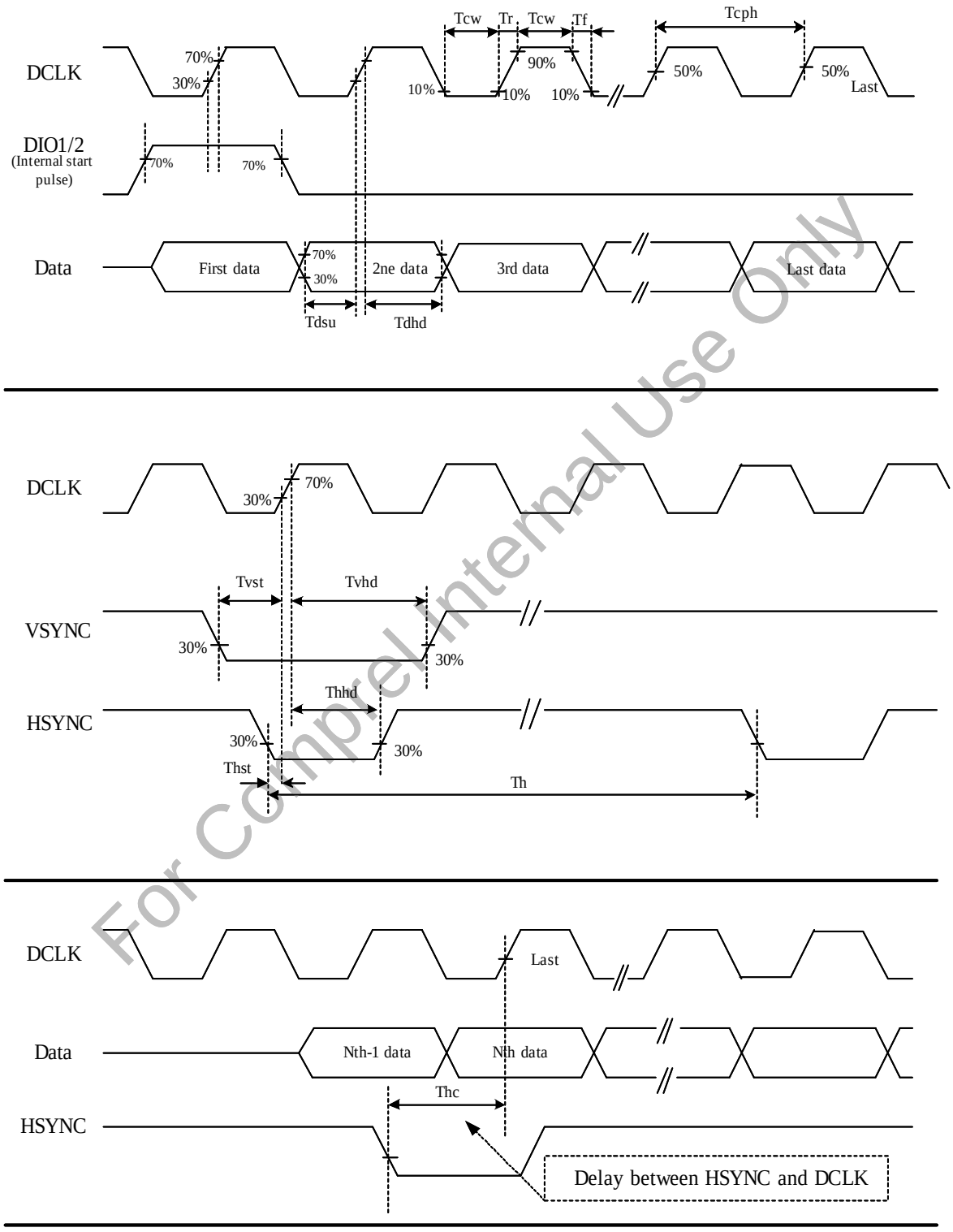


Note : “Tvs” is the blanking area of VSYNC. The fist line is at 14th that will be display on panel.

3.6.1.3 Horizontal Timing of Input



3.6.1.4 Detail Driving Timing



3.6.2 Timing condition

Parameter		Symbol	Min.	Typ.	Max.	Unit.	Remark
DCLK	Frequency	Fclk	-	19.4	25	MHz	
	Period	Tcph	-	51.5	40	ns	
	Pulse Duty	Tcw	40	50	60	%	
	Rising Edge	T_r	-	-	10	ns	Note 1
	Falling Edge	T_f	-	-	10	ns	Note 1
HSYNC	Period	Th	60	63.56	67	us	
			-	1233	-	DCLK	
	Display Period	Thd	-	49.4	-	us	
	Pulse Width	Thp	5	91	-	DCLK	
	HSYNC-DCLK Timing	Thc	-	-	1	DCLK	
HSYNC Setup Time		Thst	12	-	-	ns	
HSYNC Hold Time		Thhd	12	-	-	ns	
Delay from HSYNC to 1st data		Ths	---	194	---	DCLK	Note 2
Horizontal Lines Per Field		t_V	256	262	268	Th	NTSC
VSYNC	Period	Tv	-	16.6	-	ms	
			-	262	-	Th	
	Display Period	Tvd	-	14.83	-	ms	
	Pulse Width	Tvp	1	-	-	DCLK	
			-	3	-	Th	
Vsync Setup Time		Tvst	12	-	-	ns	
Vsync Hold Time		Tvhd	12	-	-	ns	
Delay from VSYNC to 1st line		Tvs	-	13	-	Th	Note 2
DATA D00~D07	Setup Time	Tdsu	12	-	-	ns	
	Hold Time	Tdhd	12	-	-	ns	

Note 1: DCLK Tr and Tf is defined at 10%~90% from square wave or sine wave. Refer to 3.6.1.4.

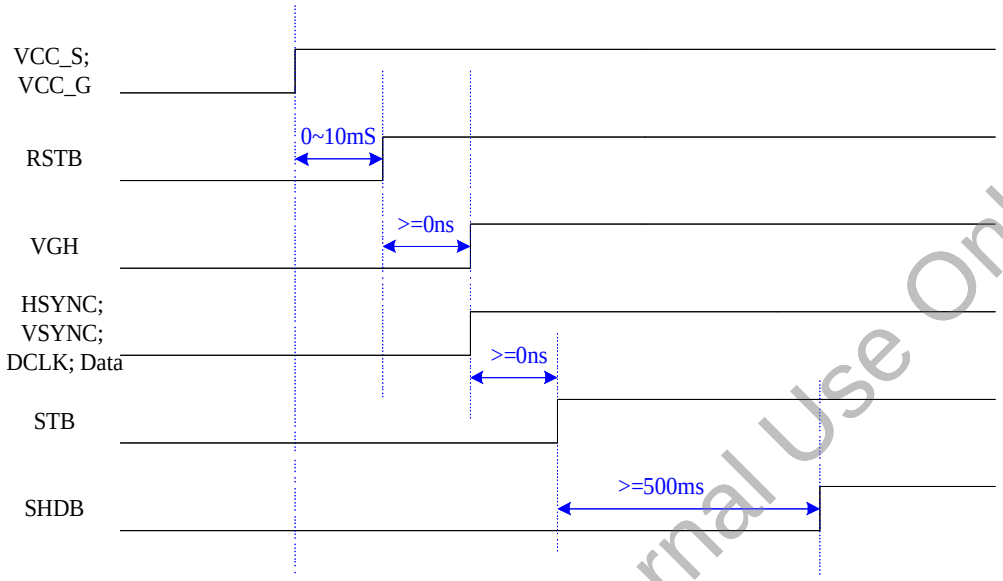
Note 2: Ths and Tvs is invalid data period, and customer should latch data at Ths = 195 DCLK, and Tvs = 14 Th.

Note 3: Above every operation range is based on stable operation from suggested application circuit 3.5.1.

3.7 Power-on Sequence

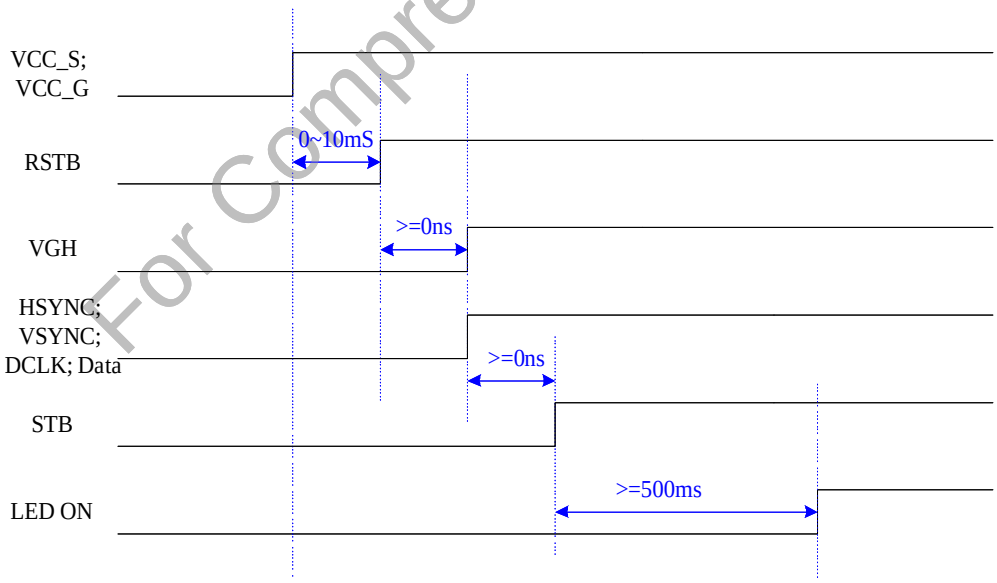
3.7.1 For Using Internal VGH and LED Backlight DC/DC Converter

* Power on Sequence for Using Internal VGH & LED Backlight DC/DC Converter



3.7.2 For Using External VGH and LED Bcaklight DC/DC Converter

* Power on Sequence for Using External VGH & LED Backlight DC/DC Converter



4. Optical specification

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response Time							
Rise	Tr	θ =0°	-	15	30	ms	Note 4
Fall	Tf		-	25	50	ms	
Contrast ratio	CR	At optimized viewing	100	150	-		Note 6, 7
Viewing Angle							
Top			10		-		
Bottom		CR≧10	30		-	deg.	Note 8
Left			40	45			
Right			40	45			
Brightness	Y_L	θ =0°	200	250	-	cd/m^2	Note 9
White Chromaticity	X	θ =0°	0.26	0.31	0.36		
	y	θ =0°	0.28	0.33	0.38		

Note 1: Measurement is in the dark room, optical ambient temperature =25℃, and backlight current IL=20 mA

Note 2: To be measured in the dark room.

Note 3:To be measured on the center area of panel with a field angle of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4: Definition of response time:
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

Note 5. From liquid crystal characteristics, response time will become slower and the color of panel will become darker when ambient temperature is below 25℃.

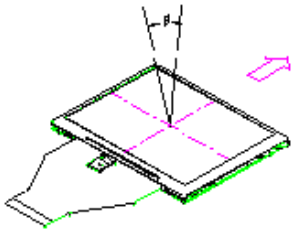
Note 6. Definition of contrast ratio:
Contrast ratio is calculated with the following formula.

$$\text{Contrastratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 7. White $Vi=V_{i50} \mp 1.5V$
Black $Vi=V_{i50} \pm 2.0V$

"±" means that the analog input signal swings in phase with COM signal.
"∓" means that the analog input signal swings out of phase with COM signal.
V_{i50} : The analog input voltage when transmission is 50%
The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 8. Definition of viewing angle: refer to figure as below.



Note 9. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.

5. Absolute Ratings of Ambient Environment

No.	Test items	Conditions	Remark
1	High Temperature Storage	Ta= 80℃ 240Hrs	
2	Low Temperature Storage	Ta= -25℃ 240Hrs	
3	High Ttemperature Operation	Ta= 60℃ 240Hrs	
4	Low Temperature Operation	Ta= 0℃ 240Hrs	
5	High Temperature & High	Ta= 60℃. 90% RH 240Hrs	Operation
6	Heat Shock	-25℃~80℃, 50 cycle, 2Hrs/cycle	Non-operation
7	Electrostatic Discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	Non-operation JIS C7021, A-10 condition A
9	Mechanical Shock	100G . 6ms, ±X,±Y,±Z 3 times for each direction	Non-operation JIS C7021, A-7
10	Vibration (With Carton)	Random vibration: 0.015G^2/Hz from 5~200Hz	IEC 68-34
11	Drop (With Carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	

Note: Ta: Ambient Temperature.

6. Packing Form