



# Specification

**A040CN01 V3**

**Version April 2006**

## Record of Revision

Version	Revise Date	Page	Content
0	12/Dec/2004	-	First draft ( Outline and Packing not define )
1	04/19/2005	5,6.7	Electrical characteristics compatible to A040CN01
2	06/15/2005	12	TFT-LCD module color coordinates
3	07/12/2005	11	Packing form add up PULL SEAL drawing



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## A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	480(W)×234(H)	
2	Active area (mm)	82.11(W)×61.77(H)	
3	Screen size (inch)	4.05(Diagonal)	
4	Dot pitch (mm)	0.171(W)×0.264(H)	
5	Color configuration	R. G. B. delta	
6	Overall dimension (mm)	95.35(W)×77.0(H)×3.5(D)	Note 1
7	Weight (g)	50±5	

Note 1: Refer to Fig. 1.



## B. Electrical specifications

### 1.Pin assignment

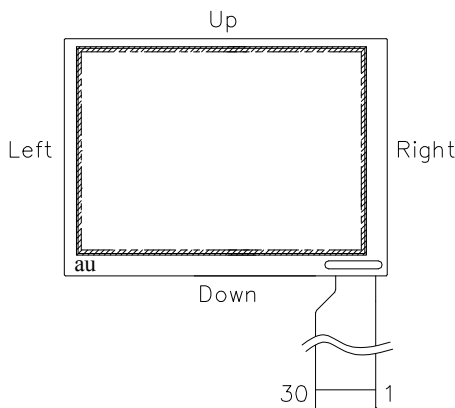
Pin No.	Symbol	I/O	Description	Remark
01	GND		Ground for logic circuit	
02	VCC		Supply voltage of logic control circuit for scan driver	
03	VGL	I	Negative power for scan driver	
04	VGH	I	Positive power for scan driver	
05	STVR	I/O	Vertical start pulse	
06	STVL	I/O	Vertical start pulse	
07	CKV	I	Shift clock input for scan driver	
08	U/D	I	Up/Down scan control input	
09	OEV	I	Output enable input for scan driver	
10	VCOM	I	Common electrode driving signal	
11	VCOM	I	Common electrode driving signal	
12	GLED1		LED module 1 Cathode	
13	VLED1		LED module 1 Anode	
14	VLED2		LED module 2 Anode	
15	GLED2		LED module 2 Cathode	
16	L/R	I	Left/Right scan control input	
17	Q1H	I	Analog signal rotate input	
18	OEH	I	Output enable input for data driver	
19	STHL	I/O	Start pulse for horizontal scan line	
20	STHR	I/O	Start pulse for horizontal scan line	
21	CPH3	I	Sampling and shifting clock pulse for data driver	
22	CPH2	I	Sampling and shifting clock pulse for data driver	
23	CPH1	I	Sampling and shifting clock pulse for data driver	
24	DVDD		Supply voltage of logic control for data driver	
25	DVSS		Ground for logic circuit	
26	VA	I	Alternated video signal input (Red)	
27	VB	I	Alternated video signal input (Green)	
28	VC	I	Alternated video signal input (Blue)	
29	AVDD		Supply voltage for analog circuit	
30	AVSS		Ground for analog circuit	

Note 1 : Selection of scanning mode

Setting of scan control input		IN/OUT state For start pulse				Scanning direction
U/D	L/R	STVR	STVL	STHR	STHL	
GND	V <sub>CC</sub>	OUT	IN	OUT	IN	From up to down, and from left to right.
V <sub>CC</sub>	GND	IN	OUT	IN	OUT	From down to up, and from right to left.
GND	GND	OUT	IN	IN	OUT	From up to down, and from right to left.
V <sub>CC</sub>	V <sub>CC</sub>	IN	OUT	OUT	IN	From down to up, and from left to right.

IN: Input; OUT: Output.

Note 2 : Definition of scanning direction. Refer to figure as below:



## 2. Absolute maximum ratings

Item	Symbol	Condition	Min.	Max.	Unit	Remark
Power voltage	V <sub>CC</sub>	GND=0	-0.3	7	V	
	AV <sub>DD</sub>	AV <sub>SS</sub> =0	-0.3	7	V	
	V <sub>GH</sub>	GND=0	-0.3	18	V	
	V <sub>GL</sub>		-15	0.3	V	
	V <sub>GH</sub> -V <sub>GL</sub>		-	33	V	
Input signal voltage	V <sub>i</sub>		-0.3	AV <sub>DD</sub> +0.3	V	Note 1
	V <sub>i</sub>		-0.3	V <sub>CC</sub> +0.3	V	Note 2
	V <sub>COM</sub>		-2.9	5.2	V	
Operating temperature	Topa		0	60	°C	Ambient temperature
Storage temperature	Tstg		-25	80	°C	Ambient temperature

Note 1: VR, VG, VB

Note 2: STHL, STHR, Q1H, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.



### 3. Electrical characteristics

#### a. Typical operating conditions (GND=AVss=0V, Note 5)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power supply	$V_{CC}$	4.8	5	5.2	V	
	$AV_{DD}$	4.8	5	5.2	V	
	$V_{GH}$	14.3	15	15.7	V	
	$V_{GLAC}$	3.5	5	7.5	Vp-p	AC component of $V_{GL}$ . Note 1
	$V_{GL\_H}$	-10.5	-10	-9.5	V	High level of $V_{GL}$ .
Video signal Amplitude (VR, VG, VB)	$V_{iA}$	$AV_{SS}+0.4$	-	$AV_{DD}-0.8$	V	Note 2
	$V_{iAC}$	-	3	-	V	AC component
	$V_{iDC}$	-	$AV_{DD}/2$	-	V	DC component
VCOM	$V_{CAC}$	3.5	5	7.5	Vp-p	AC component, Note 3
	$V_{CDC}$	-	1.3	-	V	DC component
Input Signal voltage	H Level	$V_{IH}$	4	-	$V_{CC}$	Note 4
	L Level	$V_{IL}$	0	-	1	

Note 1: The same phase and amplitude with common electrode driving signal (VCOM).

Note 2: Refer to Fig.4- (a)

Note 3: The brightness of LCD panel could be adjusted by the adjustment of the AC component of VCOM.

Note 4: STHL, STHR, Q1H, OEH, L/R, CPH1~CPH3, STVR, STVL, OEV, CKV, U/D.

Note 5: Be sure to apply GND,  $V_{CC}$ ,  $V_{GL}$  to the LCD first, and then apply  $V_{GH}$ .

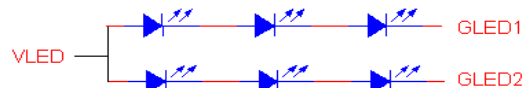
#### b. Current consumption (GND=AVss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Current for driver	$I_{GH}$	$V_{GH}=15V$	-	80	150	$\mu A$	
	$I_{GL}$	$V_{GL\_H}=-10V$	-	-0.2	-0.4	mA	
	$I_{CC}$	$V_{CC}=5V$	-	2.0	4.0	mA	
	$I_{DD}$	$AV_{DD}=5V$	-	5	10	mA	

#### c. LED driving conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	$I_L$		20		mA	
LED voltage	$V_L$		9.9	12	V	Note 1
LED Life Time	$L_L$	(10000)			Hr	Note 2,3

Note 1 : LED backlight is two parallel types and three LEDs serial type as figure.







Note 2 : Ta. = 25°C, I<sub>L</sub> = 20mA / per LED

Note 3 : Brightness to be decreased to 50% of the initial value.

#### 4. AC Timing

##### a. Timing conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Remark
Rising time	t <sub>r</sub>	-	-	10	ns	Note 1
Falling time	t <sub>f</sub>	-	-	10	ns	Note 1
High and low level pulse width	t <sub>CPH</sub>	299	308	319	ns	CPH1~CPH3
CPH pulse duty	t <sub>CWH</sub>	40	50	60	%	CPH1~CPH3
CPH pulse delay	t <sub>C12</sub> t <sub>C23</sub> t <sub>C31</sub>	70	t <sub>CPH</sub> /3	t <sub>CPH</sub> /2	ns	CPH1~CPH3
STH setup time	t <sub>SUH</sub>	35	-	-	ns	STHR,STHL
STH hold time	t <sub>HDH</sub>	35	-	-	ns	STHR,STHL
STH pulse width	t <sub>STH</sub>	-	1	-	t <sub>CPH</sub>	STHR,STHL
STH period	t <sub>H</sub>	61.5	63.5	65.5	μs	STHR,STHL
OEH pulse width	t <sub>OEH</sub>	-	3	-	t <sub>CPH</sub>	OEH
Sample and hold disable time	t <sub>DIS1</sub>	-	28	-	t <sub>CPH</sub>	
OEV pulse width	t <sub>OEV</sub>	-	12	-	t <sub>CPH</sub>	OEV
CKV pulse width	t <sub>CKV</sub>	16	28	40	t <sub>CPH</sub>	CKV
Clean enable time	t <sub>DIS2</sub>	-	10	-	t <sub>CPH</sub>	
Horizontal display start	t <sub>SH</sub>	-	0	-	t <sub>CPH</sub> /3	
Horizontal display timing range	t <sub>DH</sub>	-	480	-	t <sub>CPH</sub> /3	
STV setup time	t <sub>SUV</sub>	400	-	-	ns	STVL,STVR
STV hold time	t <sub>HDV</sub>	400	-	-	ns	STVL,STVR
STV pulse width	t <sub>STV</sub>	-	-	1	t <sub>H</sub>	STVL,STVR
Horizontal lines per field	t <sub>V</sub>	256	262	268	t <sub>H</sub>	Note 2
Vertical display start	t <sub>SV</sub>	-	3	-	t <sub>H</sub>	
Vertical display timing range	t <sub>DV</sub>	-	234	-	t <sub>H</sub>	
VCOM rising time	t <sub>rCOM</sub>	-	-	3	μs	
VCOM falling time	t <sub>fCOM</sub>	-	-	3	μs	
VCOM delay time	t <sub>DCOM</sub>	-	-	3	μs	
RGB delay time	t <sub>DRGB</sub>	-	-	1	μs	

Note 1: For all of the logic signals.

Note 2: Please don't use odd horizontal lines to drive LCD panel for both odd and even fields simultaneously.

##### b. Timing diagram

Please refer to the attached drawings, from Fig.2 to Fig.6.



### C. Optical specification (Note 1, Note 2, Note 3)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise	$\theta = 0^\circ$	-	15	30	ms	Note 4, 6
	Fall		-	20	40	ms	
Contrast ratio	CR	At optimized viewing angle	100	150	-		Note 5, 6
Viewing angle	Top	$CR \geq 10$	10	-	-	deg.	Note 6, 7
	Bottom		30	-	-		
	Left		40	45	-		
	Right		40	45	-		
Brightness	$Y_L$	$\theta = 0^\circ$	200	250	-	nit	Note 8
White chromaticity shift	X	$\theta = 0^\circ$	0.25	0.3	0.35		
	y		0.3	0.35	0.4		

Note 1: Ambient temperature =25°C.

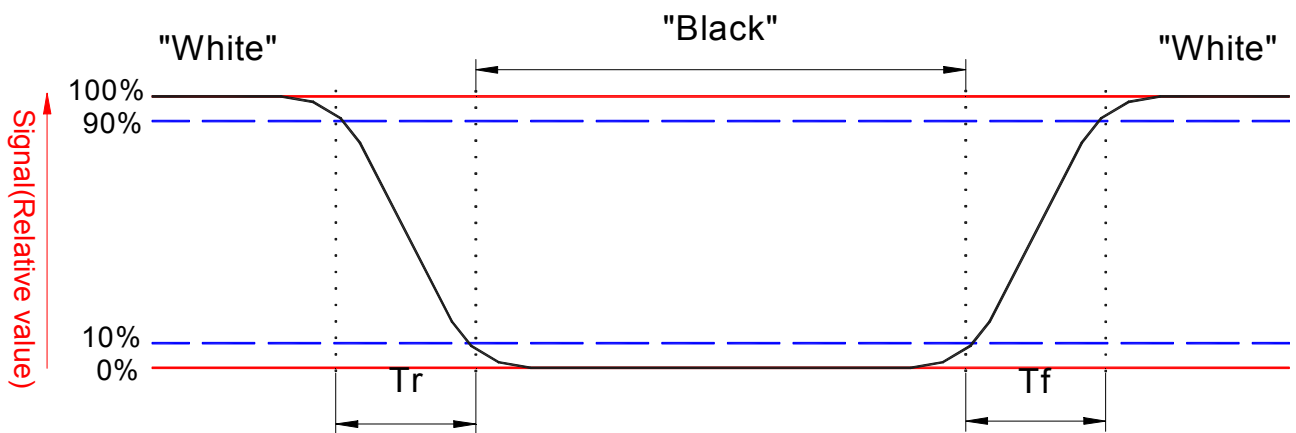
Note 2: To be measured in the dark room.

Note 3: To be measured at the center area of panel with a viewing cone of 1° by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.

The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:

Contrast ratio is calculated with the following formula.



$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at "White" state}}{\text{Photo detector output when LCD is at "Black" state}}$$

Note 6. White  $V_i = V_{i50} \mp 1.5V$

Black  $V_i = V_{i50} \pm 2.0V$

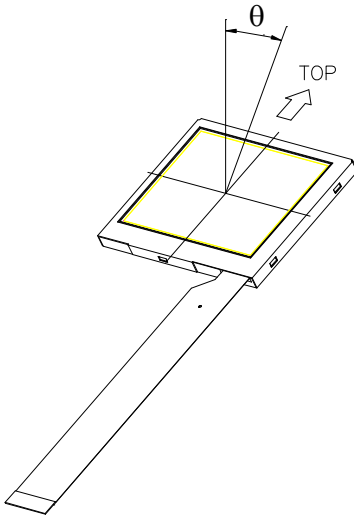
" $\pm$ " means that the analog input signal swings in phase with COM signal.

" $\mp$ " means that the analog input signal swings out of phase with COM signal.

$V_{i50}$  : The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle: Refer to figure as below.



Note 8. Measured at the center area of the panel when all the input terminals of LCD panel are electrically opened.



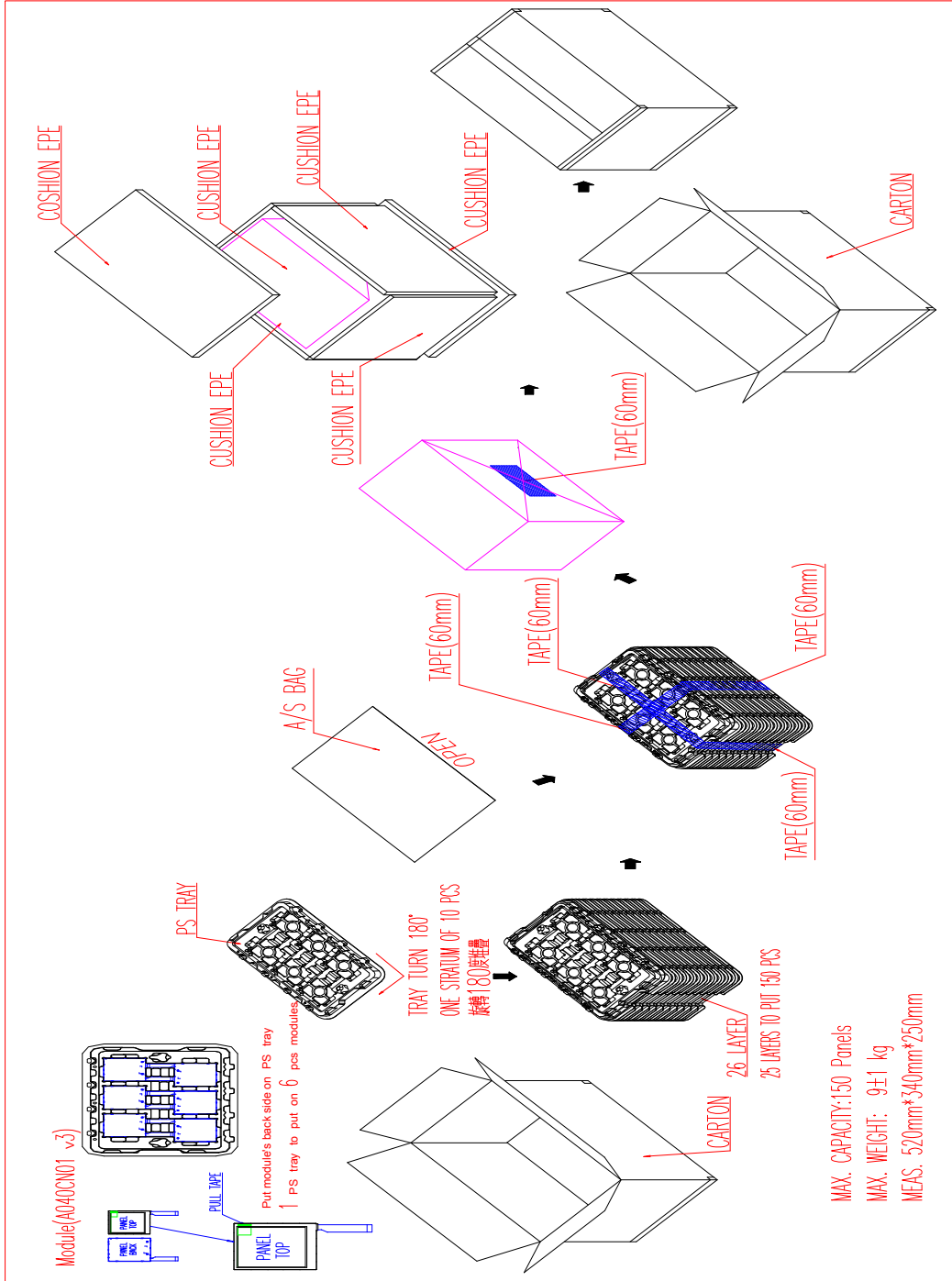
#### D. Reliability test items:

No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 80°C 240Hrs	
2	Low temperature storage	Ta= -25°C 240Hrs	
3	High temperature operation	Ta= 60°C 240Hrs	
4	Low temperature operation	Ta= 0°C 240Hrs	
5	High temperature and high humidity	Ta= 60°C . 95% RH 240Hrs	Operation
6	Heat shock	-25°C~80°C , 50 cycles, 2H/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω) , once for each terminal	Non-operation
8	Vibration	Frequency range : 10~55Hz Stoke : 1.5mm Sweep : 10~55Hz~10Hz 2 hours for each direction of X,Y,Z (6 hours for total)	JIS C7021, A-10 condition A
9	Mechanical shock	100G 6ms, ±X,±Y,±Z 3 times for each direction	JIS C7021, A-7 condition C
10	Vibration (with carton)	Random vibration: 0.015G <sup>2</sup> /Hz from 5~200Hz -6dB/Octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 80cm 1 corner, 3 edges, 6 surfaces	

**Note: Ta: Ambient temperature.**



### E. Packing form





## F. TFT-LCD Module Color Coordinates

- a) A040CN01 V3 adapts Nichia LED for Backlight.
- b) A040CN01 V3 only use LED color rank B5 and only one rank in one panel.
- c) Color Coordinates Measurement allowance is  $\pm 0.01$  .
- d) TFT-LCD Module color rank as list :

Color Coordinates	Spec.			CS Optical Data					
	Min	Typ	max	Min	Max	Average	$\sigma$	AVG-3 $\sigma$	AVG+3 $\sigma$
Wx	<b>0.25</b>	<b>0.3</b>	<b>0.35</b>	0.305	0.314	0.311	0.003	0.303	0.319
Wy	<b>0.3</b>	<b>0.35</b>	<b>0.4</b>	0.334	0.346	0.34	0.004	0.329	0.352
Rx				0.622	0.628	0.624	0.002	0.619	0.629
Ry				0.354	0.359	0.356	0.001	0.353	0.36
Gx				0.319	0.326	0.323	0.002	0.315	0.33
Gy				0.577	0.585	0.581	0.003	0.571	0.591
Bx				0.146	0.149	0.147	0.001	0.145	0.149
By				0.134	0.149	0.142	0.005	0.128	0.157

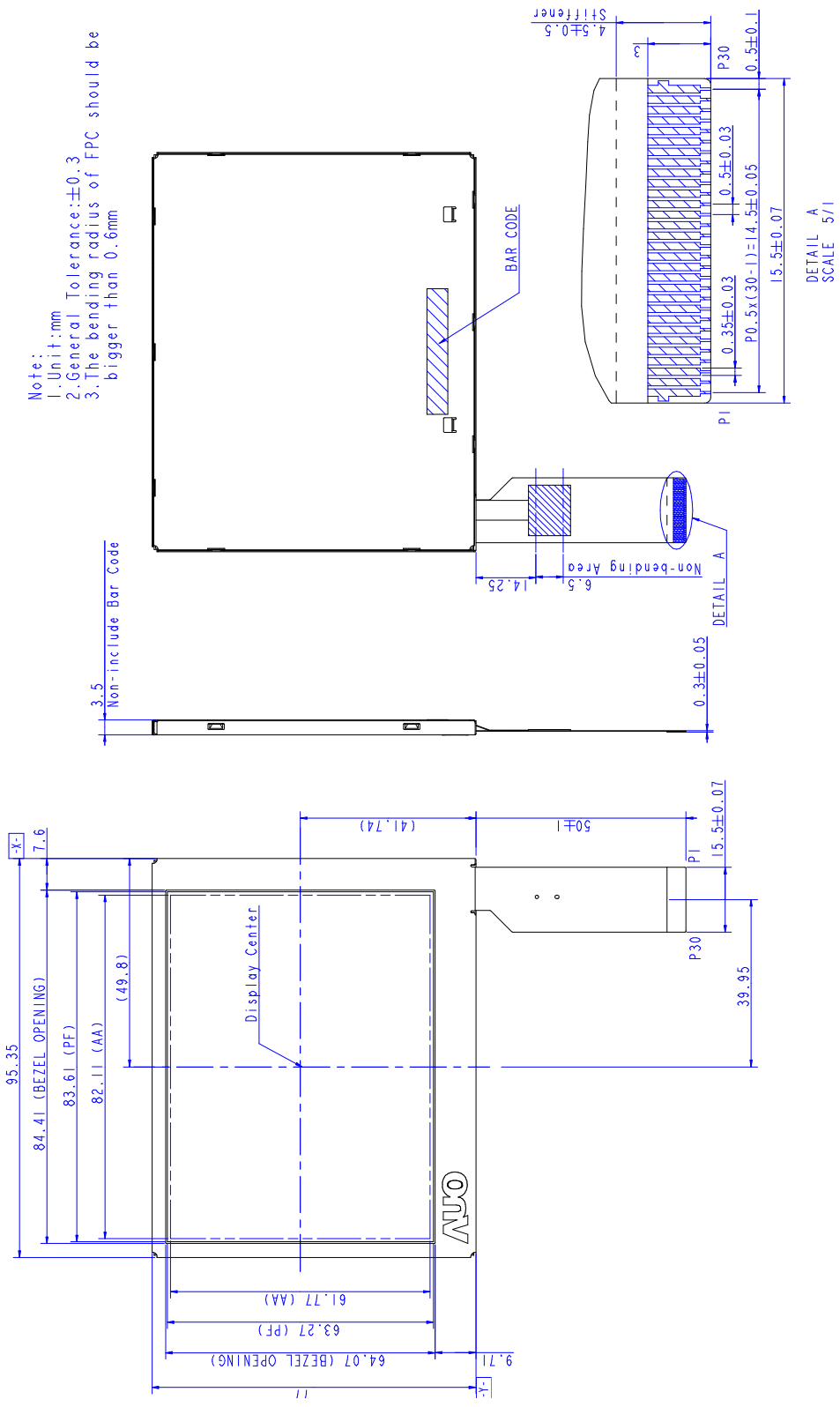


Fig.1 Outline dimension of TFT-LCD module

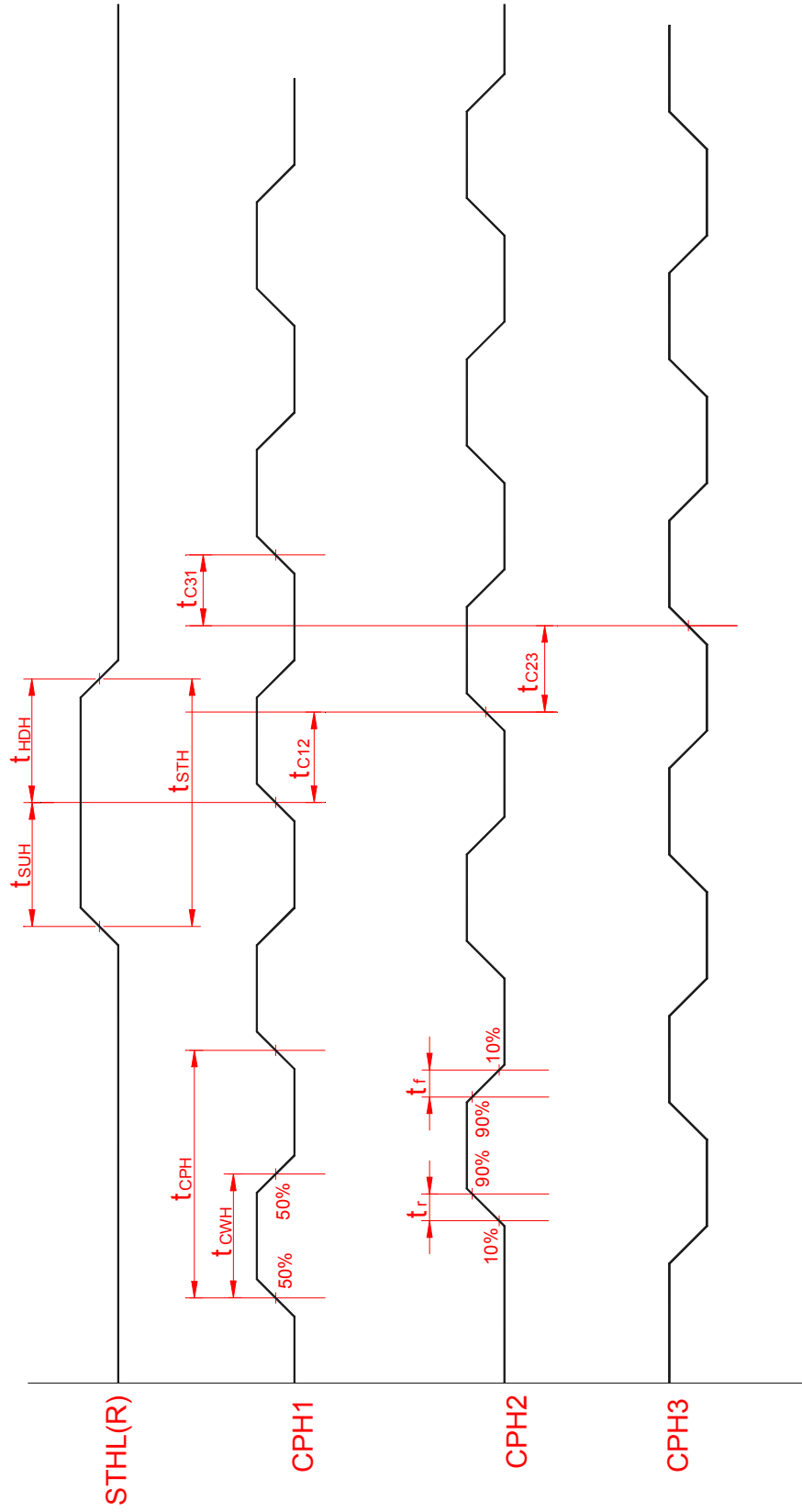
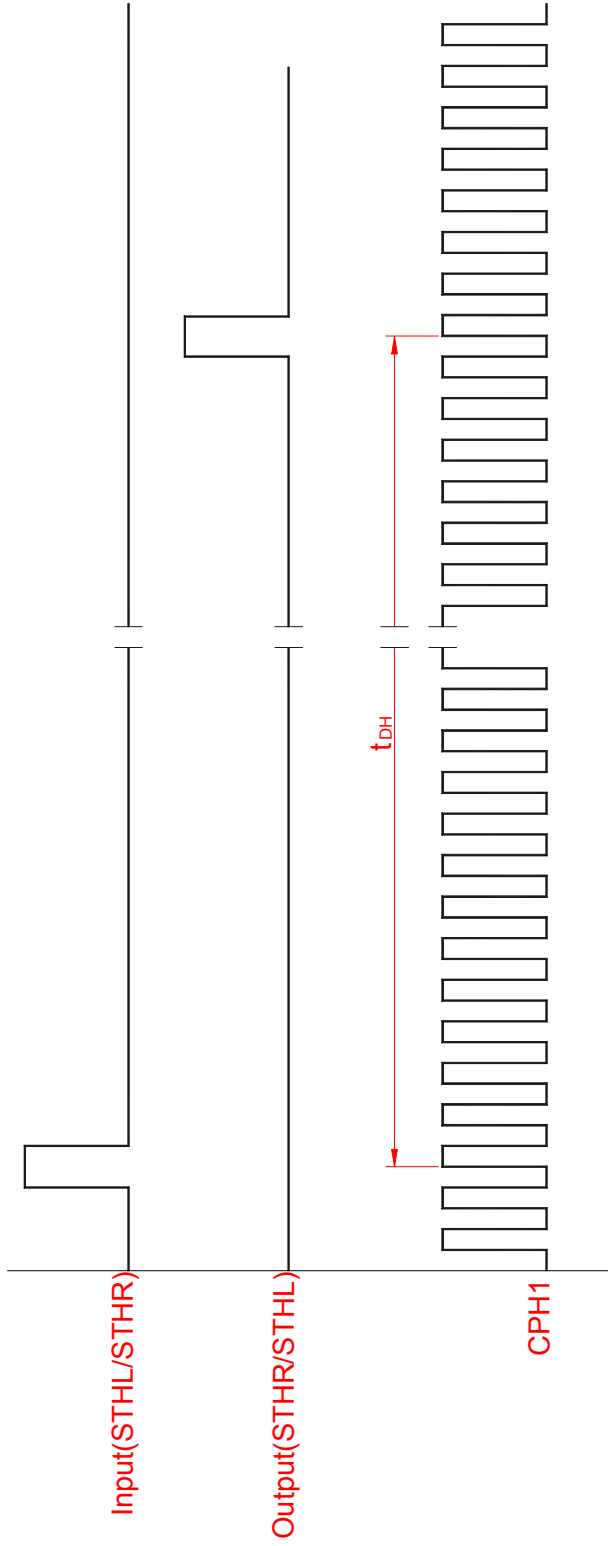


Fig.2 Sampling clock timing





**Fig.3 Horizontal display timing range**

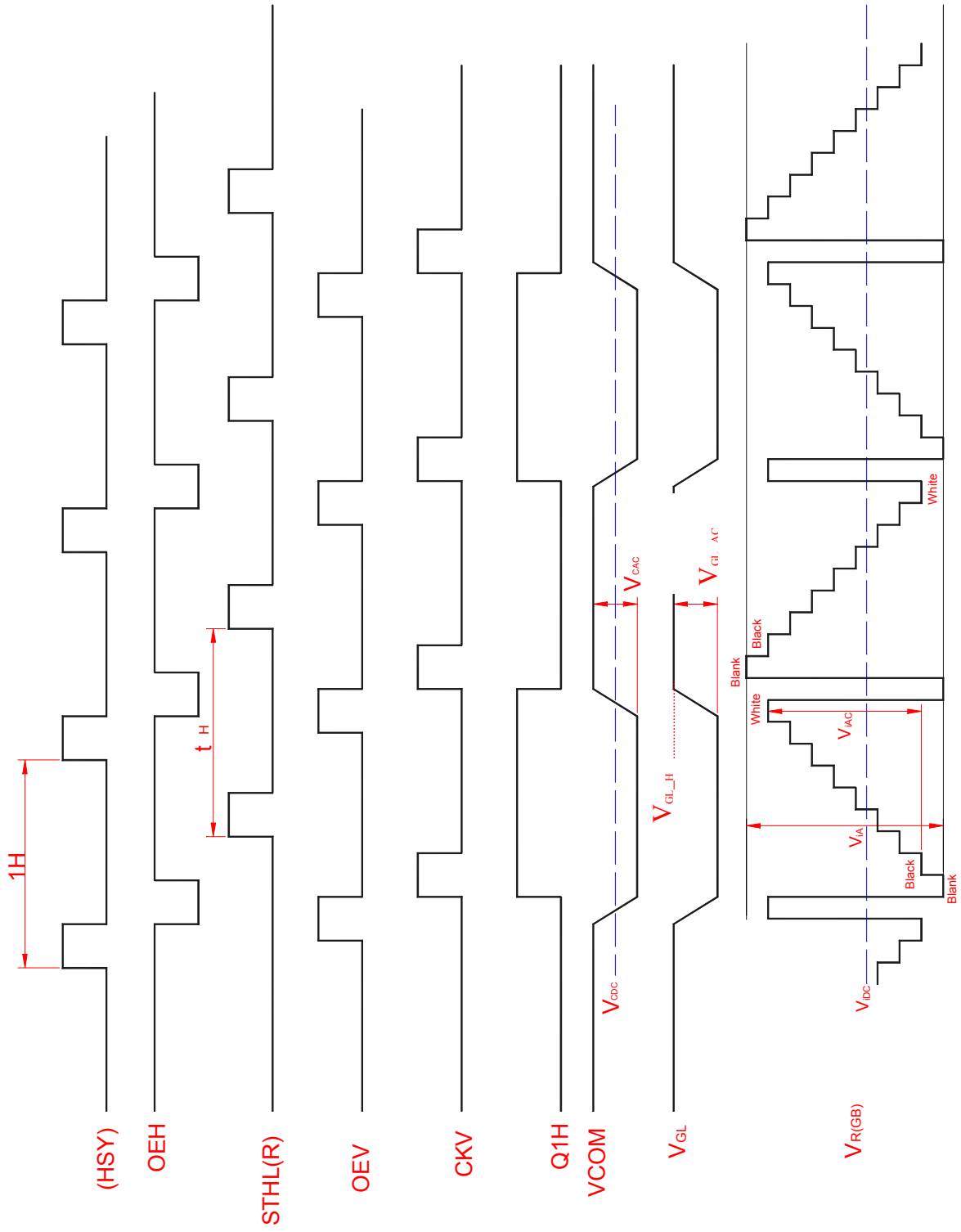
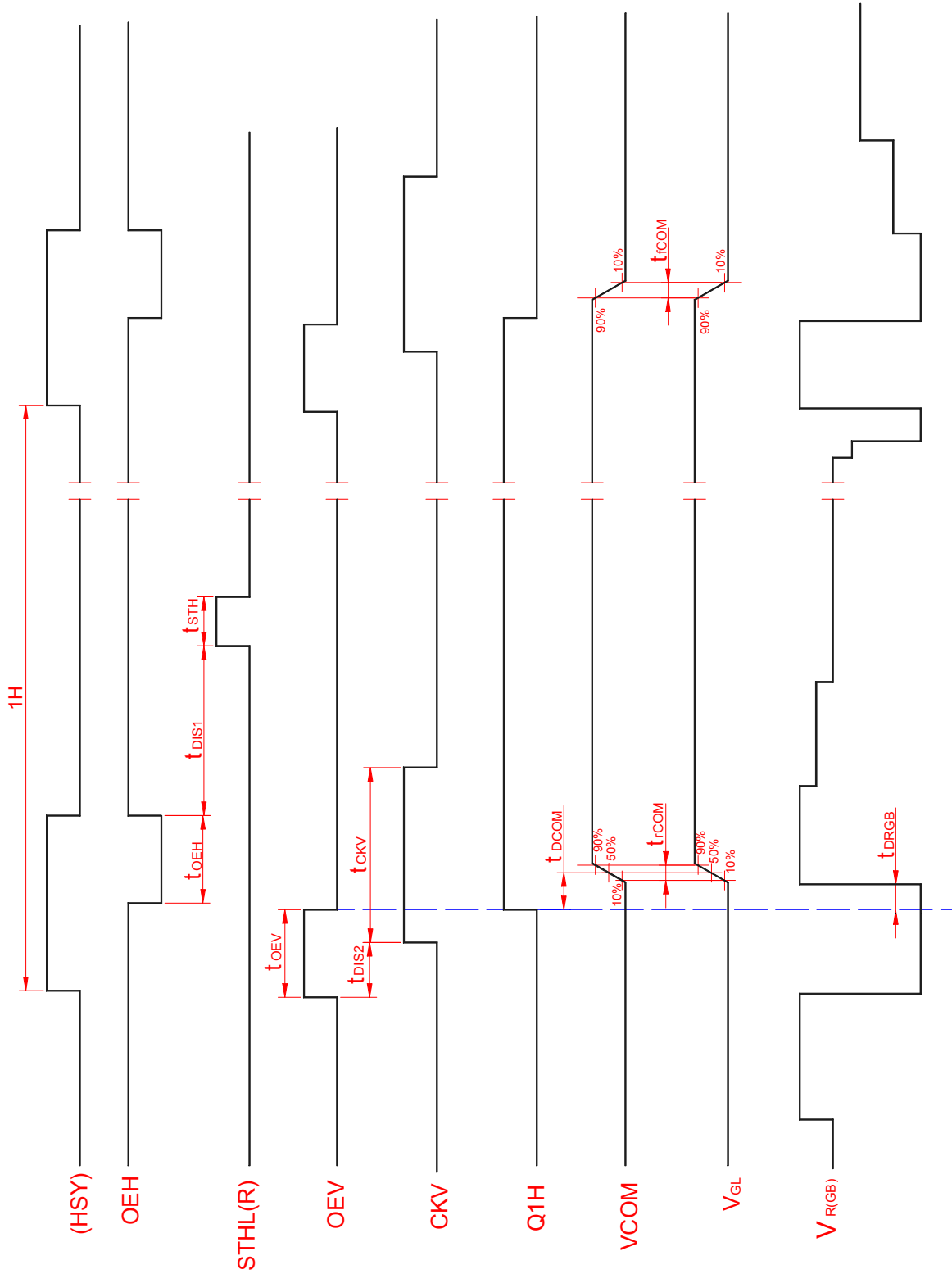


Fig.4(a) Horizontal timing



**Fig.4-(b) Detail horizontal timing**

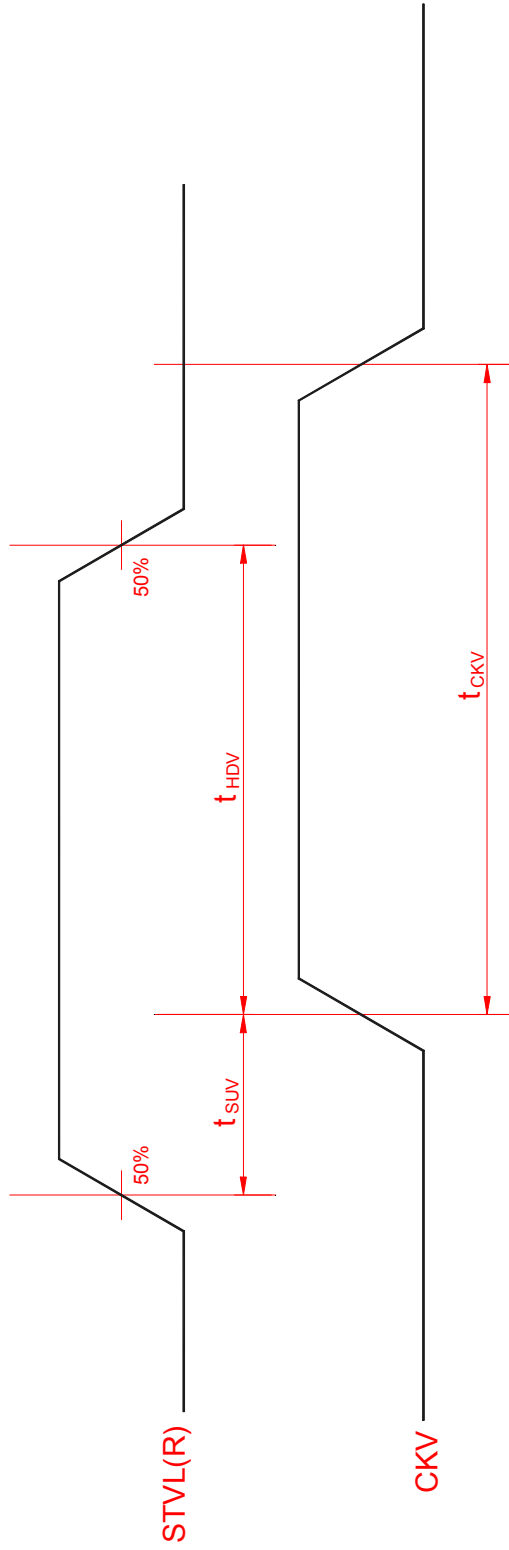


Fig.5 Vertical shift clock timing

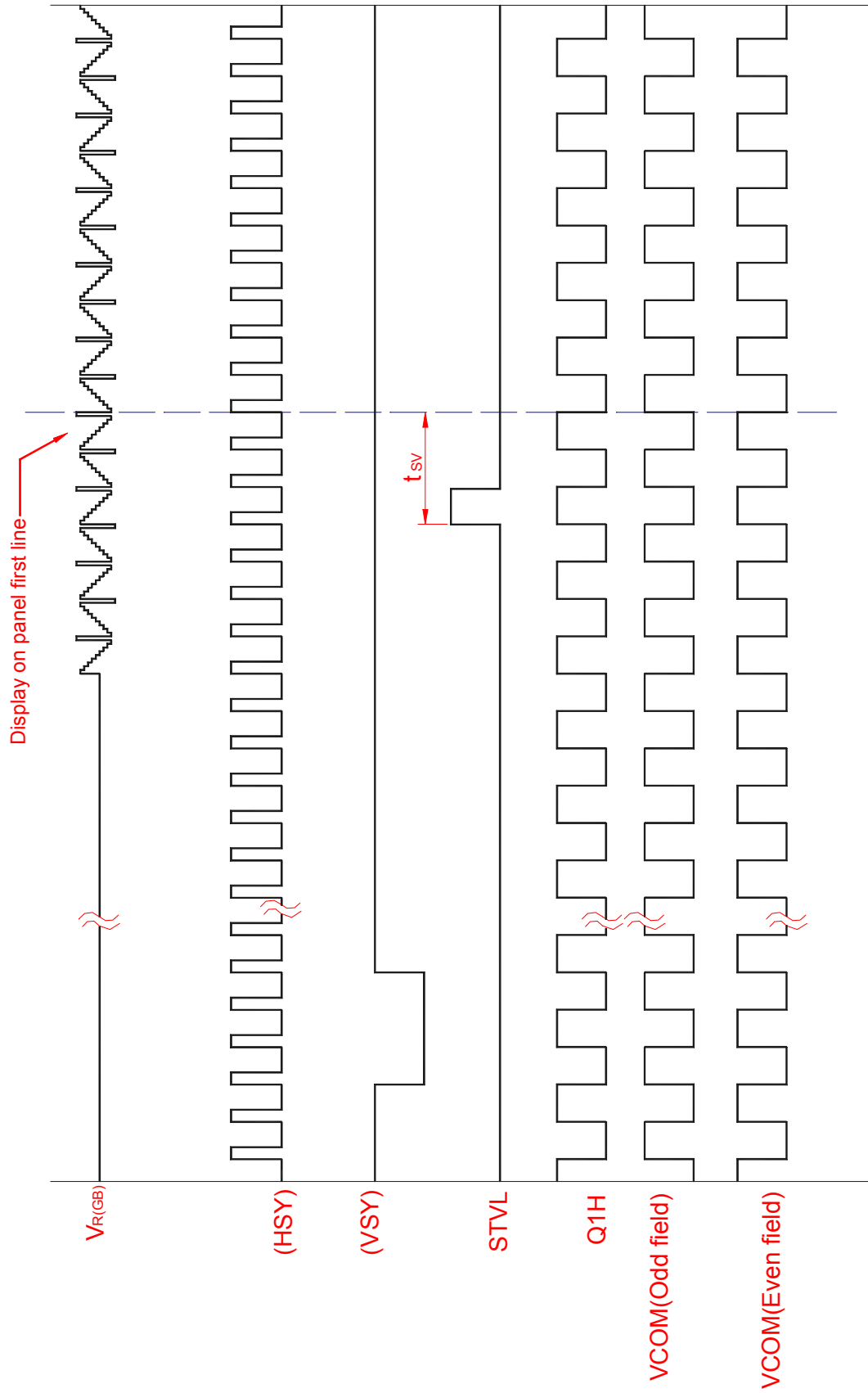


Fig.6-(a) Vertical timing (From up to down)

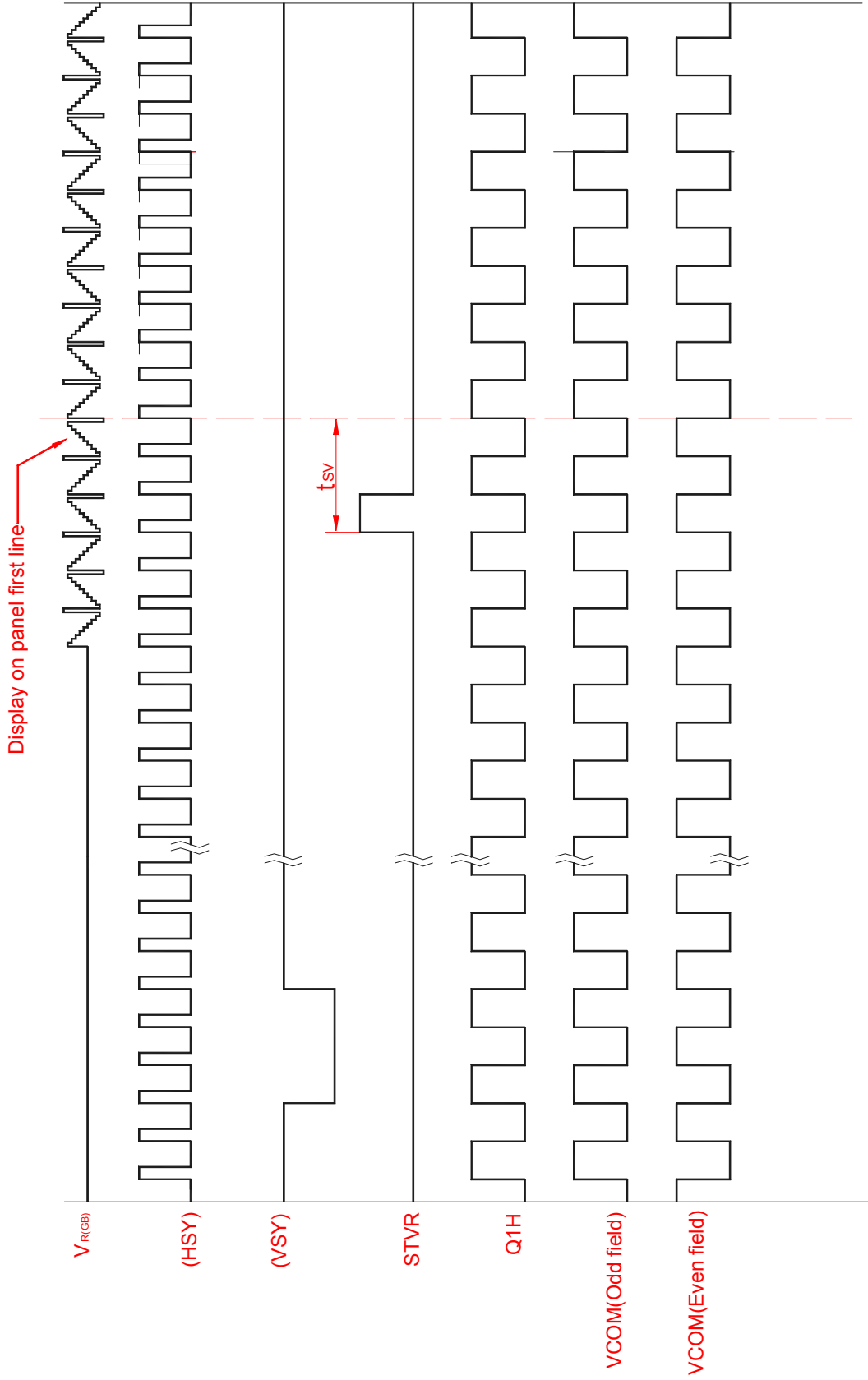


Fig.6-(b) Vertical timing (From down to up)