# CUSTOMER APPROVAL SHEET

| | |
|---|---|
| **Company Name** | |
| **MODEL** | **A060SE02 V9** |
| **CUSTOMER APPROVED** | |

- ☐ **APPROVAL FOR SPECIFICATIONS ONLY (Spec. Ver. 0.2)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND ES SAMPLE (Spec. Ver. 0.2)**
- ☐ **APPROVAL FOR SPECIFICATIONS AND CS SAMPLE (Spec. Ver. 0.2)**
- ☐ **CUSTOMER REMARK :**

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|---|---|
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# Product Specification

## 6" EPD MODULE

## Model Name： A060SE02 V9

| | |
|---|---|
| **Planned Lifetime:** | From 2010/Aug. To 2011/ Aug. |
| **Phase-out Control:** | From 2011/May. To 2011/ Aug. |
| **EOL Schedule:** | 2011/ Aug. |

< ◆ >Preliminary Specification
< >Final Specification



Note: The content of this specification is subject to change.

Record of Revision

| Version | Revise Date | Page | Content |
|---|---|---|---|
| 0.0 | 2010/11/9 | All | First Draft. |
| 0.1 | 2010/11/25 | 10 | Update absolute max rating spec |
| | | 22 | Modify application note. |
| | | 26 | Update application circuit |
| 0.2 | 2011/01/27 | 4 | Update outline dimension, changing label position. |
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# Contents

# A. General Information

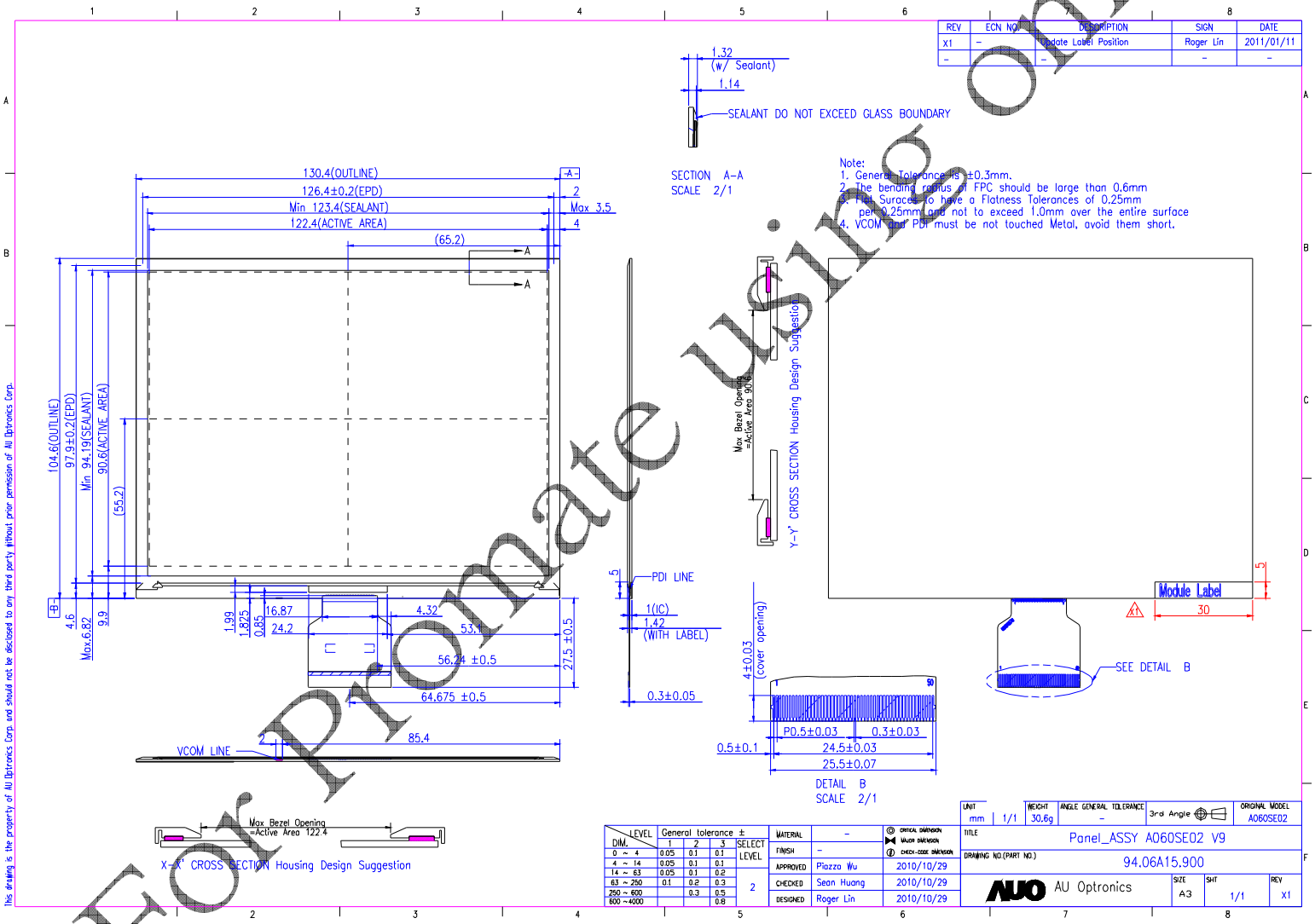
This display is a active matrix electrophoretic display (EPD), which comprises a-si TFT substrace, electrophoretic front plane, protective anti-glare top-sheet, driver ICs, and FPC. It is designed for applications such as e-book or e-reader.

| NO. | Item | Unit | Specification | Remark |
|---|---|---|---|---|
| 1 | Screen Size | inch | 6 (Diagonal) | |
| 2 | Display Resolution | dot | 800 (H)× 600 (V) | |
| 3 | Overall Dimension | mm | 130.4 (H) × 104.6 (V) × 1.32 (T) | Note 1 |
| 4 | Active Area | mm | 122.4 (H)×90.6 (V) | |
| 5 | Dot Pitch | mm | 0.153 (H)x 0.151 (V) | |
| 6 | Gray level | -- | 16 | |
| 7 | Weight | G | (30.6) | |
| 8 | Surface Treatment | | AG (7.5 ± 2%)<br>Hard coating (3H) | Note 2 |

Note 1: Not include FPC. Refer next page to get further information.

Note 2: 750 g load force on UNI/JPIA 3H pencil, speed is 3.5mm/s on the AG film and scratch length is 1cm and write 5 handwriting, Scratch no. ≦2 is OK

# B. Outline Dimension



# C. Electrical Specifications

## 1. Pin Assignment

Recommended connector : FH12-50S-0.5SH.

| Pin No. | Symbol | I/O | I/O Structure | Description | Remark |
|---|---|---|---|---|---|
| 1 | Dummy | -- | -- | Dummy pin | |
| 2 | VCOM | O | -- | VCOM polarity output signal | |
| 3 | VCOM_BOT | I | -- | VCOM signal setting pin | |
| 4 | VCOMDC | P | Type2 | External voltage for VCOMDC power. | |
| 5 | VCOMH | P | -- | External voltage for VCOM high power. | |
| 6 | VCOML | P | -- | External voltage for VCOM low power. | |
| 7 | RST_N | I | Type 3 | Global reset pin. Low reset. | |
| 8 | SHD_N | I | Type 3 | DC-DC converter shut down pin.<br>"0" : Enable.(Panel shut down) **Default**)<br>"1" : Disable. | |
| 9 | PWR_RDY | O | Type 1 | Power ready output.<br>When SHD_N from "1" to "0": PWR_RDY will become "0".<br>When SHD_N from "0" to "1": after 100ms, PWR_RDY will become "1". | Note1 |
| 10 | VCOMIN_0 | I | Type 2 | Logic Input for VCOM voltage generate. | |
| 11 | VCOMIN_1 | I | Type 2 | Logic Input for VCOM voltage generate. | |
| 12 | YOE | I | Type 3 | Vertical output enable pin. | Note2 |
| 13 | YCLK | I | Type 3 | Vertical clock. input | Note2 |
| 14 | UD | I | Type 3 | Vertical (up/down) scan direction.<br>U/D = "L": Shift up to down. **Default**<br>U/D = "H": Shift down to up. | |

<table>
<tr><td>15</td><td>YDIOD</td><td>I/O</td><td>Type 5</td><td rowspan="2">Vertical start pulse input/output.<br>These pins are used to input and output shift data. These pins are switched as input or output by setting the UD pin as follow.<br><table><tr><th>UD</th><th>YDIOU</th><th>YDIOD</th></tr><tr><td>L</td><td>Output</td><td>Input</td></tr><tr><td>H</td><td>Input</td><td>Output</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>16</td><td>YDIOU</td><td>I/O</td><td>Type 5</td></tr>
<tr><td>17</td><td>XDIOL</td><td>I/O</td><td>Type 5</td><td rowspan="2">Horizontal start pulse input/output.<br>These pins are used to input and output shift data. These pins are switched as input or output by setting the SHL pin as follow.<br><table><tr><th>SHL</th><th>XDIOL</th><th>XDIOR</th></tr><tr><td>L</td><td>Input</td><td>Output</td></tr><tr><td>H</td><td>Output</td><td>Input</td></tr></table></td><td rowspan="2"></td></tr>
<tr><td>18</td><td>XDIOR</td><td>I/O</td><td>Type 5</td></tr>
<tr><td>19</td><td>LD</td><td>I</td><td>Type 3</td><td>Latch data.</td><td></td></tr>
<tr><td>20</td><td>D0</td><td>I</td><td>Type 3</td><td>Data input, First pixel LSB</td><td></td></tr>
<tr><td>21</td><td>D1</td><td>I</td><td>Type 3</td><td>Data input, First pixel MSB</td><td></td></tr>
<tr><td>22</td><td>D2</td><td>I</td><td>Type 3</td><td>Data input, Second pixel LSB</td><td></td></tr>
<tr><td>23</td><td>D3</td><td>I</td><td>Type 3</td><td>Data input, Second pixel MSB</td><td></td></tr>
<tr><td>24</td><td>D4</td><td>I</td><td>Type 3</td><td>Data input, Third pixel LSB</td><td></td></tr>
<tr><td>25</td><td>D5</td><td>I</td><td>Type 3</td><td>Data input, Third pixel MSB</td><td></td></tr>
<tr><td>26</td><td>D6</td><td>I</td><td>Type 3</td><td>Data input, Forth pixel LSB</td><td></td></tr>
<tr><td>27</td><td>D7</td><td>I</td><td>Type 3</td><td>Data input, Forth pixel MSB</td><td></td></tr>
<tr><td>28</td><td>SHL</td><td>I</td><td>Type 3</td><td>Horizontal (left/right) scan direction.<br>SHL = “L”: Shift right to left.<br>SHL = “H”:Shift left to right. Default</td><td></td></tr>
<tr><td>29</td><td>XCLK</td><td>I</td><td>Type 3</td><td>Horizontal Clock input..</td><td>Note3</td></tr>
<tr><td>30</td><td>VREF</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>31</td><td>VR</td><td>P</td><td>--</td><td>VCOMDC reference voltage</td><td></td></tr>
<tr><td>32</td><td>AVDD</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>33</td><td>C1P</td><td>C</td><td>--</td><td>For charge pump capactor connected pin.</td><td></td></tr>
<tr><td>34</td><td>C1N</td><td>C</td><td>--</td><td>For charge pump capactor connected pin.</td><td></td></tr>
<tr><td>35</td><td>VSS</td><td>P</td><td>--</td><td>Digital ground</td><td></td></tr>
<tr><td>36</td><td>VSSA</td><td>P</td><td>--</td><td>Analog ground.</td><td></td></tr>
<tr><td>37</td><td>VDD</td><td>P</td><td>--</td><td>Analog power.</td><td></td></tr>
<tr><td>38</td><td>VREF_POS</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
<tr><td>39</td><td>VREF_NEG</td><td>C</td><td>--</td><td>For power setting capactor connected pin.</td><td></td></tr>
</table>

| | | | | | |
|---|---|---|---|---|---|
| 40 | VDDX8 | P | -- | DCDC positive voltage | |
| 41 | NVDDX8 | P | -- | DCDC negative voltage | |
| 42 | VDD_DRV | P | -- | DCDC power. | |
| 43 | ADRVU | O | Type 1 | PWM output for DCDC converter. | |
| 44 | ADRVD | O | Type 1 | PWM output for DCDC converter. | |
| 45 | VSS_DRV | P | -- | DCDC ground. | |
| 46 | VDPS | P | -- | External voltage for source postive power. | |
| 47 | VDNS | P | -- | External voltage for source negative power. | |
| 48 | VDPG | C | -- | For power setting capactor connected pin. | |
| 49 | VDNG | C | -- | For power setting capactor connected pin. | |
| 50 | Dummy | D | -- | Dummy pin | |

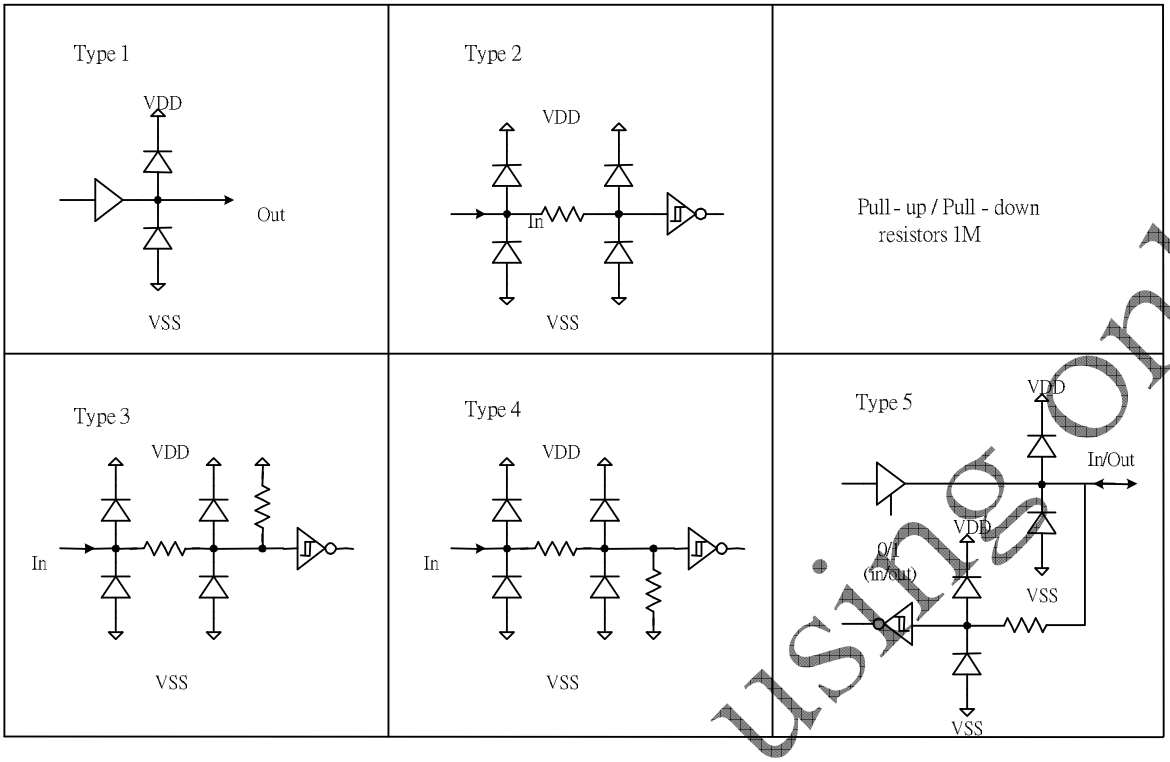
I: Input pin; O:output pin, I/O: Input / Output; P: Power pin; C: capacitor pin; D：Dummy

Note 1: Please reference chapter F

Note 2: Please reference chapter E

Note 3: Please reference chapter E

**I/O Pin Structure:**



## 2. Absolute Maximum Ratings

| Item | Symbol | Condition | Min. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Power voltage | VDD | VSSA=VSS=0 | -0.3 | +5.0 | V | |
| Power voltage | VDD_DRV | VSS_DRV=0 | -0.3 | +5.0 | V | |
| Source voltage | VDPS | VSSA=VSS=0 | | +20 | V | |
| | VDNS | VSSA=VSS=0 | -20 | | V | |
| Gate voltage | VDPG | VSSA=VSS=0 | -0.3 | VDNG+40 | V | |
| | VDNG | VSSA=VSS=0 | VDPG-40 | +0.3 | V | |
| VCOM voltage | VCOMH | VSSA=VSS=0 | 0 | VNPG-1 | V | |
| | VCOML | VSSA=VSS=0 | VDNG+1 | 0 | V | |
| Storage temperature | Tstg | - | -25 | 70 | ℃ | |
| Operating | Topa | - | 0 | 40 | ℃ | |

## 3. Operation Ratings

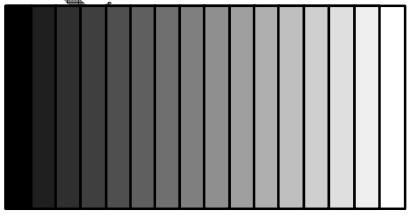
| Item | Symbol | Min. | Typical | Max. | Unit | Remark |
|---|---|---|---|---|---|---|
| Power voltage | VDD=VCC | 3.0 | 3.3 | 3.6 | V | |
| Power voltage | VDD_DRV | 3.0 | 3.3 | 3.6 | V | |
| Source voltage | VDPS | 14.5 | 15 | 15.5 | V | |
| | VDNS | -15.5 | -15 | -14.5 | V | |
| Gate voltage | VDPG | 19 | 20 | 21 | V | |
| | VDNG | -21 | -20 | -19 | V | |
| VCOM voltage | VCOMH | 10.5 | 11 | 11.5 | V | |
| | VCOML | -19.5 | -19 | -18.5 | V | |

# D. Electrical Characteristics

## 1. Panel Power Consumption

| Item | Symbol | Condition | Min. | Typical | Max. | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | VSSA=VSS=VSS_DRV=0V | -- | 3.3 | -- | V |
| | VDD_DRV | VSSA=VSS=VSS_DRV=0V | -- | 3.3 | -- | |
| Low Level Input Voltage | Vil | Digital input pins | GND | - | 0.3xVDD | V |
| High Level Input Voltage | Vih | Digital input pins | 0.7xVDD | - | VDD | V |
| Operating temperature | $T_{op}$ | | - | 25 | - | ℃ |
| Operation Power Dissipation | P | VDD=VDD_DRV=3.3V | -- | 1.07 | 2 | mA |
| | | VDNS=-15V | | 0.82 | 1.5 | mA |
| | | VDPS=15V | | 0.86 | 1.5 | mA |
| | | VDPG=20V | | 1.23 | 2 | mA |
| | | VDNG=-20V | | 0.66 | 1.5 | mA |
| | | VCOMH=11V | | 0.36 | 1 | mA |
| | | VCOML=-19V | | 0.56 | 1 | mA |
| Standby Power Dissipation | P | VDD=VDD_DRV=3.3V | -- | 0.06 | 0.15 | mA |
| | | VDNS=0V | | 0.02 | 0.1 | mA |
| | | VDPS=0V | | 0.02 | 0.1 | mA |
| | | VDPG=3.3V | | 0.02 | 0.1 | mA |
| | | VDNG=0V | | 0.02 | 0.1 | mA |
| | | VCOMH=0V， | | 0.01 | 0.1 | mA |
| | | VCOML=0V | | 0.02 | 0.1 | mA |
| Image Update Time | | T=25℃ | -- | 950 | 1010 | ms |
| | | T=10℃ | -- | 2310 | 2450 | ms |
| | | T=0℃ | -- | 2750 | 3150 | ms |

*: Typical power consumption measured by following pattern



# E. Input timing AC Characteristics

## 1. Horizontal Input Timing

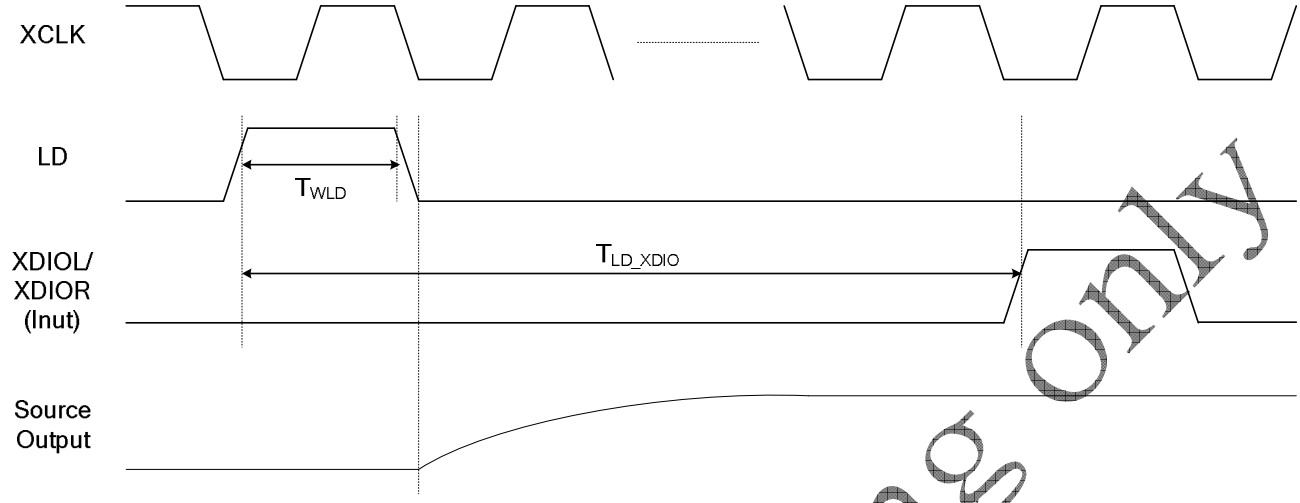
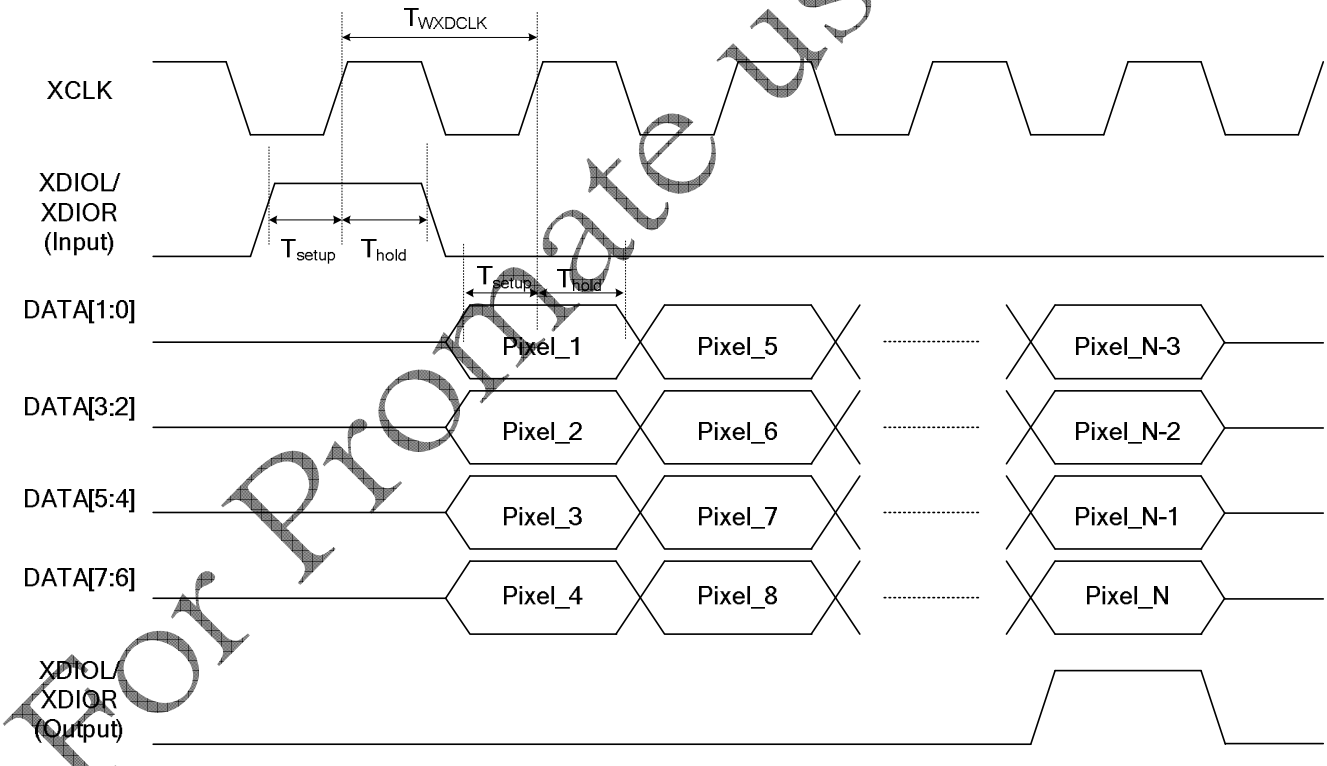



**Figure 1:** LD input timing




**N=800**

**Figure 2:** Horizontal data Input timing

(VDD=VDD_DRV=3.3V, VSSA=VSS=VSS_DRV=0V, TA=25℃)

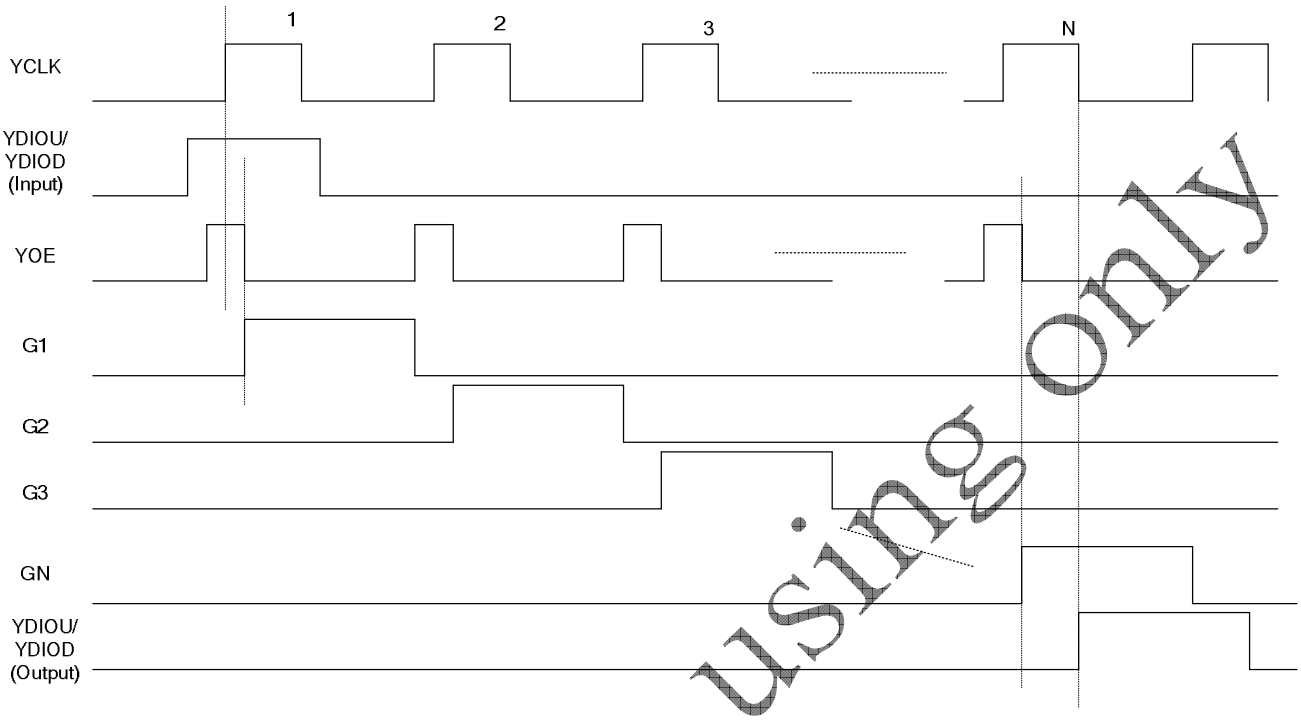
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Clock pulse width | $T_{WXDCLK}$ | 13 | | | ns |
| Data setup time | $T_{setup}$ | 2 | - | - | ns |
| Data hold time | $T_{hold}$ | 2 | - | - | ns |
| LD pulse width | $T_{WLD}$ | 1 | - | - | XCLK |
| Time from LD to XDIOL/XDIOR | $T_{LD\_DIO}$ | 5 | - | - | XCLK |

## 1.1 Relationship of Input Data and Source Output Voltage

The source driver output voltage will base on input 2 bits data, and the relationship is as below:

| MSB | LSB | Function |
|---|---|---|
| 0 | 0 | Source output is 0V |
| 0 | 1 | Source output is VDPS(+15V) |
| 1 | 0 | Source output is VDNS(-15V) |
| 1 | 1 | Source output is floating |

## 2. Vertical Input Timing




**N=600**

**Figure 3:** Vertical input timing

## 3. VCOM Voltage Definition

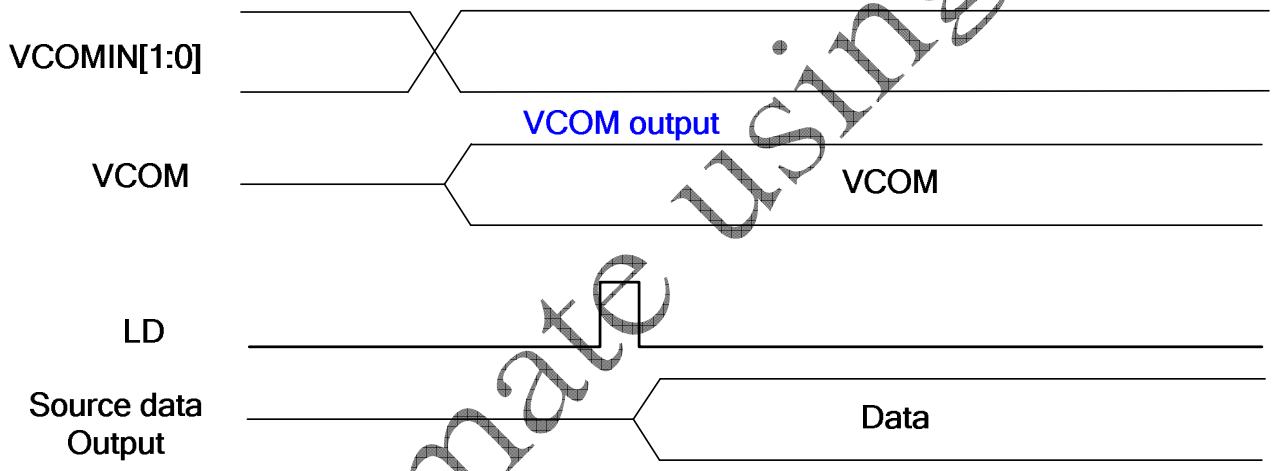
The VCOM output voltage will base on input pins VCOMIN[1:0], and the relationship is as below:

| VCOMIN[1 :0] | Function |
|---|---|
| 00 | VCOM output is (-VDC) v |
| 01 | VCOM output is (VDPS-VDC) v |
| 10 | VCOM output is (VDNS-VDC) v |
| 11 | VCOM output is floating |

## 4. VCOM Relationship

VCOM will change while VOCMIN change

Source output will change while LD signal falling edge.

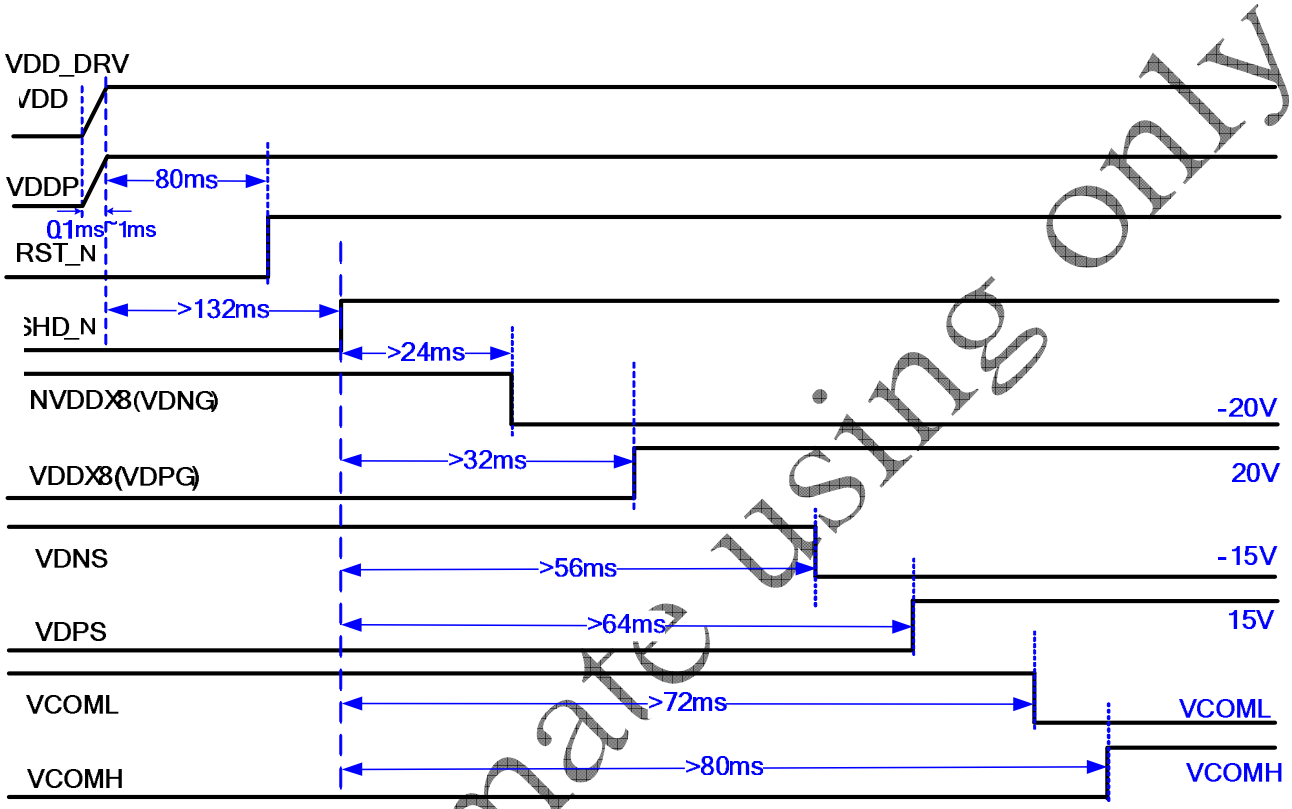


# F. Power On/Off Characteristics

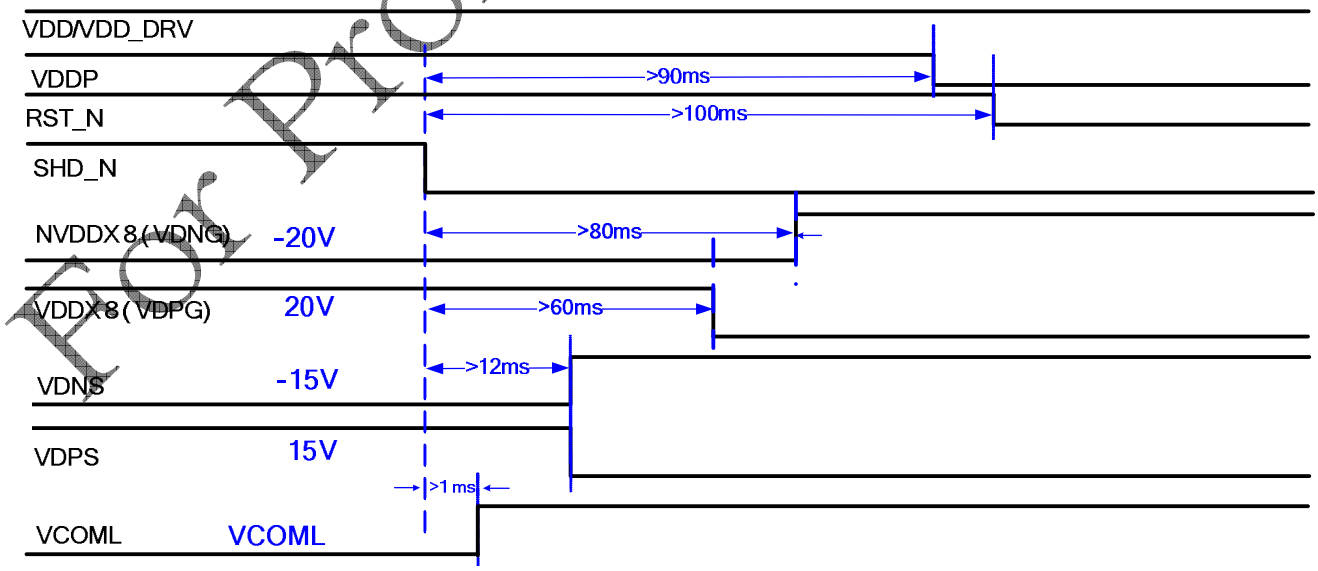
## 1. Recommended Power On/Off Sequence

The suggested power on/off sequence is below:

### 1.1 Power On Sequence:




### 1.2 Power Off Sequence:



# G. Optical Specification

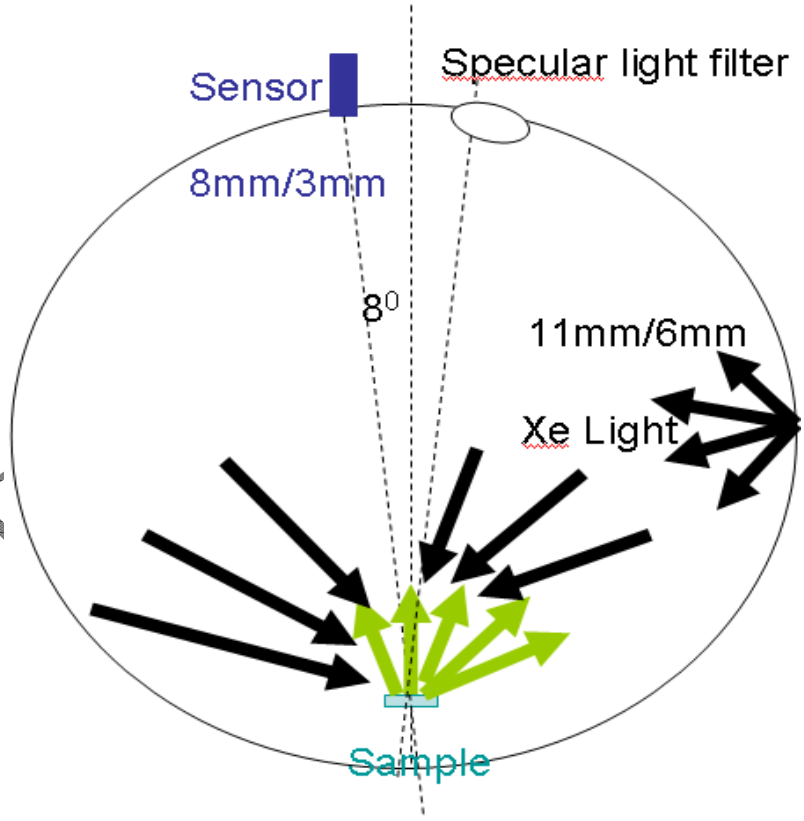
All optical specification is measured under typical condition (Note 1, 2)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Remark |
|---|---|---|---|---|---|---|---|
| Reflectance | R | white | 28 | 30 | -- | % | Note1,2,3,4 |
| Contrast Ratio | CR | At optimized viewing angle | 5 | 6 | -- | | Note1,2,3,5 |
| Update Time | T | T=25℃<br>T=10℃<br>T=0℃ | -- | 950<br>2310<br>2750 | 1010<br>2450<br>3150 | ms | Note 3 |

Note 1. Ambient temperature =25℃

Note 2. Reflectance and constrast ratio are measured by KONICA MINOLTA spectrophotometer CM-2600d.

Note 3: The measurement shall be conducted under AUO specificed driving condition, including LUT and TCON codes.



Note 4. Definition of Reflectance:

The Reflectance is expressed as:

R = Reflectance Factor$_{\text{white board}}$ x ($L_{\text{center}}$ / $L_{\text{white board}}$)

$L_{\text{center}}$ is the luminance measured at center in a white area. $L_{\text{white board}}$ is the luminance of a standard white board.

Note 5. Definition of contrast ratio:

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and reflectance in a dark area (Rd).

$$\text{Contrast ratio (CR)} = \frac{\text{Rl}}{\text{Rd}}$$

# H. Reliability Test Items

| | Test | Condition | Condition | Remark |
|---|---|---|---|---|
| 1 | High-Temperature Operation | Tamb=+40℃, RH=30% for 240hrs | IEC 60068-2-2Bp | Update pattern four times per minute. |
| 2 | Low-Temperature Operation | Tamb=0℃ for 240hrs | IEC 60068-2-2Ab | Update pattern four times per minute. |
| 3 | High-Temperature Storage | Tamb=+70℃, RH=23% for 240hrs | IEC 60068-2-2Bp | |
| 4 | Low-Temperature Storage | Tamb=-25℃ for 240hrs | IEC 60068-2-2Ab | |
| 5 | High-Temperature, High-Humidity Operation | Tamb=+40℃, RH=90% for 168hrs | IEC 60068-2-3CA | Update pattern four times per minute. |
| 6 | High-Temperature, High-Humidity Storage | Tamb=+60℃, RH=80% for 240hrs | IEC 60068-2-3CA | |
| 7 | Temperature Cycle | 1 Cycle：[-25° C 30min] → [+70° C 30min]：100 cycles | IEC 60068-2-14 | |
| 8 | UV Exposure Resistance | Condition: 1120W/m2, 40℃<br>Test Duration: 3 cycles<br>(Definition of 1 cycle:<br>8 hr at exposure state and 16 Hr at non-exposure state) | IEC 60068-2-5Sa | |
| 9 | Package Vibration | 1.04G, Frequency：10 ~ 500HZ<br>Direction：X, Y, Z<br>Duration：1 hours in each direction | | |
| 10 | Package Drop Impact | Drop from height of 100 cm on concrete surface.<br>Drop sequence：1 corner, 3 edges, 6 faces one drop for each. | | |
| 11 | Electrostatic discharge | Air-mode : +/- 6kV<br>Contact-mode : +/- 2kV | IEC 61000-4-2 | |
| 12 | FPC Bonding Strength | Pull the FPC Stiffener part with a force of 500gf in the horizontal and vertical directions | | |

| | | | | |
|---|---|---|---|---|
| 13 | FPC bending Performance | Apply MIT method.<br>Bending rate radius：1.0mm<br>Weight 500gf, Bending angle：±135° Bending cycle：20 times | | |
| 14 | Stylus Tapping | POLYACETAL Pen：Top R0.8mm<br>Load：300gf<br>Speed：3 times/sec<br>Total 13,500 times | | Pass criteria - no glass breakage or damage to micro-cups. |

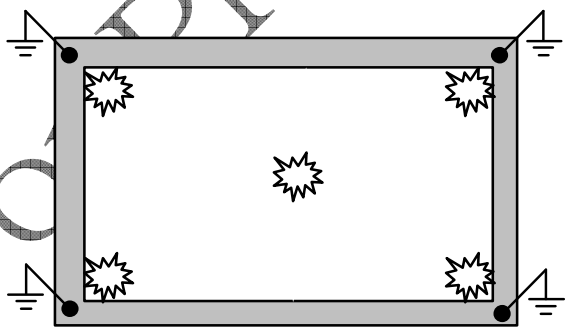
Note 1. In the above conditions, there is no display function NG issue occurred. All the cosmetic specification is judged before the reliability stress.

Note 2. The test modules will be kept at 25℃ environment for 4 hours after finish the environmental test and make measurement after AUO specified TCON code and waveform re-driving. The judgement of above tests should satisfy minimum contrast ratio and minimum reflectance.

Note 3. For Item 8, in addition to satisfy minimum contrast ratio and minimum reflectance, the display shall be able to identify 8 gray levels, including Black and White when being driven under AUO specified driving condition at the end of test.

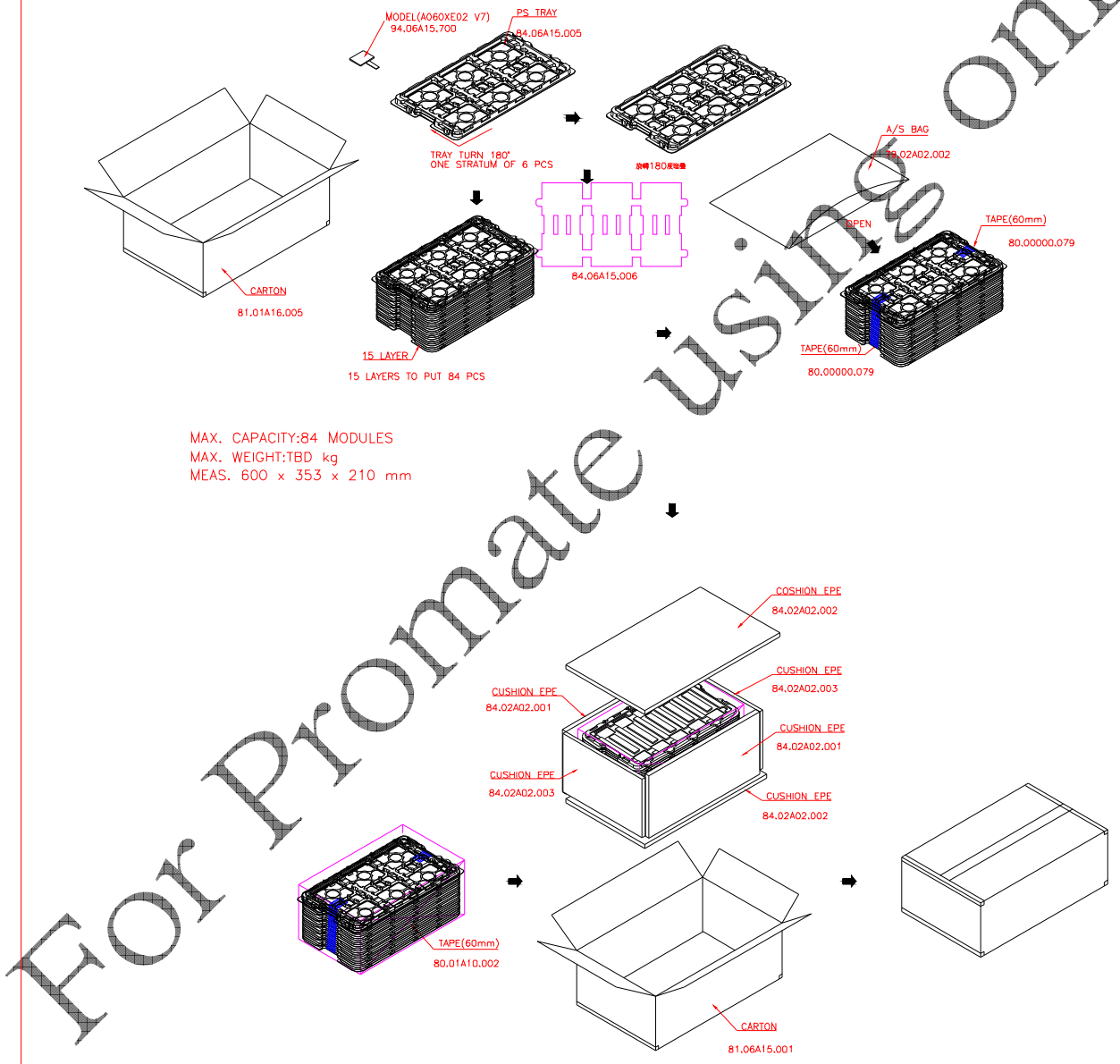
Note 4. ESD testing method.

1. Ambient: 24~26℃, 56~65%RH, atmospheric pressure : 940~960hPa
2. Instruments:NoisekenESS-2000,
3. Operation System: AUO pattern generator
4. Test Mode: Non-operating mode, test pattern: chess
5. Test Method:
   a. Contact Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
   b. Air Discharge: 150pF(330Ω) 1sec, 5 points, 10 times/point
6. Test point:



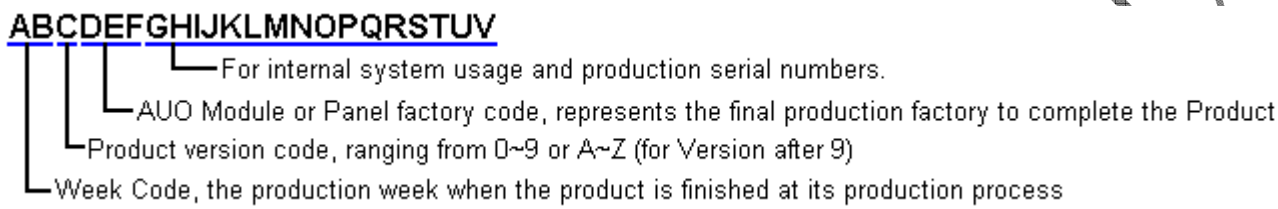
# I. Packing and Marking

## 1. Packing Form



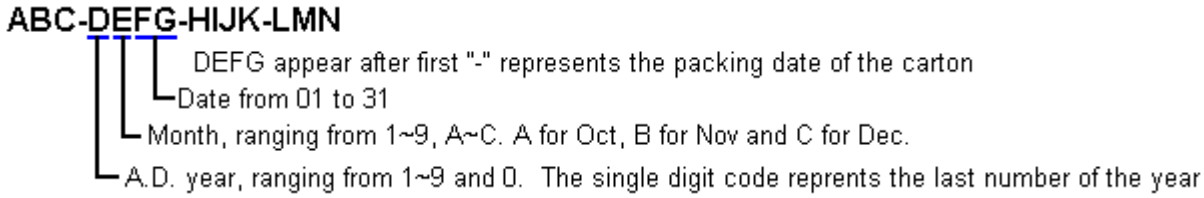
## 2. Module/Panel Label Information

The module/panel (collectively called as the “Product”) will be attached with a label of Shipping Number which represents the identification of the Product at a specific location. Refer to the Product outline drawing for detailed location and size of the label. The label is composed of a 22-digit serial number and printed with code 39/128 with the following definition:




## 3. Carton Label Information

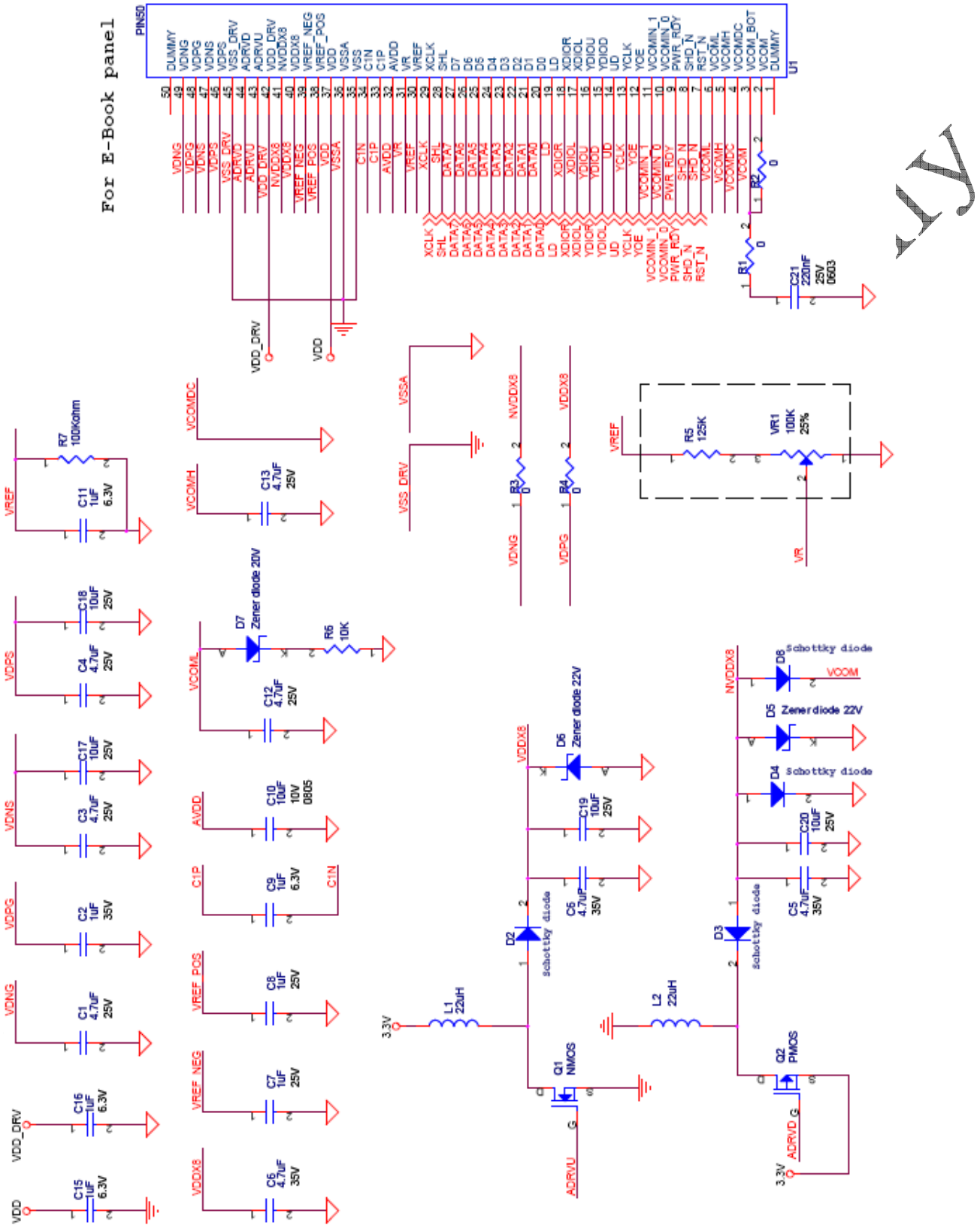
The packing carton will be attached with a carton label where packing Q’ty, AUO Model Name, AUO Part Number, Customer Part Number (Optional) and a series of Carton Number in 13 or 14 digits are printed. The Carton Number is apparing in the following format:




Refer to the drawing of packing format for the location and size of the carton label.

# J. Application Note

## 1. Application Circuit



# K. Precautions

1. Do not twist or bend the module and prevent the unsuitable external force for display module during assembly.
2. Adopt measures for good heat radiation. Be sure to use the module with in the specified temperature.
3. Avoid dust or oil mist during assembly.
4. Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module.
5. Less EMI: it will be more safety and less noise.
6. Please operate module in suitable temperature. The response time & brightness will drift by different temperature.
7. Be sure to turn off the power when connecting or disconnecting the circuit.
8. Display surface never likes dirt or stains.
9. A dewdrop may lead to destruction. Please wipe off any moisture before using module.
10. High temperature and humidity may degrade performance. Please do not expose the module to the direct sunlight and so on.
11. Acetic acid or chlorine compounds are not friends with display module.
12. Static electricity will damage the module, please do not touch the module without any grounded device.
13. Do not disassemble and reassemble the module by self.
14. Be careful do not touch the rear side directly.
15. No strong vibration or shock. It will cause module broken.
16. Storage the modules in suitable environment with regular packing.
17. Be careful of injury from a broken display module.
18. Please avoid the pressure adding to the surface (front or rear side) of modules, because it will cause the display non-uniformity or other function issue.
19. Application under direct sunlight is strongly not recommended as it would result in display performance degradation.
20. It is highly recommended that the display is exposed to an even lighting condition to ensure a good display uniformity.
21. Elimination of light exposure to the display by applying proper means, e.g. lighting shielding cover is suggested when the display is not being used to extend the life performance of the device.
22. Heat isolation or heat sink to control uniformity of panel temperature should smaller than 3℃
23. Any performance degradation or display distortion which can be eliminated by display refreshing should not be regarded as a defect.