Version	4
Total pages	18
Date	2007.07.27

Product Specification

10.2″ color TFT-LCD

MODEL NAME: A102VW01 V8

(◆) Preliminary Specification
( ) Final Specification

Note: The content of this specification is subject to change.

Record of Revision

Version	Revise Date	Page	Content
1	21/Nov./2006	0	First draft.
2	30/Nov./2006	3	Correct overall outline dimension
3	18/Jan./2007	All	New Cell Version (.801)
4	27/Jul/2007	18	Add reference gamma voltage

A. Physical specifications

NO.	Item	Specification	Remark
1	Display resolution (dot)	800RGB(W)×480(H)	
2	Active area (mm)	222.0(W)×133.2(H)	
3	Screen size (inch)	10.2(Diagonal)	
4	Pixel pitch (mm)	0.2775(W)×0.2775(H)	
5	Color configuration	R. G. B. stripe	
6	Overall dimension (mm)	230.6(W)×142.3(H)×1.75(D)	Note 1
7	Weight (g)	125 ±10	
8	Surface treatment	Anti-Glare	

Note 1: Refer to Fig.1

B. Electrical specifications

1. Absolute Maximum Ratings

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	Vcc	-0.5		5	V
	AVDD	-0.5		12	V
	VGH	-0.3		18	V
	VGL	-15		0.3	V
	VGH-VGL			33	V
Input Signal Voltage	Vi	-0.3		Vcc+0.3	V
	Vref(V1~V7)	0.4AVDD		AVDD+0.3	V
	Vref(V8~V14)	-0.3		0.6AVDD	V
	Vcom	3.27		3.89	V
Operating Temperature	Topa	-30		85	℃
Storage Temperature	Tstg	-40		85	℃

2. Typical operating conditions (GND=AVSS=0V)

Items	Symbol	Product Specification			Unit
		Min.	Typ.	Max.	
Power Voltage	VCC	3.0	3.3	3.6	V
	AVDD	8.2	8.8	9.2	V
	VGH	14	15	16	V
	VCOM	3.3	3.6	3.8	V
	VGL	-6.8	-7.0	-7.2	V
Input Reference Voltage	V1~V7	0.4AVDD	—	AVDD-0.3	V
	V8~V14	0.1	—	0.6AVDD	V
Input H/L level Voltage	VIH	0.8VCC	—	VCC	V
	VIL	0	—	0.2VCC	V

3. Current consumption conditions(GND=Avss=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Current For Driver	IGH	VGH=15V		50	100	uA
	IGL	VGL=-7V		-0.2	-0.6	mA
	ICC	VCC=3.3V		3.5	5	mA
	IDD	AVDD=8.8V		20	30	mA

4. Timing conditions

AC Electrical Characteristics (VCC=3.3V, AVDD=8.4V, AVSS=GND=0V, TA=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK frequency	Fclk		40	42	MHz
CLK pulse width	TCW	6			ns
Data set-up time	Tsu	4			ns
Data hold time	Thd	2			ns
Propagation delay of DIO2/1	Tphl	6	10	15	ns
Time that the last data to LD	Tld	1			Tcw
Pulse width of LD	Twld	2			Tcw
Time that LD to DIO1/2	Tlds	5			Tcw
POL set-up time	Tpsu	6			ns
POL hold time	Tphd	6			ns
CKV pulse width	TCKV	16	28	40	Tcw
STV setup time	TSUV	400			ns
STV hold time	THDV	400			ns
Vertical display start	TSV		3		TDH
Output stable time	Tst			15	us

5. Pin assignment

TFT-LCD panel driving section

(1.) FH12-30S-0.5SH(Hirose) — FPC I/O Pin Assignment

Pin no	Symbol	I/O	Description	Remark
1	POL	O	Polarity selection	
2	DIO2	I/O	Vertical start pulse signal input or output	
3	OE	I	Output enable	
4	CPV	I	Vertical clock	
5	DIO1	I	Vertical start pulse signal input or output	
6	GND	P	Power ground	
7	EDGSL	I	Select rising edge or rising/falling edge	
8	VCC	P	Digital voltage for source driver	
9	V9	I	Gamma voltage level 9	
10	VGL	P	Gate OFF voltage	
11	V2	I	Gamma voltage level 2	
12	VGH	P	Gate ON voltage	
13	V6	I	Gamma voltage level 6	
14	U/D	I	Up/down selection	
15	VCOM1	I	Common voltage	
16	GND	P	Power ground	
17	AVDD1	P	Power supply for analog circuit	
18	V14	I	Gamma voltage level 14	
19	V11	I	Gamma voltage level 11	
20	V8	I	Gamma voltage level 8	
21	V5	I	Gamma voltage level 5	
22	V3	I	Gamma voltage level 3	
23	GND	P	Power ground	
24	R5	I	Red data(MSB)	
25	R4	I	Red data	
26	R3	I	Red data	
27	R2	I	Red data	
28	R1	I	Red data	
29	R0	I	Red data(LSB)	
30	GND	P	Power ground	

Pin no	Symbol	I/O	Description	Remark
31	GND	P	Power ground	
32	G5	I	Green data (MSB)	
33	G4	I	Green data	
34	G3	I	Green data	
35	G2	I	Green data	
36	G1	I	Green data	
37	G0	I	Green data (LSB)	
38	STHL	I/O	Horizontal start pulse signal input or output	
39	INV	I	Control signal are inverted by ASIC or not	
40	GND	P	Power ground	
41	DCLK	I	Sample clock	
42	DVDD	P	Voltage for digital circuit	
43	STHR	I/O	Horizontal start pulse signal input or output	
44	LD	I	Latches the polarity of outputs and switches the new data to outputs	
45	B5	I	Blue data (MSB)	
46	B4	I	Blue data	
47	B3	I	Blue data	
48	B2	I	Blue data	
49	B1	I	Blue data	
50	B0	I	Blue data (LSB)	
51	R/L	I	Right/ left selection	
52	V1	I	Gamma voltage level 1	
53	V4	I	Gamma voltage level 4	
54	V7	I	Gamma voltage level 7	
55	V10	I	Gamma voltage level 10	
56	V12	I	Gamma voltage level 12	
57	V13	I	Gamma voltage level 13	
58	AVDD2	P	Voltage for analog circuit	
59	GND	P	Power ground	
60	VCOM2	I	Common voltage	

※I: Input. O: Output. P: Power.

C. Optical specification (Note 1, Note 2, Note 3)

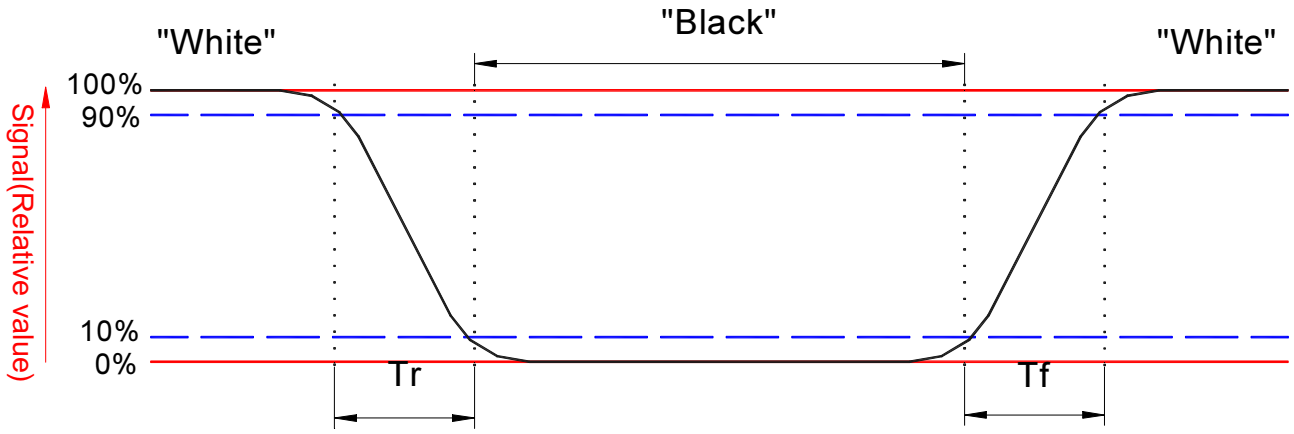
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Response time	Rise Fall	Tr Tf	θ =0°	- -	12 18	50 60	ms ms	Note 4,6
Contrast ratio		CR	At optimized Viewing angle	200	350	-		Note 5,6
Viewing angle	Top Bottom Left Right		CR≧10	20 40 45 45	35 60 60 60	- - - -	deg.	Note 6,7
Transmission		Y_L	θ =0°	7.0	7.8	-	%	Note 8

Note 1 : Ambient temperature =25℃. And lamp current I_L = 6.5 mArms.
Designate backlight unit: AUO A102VW01 V7 Backlight Unit

Note 2: To be measured in the dark room.

Note 3 :To be measured on the center area of panel with a viewing cone of 1°by Topcon luminance meter BM-7, after 10 minutes operation.

Note 4. Definition of response time:
The output signals of photo detector are measured when the input signals are changed from “black” to “white”(falling time) and from “white” to “black”(rising time), respectively.
The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5. Definition of contrast ratio:
Contrast ratio is calculated with the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Photo detector output when LCD is at “White” state}}{\text{Photo detector output when LCD is at “Black” state}}$$

Note 6. Note 4. White Vi=V_{i50} ＋ 1.5V

Black Vi=V_{i50} ± 2.0V

“±” means that the analog input signal swings in phase with V_{COM} signal.

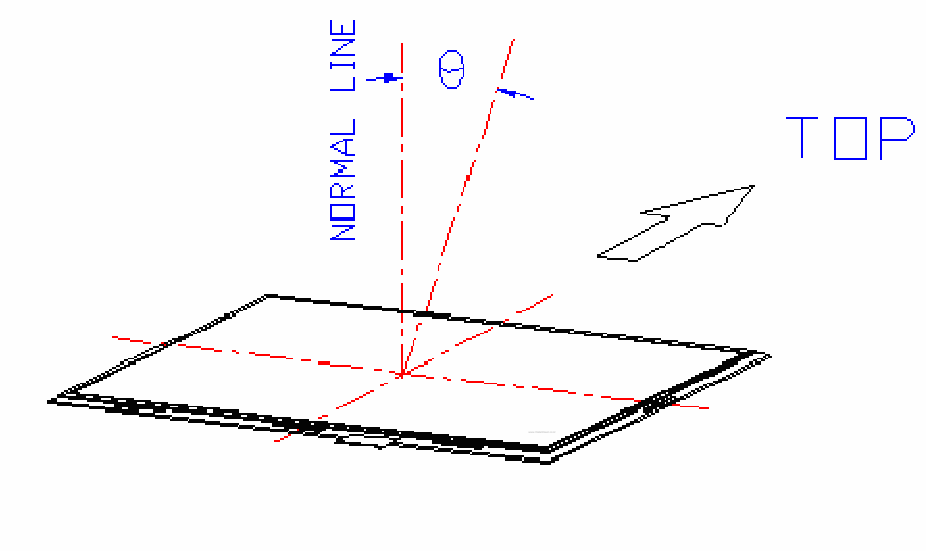
“∓” means that the analog input signal swings out of phase with V_{COM} signal.

V_{i50} ： The analog input voltage when transmission is 50%

The 100% transmission is defined as the transmission of LCD panel when all the input terminals of module are electrically opened.

Note 7. Definition of viewing angle:

Refer to figure as below.



Note 8. Transmission is defined as follow:(θ =0°)

Transmission = B1/B2

B1=Photo detector output voltage when measuring the brightness of the LCD panel placed on the light source with no applied voltage

B2=Photo detector output voltage when measuring the light source

D. Reliability test items (Note 2):

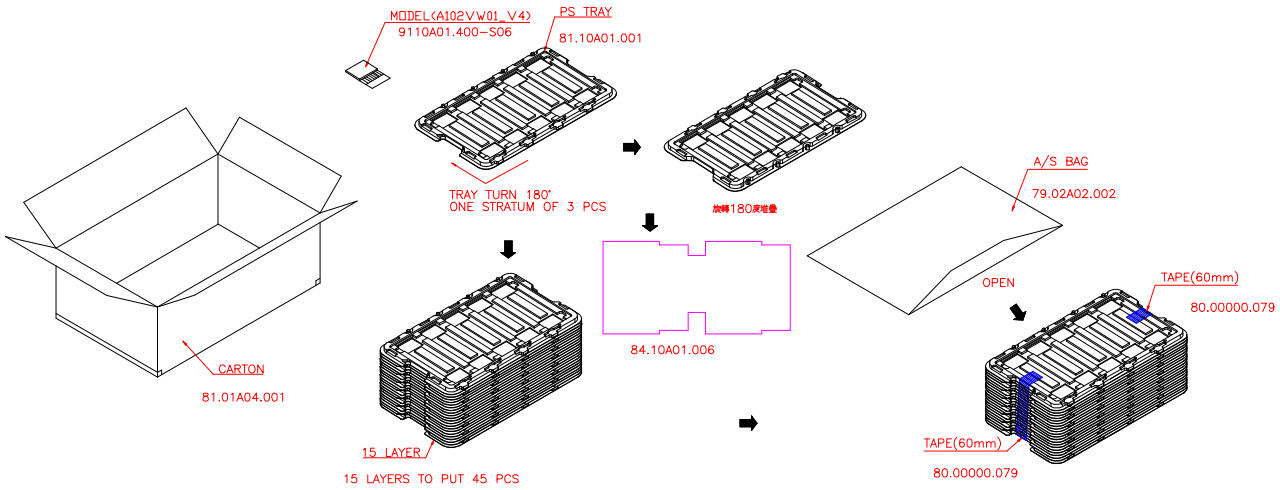
No.	Test items	Conditions	Remark
1	High temperature storage	Ta= 70℃ 240Hrs	
2	Low temperature storage	Ta= -20℃ 240Hrs	
3	High temperature operation	Tp= 60℃ 240Hrs	
4	Low temperature operation	Ta= -10℃ 240Hrs	
5	High temperature and high humidity	Tp= 50℃, 80% RH 240Hrs	Operation
6	Thermal shock	-20℃~70℃/ 100 cycles 1Hrs/cycle	Non-operation
7	Electrostatic discharge	±200V,200pF(0Ω), once for each terminal	Non-operation
8	Vibration	Frequency range : 8~33.3Hz Stoke : 1.3mm Sweep : 2.9G, 33.3 ~ 400Hz Cycle : 15 minutes 2 hours for each direction of X,Z 4 hours for Y direction	JIS D1601, A-10 Condition A
9	Mechanical shock	100G, 6ms, ±X,±Y,±Z 3 times for each direction	JIS C0041, A-7 Condition C
10	Vibration (with carton)	Random vibration: 0.015G^2/Hz from 5~200Hz –6dB/octave from 200~500Hz	IEC 68-34
11	Drop (with carton)	Height: 60cm 1 corner, 3 edges, 6 surfaces	JIS Z0202

Note1: Ta: Ambient temperature.

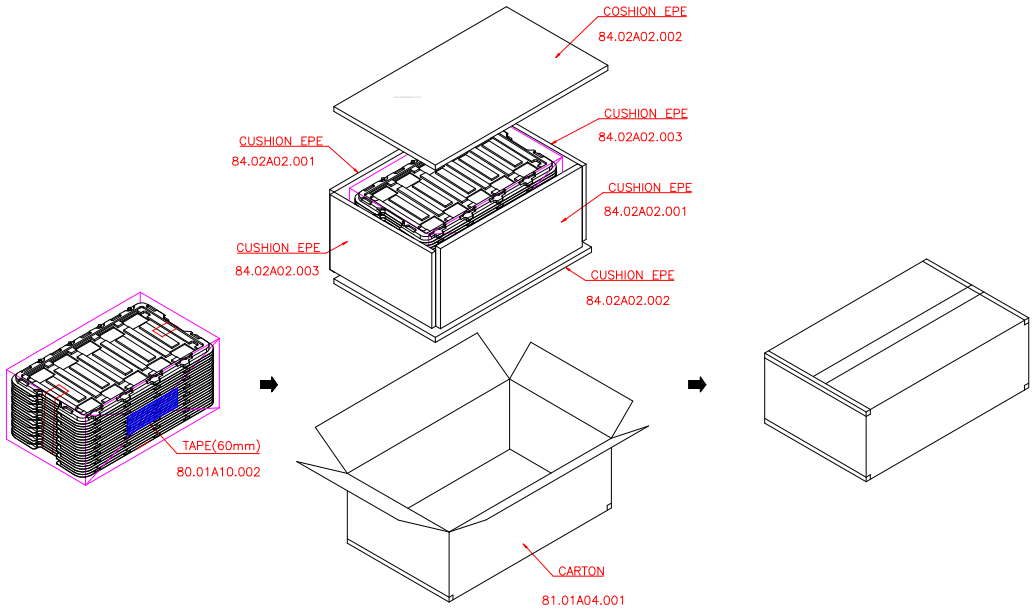
Note2: Tp: Panel Surface Temperature

Note3: All the cosmetic specification is judged before the reliability stress.

E. Packing form



MAX. CAPACITY:30 MODULES
MAX. WEIGHT:10kg
MEAS. 600mmX353mmX210mm



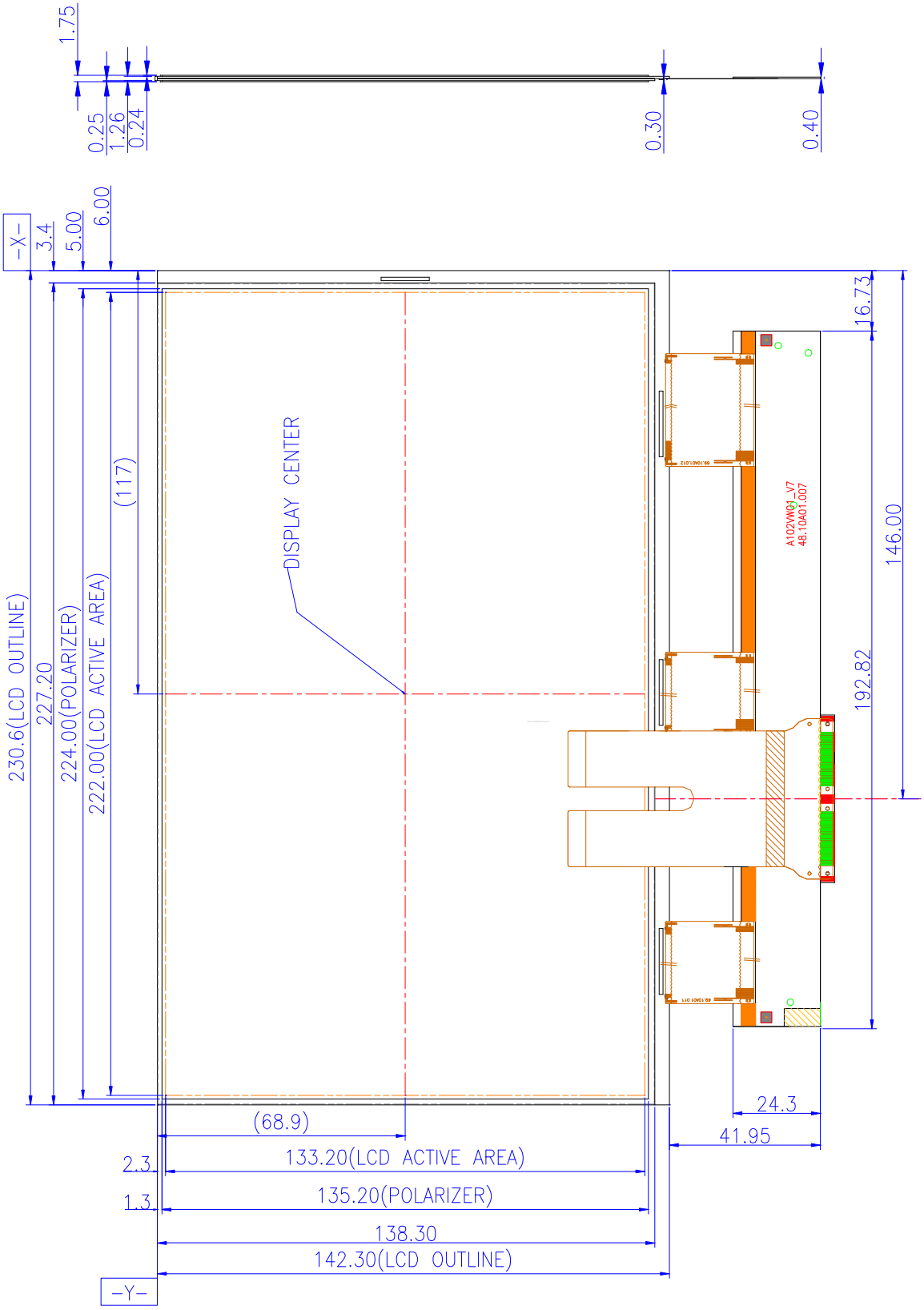


Fig.1 Outline dimension of TFT-LCD (Front Side)

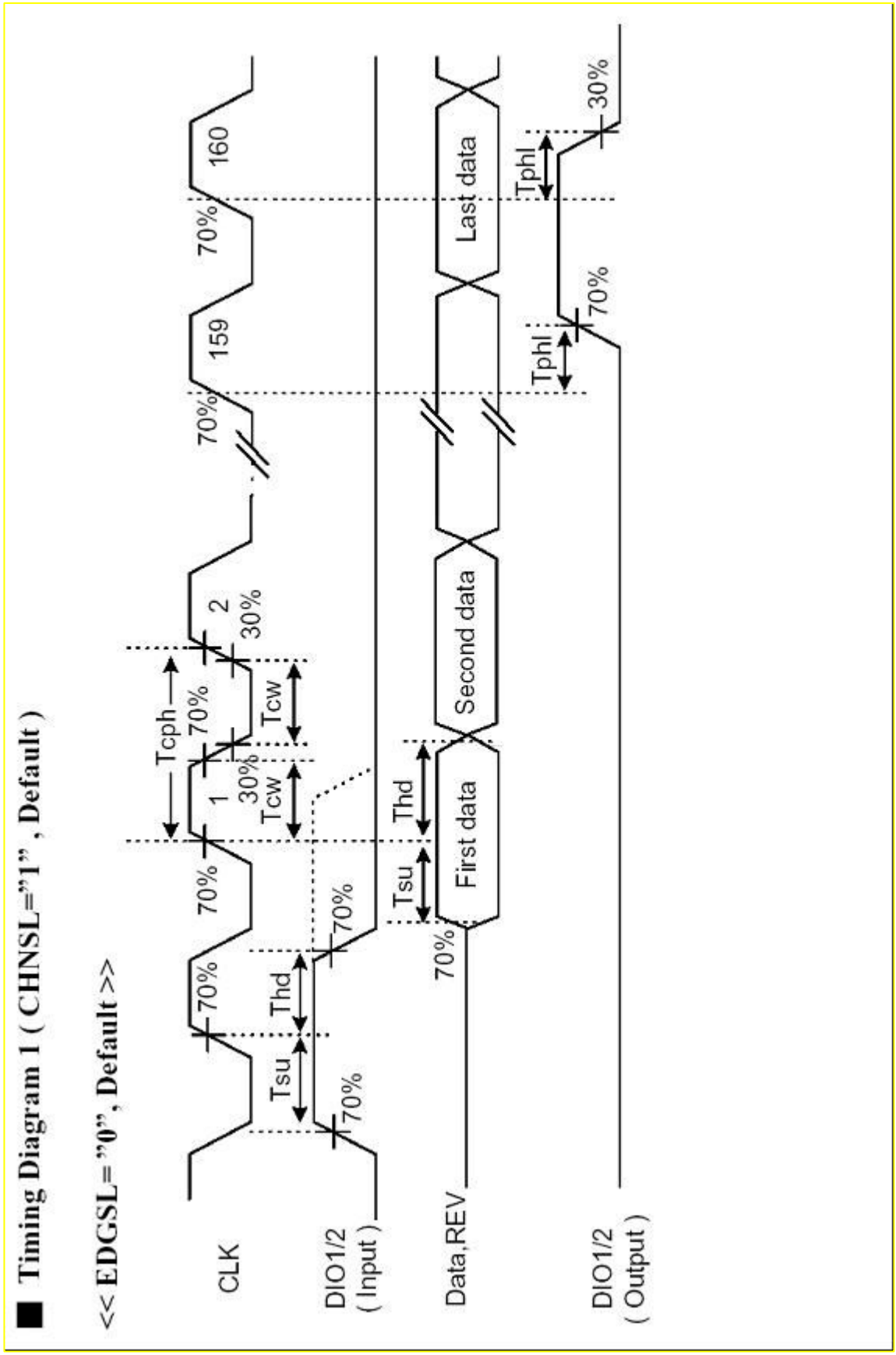


Fig.2 Operation Mode 1

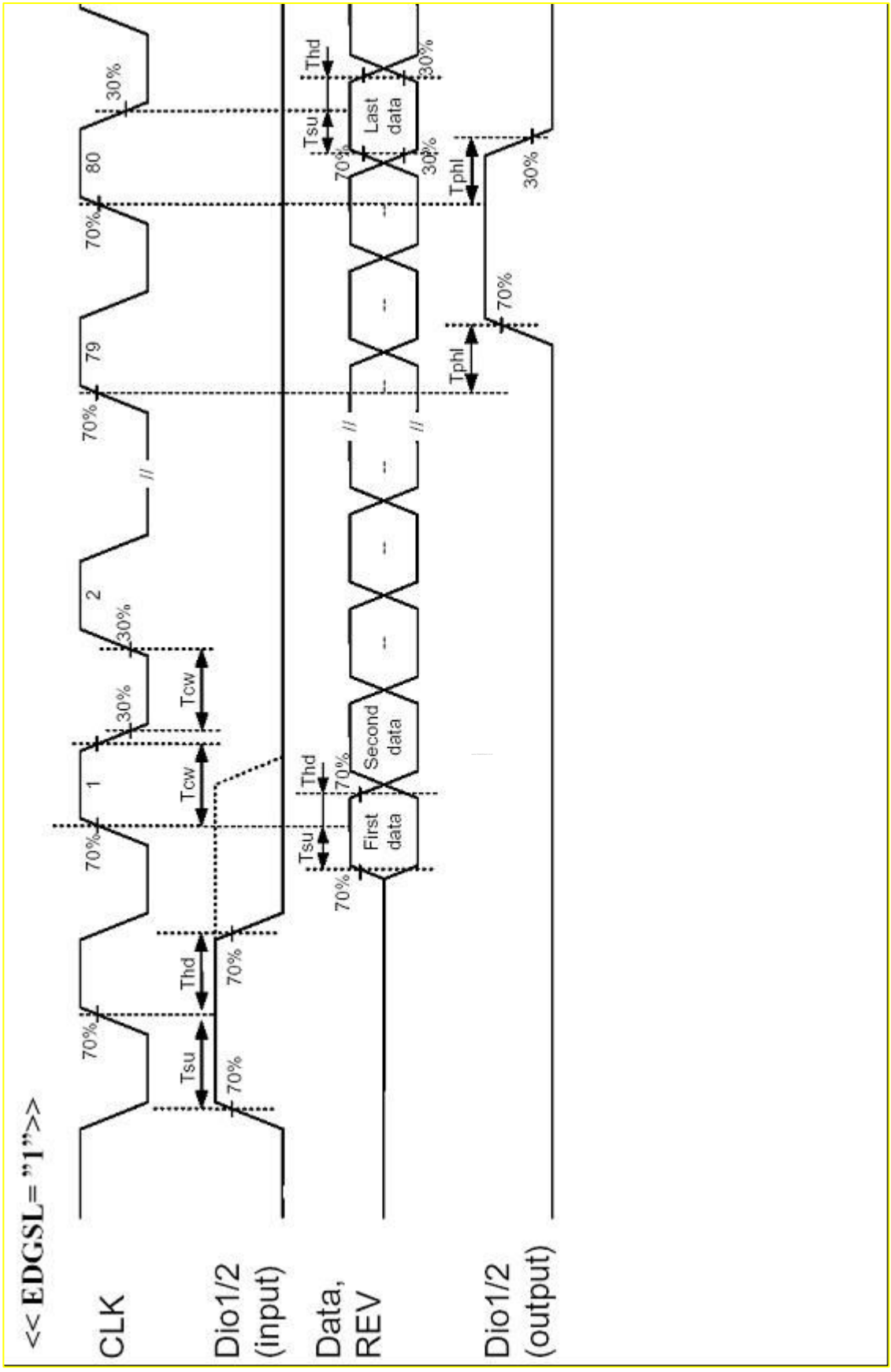


Fig.3 Operation Mode 2

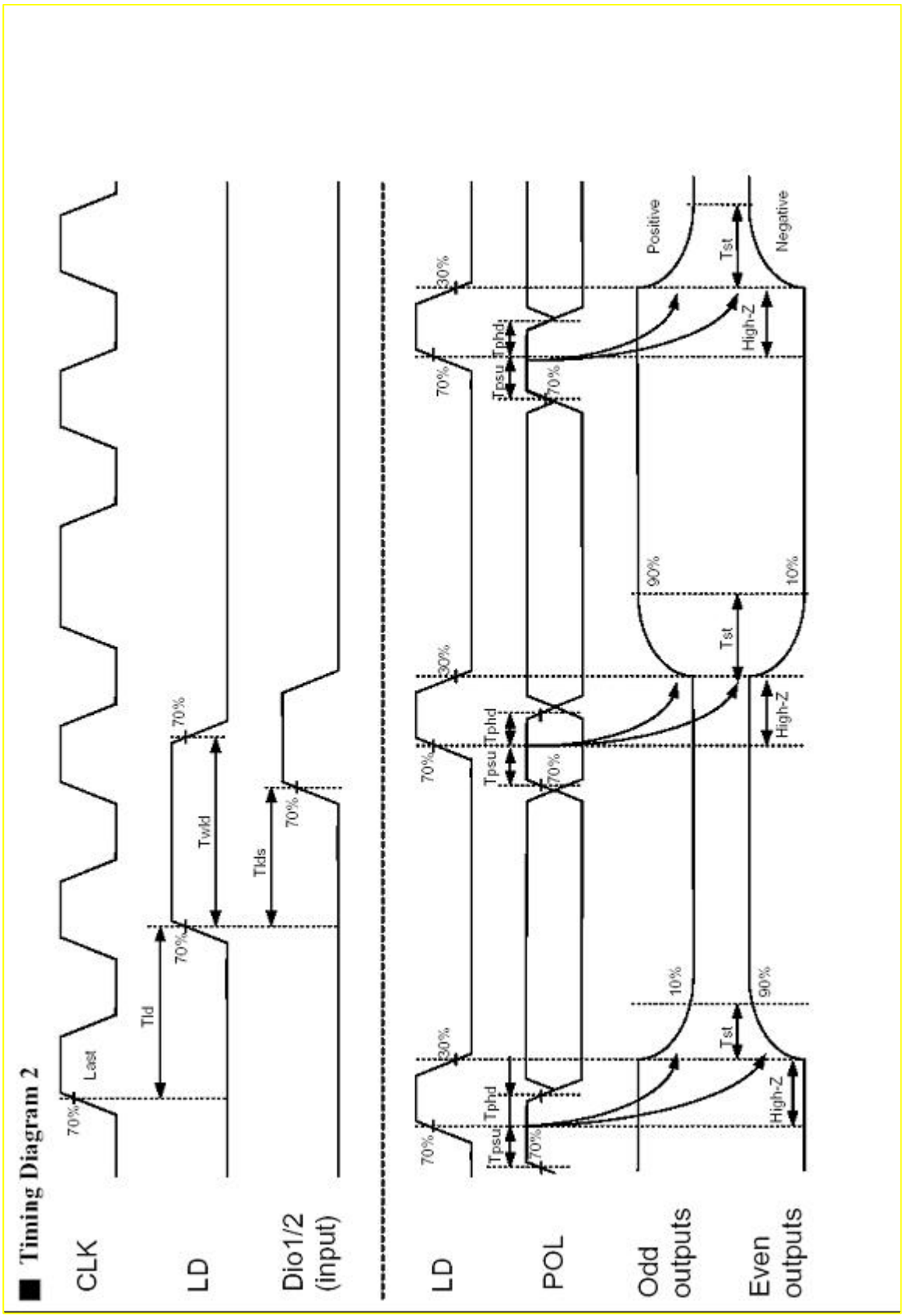


Fig.4 Horizontal timing

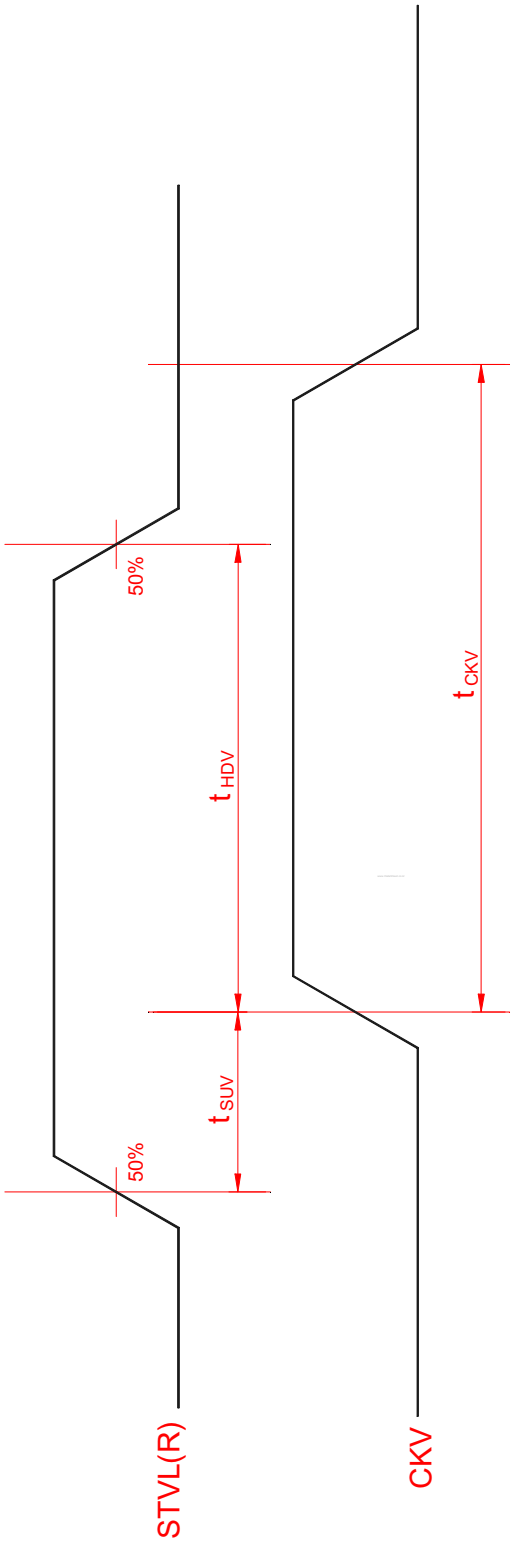


Fig.5 Vertical shift clock timing

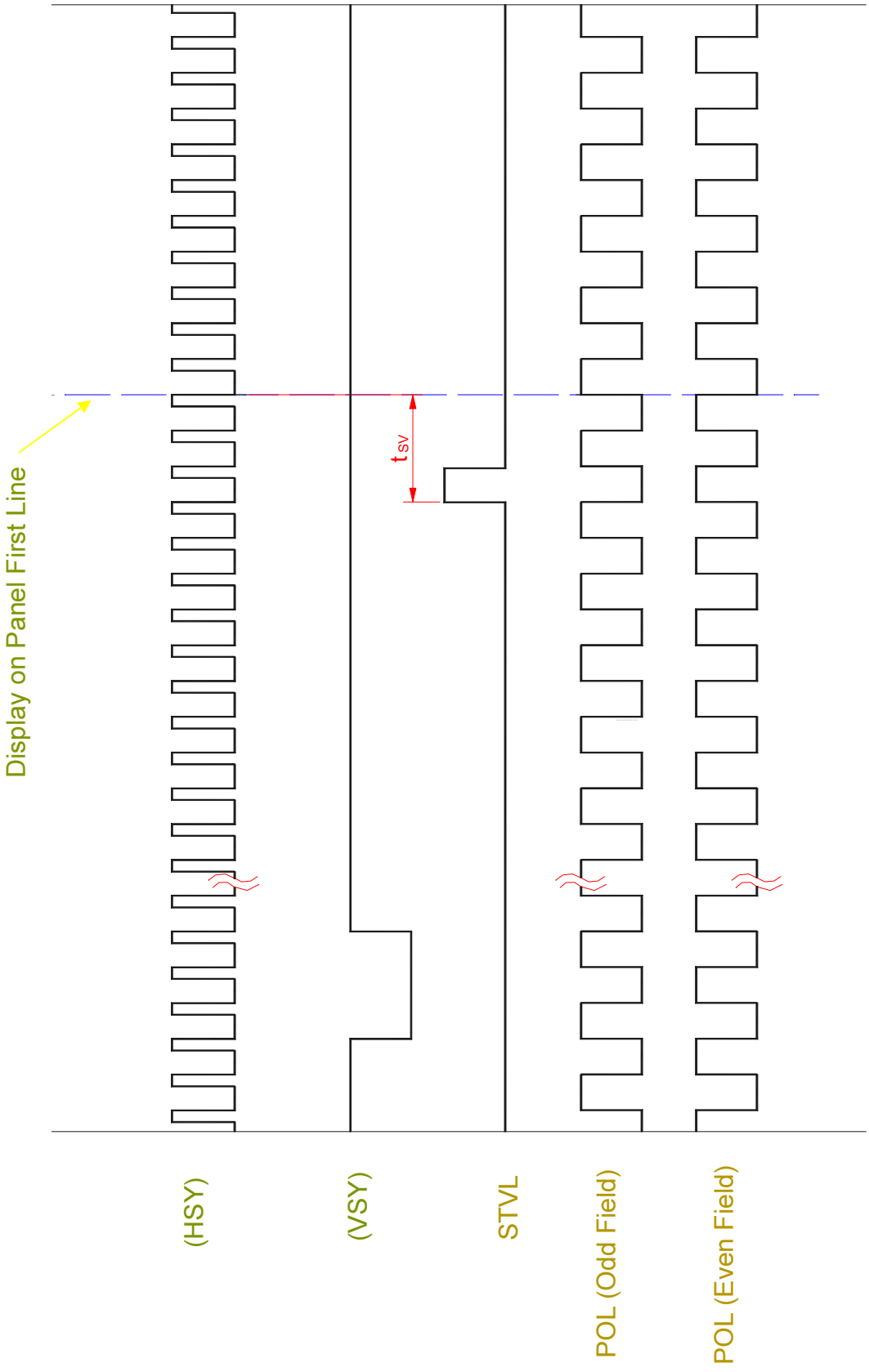
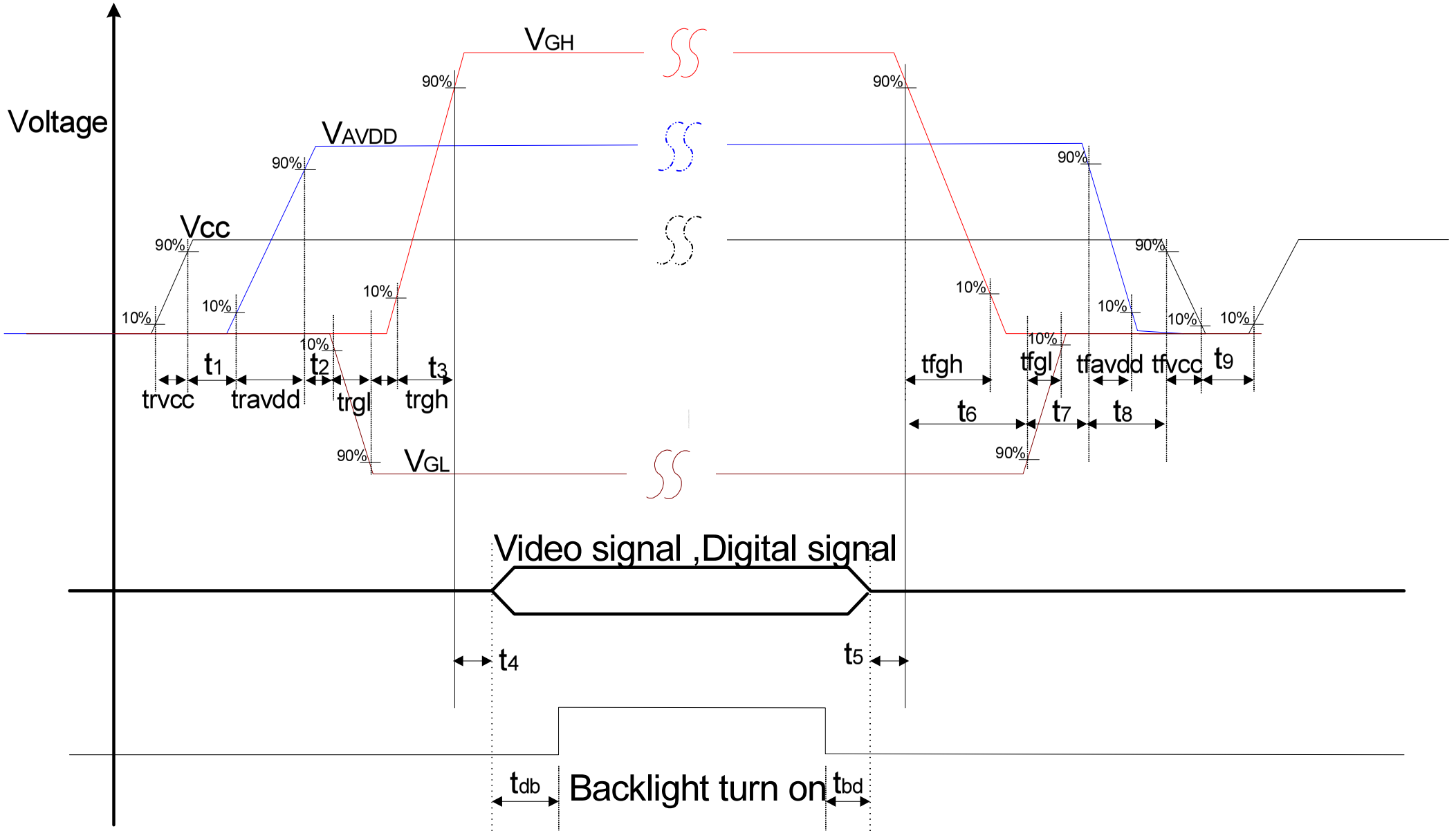
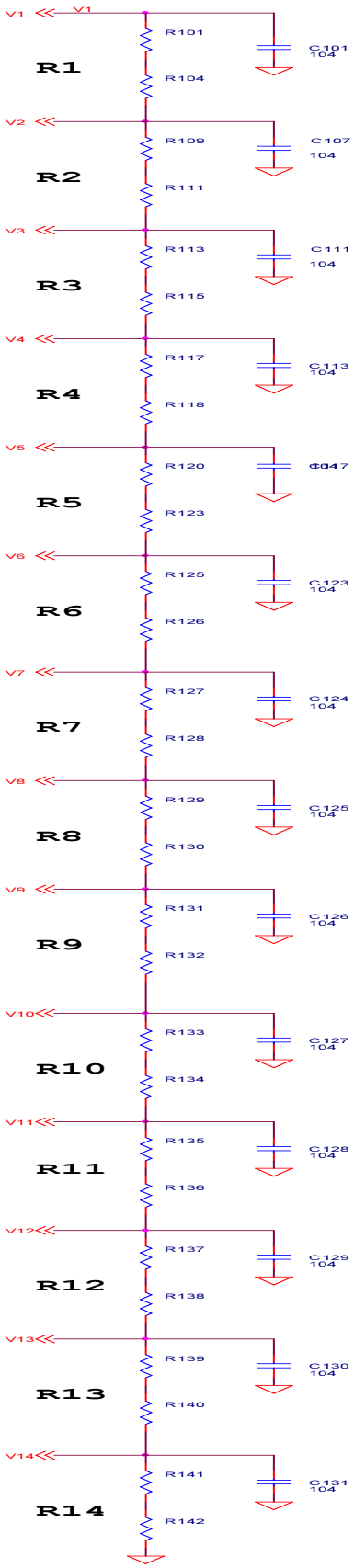


Fig.6 Vertical timing (from up to down)



trvcc≦15ms(From 10%Vcc to 90%Vcc ,when Vcc is low to high)
travdd≦15ms(From 10%Vavdd to 90%Vcc ,when Vavdd is low to high)
trgh≦15ms(From 10%Vgh to 90%Vcc ,when Vgh is low to high)
trgl≦15ms(From 10%Vgl to 90%Vcc ,when Vgl is low to high)
tfvcc≦20ms(From 90%Vcc to 10%Vcc ,when Vcc is high to low)
tfavdd≦20ms(From 90%Vavdd to 10%Vcc ,when Vavdd is high to low)
tfgh≦20ms(From 90%Vgh to 10%Vcc ,when Vgh is high to low)
tfgl≦20ms(From 90%Vgl to 10%Vcc ,when Vgl is high to low)
0≦t1≦10ms(From 90%Vcc to 10% Vavdd , when Vcc is low to high)
0≦t2≦10ms(From 90%Vavdd to 10% Vgl , when Vcc is low to high)
0≦t3≦10ms(From 90%Vgl to 10% Vgh , when Vcc is low to high)
0≦t4≦10ms(From 90%Vgh to video signal ,when Vgh is low to high)
0≦t5≦10ms(From video signal 90%Vvgh ,when Vgh is low to high)
0≦t6≦10ms(From 90%Vgh to 90% Vgl ,when Vcc is high to low)
0≦t7≦10ms(From 90%Vgl to 90% Vavdd , when Vcc is high to low)
0≦t8≦10ms(From 90%Vavdd to 90% Vcc , when Vcc is high to low)
t9≧0.4s(From 10%Vcc is H → L to 10% Vcc is L → H)
0≦tdb≦10ms(From video signal on to backlight on)
0≦tbd≦10ms(From backlight off to video signal off)

Fig.7 Power sequence



R101=14	R104=0	V18.6
R109=127	R111=0	V28.48
R113=68	R115=0	V37.32
R117=52.3	R118=0	V46.72
R120=60.4	R123=0	V56.27
R125=91	R126=0	V65.73
R127=86.6	R128=0	V75.15
R129=215	R130=0	V84.29
R131=102	R132=0	V93.35
R133=56.2	R134=0	V102.5
R135=51.1	R136=0	V112.03
R137=133	R138=0	V121.57
R139=17.8	R140=0	V130.355
R141=19.6	R142=0	V140.195

Fig.8 Reference Gamma Voltage