# ACT™ 2 Family FPGAs

## Features

- Up to 8000 Gate Array Gates (20,000 PLD equivalent gates)
- Replaces up to 200 TTL Packages
- Replaces up to eighty 20-Pin PAL® Packages
- Design Library with over 500 Macro Functions
- Single-Module Sequential Functions
- Wide-Input Combinatorial Functions
- Up to 1232 Programmable Logic Modules
- Up to 998 Flip-Flops
- Datapath Performance at 105 MHz
- 16-Bit Accumulator Performance to 39 MHz
- Two In-Circuit Diagnostic Probe Pins Support Speed Analysis to 50 MHz
- Two High-Speed, Low-Skew Clock Networks
- I/O Drive to 10 mA
- Nonvolatile, User Programmable
- Logic Fully Tested Prior to Shipment
- 1.0-micron CMOS Technology

## Product Family Profile

| Device | A1225A | A1240A | A1280A |
|---|---|---|---|
| Capacity | | | |
| Gate Array Equivalent Gates | 2,500 | 4,000 | 8,000 |
| PLD Equivalent Gates | 6,250 | 10,000 | 20,000 |
| TTL Equivalent Packages | 63 | 100 | 200 |
| 20-Pin PAL Equivalent Packages | 25 | 40 | 80 |
| Logic Modules | 451 | 684 | 1,232 |
| S-Modules | 231 | 348 | 624 |
| C-Modules | 220 | 336 | 608 |
| Flip-Flops (maximum) | 382 | 568 | 998 |
| Routing Resources | | | |
| Horizontal Tracks/Channel | 36 | 36 | 36 |
| Vertical Tracks/Channel | 15 | 15 | 15 |
| PLICE Antifuse Elements | 250,000 | 400,000 | 750,000 |
| User I/Os (maximum) | 83 | 104 | 140 |
| Packages[1] | 100 CPGA<br>100 PQFP<br>100 VQFP<br>84 PLCC | 132 CPGA<br>144 PQFP<br>176 TQFP<br>84 PLCC | 176 CPGA<br>160 PQFP<br>176 TQFP<br>84 PLCC<br>172 CQFP |
| Performance[2] | | | |
| 16-Bit Prescaled Counters | 105 MHz | 100 MHz | 85 MHz |
| 16-Bit Loadable Counters | 70 MHz | 69 MHz | 67 MHz |
| 16-Bit Accumulators | 39 MHz | 38 MHz | 36 MHz |

***Notes:***

1. *See the "Product Plan" on page 3 for package availability.*
2. *Performance is based on '–2' speed devices at commercial worst-case operating conditions using PREP Benchmarks, Suite #1, Version 1.2, dated 3-28-93, any analysis is not endorsed by PREP.*

## Description

The ACT™ 2 family represents Actel's second generation of field programmable gate arrays (FPGAs). The ACT 2 family presents a two-module architecture, consisting of C-modules and S-modules. These modules are optimized for both combinatorial and sequential designs. Based on Actel's patented channeled array architecture, the ACT 2 family provides significant enhancements to gate density and performance while maintaining downward compatibility with the ACT 1 design environment and upward compatibility with the ACT 3 design environment. The devices are implemented in silicon gate, 1.0-µm, two-level metal CMOS, and employ Actel's PLICE® antifuse technology. This revolutionary architecture offers gate array design flexibility, high performance, and fast

time-to-production with user programming. The ACT 2 family is supported by the Designer and Designer Advantage Systems, which offers automatic pin assignment, validation of electrical and design rules, automatic placement and routing, timing analysis, user programming, and diagnostic probe capabilities. The systems are supported on the following platforms: 386/486™ PC, Sun™, and HP™ workstations. The systems provide CAE interfaces to the following design environments: Cadence, Viewlogic®, Mentor Graphics®, and OrCAD™.

## Ordering Information

**A1280 A – 1 PG 176 C**

Application (Temperature Range)
- C = Commercial (0 to +70°C)
- I = Industrial (–40 to +85°C)
- M = Military (–55 to +125°C)
- B = MIL-STD-883

Package Lead Count

Package Type
- PL = Plastic J-Leaded Chip Carrier
- PQ = Plastic Quad Flat Pack
- CQ = Ceramic Quad Flat Pack
- PG = Ceramic Pin Grid Array
- TQ = Thin (1.4 mm) Quad Flat Pack
- VQ = Very Thin (1.0 mm) Quad Flat Pack

Speed Grade
- Blank = Standard Speed
- –1 = Approximately 15% faster than Standard
- –2 = Approximately 25% faster than Standard

Die Revision
- A = 1.0-µm CMOS process

Part Number
- A1225 = 2500 Gates
- A1240 = 4000 Gates
- A1280 = 8000 Gates

## Product Plan

| | Speed Grade* | | | Application | | | |
|---|---|---|---|---|---|---|---|
| | Std | –1 | –2 | C | I | M | B |
| **A1225A Device** | | | | | | | |
| 100-pin Ceramic Pin Grid Array (PG) | ✔ | ✔ | ✔ | ✔ | — | — | — |
| 100-pin Plastic Quad Flat Pack (PQ) | ✔ | ✔ | ✔ | ✔ | ✔ | — | — |
| 100-pin Very Thin (1.0 mm) Quad Flat Pack (VQ) | ✔ | ✔ | ✔ | ✔ | — | — | — |
| 84-pin Plastic Leaded Chip Carrier (PL) | ✔ | ✔ | ✔ | ✔ | ✔ | — | — |
| **A1240A Device** | | | | | | | |
| 132-pin Ceramic Pin Grid Array (PG) | ✔ | ✔ | ✔ | ✔ | — | ✔ | ✔ |
| 176-pin Thin (1.4 mm) Quad Flat Pack (TQ) | ✔ | ✔ | ✔ | ✔ | — | — | — |
| 144-pin Plastic Quad Flat Pack (PQ) | ✔ | ✔ | ✔ | ✔ | ✔ | — | — |
| 84-pin Plastic Leaded Chip Carrier (PL) | ✔ | ✔ | ✔ | ✔ | ✔ | — | — |
| **A1280A Device** | | | | | | | |
| 176-pin Ceramic Pin Grid Array (PG) | ✔ | ✔ | ✔ | ✔ | — | ✔ | ✔ |
| 176-pin Thin (1.4 mm) Quad Flat Pack (TQ) | ✔ | ✔ | ✔ | ✔ | — | — | — |
| 160-pin Plastic Quad Flat Pack (PQ) | ✔ | ✔ | ✔ | ✔ | ✔ | — | — |
| 172-pin Ceramic Quad Flat Pack (CQ) | ✔ | ✔ | ✔ | ✔ | — | ✔ | ✔ |

*Contact your Actel sales representatives for product availability.*

*Applications:* *C = Commercial* *I = Industrial* *M = Military* *B = MIL-STD-883*

*Availability:* ✔ = *Available* *P = Planned* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard*

## Device Resources

| Device Series | Logic Modules | Gates | User I/Os | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | CPGA | | | PQFP | | | PLCC | CQFP | TQFP | VQFP |
| | | | 176-pin | 132-pin | 100-pin | 160-pin | 144-pin | 100-pin | 84-pin | 172-pin | 176-pin | 100-pin |
| A1225A | 451 | 2500 | — | — | 83 | — | — | 83 | 72 | — | — | 83 |
| A1240A | 684 | 4000 | — | 104 | — | — | 104 | — | 72 | — | 104 | — |
| A1280A | 1232 | 8000 | 140 | — | — | 125 | — | — | 72 | 140 | 140 | — |

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## Operating Conditions

### Absolute Maximum Ratings[1]

**Free air temperature range**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | –0.5 to +7.0 | V |
| $V_I$ | Input Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $V_O$ | Output Voltage | –0.5 to $V_{CC}$ +0.5 | V |
| $I_{IO}$ | I/O Source/Sink Current[2] | ±20 | mA |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |

***Notes:***

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than $V_{CC}$ + 0.5 V or less than GND – 0.5 V, the internal protection diode will be forward biased and can draw excessive current.*

### Recommended Operating Conditions

| Parameter | Commercial | Industrial | Military | Units |
|---|---|---|---|---|
| Temperature Range[1] | 0 to +70 | –40 to +85 | –55 to +125 | °C |
| Power Supply Tolerance | ±5 | ±10 | ±10 | %$V_{CC}$ |

***Note:***

1. *Ambient temperature ($T_A$) is used for commercial and industrial; case temperature ($T_C$) is used for military.*

### Electrical Specifications

| Symbol | Parameter | Commercial | | Industrial | | Military | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| $V_{OH}$[1] | ($I_{OH}$ = –10 mA)[2] | 2.4 | | | | | | V |
| | ($I_{OH}$ = –6 mA) | 3.84 | | | | | | V |
| | ($I_{OH}$ = –4 mA) | | | 3.7 | | 3.7 | | V |
| $V_{OL}$[1] | ($I_{OL}$ = 10 mA)[2] | | 0.5 | | | | | V |
| | ($I_{OL}$ = 6 mA) | | 0.33 | | 0.40 | | 0.40 | V |
| $V_{IL}$ | | –0.3 | 0.8 | –0.3 | 0.8 | –0.3 | 0.8 | V |
| $V_{IH}$ | | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | 2.0 | $V_{CC}$ + 0.3 | V |
| Input Transition Time $t_R$, $t_F$[2] | | | 500 | | 500 | | 500 | ns |
| $C_{IO}$ I/O Capacitance[2, 3] | | | 10 | | 10 | | 10 | pF |
| Standby Current, $I_{CC}$[4] (typical = 1 mA) | | | 2 | | 10 | | 20 | mA |
| Leakage Current[5] | | –10 | 10 | –10 | 10 | –10 | 10 | µA |

***Notes:***

1. *Only one output tested at a time. $V_{CC}$ = min.*
2. *Not tested, for information only.*
3. *Includes worst-case 176 CPGA package capacitance. $V_{OUT}$ = 0 V, f = 1 MHz.*
4. *All outputs unloaded. All inputs = $V_{CC}$ or GND, typical $I_{CC}$ = 1 mA. $I_{CC}$ limit includes $I_{PP}$ and $I_{SV}$ during normal operation.*
5. *$V_{OUT}$, $V_{IN}$ = $V_{CC}$ or GND.*

## Package Thermal Characteristics

The device junction to case thermal characteristic is θjc, and the junction to ambient air characteristic is θja. The thermal characteristics for θja are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta ja\ (°C/W)} = \frac{150°C - 70°C}{33°C/W} = 2.4\ W$$

| Package Type | Pin Count | θjc | θja Still Air | θja 300 ft/min | Units |
|---|---|---|---|---|---|
| Ceramic Pin Grid Array | 100 | 5 | 35 | 17 | °C/W |
| | 132 | 5 | 30 | 15 | °C/W |
| | 176 | 8 | 23 | 12 | °C/W |
| Ceramic Quad Flat Pack | 172 | 8 | 25 | 15 | °C/W |
| Plastic Quad Flat Pack[1] | 100 | 13 | 48 | 40 | °C/W |
| | 144 | 15 | 40 | 32 | °C/W |
| | 160 | 15 | 38 | 30 | °C/W |
| Plastic Leaded Chip Carrier[2] | 84 | 12 | 37 | 28 | °C/W |
| Very Thin Quad Flat Pack[3] | 100 | 12 | 43 | 35 | °C/W |
| Thin Quad Flat Pack[4] | 176 | 15 | 32 | 25 | °C/W |

***Notes:(Maximum Power in Still Air)***

1. *Maximum Power Dissipation for PQFP packages are 1.9 Watts (100-pin), 2.3 Watts (144-pin), and 2.4 Watts (160-pin).*
2. *Maximum Power Dissipation for PLCC packages is 2.7 Watts.*
3. *Maximum Power Dissipation for VQFP packages is 2.3 Watts.*
4. *Maximum Power Dissipation for TQFP packages is 3.1 Watts.*

## Power Dissipation

$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$

Where:

$I_{CC}$ standby is the current flowing when no inputs or outputs are changing.

$I_{CC}$ active is the current flowing due to CMOS switching.

$I_{OL}$, $I_{OH}$ are TTL sink/source currents.

$V_{OL}$, $V_{OH}$ are TTL level output voltages.

N equals the number of outputs driving TTL loads to $V_{OL}$.

M equals the number of outputs driving TTL loads to $V_{OH}$.

An accurate determination of N and M is problematical because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

### Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial, worst case conditions.

| $I_{CC}$ | $V_{CC}$ | Power |
|---|---|---|
| 2 mA | 5.25V | 10.5 mW |

The static power dissipated by TTL loads depends on the number of outputs driving high or low and the DC load current. Again, this value is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33 V will generate 42 mW with all outputs driving low, and 140 mW with all outputs driving high. The actual dissipation will average somewhere between as I/Os switch states with time.

### Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces

and load device inputs. An additional component of the active power dissipation is the totem-pole current in CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

### Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by the Equation 1.

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

Where:

$C_{EQ}$ is the equivalent capacitance expressed in pF.

$V_{CC}$ is the power supply in volts.

F is the switching frequency in MHz.

Equivalent capacitance is calculated by measuring ICC active at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency independent so that the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

### $C_{EQ}$ Values for Actel FPGAs

| | |
|---|---|
| Modules ($C_{EQM}$) | 5.8 |
| Input Buffers ($C_{EQI}$) | 12.9 |
| Output Buffers ($C_{EQO}$) | 23.8 |
| Routed Array Clock Buffer Loads ($C_{EQCR}$) | 3.9 |

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m * C_{EQM} * f_m)_{modules} + (n * C_{EQI} * f_n)_{inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2}] \quad (2)$$

Where:

| | | |
|---|---|---|
| m | = | Number of logic modules switching at fm |
| n | = | Number of input buffers switching at fn |
| p | = | Number of output buffers switching at fp |
| q1 | = | Number of clock loads on the first routed array clock |
| q2 | = | Number of clock loads on the second routed array clock |
| $r_1$ | = | Fixed capacitance due to first routed array clock |
| $r_2$ | = | Fixed capacitance due to second routed array clock |
| $C_{EQM}$ | = | Equivalent capacitance of logic modules in pF |
| $C_{EQI}$ | = | Equivalent capacitance of input buffers in pF |
| $C_{EQO}$ | = | Equivalent capacitance of output buffers in pF |
| $C_{EQCR}$ | = | Equivalent capacitance of routed array clock in pF |
| $C_L$ | = | Output lead capacitance in pF |
| $f_m$ | = | Average logic module switching rate in MHz |
| $f_n$ | = | Average input buffer switching rate in MHz |
| $f_p$ | = | Average output buffer switching rate in MHz |
| $f_{q1}$ | = | Average first routed array clock rate in MHz |
| $f_{q2}$ | = | Average second routed array clock rate in MHz |

### Fixed Capacitance Values for Actel FPGAs (pF)

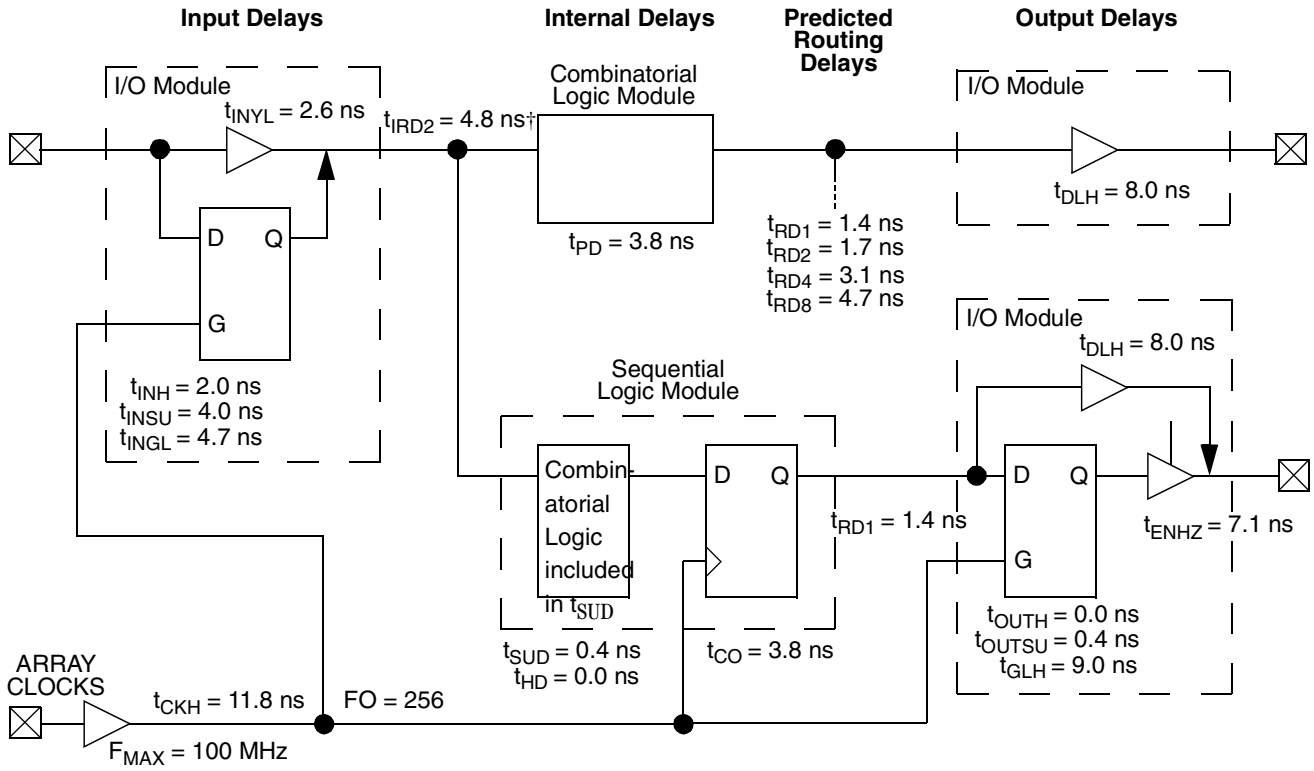
| Device Type | r1 routed_Clk1 | r2 routed_Clk2 |
|---|---|---|
| A1225A | 106 | 106.0 |
| A1240A | 134 | 134.2 |
| A1280A | 168 | 167.8 |

### Determining Average Switching Frequency

To determine the switching frequency for a design, you must have a detailed understanding of the data input values to the circuit. The following guidelines are meant to represent worst-case scenarios so that they can be generally used to predict the upper limits of power dissipation. These guidelines are as follows:

| | |
|---|---|
| Logic Modules (m) | 80% of modules |
| Inputs switching (n) | # inputs/4 |
| Outputs switching (p) | # outputs/4 |
| First routed array clock loads ($q_1$) | 40%of sequential modules |
| Second routed array clock loads ($q_2$) | 40%of sequential modules |
| Load capacitance ($C_L$) | 35 pF |
| Average logic module switching rate ($f_m$) | F/10 |
| Average input switching rate ($f_n$) | F/5 |
| Average output switching rate ($f_p$) | F/10 |
| Average first routed array clock rate ($f_{q1}$) | F |
| Average second routed array clock rate ($f_{q2}$) | F/2 |

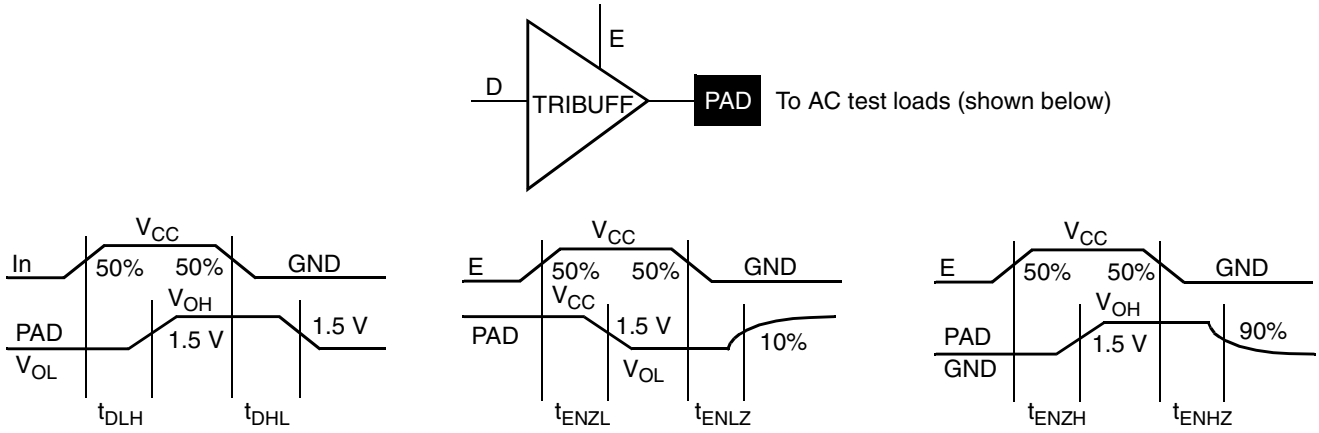
## ACT 2 Timing Model*




**Values shown for A1240A-2 at worst-case commercial conditions.* *† Input Module Predicted Routing Delay*

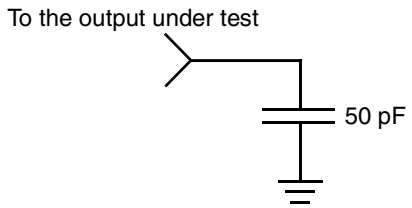
## Parameter Measurement

### Output Buffer Delays

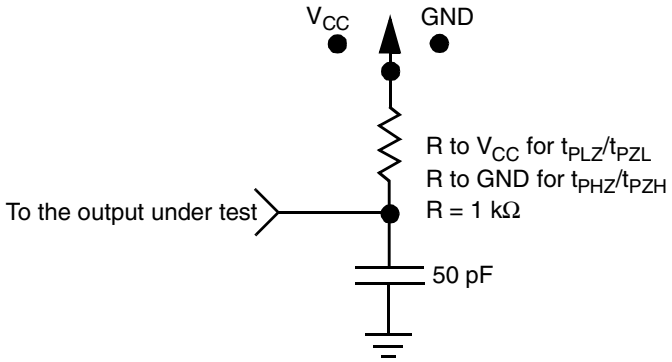



### AC Test Loads

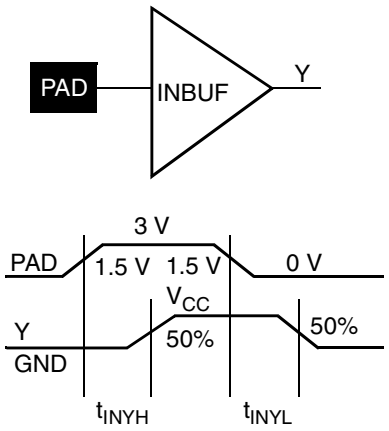
**Load 1**
**(Used to measure propagation delay)**



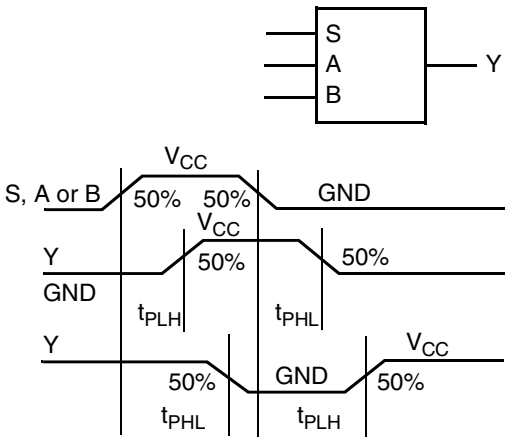

**Load 2**
**(Used to measure rising/falling edges)**




### Input Buffer Delays

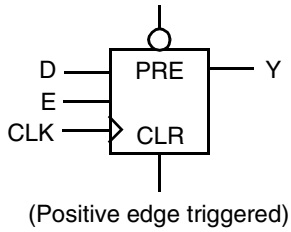



### Module Delays

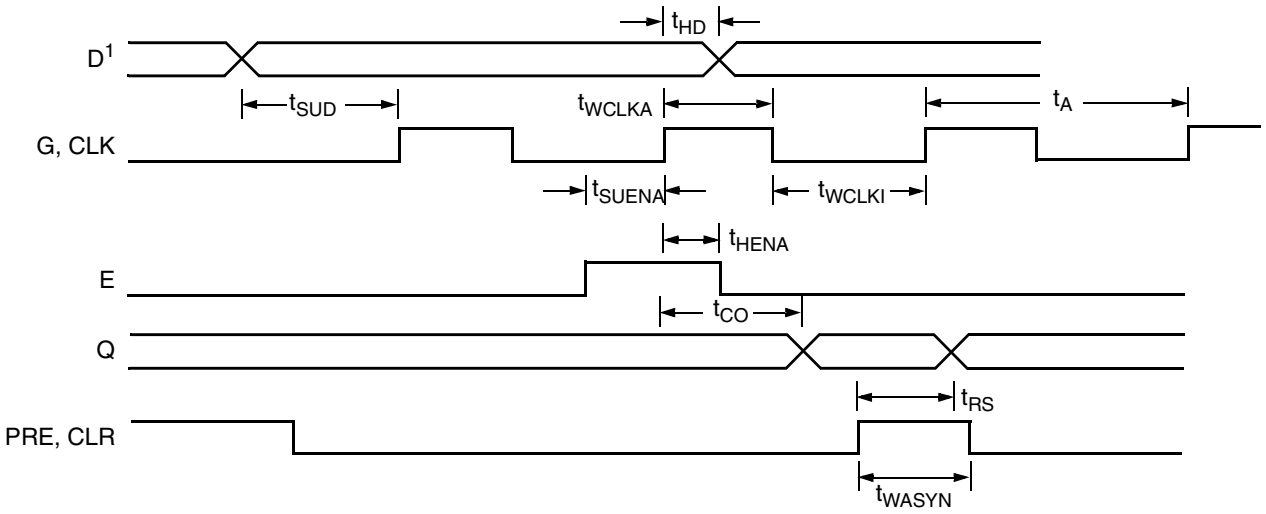


## Sequential Module Timing Characteristics

### Flip-Flops and Latches



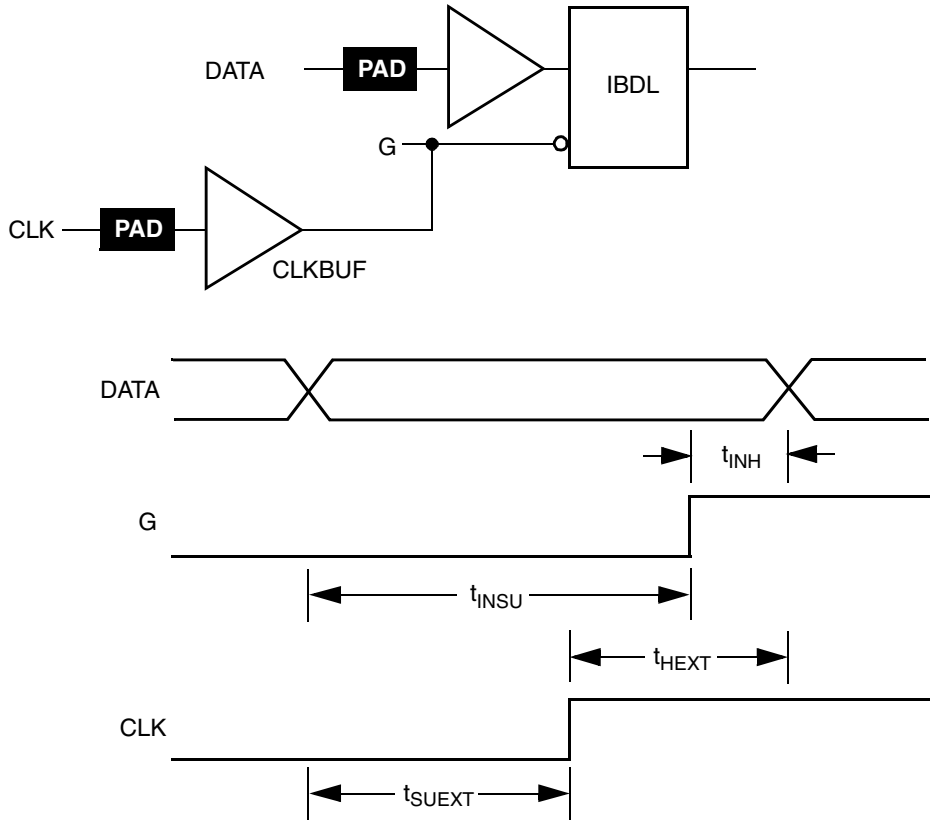

(Positive edge triggered)



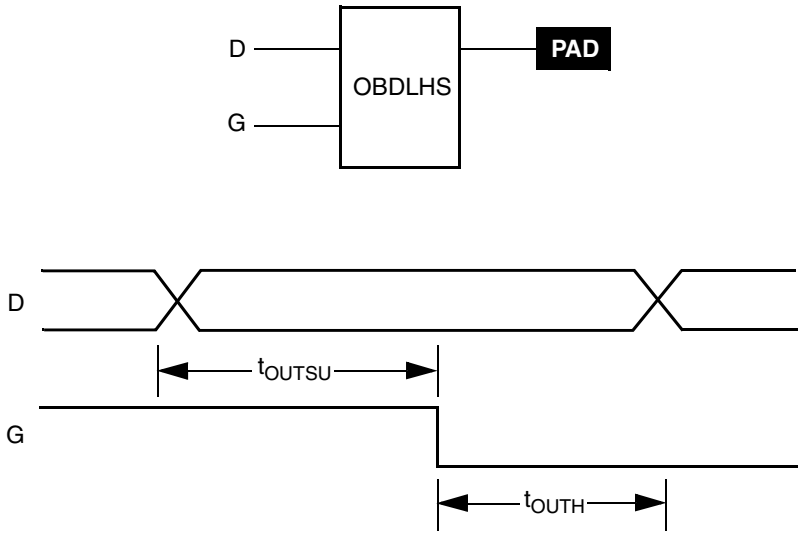

***Note:*** *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

## Sequential Timing Characteristics (continued)

### Input Buffer Latches




### Output Buffer Latches



## Timing Derating Factor (Temperature and Voltage)

| | Industrial | | Military | |
|---|---|---|---|---|
| | Min. | Max. | Min. | Max. |
| (Commercial Minimum/Maximum Specification) x | 0.69 | 1.11 | 0.67 | 1.23 |

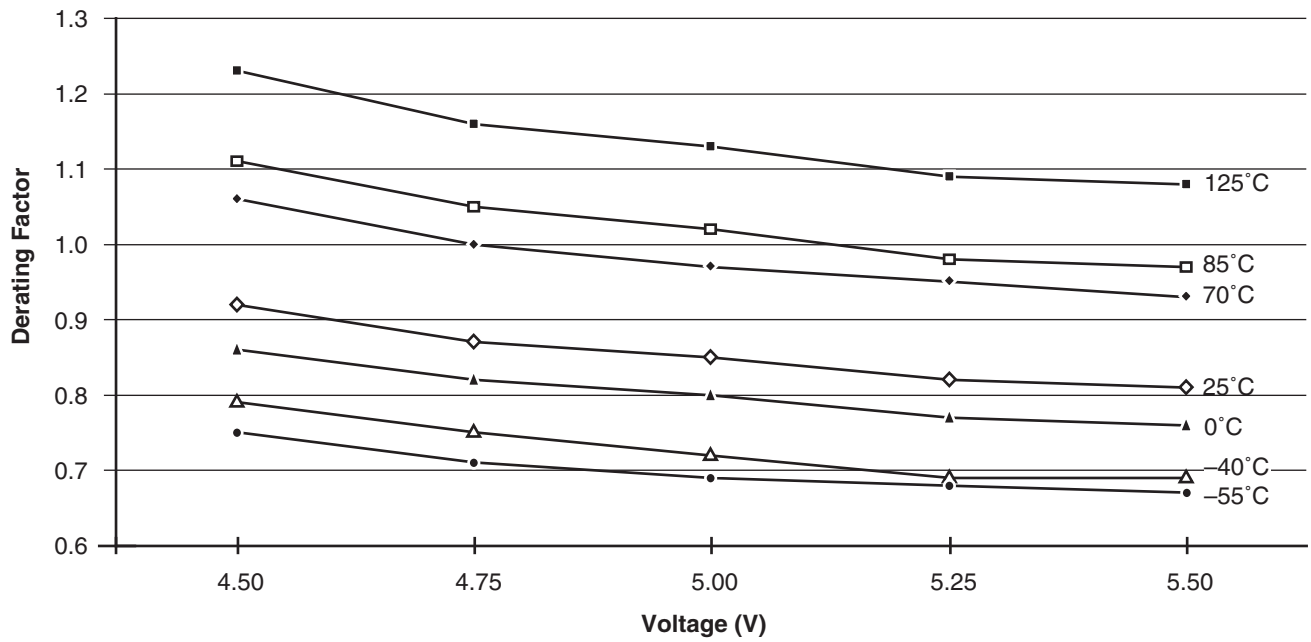
## Timing Derating Factor for Designs at Typical Temperature ($T_J$ = 25°C) and Voltage (5.0 V)

| | |
|---|---|
| (Commercial Maximum Specification) x | 0.85 |

## Temperature and Voltage Derating Factors (normalized to Worst-Case Commercial, $T_J$ = 4.75 V, 70°C)

| | –55 | –40 | 0 | 25 | 70 | 85 | 125 |
|---|---|---|---|---|---|---|---|
| **4.50** | 0.75 | 0.79 | 0.86 | 0.92 | 1.06 | 1.11 | 1.23 |
| **4.75** | 0.71 | 0.75 | 0.82 | 0.87 | 1.00 | 1.05 | 1.16 |
| **5.00** | 0.69 | 0.72 | 0.80 | 0.85 | 0.97 | 1.02 | 1.13 |
| **5.25** | 0.68 | 0.69 | 0.77 | 0.82 | 0.95 | 0.98 | 1.09 |
| **5.50** | 0.67 | 0.69 | 0.76 | 0.81 | 0.93 | 0.97 | 1.08 |

**Junction Temperature and Voltage Derating Curves (normalized to Worst-Case Commercial, $T_J$ = 4.75V, 70°C)**




*Note: This derating factor applies to all routing and propagation delays.*

## A1225A Timing Characteristics

**(Worst-Case Commercial Conditions, $V_{CC}$ = 4.75 V, $T_J$ = 70°C)**

| Logic Module Propagation Delays[1] | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{PD1}$ | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{GO}$ | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | |
| $t_{RD1}$ | FO=1 Routing Delay | | 1.1 | | 1.2 | | 1.4 | ns |
| $t_{RD2}$ | FO=2 Routing Delay | | 1.7 | | 1.9 | | 2.2 | ns |
| $t_{RD3}$ | FO=3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| $t_{RD4}$ | FO=4 Routing Delay | | 2.8 | | 3.1 | | 3.7 | ns |
| $t_{RD8}$ | FO=8 Routing Delay | | 4.4 | | 4.9 | | 5.8 | ns |
| **Sequential Timing Characteristics[3,4]** | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5 | | 5.0 | | 6.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 9.4 | | 11.0 | | 13.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 105.0 | | 90.0 | | 75.0 | MHz |

*Notes:*

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

## A1225A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Input Module Propagation Delays | | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{INYH}$ | Pad to Y High | | | 2.9 | | 3.3 | | 3.8 | ns |
| $t_{INYL}$ | Pad to Y Low | | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{INGH}$ | G to Y High | | | 5.0 | | 5.7 | | 6.6 | ns |
| $t_{INGL}$ | G to Y Low | | | 4.7 | | 5.4 | | 6.3 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | |
| $t_{IRD1}$ | FO=1 Routing Delay | | | 4.1 | | 4.6 | | 5.4 | ns |
| $t_{IRD2}$ | FO=2 Routing Delay | | | 4.6 | | 5.2 | | 6.1 | ns |
| $t_{IRD3}$ | FO=3 Routing Delay | | | 5.3 | | 6.0 | | 7.1 | ns |
| $t_{IRD4}$ | FO=4 Routing Delay | | | 5.7 | | 6.4 | | 7.6 | ns |
| $t_{IRD8}$ | FO=8 Routing Delay | | | 7.4 | | 8.3 | | 9.8 | ns |
| **Global Clock Network** | | | | | | | | | |
| $t_{CKH}$ | Input Low to High | FO = 32<br>FO = 256 | | 10.2<br>11.8 | | 11.0<br>13.0 | | 12.8<br>15.7 | ns |
| $t_{CKL}$ | Input High to Low | FO = 32<br>FO = 256 | | 10.2<br>12.0 | | 11.0<br>13.2 | | 12.8<br>15.9 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | FO = 32<br>FO = 256 | 3.4<br>3.8 | | 4.1<br>4.5 | | 4.5<br>5.0 | | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | FO = 32<br>FO = 256 | 3.4<br>3.8 | | 4.1<br>4.5 | | 4.5<br>5.0 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32<br>FO = 256 | | 0.7<br>3.5 | | 0.7<br>3.5 | | 0.7<br>3.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup | FO = 32<br>FO = 256 | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32<br>FO = 256 | 7.0<br>11.2 | | 7.0<br>11.2 | | 7.0<br>11.2 | | ns |
| $t_P$ | Minimum Period | FO = 32<br>FO = 256 | 7.7<br>8.1 | | 8.3<br>8.8 | | 9.1<br>10.0 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32<br>FO = 256 | | 130.0<br>125.0 | | 120.0<br>115.0 | | 110.0<br>100.0 | MHz |

***Note:***

1. *These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1225A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Output Module Timing | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 8.0 | | 9.0 | | 10.6 | ns |
| $t_{DHL}$ | Data to Pad Low | | 10.1 | | 11.4 | | 13.4 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.6 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.3 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 8.9 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| **CMOS Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 10.1 | | 11.5 | | 13.5 | ns |
| $t_{DHL}$ | Data to Pad Low | | 8.4 | | 9.6 | | 11.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.6 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.3 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 8.9 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

*Note:*

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at http://www.actel.com/support/appnotes/appnotes_design.html#board.*

## A1240A Timing Characteristics

**(Worst-Case Commercial Conditions, $V_{CC}$ = 4.75 V, $T_J$ = 70°C)**

| Logic Module Propagation Delays[1] | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{PD1}$ | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{GO}$ | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | |
| $t_{RD1}$ | FO=1 Routing Delay | | 1.4 | | 1.5 | | 1.8 | ns |
| $t_{RD2}$ | FO=2 Routing Delay | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{RD3}$ | FO=3 Routing Delay | | 2.3 | | 2.6 | | 3.0 | ns |
| $t_{RD4}$ | FO=4 Routing Delay | | 3.1 | | 3.5 | | 4.1 | ns |
| $t_{RD8}$ | FO=8 Routing Delay | | 4.7 | | 5.4 | | 6.3 | ns |
| **Sequential Timing Characteristics[3, 4]** | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 4.5 | | 6.0 | | 6.5 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 9.8 | | 12.0 | | 15.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 100.0 | | 80.0 | | 66.0 | MHz |

***Notes:***

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

## A1240A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Input Module Propagation Delays | | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{INYH}$ | Pad to Y High | | | 2.9 | | 3.3 | | 3.8 | ns |
| $t_{INYL}$ | Pad to Y Low | | | 2.6 | | 3.0 | | 3.5 | ns |
| $t_{INGH}$ | G to Y High | | | 5.0 | | 5.7 | | 6.6 | ns |
| $t_{INGL}$ | G to Y Low | | | 4.7 | | 5.4 | | 6.3 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | |
| $t_{IRD1}$ | FO=1 Routing Delay | | | 4.2 | | 4.8 | | 5.6 | ns |
| $t_{IRD2}$ | FO=2 Routing Delay | | | 4.8 | | 5.4 | | 6.4 | ns |
| $t_{IRD3}$ | FO=3 Routing Delay | | | 5.4 | | 6.1 | | 7.2 | ns |
| $t_{IRD4}$ | FO=4 Routing Delay | | | 5.9 | | 6.7 | | 7.9 | ns |
| $t_{IRD8}$ | FO=8 Routing Delay | | | 7.9 | | 8.9 | | 10.5 | ns |
| **Global Clock Network** | | | | | | | | | |
| $t_{CKH}$ | Input Low to High | FO = 32<br>FO = 256 | | 10.2<br>11.8 | | 11.0<br>13.0 | | 12.8<br>15.7 | ns |
| $t_{CKL}$ | Input High to Low | FO = 32<br>FO = 256 | | 10.2<br>12.0 | | 11.0<br>13.2 | | 12.8<br>15.9 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | FO = 32<br>FO = 256 | 3.8<br>4.1 | | 4.5<br>5.0 | | 5.5<br>5.8 | | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | FO = 32<br>FO = 256 | 3.8<br>4.1 | | 4.5<br>5.0 | | 5.5<br>5.8 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32<br>FO = 256 | | 0.5<br>2.5 | | 0.5<br>2.5 | | 0.5<br>2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup | FO = 32<br>FO = 256 | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32<br>FO = 256 | 7.0<br>11.2 | | 7.0<br>11.2 | | 7.0<br>11.2 | | ns |
| $t_P$ | Minimum Period | FO = 32<br>FO = 256 | 8.1<br>8.8 | | 9.1<br>10.0 | | 11.1<br>11.7 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32<br>FO = 256 | | 125.0<br>115.0 | | 110.0<br>100.0 | | 90.0<br>85.0 | MHz |

*Note:*

*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1240A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Output Module Timing | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 8.0 | | 9.0 | | 10.6 | ns |
| $t_{DHL}$ | Data to Pad Low | | 10.1 | | 11.4 | | 13.4 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| **CMOS Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 10.2 | | 11.5 | | 13.5 | ns |
| $t_{DHL}$ | Data to Pad Low | | 8.4 | | 9.6 | | 11.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 8.9 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.7 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.2 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

***Note:***

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at http://www.actel.com/support/appnotes/appnotes_design.html#board.*

## A1280A Timing Characteristics

**(Worst-Case Commercial Conditions, $V_{CC}$ = 4.75 V, $T_J$ = 70°C)**

| Logic Module Propagation Delays[1] | | ‘–2’ Speed | | ‘–1’ Speed | | ‘Std’ Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{PD1}$ | Single Module | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{CO}$ | Sequential Clk to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{GO}$ | Latch G to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| $t_{RS}$ | Flip-Flop (Latch) Reset to Q | | 3.8 | | 4.3 | | 5.0 | ns |
| **Predicted Routing Delays[2]** | | | | | | | | |
| $t_{RD1}$ | FO=1 Routing Delay | | 1.7 | | 2.0 | | 2.3 | ns |
| $t_{RD2}$ | FO=2 Routing Delay | | 2.5 | | 2.8 | | 3.3 | ns |
| $t_{RD3}$ | FO=3 Routing Delay | | 3.0 | | 3.4 | | 4.0 | ns |
| $t_{RD4}$ | FO=4 Routing Delay | | 3.7 | | 4.2 | | 4.9 | ns |
| $t_{RD8}$ | FO=8 Routing Delay | | 6.7 | | 7.5 | | 8.8 | ns |
| **Sequential Timing Characteristics[3,4]** | | | | | | | | |
| $t_{SUD}$ | Flip-Flop (Latch) Data Input Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{HD}$ | Flip-Flop (Latch) Data Input Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{SUENA}$ | Flip-Flop (Latch) Enable Setup | 0.8 | | 0.9 | | 1.0 | | ns |
| $t_{HENA}$ | Flip-Flop (Latch) Enable Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{WCLKA}$ | Flip-Flop (Latch) Clock Active Pulse Width | 5.5 | | 6.0 | | 7.0 | | ns |
| $t_{WASYN}$ | Flip-Flop (Latch) Asynchronous Pulse Width | 5.5 | | 6.0 | | 7.0 | | ns |
| $t_A$ | Flip-Flop Clock Input Period | 11.7 | | 13.3 | | 18.0 | | ns |
| $t_{INH}$ | Input Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{INSU}$ | Input Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $t_{OUTH}$ | Output Buffer Latch Hold | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTSU}$ | Output Buffer Latch Setup | 0.4 | | 0.4 | | 0.5 | | ns |
| $f_{MAX}$ | Flip-Flop (Latch) Clock Frequency | | 85.0 | | 75.0 | | 50.0 | MHz |

***Notes:***

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Setup and hold timing parameters for the Input Buffer Latch are defined with respect to the PAD and the D input. External setup/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal setup (hold) time.*

## A1280A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Input Module Propagation Delays | | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| $t_{INYH}$ | Pad to Y High | | | 2.9 | | 3.3 | | 3.8 | ns |
| $t_{INYL}$ | Pad to Y Low | | | 2.7 | | 3.0 | | 3.5 | ns |
| $t_{INGH}$ | G to Y High | | | 5.0 | | 5.7 | | 6.6 | ns |
| $t_{INGL}$ | G to Y Low | | | 4.8 | | 5.4 | | 6.3 | ns |
| **Input Module Predicted Routing Delays[1]** | | | | | | | | | |
| $t_{IRD1}$ | FO=1 Routing Delay | | | 4.6 | | 5.1 | | 6.0 | ns |
| $t_{IRD2}$ | FO=2 Routing Delay | | | 5.2 | | 5.9 | | 6.9 | ns |
| $t_{IRD3}$ | FO=3 Routing Delay | | | 5.6 | | 6.3 | | 7.4 | ns |
| $t_{IRD4}$ | FO=4 Routing Delay | | | 6.5 | | 7.3 | | 8.6 | ns |
| $t_{IRD8}$ | FO=8 Routing Delay | | | 9.4 | | 10.5 | | 12.4 | ns |
| **Global Clock Network** | | | | | | | | | |
| $t_{CKH}$ | Input Low to High | FO = 32<br>FO = 384 | | 10.2<br>13.1 | | 11.0<br>14.6 | | 12.8<br>17.2 | ns |
| $t_{CKL}$ | Input High to Low | FO = 32<br>FO = 384 | | 10.2<br>13.3 | | 11.0<br>14.9 | | 12.8<br>17.5 | ns |
| $t_{PWH}$ | Minimum Pulse Width High | FO = 32<br>FO = 384 | 5.0<br>5.8 | | 5.5<br>6.4 | | 6.6<br>7.6 | | ns |
| $t_{PWL}$ | Minimum Pulse Width Low | FO = 32<br>FO = 384 | 5.0<br>5.8 | | 5.5<br>6.4 | | 6.6<br>7.6 | | ns |
| $t_{CKSW}$ | Maximum Skew | FO = 32<br>FO = 384 | | 0.5<br>2.5 | | 0.5<br>2.5 | | 0.5<br>2.5 | ns |
| $t_{SUEXT}$ | Input Latch External Setup | FO = 32<br>FO = 384 | 0.0<br>0.0 | | 0.0<br>0.0 | | 0.0<br>0.0 | | ns |
| $t_{HEXT}$ | Input Latch External Hold | FO = 32<br>FO = 384 | 7.0<br>11.2 | | 7.0<br>11.2 | | 7.0<br>11.2 | | ns |
| $t_P$ | Minimum Period | FO = 32<br>FO = 384 | 9.6<br>10.6 | | 11.2<br>12.6 | | 13.3<br>15.3 | | ns |
| $f_{MAX}$ | Maximum Frequency | FO = 32<br>FO = 384 | | 105.0<br>95.0 | | 90.0<br>80.0 | | 75.0<br>65.0 | MHz |

*Note:*

*These parameters should be used for estimating device performance. Optimization techniques may further reduce delays by 0 to 4 ns. Routing delays are for typical designs across worst-case operating conditions. Post-route timing analysis or simulation is required to determine actual worst-case performance. Post-route timing is based on actual routing delay measurements performed on the device prior to shipment.*

## A1280A Timing Characteristics (continued)

**(Worst-Case Commercial Conditions)**

| Output Module Timing | | '–2' Speed | | '–1' Speed | | 'Std' Speed | | |
|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min.** | **Max.** | **Min.** | **Max.** | **Min.** | **Max.** | **Units** |
| **TTL Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 8.1 | | 9.0 | | 10.6 | ns |
| $t_{DHL}$ | Data to Pad Low | | 10.2 | | 11.4 | | 13.4 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.07 | | 0.08 | | 0.09 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| **CMOS Output Module Timing[1]** | | | | | | | | |
| $t_{DLH}$ | Data to Pad High | | 10.3 | | 11.5 | | 13.5 | ns |
| $t_{DHL}$ | Data to Pad Low | | 8.5 | | 9.6 | | 11.2 | ns |
| $t_{ENZH}$ | Enable Pad Z to High | | 9.0 | | 10.0 | | 11.8 | ns |
| $t_{ENZL}$ | Enable Pad Z to Low | | 11.8 | | 13.2 | | 15.5 | ns |
| $t_{ENHZ}$ | Enable Pad High to Z | | 7.1 | | 8.0 | | 9.4 | ns |
| $t_{ENLZ}$ | Enable Pad Low to Z | | 8.4 | | 9.5 | | 11.1 | ns |
| $t_{GLH}$ | G to Pad High | | 9.0 | | 10.2 | | 11.9 | ns |
| $t_{GHL}$ | G to Pad Low | | 11.3 | | 12.7 | | 14.9 | ns |
| $d_{TLH}$ | Delta Low to High | | 0.12 | | 0.13 | | 0.16 | ns/pF |
| $d_{THL}$ | Delta High to Low | | 0.09 | | 0.10 | | 0.12 | ns/pF |

*Note:*

1. *Delays based on 50 pF loading.*
2. *SSO information can be found at http://www.actel.com/support/appnotes/appnotes_design.html#board.*

## Pin Description

**CLKA Clock A (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**CLKB Clock B (Input)**

TTL Clock input for clock distribution networks. The Clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

**DCLK Diagnostic Clock (Input)**

TTL Clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**GND Ground**

LOW supply voltage.

**I/O Input/Output (Input, Output)**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the ALS software.

**MODE Mode (Input)**

The MODE pin controls the use of multifunction pins (DCLK, PRA, PRB, SDI). When the MODE pin is HIGH, the special functions are active. When the MODE pin is LOW, the pins function as I/Os. To provide Actionprobe capability, the MODE pin should be terminated to GND through a 10K resistor so that the MODE pin can be pulled high when required.

**NC No Connection**

This pin is not connected to circuitry within the device.

**PRA Probe A (Output)**

The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**PRB Probe B (Output)**

The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**SDI Serial Data Input (Input)**

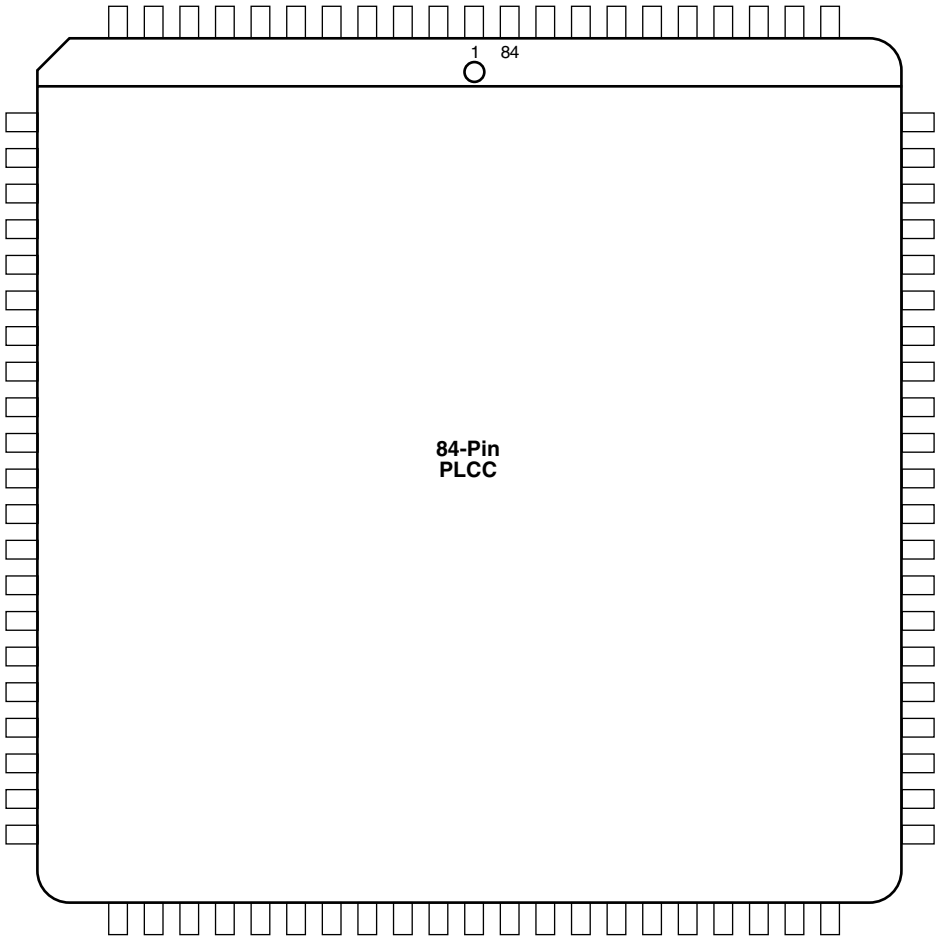
Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

**$V_{CC}$ 5.0V Supply Voltage**

HIGH supply voltage.

## Package Pin Assignments

### 84-Pin PLCC



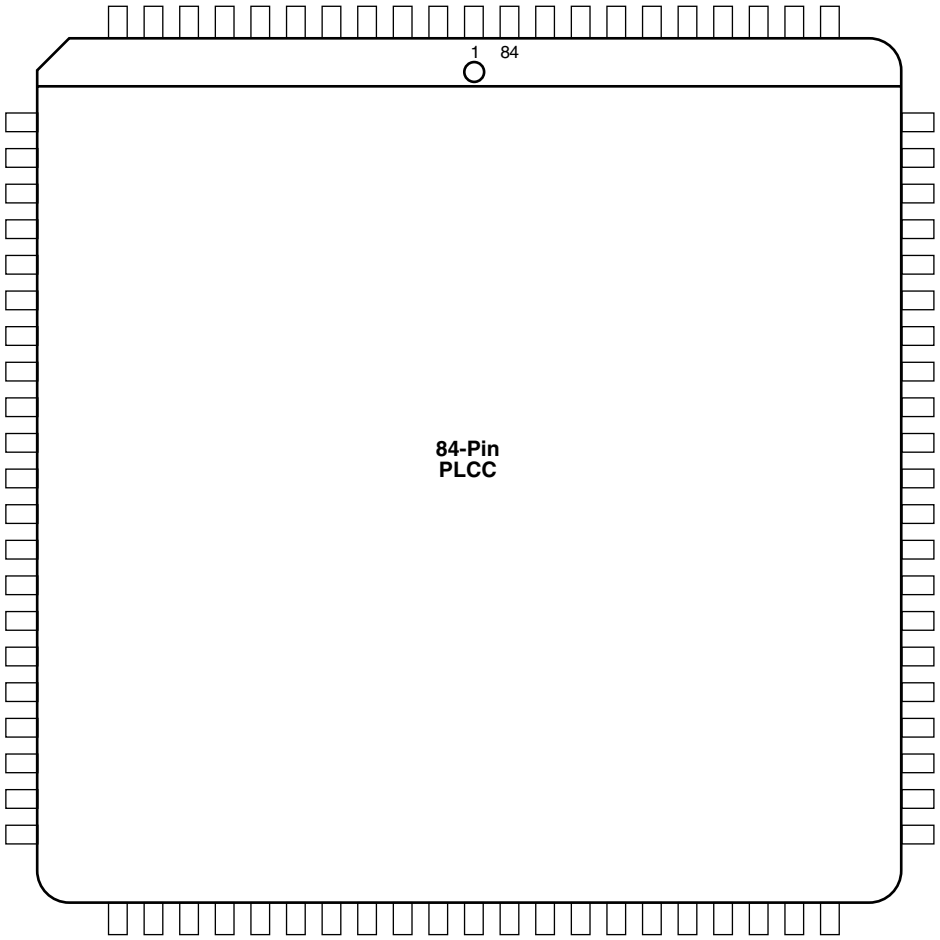

| Signal | A1225A Function | A1240A Function | A1280A Function |
|---|---|---|---|
| 2 | CLKB, I/O | CLKB, I/O | CLKB, I/O |
| 4 | PRB, I/O | PRB, I/O | PRB, I/O |
| 6 | GND | GND | GND |
| 10 | DCLK, I/O | DCLK, I/O | DCLK, I/O |
| 12 | MODE | MODE | MODE |
| 22 | VCC | VCC | VCC |
| 23 | VCC | VCC | VCC |
| 28 | GND | GND | GND |

***Notes:***

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments

### 84-Pin PLCC



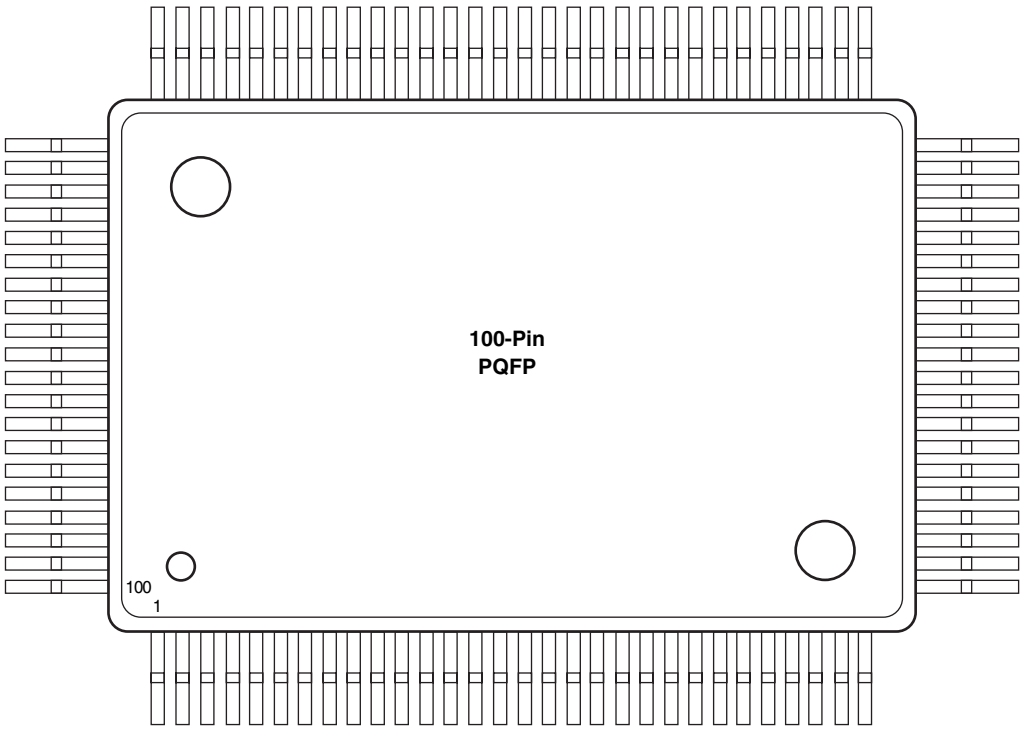

| Signal | A1225A Function | A1240A Function | A1280A Function |
|---|---|---|---|
| 43 | VCC | VCC | VCC |
| 49 | GND | GND | GND |
| 63 | GND | GND | GND |
| 64 | VCC | VCC | VCC |
| 65 | VCC | VCC | VCC |
| 70 | GND | GND | GND |
| 76 | SDI, I/O | SDI, I/O | SDI, I/O |
| 81 | PRA, I/O | PRA, I/O | PRA, I/O |
| 83 | CLKA, I/O | CLKA, I/O | CLKA, I/O |
| 84 | VCC | VCC | VCC |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 100-Pin PQFP




| Pin Number | A1225A Function |
|---|---|
| 2 | DCLK, I/O |
| 4 | MODE |
| 9 | GND |
| 16 | VCC |
| 17 | VCC |
| 22 | GND |
| 34 | GND |
| 40 | VCC |
| 46 | GND |
| 57 | GND |
| 64 | GND |
| 65 | VCC |

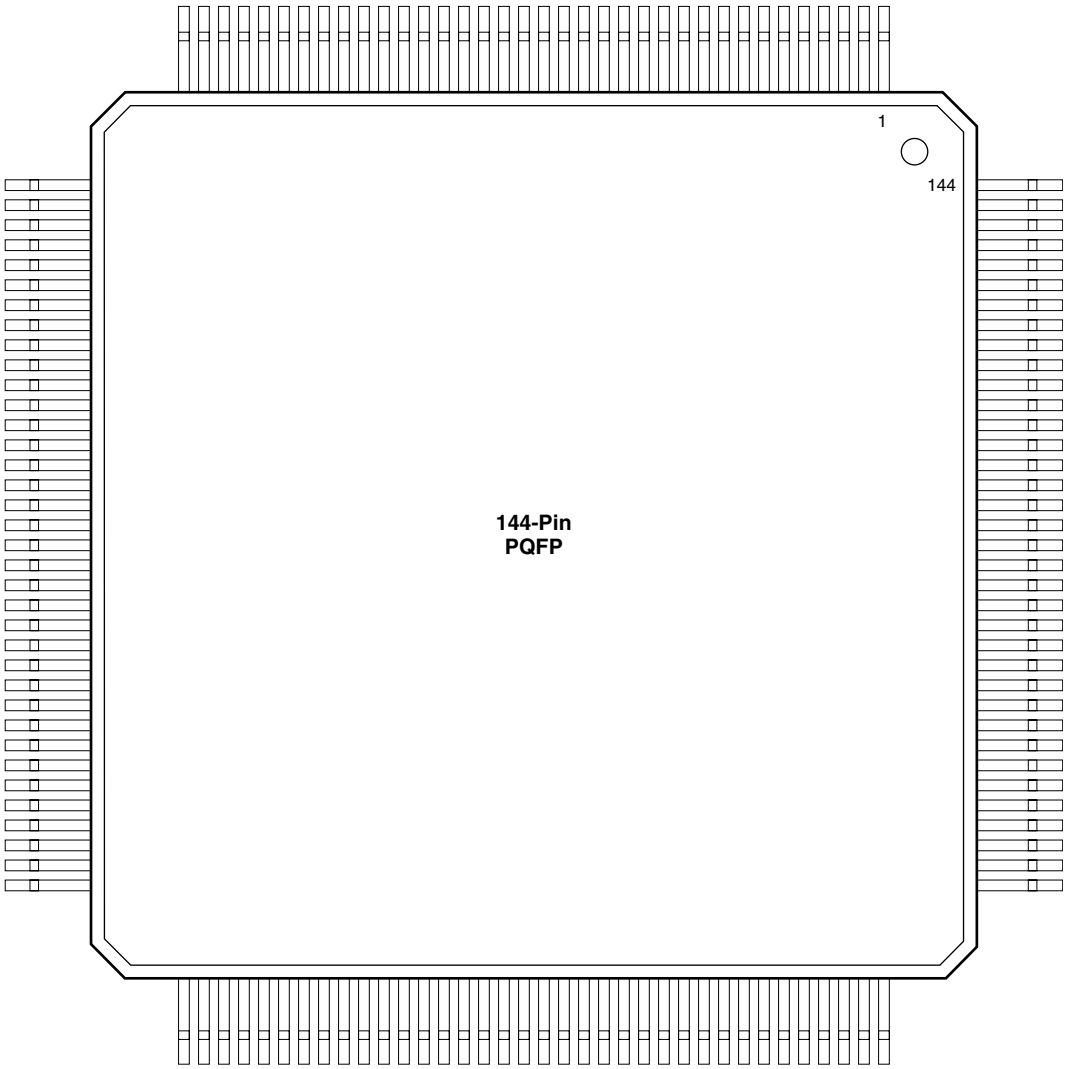
| Pin Number | A1225A Function |
|---|---|
| 66 | VCC |
| 67 | VCC |
| 72 | GND |
| 79 | SDI, I/O |
| 84 | GND |
| 87 | PRA, I/O |
| 89 | CLKA, I/O |
| 90 | VCC |
| 92 | CLKB, I/O |
| 94 | PRB, I/O |
| 96 | GND |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 144-Pin PQFP



### 144-Pin PQFP

| Pin Number | A1240A Function |
|---|---|
| 2 | MODE |
| 9 | GND |
| 10 | GND |
| 11 | GND |
| 18 | VCC |
| 19 | VCC |
| 20 | VCC |
| 21 | VCC |
| 28 | GND |
| 29 | GND |
| 30 | GND |
| 44 | GND |
| 45 | GND |
| 46 | GND |
| 54 | VCC |
| 55 | VCC |
| 56 | VCC |
| 64 | GND |
| 65 | GND |
| 79 | GND |
| 80 | GND |
| 81 | GND |
| 88 | GND |

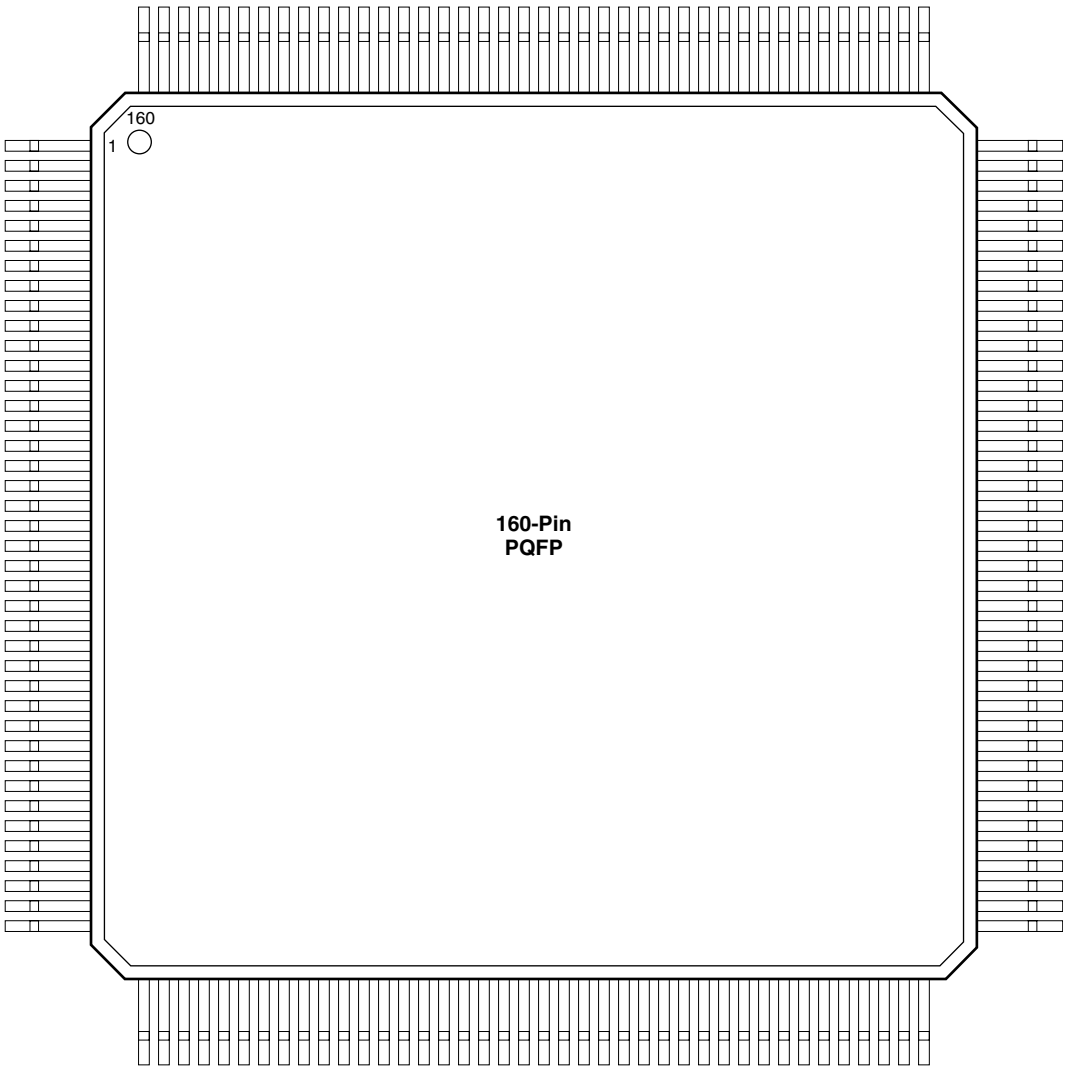
| Pin Number | A1240A Function |
|---|---|
| 89 | VCC |
| 90 | VCC |
| 91 | VCC |
| 92 | VCC |
| 93 | VCC |
| 100 | GND |
| 101 | GND |
| 102 | GND |
| 110 | SDI, I/O |
| 116 | GND |
| 117 | GND |
| 118 | GND |
| 123 | PRA, I/O |
| 125 | CLKA, I/O |
| 126 | VCC |
| 127 | VCC |
| 128 | VCC |
| 130 | CLKB, I/O |
| 132 | PRB, I/O |
| 136 | GND |
| 137 | GND |
| 138 | GND |
| 144 | DCLK, I/O |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 160-Pin PQFP



### 160-Pin PQFP

| Pin Number | A1280A Function |
|---|---|
| 2 | DCLK, I/O |
| 6 | VCC |
| 11 | GND |
| 16 | PRB, I/O |
| 18 | CLKB, I/O |
| 20 | VCC |
| 21 | CLKA, I/O |
| 23 | PRA, I/O |
| 30 | GND |
| 35 | VCC |
| 38 | SDI, I/O |
| 40 | GND |
| 44 | GND |
| 49 | GND |
| 54 | VCC |
| 57 | VCC |
| 58 | VCC |
| 59 | GND |
| 60 | VCC |
| 61 | GND |
| 64 | GND |

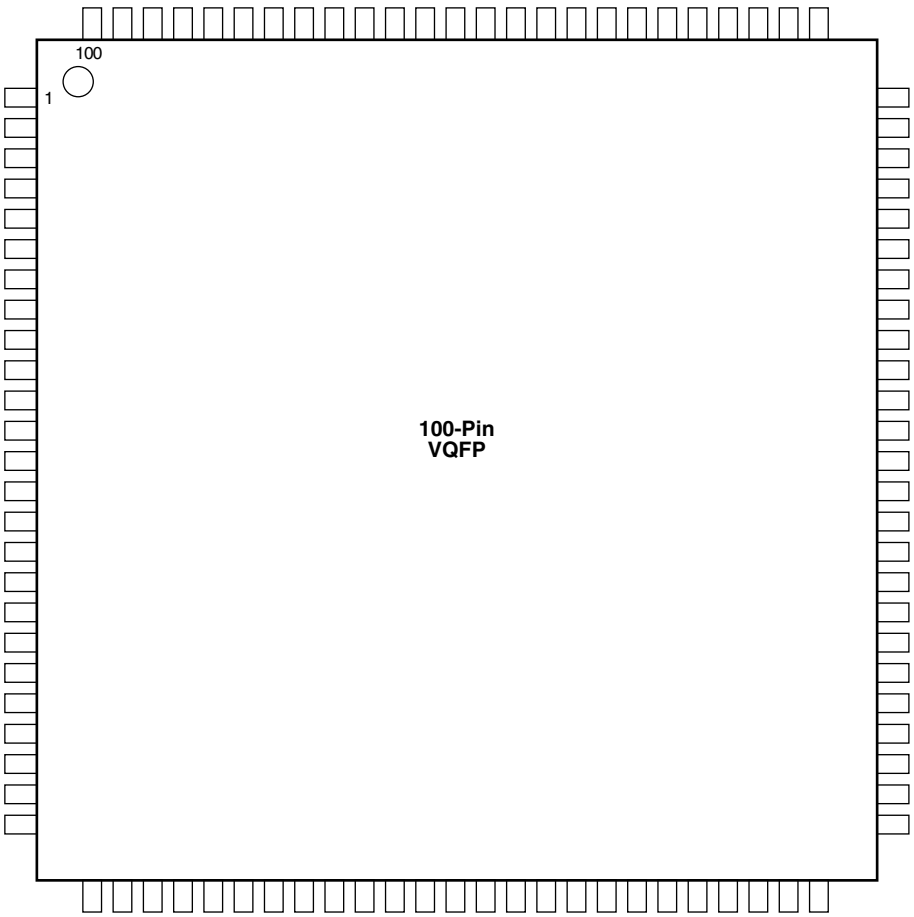
| Pin Number | A1280A Function |
|---|---|
| 69 | GND |
| 80 | GND |
| 86 | VCC |
| 89 | GND |
| 98 | VCC |
| 99 | GND |
| 109 | GND |
| 114 | VCC |
| 120 | GND |
| 125 | GND |
| 130 | GND |
| 135 | VCC |
| 138 | VCC |
| 139 | VCC |
| 140 | GND |
| 145 | GND |
| 150 | VCC |
| 155 | GND |
| 159 | MODE |
| 160 | GND |

***Notes:***

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 100-Pin VQFP




### 100-Pin VQFP

| Pin Number | A1225A Function |
|---|---|
| 2 | MODE |
| 7 | GND |
| 14 | VCC |
| 15 | VCC |
| 20 | GND |
| 32 | GND |
| 38 | VCC |
| 44 | GND |
| 55 | GND |
| 62 | GND |
| 63 | VCC |
| 64 | VCC |

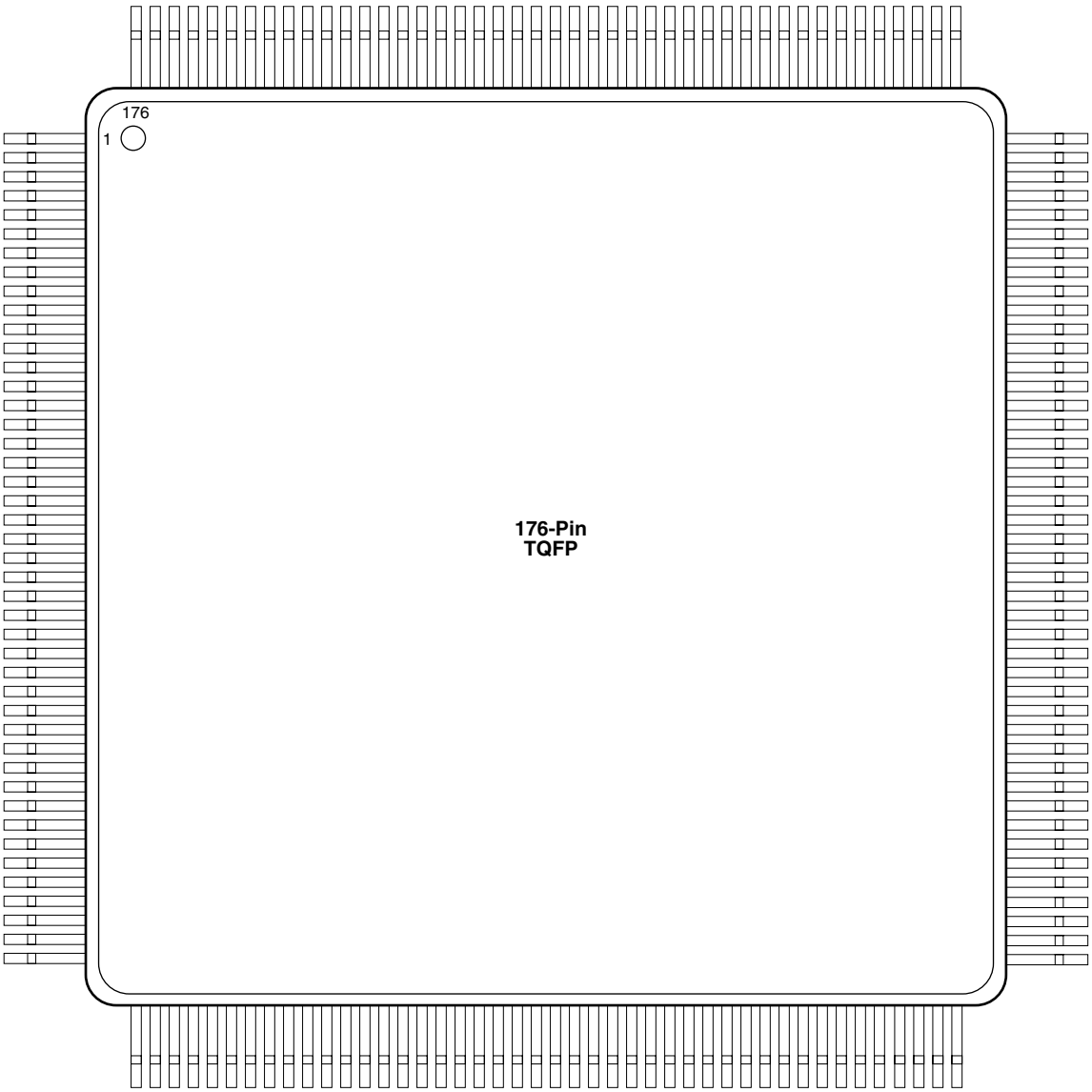
| Pin Number | A1225A Function |
|---|---|
| 65 | VCC |
| 70 | GND |
| 77 | SDI, I/O |
| 82 | GND |
| 85 | PRA, I/O |
| 87 | CLKA, I/O |
| 88 | VCC |
| 90 | CLKB, I/O |
| 92 | PRB, I/O |
| 94 | GND |
| 100 | DCLK, I/O |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 176-Pin TQFP



### 176-Pin TQFP

| Pin Number | A1240A Function | A1280A Function |
|---|---|---|
| 1 | GND | GND |
| 2 | MODE | MODE |
| 8 | NC | NC |
| 10 | NC | I/O |
| 11 | NC | I/O |
| 13 | NC | VCC |
| 18 | GND | GND |
| 19 | NC | I/O |
| 20 | NC | I/O |
| 22 | NC | I/O |
| 23 | GND | GND |
| 24 | NC | VCC |
| 25 | VCC | VCC |
| 26 | NC | I/O |
| 27 | NC | I/O |
| 28 | VCC | VCC |
| 29 | NC | I/O |
| 33 | NC | NC |
| 37 | NC | I/O |
| 38 | NC | NC |
| 45 | GND | GND |
| 52 | NC | VCC |
| 54 | NC | I/O |
| 55 | NC | I/O |
| 57 | NC | NC |
| 61 | NC | I/O |
| 64 | NC | I/O |
| 66 | NC | I/O |
| 67 | GND | GND |
| 68 | VCC | VCC |
| 74 | NC | I/O |
| 77 | NC | NC |
| 78 | NC | I/O |
| 80 | NC | I/O |
| 82 | NC | VCC |
| 86 | NC | I/O |
| 89 | GND | GND |
| 96 | NC | I/O |
| 97 | NC | I/O |

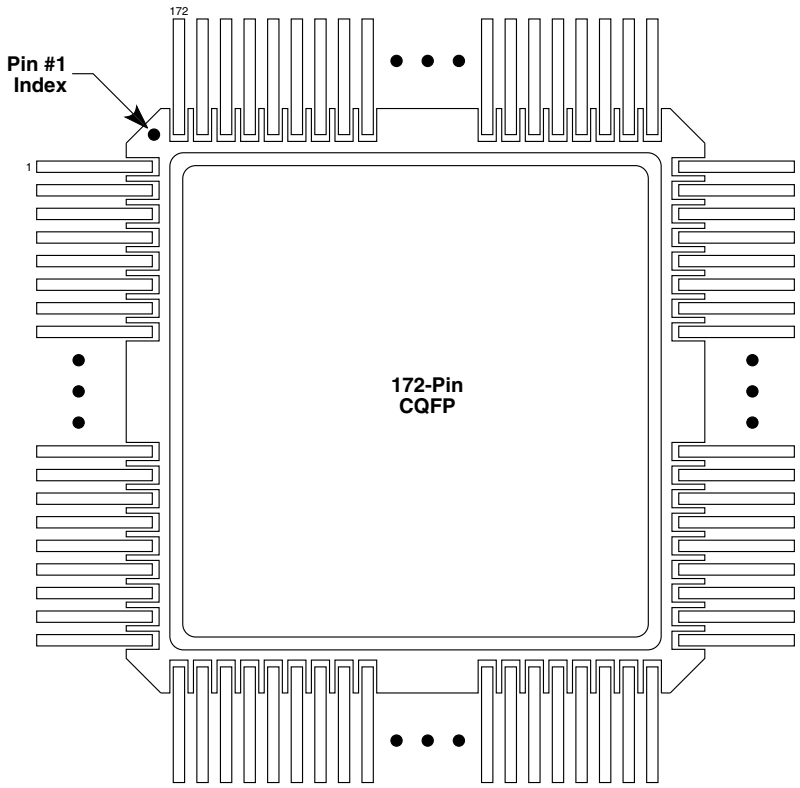
| Pin Number | A1240A Function | A1280A Function |
|---|---|---|
| 101 | NC | NC |
| 103 | NC | I/O |
| 106 | GND | GND |
| 107 | NC | I/O |
| 108 | NC | I/O |
| 109 | GND | GND |
| 110 | VCC | VCC |
| 111 | GND | GND |
| 112 | VCC | VCC |
| 113 | VCC | VCC |
| 114 | NC | I/O |
| 115 | NC | I/O |
| 116 | NC | VCC |
| 121 | NC | NC |
| 124 | NC | I/O |
| 125 | NC | I/O |
| 126 | NC | NC |
| 133 | GND | GND |
| 135 | SDI, I/O | SDI, I/O |
| 136 | NC | I/O |
| 140 | NC | VCC |
| 143 | NC | I/O |
| 144 | NC | I/O |
| 145 | NC | NC |
| 147 | NC | I/O |
| 151 | NC | I/O |
| 152 | PRA, I/O | PRA, I/O |
| 154 | CLKA, I/O | CLKA, I/O |
| 155 | VCC | VCC |
| 156 | GND | GND |
| 158 | CLKB, I/O | CLKB, I/O |
| 160 | PRB, I/O | PRB, I/O |
| 161 | NC | I/O |
| 165 | NC | NC |
| 166 | NC | I/O |
| 168 | NC | I/O |
| 170 | NC | VCC |
| 173 | NC | I/O |
| 175 | DCLK, I/O | DCLK, I/O |

***Notes:***

1. *NC: Denotes No Connection*
2. *All unlisted pin numbers are user I/Os.*
3. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 172-Pin CQFP




### 172-Pin CQFP

| Pin Number | A1280A Function |
|---|---|
| 1 | MODE |
| 7 | GND |
| 12 | VCC |
| 17 | GND |
| 22 | GND |
| 23 | VCC |
| 24 | VCC |
| 27 | VCC |
| 32 | GND |
| 37 | GND |
| 50 | VCC |
| 55 | GND |
| 65 | GND |
| 66 | VCC |
| 75 | GND |
| 80 | VCC |
| 98 | GND |
| 103 | GND |
| 106 | GND |

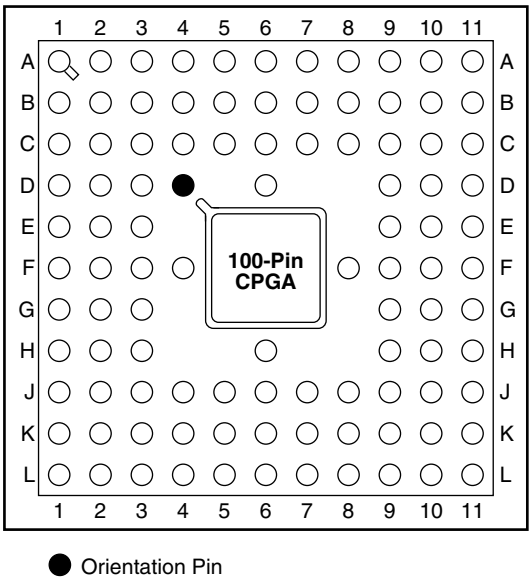
| Pin Number | A1280A Function |
|---|---|
| 107 | VCC |
| 108 | GND |
| 109 | VCC |
| 110 | VCC |
| 113 | VCC |
| 118 | GND |
| 123 | GND |
| 131 | SDI, I/O |
| 136 | VCC |
| 141 | GND |
| 148 | PRA, I/O |
| 150 | CLKA, I/O |
| 151 | VCC |
| 152 | GND |
| 154 | CLKB, I/O |
| 156 | PRB, I/O |
| 161 | GND |
| 166 | VCC |
| 171 | DCLK, I/O |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 100-Pin CPGA




| Pin Number | A1225A Function |
|---|---|
| A4 | PRB, I/O |
| A7 | PRA, I/O |
| B6 | VCC |
| C2 | MODE |
| C3 | DCLK, I/O |
| C5 | GND |
| C6 | CLKA, I/O |
| C7 | GND |
| C8 | SDI, I/O |
| D6 | CLKB, I/O |
| D10 | GND |
| E3 | GND |

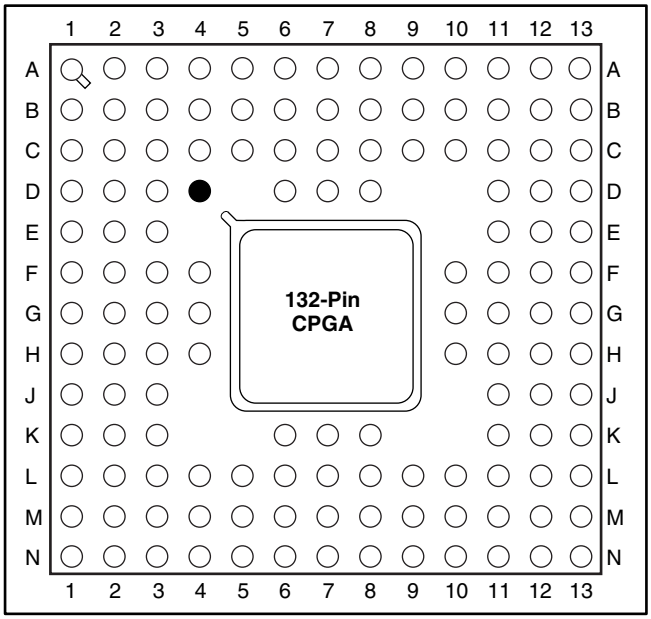
| Pin Number | A1225A Function |
|---|---|
| E11 | VCC |
| F3 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| G1 | VCC |
| G3 | GND |
| G9 | GND |
| J5 | GND |
| J7 | GND |
| K6 | VCC |

*Note:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 132-Pin CPGA




| Pin Number | A1240A Function |
|---|---|
| A1 | MODE |
| B5 | GND |
| B6 | CLKB, I/O |
| B7 | CLKA, I/O |
| B8 | PRA, I/O |
| B9 | GND |
| B12 | SDI, I/O |
| C3 | DCLK, I/O |
| C5 | GND |
| C6 | PRB, I/O |
| C7 | VCC |
| C9 | GND |
| D7 | VCC |
| E3 | GND |
| E11 | GND |
| E12 | GND |
| F4 | GND |

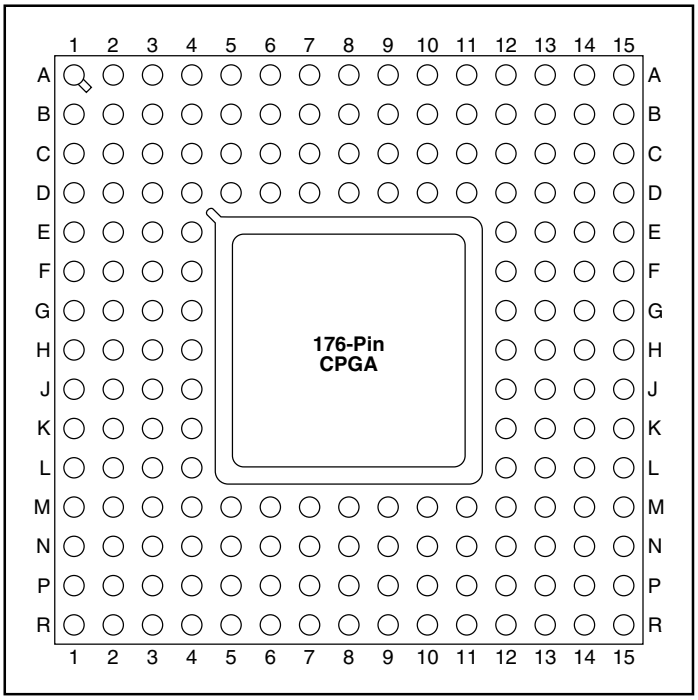
| Pin Number | A1240A Function |
|---|---|
| G2 | VCC |
| G3 | VCC |
| G4 | VCC |
| G10 | VCC |
| G11 | VCC |
| G12 | VCC |
| G13 | VCC |
| H13 | GND |
| J2 | GND |
| J3 | GND |
| J11 | GND |
| K7 | VCC |
| K12 | GND |
| L5 | GND |
| L7 | VCC |
| L9 | GND |
| M9 | GND |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## Package Pin Assignments (continued)

### 176-Pin CPGA




| Pin Number | A1280A Function |
|---|---|
| A9 | CLKA, I/O |
| B3 | DCLK, I/O |
| B8 | CLKB, I/O |
| B14 | SDI, I/O |
| C3 | MODE |
| C8 | GND |
| C9 | PRA, I/O |
| D4 | GND |
| D5 | VCC |
| D6 | GND |
| D7 | PRB, I/O |
| D8 | VCC |
| D10 | GND |
| D11 | VCC |
| D12 | GND |
| E4 | GND |
| E12 | GND |
| F4 | VCC |
| F12 | GND |
| G4 | GND |
| G12 | VCC |

| Pin Number | A1280A Function |
|---|---|
| H2 | VCC |
| H3 | VCC |
| H4 | GND |
| H12 | GND |
| H13 | VCC |
| H14 | VCC |
| J4 | VCC |
| J12 | GND |
| J13 | GND |
| J14 | VCC |
| K4 | GND |
| K12 | GND |
| L4 | GND |
| M4 | GND |
| M5 | VCC |
| M6 | GND |
| M8 | GND |
| M10 | GND |
| M11 | VCC |
| M12 | GND |
| N8 | VCC |

*Notes:*

1. *All unlisted pin numbers are user I/Os.*
2. *MODE pin should be terminated to GND through a 10K resistor to enable Actionprobe usage, otherwise it can be terminated directly to GND.*

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous version | Changes in current version (production (unmarked) v4.0.1–web-only) | Page |
|---|---|---|
| unspecified | In the 176-Pin CPGA package, pin A3 was incorrectly assigned as CLKA, I/O. A3 is a user I/O. Pin A9 is CLKA, I/O | 35 |

## Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as "Advanced" or Preliminary" data sheets. The definition of these categories are as follows:

### Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

### Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Unmarked (production)

The data sheet contains information that is considered to be final.

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