v3.0

Integrator Series FPGAs: 1200XL and 3200DX Families

Features

High Capacity

- 2,500 to 30,000 Logic Gates
- Up to 3Kbits Configurable Dual-Port SRAM
- Fast Wide-Decode Circuitry
- Up to 250 User-Programmable I/O Pins

High Performance

- 225 MHz Performance
- 5 ns Dual-Port SRAM Access
- 100 MHz FIFOs
- 7.5 ns 35-Bit Address Decode

Ease-of-Integration

- Synthesis-Friendly Architecture Supports ASIC Design Methodologies.
- 95–100% Device Utilization using Automatic Place-and-Route Tools.
- Deterministic, User-Controllable Timing Via Timing Driven Software Tools with Up To 100% Pin Fixing.
- IEEE Standard 1149.1 (JTAG) Boundary Scan Testing.

General Description

Actel's Integrator Series FPGAs are the first programmable logic devices optimized for high-speed system logic integration. Based on Actel's proprietary antifuse technology and 0.6-micron double metal CMOS process, Integrator Series devices offer a fine-grained, register-rich architecture with embedded dual-port SRAM and wide-decode circuitry.

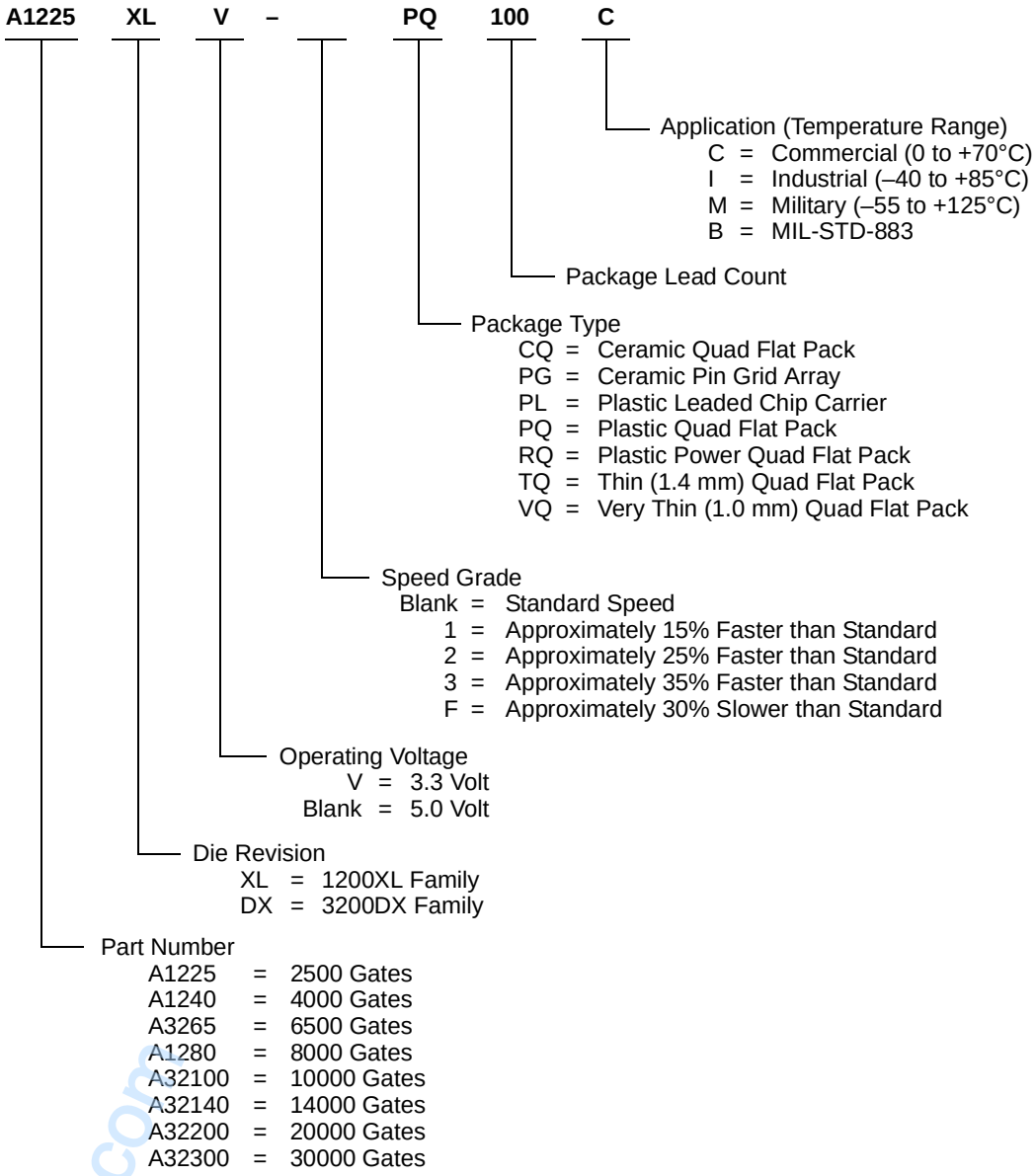
Integrator Series' 3200DX and 1200XL families were designed to integrate system logic which is typically implemented in multiple CPLDs, PALs, and FPGAs. These devices provide the features and performance required for today's complex, high-speed digital logic systems. The 3200DX family offers fast dual-port SRAM for implementing FIFOs, LIFOs, and temporary data storage. The large number of storage elements can efficiently address applications requiring wide datapath manipulation and transformation functions such as telecommunications, networking, and DSP.

Integrator Series Product Profile Family

	1200XL			3200DX				
Device	**A1225XL**	**A1240XL**	**A1280XL**	**A3265DX**	**A32100DX**	**A32140DX**	**A32200DX**	**A32300DX**
Capacity								
Logic Gates[1]	2,500	4,000	8,000	6,500	10,000	14,000	20,000	30,000
SRAM Bits	N/A	N/A	N/A	N/A	2,048	N/A	2,560	3,072
Logic Modules								
Sequential	231	348	624	510	700	954	1,230	1,888
Combinatorial	220	336	608	475	662	912	1,184	1,833
Decode	N/A	N/A	N/A	20	20	24	24	28
SRAM Modules (64x4 or 32x8)	N/A	N/A	N/A	N/A	8	N/A	10	12
Dedicated Flip-Flops	231	348	624	510	700	954	1,230	1,888
Clocks	2	2	2	2	6	2	6	6
User I/O (Maximum)	83	104	140	126	152	176	202	250
JTAG	No	No	No	No	Yes	Yes	Yes	Yes
Packages	PL84 PQ100 VQ100 PG100	PL84 PQ100 PQ144 TQ176 PG132	PL84 PQ160 PQ208 TQ176 PG176 CQ172	PL84 PQ100 PQ160 TQ176	PL84 PQ160 PQ208 TQ176 CQ84	PL84 PQ160 PQ208 TQ176 CQ256	PQ208 RQ208 RQ240 CQ208 CQ256	RQ208 RQ240 CQ256

Note: *Logic gate capacity does not include SRAM bits as logic.*

Ordering Information



Product Plan

	Speed Grade*					Application			
	–F	Std	–1	–2	–3	C	I	M	B
A1225XL Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	—	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	✔	✔	✔	✔	—	✔	✔	—	—
100-Pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	—	✔	—	—	—
A1225XLV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
100-Pin Very Thin Plastic Quad Flat Pack (VQFP)	—	✔	—	—	—	✔	—	—	—
A1240XL Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	—	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
132-Pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	—	✔	—	—	—
144-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	—	✔	✔	—	—
A1240XLV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	—	✔	—	—	—	✔	—	—	—
A3265DX Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	—	✔	✔	—	—
100-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	—	✔	✔	—	—
A3265DXV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	—	✔	—	—	—	✔	—	—	—
A1280XL Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	—	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
172-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	✔	—	✔	—	✔	✔
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	—	✔	✔	—	—
176-Pin Ceramic Pin Grid Array (CPGA)	—	✔	✔	✔	—	✔	—	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
A1280XLV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	—	✔	—	—	—	✔	—	—	—
A32100DX Device									
84-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	✔	—	✔	—	✔	✔
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	✔	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—

Contact your Actel sales representative for product availability.

Applications: *C = Commercial* *I = Industrial* *M = Military*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35% faster than Standard* *–F = Approx. 40% slower than Standard*

† *Only Std, –1, –2 Speed Grade*

• *Only Std, –1 Speed Grade*

Product Plan (Continued)

	Speed Grade*					Application			
	–F	Std	–1	–2	–3	C	I	M	B
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
A32100DXV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	—	✔	—	—	—	✔	—	—	—
A32140DX Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	✔	✔	✔	✔	—	✔	✔	—	—
160-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	✔	✔	✔	✔	—	✔	✔	—	—
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	—	✔	✔	—	—
256-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	—	—	✔	—	✔	✔
A32140DXV Device									
84-Pin Plastic Leaded Chip Carrier (PLCC)	—	✔	—	—	—	✔	—	—	—
176-Pin Thin Plastic Quad Flat Pack (TQFP)	—	✔	—	—	—	✔	—	—	—
A32200DX Device									
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
208-Pin Plastic Power Quad Flat Pack (RQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
240-Pin Plastic Power Quad Flat Pack (RQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
208-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	—	—	✔	—	✔	✔
256-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	—	—	✔	—	✔	✔
A32200DXV Device									
208-Pin Plastic Quad Flat Pack (PQFP)	—	✔	—	—	—	✔	—	—	—
240-Pin Plastic Power Quad Flat Pack (RQFP)	—	✔	—	—	—	✔	—	—	—
A32300DX Device									
208-Pin Plastic Power Quad Flat Pack (RQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
240-Pin Plastic Power Quad Flat Pack (RQFP)	✔	✔	✔	✔	✔	✔	✔	—	—
256-Pin Ceramic Quad Flat Pack (CQFP)	—	✔	✔	—	—	✔	—	✔	✔
A32300DXV Device									
208-Pin Plastic Power Quad Flat Pack (RQFP)	—	✔	—	—	—	✔	—	—	—
240-Pin Plastic Power Quad Flat Pack (RQFP)	—	✔	—	—	—	✔	—	—	—

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Applications: *C = Commercial* *I = Industrial* *M = Military*

Availability: ✔ = *Available* *P = Planned* — = *Not Planned*

**Speed Grade:* *–1 = Approx. 15% faster than Standard* *–2 = Approx. 25% faster than Standard* *–3 = Approx. 35% faster than Standard* *–F = Approx. 40% slower than Standard*

† *Only Std, –1, –2 Speed Grade*

• *Only Std, –1 Speed Grade*

Development Tool Support

The devices are fully supported by Actel's line of FPGA development tools, including the Actel DeskTOP series and Designer Advantage tools. The Actel DeskTOP series is an integrated design environment for PCs that includes design entry, simulation, synthesis, and place and route tools. Designer Advantage, Actel's suite of FPGA development point tools for PCs and Workstations, includes the ACTgen Macro Builder, timing-driven place and route and analysis tools, and device programming software.

In addition, the devices contain ActionProbe circuitry that provides built-in access to every node in a design, enabling 100 percent real-time observation and analysis of a device's internal logic nodes without design iteration. The probe circuitry is accessed by Silicon Explorer II, an easy-to-use integrated verification and logic analysis tool that can sample data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to only a few seconds.

Integrator Series Architectural Overview

The 1200XL and 3200DX architecture is composed of fine-grained building blocks which produce fast, efficient logic designs. All devices within the Integrator Series are composed of logic modules, routing resources, clock networks, and I/O modules which are the building blocks to design fast logic designs. In addition, a subset of devices contain embedded dual-port SRAM and wide-decode modules. The dual-port SRAM modules are optimized for high-speed datapath functions such as FIFOs, LIFOs, and scratchpad memory. The "Integrator Series Product Profile Family" on page 1 lists the specific logic resources contained within each device.

Plastic Device Resources

Device	User I/Os							
	PLCC 84-Pin	VQFP 100-Pin	PQFP 100-Pin	PQFP 144-Pin	PQFP 160-Pin	PQFP 208-Pin	RQFP 240-Pin	TQFP 176-Pin
A1225XL	72	83	83	—	—	—	—	—
A1240XL	72	—	83	104	—	—	—	103
A3265DX	72	—	83	—	125	—	—	126
A1280XL	72	—	—	—	125	140	—	140
A32100DX	72	—	—	—	125	152	—	142
A32140DX	72	—	—	—	125	176	—	150
A32200DX	—	—	—	—	—	176*	202	—
A32300DX	—	—	—	—	—	176	202	—

Package Definitions *(Consult your local Actel Sales Representative for product availability.)*

PLCC = Plastic Leaded Chip Carrier, PQFP = Plastic Quad Flat Pack, TQFP = Thin Quad Flat Pack, BGA = Ball Grid Array, VQFP = Very Thin Quad Flat Pack, RQFP = Plastic Power Quad Flat Pack

** Also available in RQFP 208-pin.*

Hermetic Device Resources

Device	User I/Os				
	CPGA 176-Pin	CQFP 84-Pin	CQFP 172-Pin	CQFP 208-Pin	CQFP 256-Pin
A1280XL	140	—	140	—	—
A32100DX	—	60	—	—	—
A32140DX	—	—	—	—	176
A32200DX	—	—	—	176	202
A32300DX	—	—	—	—	212

Package Definitions *(Consult your local Actel Sales Representative for product availability.)*

CPGA = Ceramic Pin Grid Array, CQFP = Ceramic Quad Flat Pack

Logic Modules

3200DX and 1200XL devices contain three types of logic modules: combinatorial (C-modules), sequential (S-modules), and decode (D-modules). 1200XL devices contain only the C-module and S-module, while the 3200DX devices contain D-modules and dual-port SRAM modules in addition to the S-module and C-module.

The C-module is shown in Figure 1 and implements the following function:

Y=!S1*!S0*D00+!S1*S0*D01+S1*!S0*D10+S1*S0*D11

where:

S0=A0*B0

S1=A1+B1

The S-module shown in Figure 2 is designed to implement high-speed sequential functions within a single logic module. The S-module implements the same combinatorial logic function as the C-module while adding a sequential element. The sequential element can be configured as either a D-type flip-flop or a transparent latch. To increase flexibility, the S-module register can be bypassed so that it implements purely combinatorial logic.

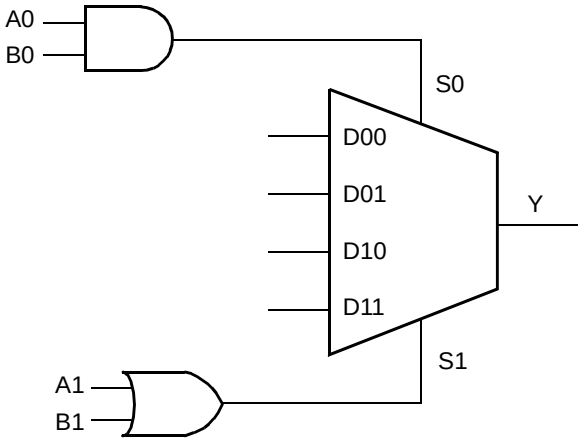


Figure 1 • C-Module Implementation

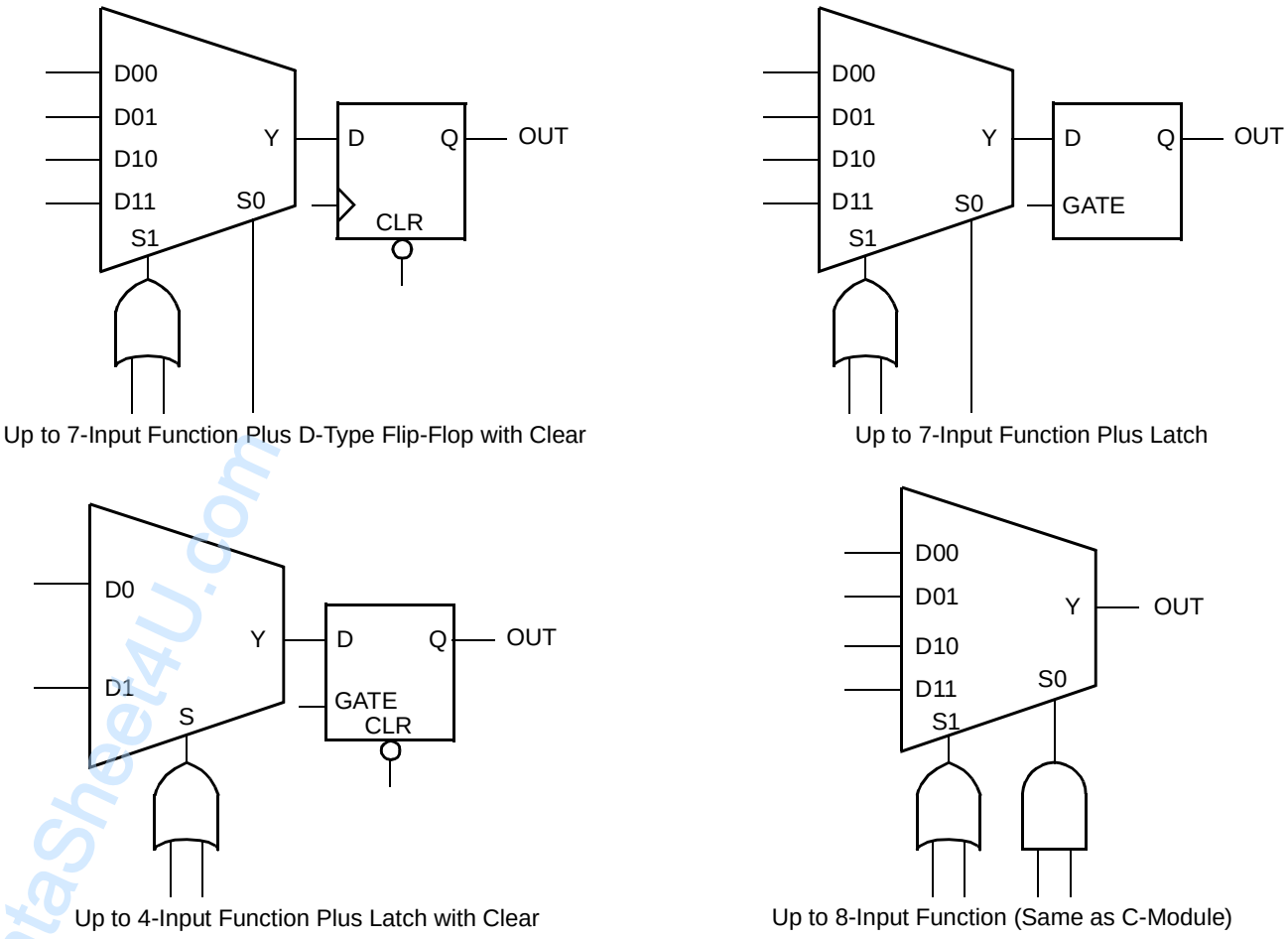


Figure 2 • S-Module Implementation

3200DX devices contain a third type of logic module, D-modules, which are arranged around the periphery of the device. D-modules contain wide-decode circuitry which provides a fast, wide-input AND function similar to that found in product term architectures (Figure 3). The D-module allows 3200DX devices to perform wide-decode functions at speeds comparable CPLDs and PAL devices. The output of the D-module has a programmable inverter for active HIGH or LOW assertion. The D-module output is hard-wired to an output pin or can be fed back into the array to be incorporated into other logic.

Dual-Port SRAM Modules

Several 3200DX devices contain dual-port SRAM modules that have been optimized for synchronous or asynchronous applications. The SRAM modules are arranged in 256-bit blocks which can be configured as 32x8 or 64x4 (refer to "Integrator Series Product Profile Family" on page 1 for the number of SRAM blocks within a particular device). SRAM modules can be cascaded together to form memory spaces of user-definable width and depth. A block diagram of the 3200DX dual-port SRAM block is shown in Figure 4.

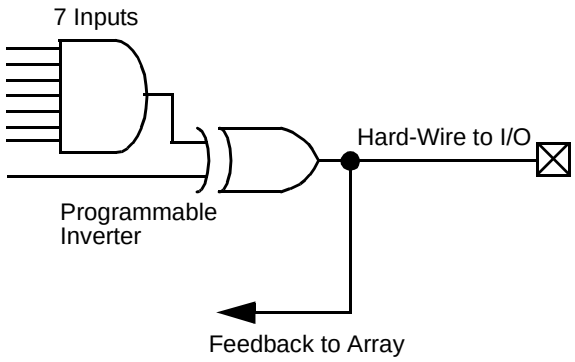


Figure 3 • D-Module Implementation

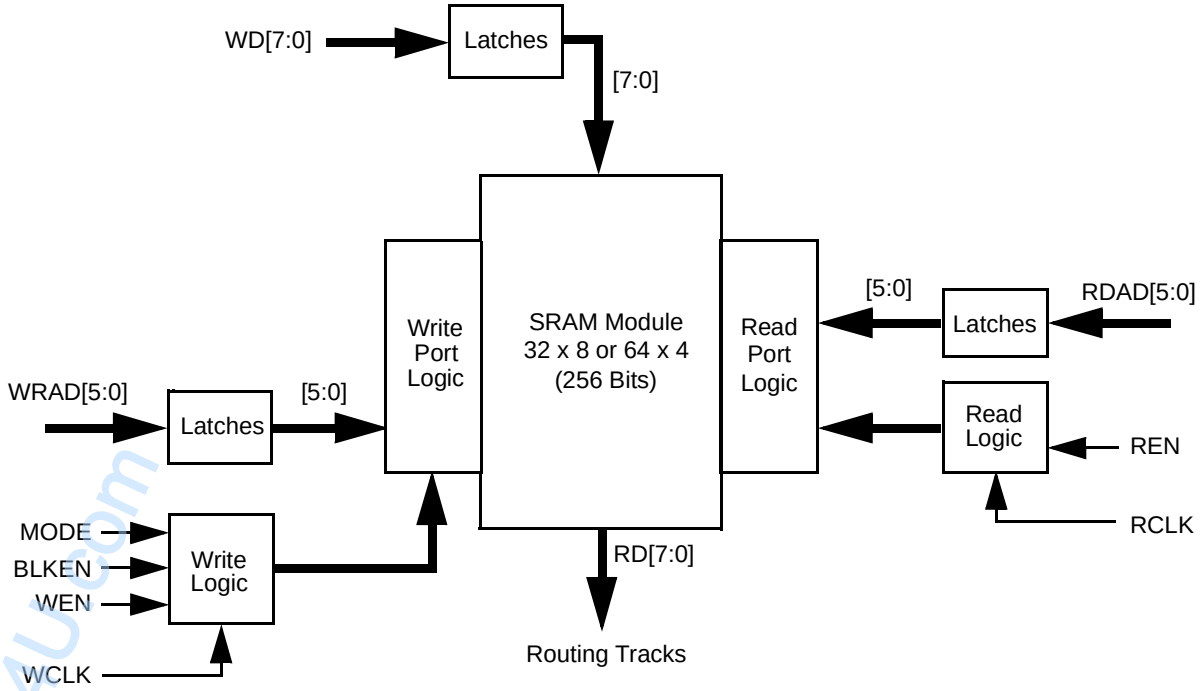


Figure 4 • 3200DX Dual-Port SRAM Block

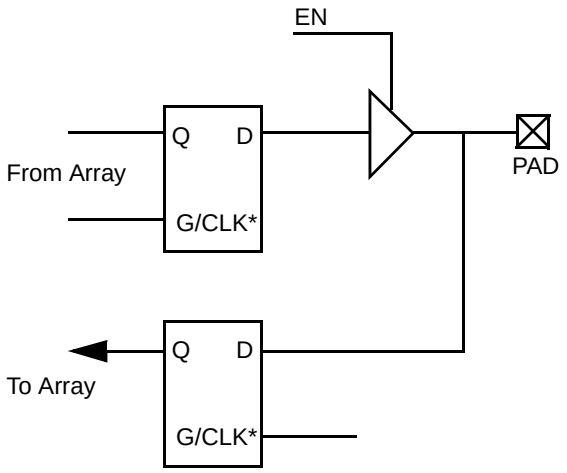
The 3200DX SRAM modules are true dual-port structures containing independent READ and WRITE ports. Each SRAM module contains six bits of read and write addressing (RDAD[5:0] and WRAD[5:0], respectively) for 64x4 bit blocks. When configured in byte mode, the highest order address bits (RDAD5 and WRAD5) are not used. The read and write ports of the SRAM block contain independent clocks (RCLK and WCLK) with programmable polarities offering active HIGH or LOW implementation. The SRAM block contains eight data inputs (WD[7:0]) and eight outputs (RD[7:0]) which are connected to segmented vertical routing tracks.

The 3200DX dual-port SRAM blocks provide an optimal solution for high-speed buffered applications requiring fast FIFO and LIFO queues. Actel's ACTgen Macro Builder provides the capability to quickly design memory functions,

such as FIFOs, LIFOs, and RAM arrays. Additionally, unused SRAM blocks can be used to implement registers for other logic within the design.

I/O Modules

The I/O modules provide the interface between the device pins and the logic array. Figure 5 is a block diagram of the I/O module. A variety of user functions, determined by a library macro selection, can be implemented in the module (refer to the Macro Library Guide for more information). I/O modules contain a tri-state buffer, input and output latches which can be configured for input, output, or bi-directional pins (Figure 5).



* Can be Configured as a Latch or D Flip-Flop (Using C-Module)

Figure 5 • I/O Module

The Integrator Series devices contain flexible I/O structures where each output pin has a dedicated output enable control. The I/O module can be used to latch input and/or output data, providing a fast set-up time. In addition, the Actel Designer Series software tools can build a D-type flip-flop using a C-module to register input and/or output signals.

Actel's Designer Series development tools provide a design library of I/O macrofunctions which can implement all I/O configurations supported by the Integrator Series FPGAs.

Routing Structure

The Integrator Series architecture uses vertical and horizontal routing tracks to interconnect the various logic and I/O modules. These routing tracks are metal interconnects that may either be of continuous length or broken into pieces called segments. Varying segment lengths allows interconnection of over 90% of design tracks to occur with only two antifuse connections. Segments can be joined together at the ends using antifuses to increase their lengths up to the full length of the track. All interconnects can be accomplished with a maximum of four antifuses.

Horizontal Routing

Horizontal channels are located between the rows of modules and are composed of several routing tracks. The horizontal routing tracks within the channel are divided into one or more segments. The minimum horizontal segment length is the width of a module pair, and the maximum horizontal segment length is the full length of the channel. Any segment that spans more than one-third the row length is considered a long horizontal segment. A typical channel is shown in Figure 6. Non-dedicated horizontal routing tracks are used to route signal nets; dedicated routing tracks are used for the global clock networks and for power and ground tie-off tracks.

Vertical Routing

Another set of routing tracks run vertically through the module. Vertical tracks are of three types: input, output, and long, and are divided into one or more segments. Each segment in an input track is dedicated to the input of a particular module; each segment in an output track is dedicated to the output of a particular module. Long segments are uncommitted and can be assigned during routing. Each output segment spans four channels (two above and two below), except near the top and bottom of the array where edge effects occur. Long Vertical Tracks contain either one or two segments. An example of vertical routing tracks and segments is shown in Figure 6.

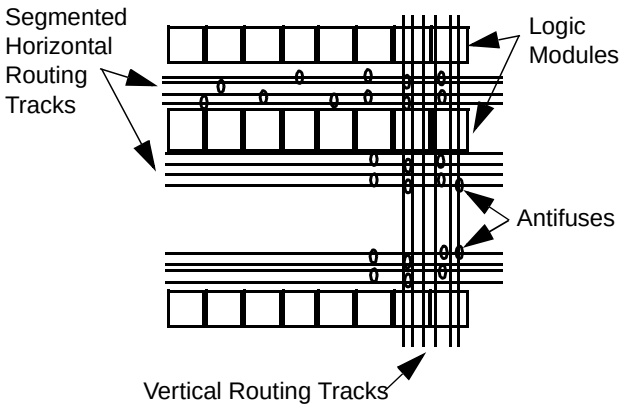


Figure 6 • Routing Structure

Antifuse Structure

An antifuse is a "normally open" structure as opposed to the normally closed fuse structure used in PROMs or PALs. The use of antifuses to implement a programmable logic device results in highly-testable structures as well as efficient

programming algorithms. The structure is highly testable because there are no pre-existing connections; therefore, temporary connections can be made using pass transistors. These temporary connections can isolate individual antifuses to be programmed and individual circuit structures to be tested, which can be done before and after programming. For example, all metal tracks can be tested for continuity and shorts between adjacent tracks, and the functionality of all logic modules can be verified.

Clock Networks

Two low-skew, high-fanout clock distribution networks are provided in each 3200DX device. These networks are referred to as CLK0 and CLK1. Each network has a clock module (CLKMOD) that selects the source of the clock signal and may be driven as follows:

1. Externally from the CLKA pad
2. Externally from the CLKB pad
3. Internally from the CLKINA input
4. Internally from the CLKINB input

The clock modules are located in the top row of I/O modules. Clock drivers and a dedicated horizontal clock track are located in each horizontal routing channel.

The user controls the clock module by selecting one of two clock macros from the macro library. The macro CLKBUF is used to connect one of the two external clock pins to a clock network, and the macro CLKINT is used to connect an internally-generated clock signal to a clock network. Since both clock networks are identical, the user does not care whether CLK0 or CLK1 is being used. The clock input pads may also be used as normal I/Os, bypassing the clock networks (see Figure 7).

The 3200DX devices which contain SRAM modules (all except A3265DX and A32140DX) have four additional register control resources, called quadrant clock networks (Figure 8 on page 10). Each quadrant clock provides a local, high-fanout resource to the contiguous logic modules within its quadrant of the device. Quadrant clock signals can originate from specific I/O pins or from the internal array and can be used as a secondary register clock, register clear, or output enable.

Test Circuitry

All devices contain Actel's ActionProbe test circuitry which test and debug a design once it is programmed into a device. Once a device has been programmed, the ActionProbe test circuitry allows the designer to probe any internal node during device operation to aid in debugging a design. In addition, 3200DX devices contain IEEE Standard 1149.1 boundary scan test circuitry.

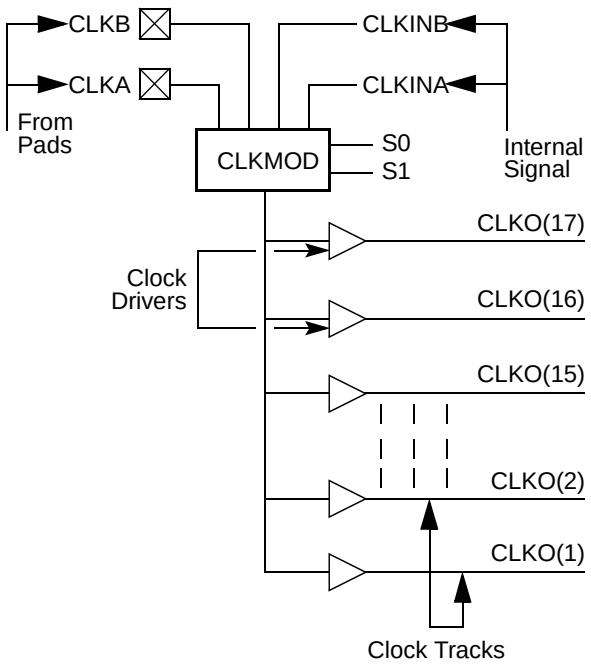


Figure 7 • Clock Networks

IEEE Standard 1149.1 Boundary Scan Testing (BST)

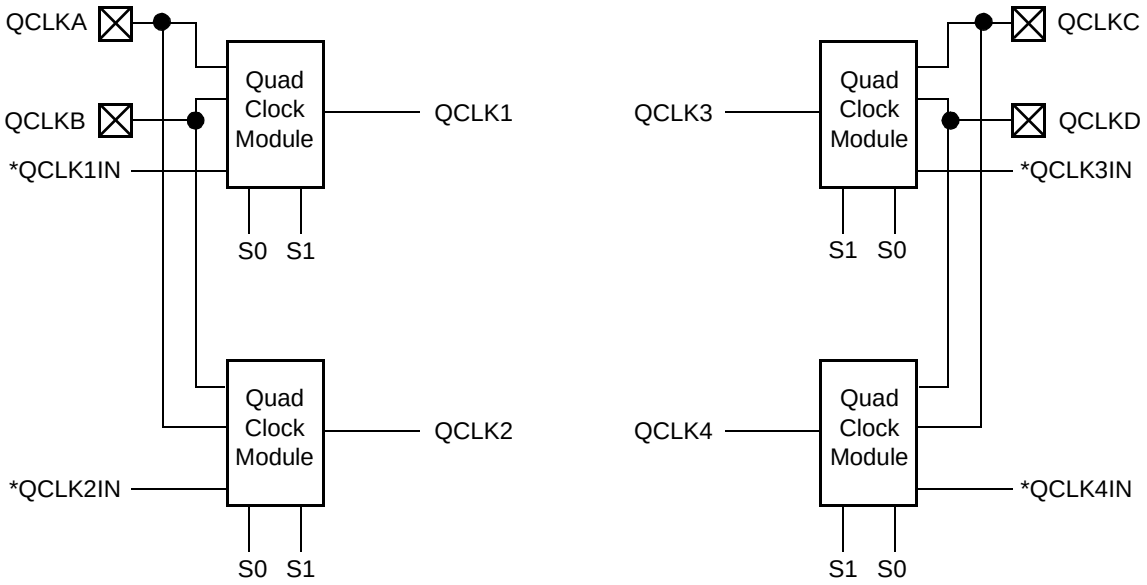
IEEE Standard 1149.1 defines a four-pin Test Access Port (TAP) interface for testing integrated circuits in a system. The 3200DX family provides five BST pins: Test Data In (TDI), Test Data Out (TDO), Test Clock (TCK), and Test Mode Select Test Reset (TRST) (3200DX24A only). Devices are configured in a test "chain" where BST data can be transmitted serially between devices via TDO-to-TDI interconnections. The TMS and TCK signals are shared among all devices in the test chain so that all components operate in the same state.

The 3200DX family implements a subset of the IEEE Standard 1149.1 BST instruction in addition to a private instruction, which allows the use of Actel's ActionProbe facility with BST. Refer to the IEEE Standard 1149.1 specification for detailed information regarding BST.

Boundary Scan Circuitry

The 3200DX boundary scan circuitry consists of a Test Access Port (TAP) controller, test instruction register, a JPROBE register, a bypass register, and a boundary scan register. Figure 9 on page 10 shows a block diagram of the 3200DX boundary scan circuitry.

When a device is operating in BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCK signals. An active reset (nTRST) pin is not supported; however, the 3200DX device contain power-on circuitry that resets the boundary scan circuitry upon power-up. Table 1 on page 11 summarizes the functions of the IEEE 1149.1 BST signals.



**QCLK1IN, QCLK2IN, QCLK3IN, and QCLK4IN are internally-generated signals.*

Figure 8 • *Quadrant Clock Network*

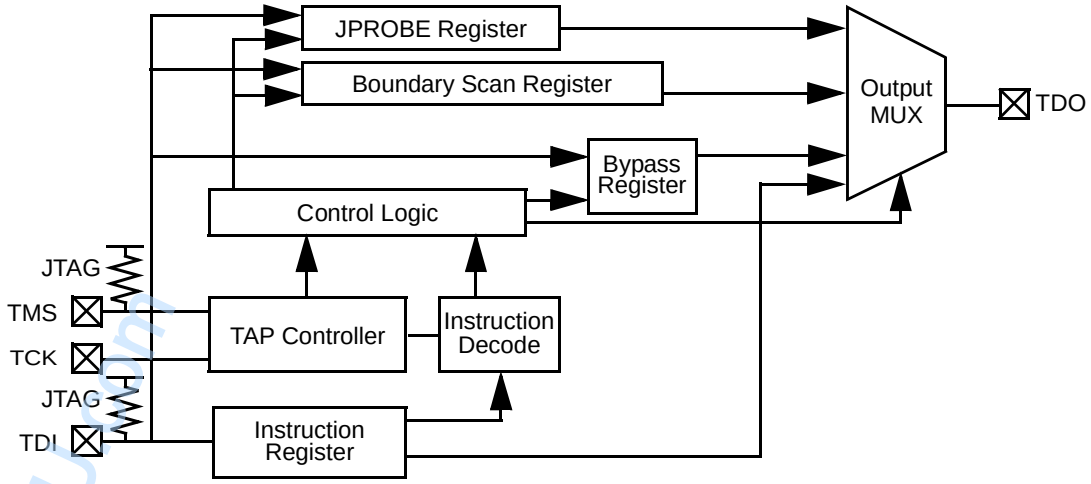


Figure 9 • *3200DX IEEE 1149.1 Boundary Scan Circuitry*

Table 1 • IEEE 1149.1 BST Signals

Signal	Name	Function
TDI	Test Data In	Serial data input for BST instructions and data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Out	Serial data output for BST instructions and test data.
TMS	Test Mode Select	Serial data input for BST mode. Data is shifted in on the rising edge of TCK.
TCK	Test Clock	Clock signal to shift the BST data into the device.

JTAG

All 3200DX devices are IEEE 1149.1 (JTAG) compliant. 3200DX devices offer superior diagnostic and testing capabilities by providing JTAG and probing capabilites. These functions are controlled through the special JTAG pins in conjunction with the program fuse.

JTAG fuse programmed:

- TCK must be terminated—logical high or low doesn't matter (to avoid floating input)
- TDI, TMS may float or at logical high (internal pull-up is present)
- TDO may float or connect to TDI of another device (it's an output)

JTAG fuse not programmed:

- TCK, TDI, TDO, TMS are user I/O. If not used, they will be configured as tristated output.

BST Instructions

Boundary scan testing within the 3200DX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the testing of the device. The BST mode is determined by the bitstream entered on the TMS pin. Table 2 describes the test instructions supported by the 3200DX devices.

Reset

The TMS pin is equipped with an internal pull-up resistor. This allows the TAP controller to remain in or return to the Test-Logic-Reset state when there is no input or when a logical 1 is on the TMS pin. To reset the controller, TMS must be HIGH for at least five TCK cycles.

When a device is operating in BST mode, four I/O pins are used for the TDI, TDO, TMS, and TCLK signals. An active reset (nTRST) pin is not supported; however, the 3200DX contains power-on circuitry which automatically resets the BST circuitry upon power-up. The following table summarizes the functions of the BST signals.

Table 2 • BST Instructions

Test Mode	Code	Description
EXTEST	000	Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
SAMPLE/ PRELOAD	001	Allows a snapshot of the signals at the device pins to be captured and examined during device operation.
JPROBE	011	A private instruction allowing the user to connect Actel's Micro Probe registers to the test chain.
USER INSTRUCTION	100	Allows the user to build application-specific instructions such as RAM READ and RAM WRITE.
HIGH Z	101	Refer to the IEEE Standard 1149.1 specification.
CLAMP	110	Refer to the IEEE Standard 1149.1 specification.
BYPASS	111	Enables the bypass register between the TDI and TDO pins. The test data passes through the selected device to adjacent devices in the test chain.

JTAG BST Instructions

JTAG BST testing within the 3200DX devices is controlled by a Test Access Port (TAP) state machine. The TAP controller drives the three-bit instruction register, a bypass register, and the boundary scan data registers within the device. The TAP controller uses the TMS signal to control the JTAG testing of the device. The JTAG test mode is determined by the bitstream entered on the TMS pin. The table in the next column describes the JTAG instructions supported by the 3200DX.

Design Tool Support ActionProbe

If a device has been successfully programmed and the security fuse has not been programmed, any internal logic or I/O module output can be observed in real time using the ActionProbe circuitry, the PRA and/or PRB pins, and Actel's Silicon Explorer diagnostic and debug tool kit.

5.0V Operating Conditions

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I[2]	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diode will be forward biased and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Industrial	Military	Units
Temperature Range[1]	0 to +70	–40 to +85	–55 to +125	°C
Power Supply Tolerance	±5	±10	±10	%V_{CC}

Note:

1. *Ambient temperature (T_A) is used for commercial and industrial; case temperature (T_C) is used for military.*

Electrical Specifications

Symbol	Parameter	Commercial		Commercial –F		Industrial		Military		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}[1]	(I_{OH} = –10 mA)	2.4		2.4						V
	(I_{OH} = –6 mA)	3.84		3.84						V
	(I_{OH} = –4 mA)					3.7		3.7		V
V_{OL}[1]	(I_{OL} = 10 mA)		0.5		0.5					V
	(I_{OL} = 6 mA)		0.33		0.33		0.40		0.40	V
V_{IL}		–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F			500		500		500		500	ns
C_{IO} I/O Capacitance[2]			10		10		10		10	pF
Standby Current, I_{CC}[3] (typical = 1 mA)			2.0		20		10		20	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See the "Power Dissipation" section on page 14.								
IV Curve[4]		Can be converted from IBIS model on the web.								

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Includes worst-case 176 CPGA package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
3. *All outputs unloaded. All inputs = V_{CC} or GND, typical I_{CC} = 1 mA. I_{CC} limit includes I_{PP} and I_{SV} during normal operation.*
4. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

3.3V Operating Conditions

Absolute Maximum Ratings[1]

Free Air Temperature Range

Symbol	Parameter	Limits	Units
V_{CC}	DC Supply Voltage	–0.5 to +7.0	V
V_I[2]	Input Voltage	–0.5 to V_{CC} +0.5	V
V_O	Output Voltage	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C

Notes:

1. *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Device should not be operated outside the Recommended Operating Conditions.*
2. *Device inputs are normally high impedance and draw extremely low current. However, when input voltage is greater than V_{CC} + 0.5V or less than GND – 0.5V, the internal protection diodes will forward bias and can draw excessive current.*

Recommended Operating Conditions

Parameter	Commercial	Units
Temperature Range[1]	0 to +70	°C
Power Supply Tolerance	±5	%V

Note:

1. *Ambient temperature (T_A) is used for commercial.*

Electrical Specifications

Parameter		Commercial		Units
		Min.	Max.	
V_{OH}[1]	(I_{OH} = –4 mA)	2.15		V
	(I_{OH} = –3.2 mA)	2.4		V
V_{OL}[1]	(I_{OL} = 6 mA)		0.4	V
V_{IL}		–0.3	0.8	V
V_{IH}		2.0	V_{CC} + 0.3	V
Input Transition Time t_R, t_F[2]			500	ns
C_{IO} I/O Capacitance[2, 3]			10	pF
Standby Current, I_{CC}[4] (typical = 0.3 mA)			0.75	mA
$I_{CC(D)}$ Dynamic V_{CC} Supply Current		See the "Power Dissipation" section on page 14.		
IV Curve[4]		Can be converted from IBIS model on the web.		

Notes:

1. *Only one output tested at a time. V_{CC} = min.*
2. *Includes worst-case 84-pin PLCC package capacitance. V_{OUT} = 0 V, f = 1 MHz.*
3. *Typical standby current = 0.3 mA. All outputs unloaded. All inputs = V_{CC} or GND.*
4. *The IBIS model can be found at www.actel.com/support/support/support_ibis.html.*

Package Thermal Characteristics

The device junction to case thermal characteristic is θ_{jc}, and the junction to ambient air characteristic is θ_{ja}. The thermal characteristics for θ_{ja} are shown with two different air flow rates.

Maximum junction temperature is 150°C.

A sample calculation of the absolute maximum power dissipation allowed for a PQFP 160-pin package with still air at commercial temperature is as follows:

$$\frac{\text{Max. junction temp. (°C)} - \text{Max. commercial temp.}}{\theta_{ja}\ (°C/W)} = \frac{150°C - 70°C}{34°C/W} = 2.4W$$

Package Type	Pin Count	θ_{ja}		Maximum Power Dissipation	
		Still Air	300 ft/min	Still Air	300 ft/min
Plastic Quad Flat Pack	100	42°C/W	33°C/W	1.9 W	2.4 W
Plastic Quad Flat Pack	144	36°C/W	29°C/W	2.2 W	2.8 W
Plastic Quad Flat Pack	160	34°C/W	27°C/W	2.4 W	3.0 W
Plastic Quad Flat Pack	208	25°C/W	16.2°C/W	3.2 W	4.9 W
Plastic Leaded Chip Carrier	84	37°C/W	28°C/W	2.2 W	2.9 W
Thin Quad Flat Pack	176	32°C/W	25°C/W	2.5 W	3.2 W
Power Quad Flat Pack	208	16.8°C/W	11.4°C/W	4.8 W	7.0 W
Power Quad Flat Pack	240	16.1°C/W	10.6°C/W	5.0 W	7.5 W
Very Thin Quad Flat Pack	100	43°C/W	35°C/W	1.9 W	2.3 W

Power Dissipation

General Power Equation

$$P = [I_{CC}standby + I_{CC}active] * V_{CC} + I_{OL} * V_{OL} * N + I_{OH} * (V_{CC} - V_{OH}) * M$$

where:

I_{CC}standby is the current flowing when no inputs or outputs are changing.

I_{CC}active is the current flowing due to CMOS switching.

I_{OL}, I_{OH} are TTL sink/source currents.

V_{OL}, V_{OH} are TTL level output voltages.

N equals the number of outputs driving TTL loads to V_{OL}.

M equals the number of outputs driving TTL loads to V_{OH}.

An accurate determination of N and M is problematic because their values depend on the family type, design details, and on the system I/O. The power can be divided into two components: static and active.

Static Power Component

Actel FPGAs have small static power components that result in lower power dissipation than PALs or PLDs. By integrating multiple PALs/PLDs into one FPGA, an even greater reduction in board-level power dissipation can be achieved.

The power dissipation due to standby current is typically a small component of the overall power. Standby power is calculated below for commercial worst case conditions.

I_{CC}	V_{CC}	Power
2 mA	5.25 V	10.5 mW

The static power dissipation by TTL loads depends on the number of outputs driving HIGH or LOW and the DC load current. Again, this number is typically small. For instance, a 32-bit bus sinking 4 mA at 0.33V will generate 42 mW with all outputs driving LOW and 140 mW with all outputs driving HIGH. The actual dissipation will average somewhere in between as I/Os switch states with time.

Active Power Component

Power dissipation in CMOS devices is usually dominated by the active (dynamic) power dissipation. This component is frequency-dependent, a function of the logic and the external I/O. Active power dissipation results from charging internal chip capacitances of the interconnect, unprogrammed antifuses, module inputs, and module outputs, plus external capacitance due to PC board traces and load device inputs. An additional component of the active power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent active power dissipation.

Equivalent Capacitance

The power dissipated by a CMOS circuit can be expressed by Equation 1

$$\text{Power } (\mu W) = C_{EQ} * V_{CC}^2 * F \quad (1)$$

where:

C_{EQ} is the equivalent capacitance expressed in picofarads (pF).

V_{CC} is power supply in volts (V).

F is the switching frequency in megahertz (MHz).

Equivalent capacitance is calculated by measuring $I_{CCactive}$ at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of V_{CC}. Equivalent capacitance is frequency-independent, so the results may be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

C_{EQ} Values for Actel FPGAs

Modules (C_{EQM})	5.2
Input Buffers (C_{EQI})	11.6
Output Buffers (C_{EQO})	23.8
Routed Array Clock Buffer Loads (C_{EQCR})	3.5

To calculate the active power dissipated from the complete design, the switching frequency of each part of the logic must be known. Equation 2 shows a piece-wise linear summation over all components.

$$\text{Power} = V_{CC}^2 * [(m \times C_{EQM} * f_m)_{Modules} + (n * C_{EQI} * f_n)_{Inputs} + (p * (C_{EQO} + C_L) * f_p)_{outputs} + 0.5 * (q_1 * C_{EQCR} * f_{q1})_{routed\_Clk1} + (r_1 * f_{q1})_{routed\_Clk1} + 0.5 * (q_2 * C_{EQCR} * f_{q2})_{routed\_Clk2} + (r_2 * f_{q2})_{routed\_Clk2} \quad (2)$$

where:

m = Number of logic modules switching at frequency f_m

n = Number of input buffers switching at frequency f_n

p = Number of output buffers switching at frequency f_p

q_1 = Number of clock loads on the first routed array clock

q_2 = Number of clock loads on the second routed array clock

r_1 = lFixed capacitance due to first routed array clock

r_2 = Fixed capacitance due to second routed array clock

C_{EQM} = Equivalent capacitance of logic modules in pF

C_{EQI} = Equivalent capacitance of input buffers in pF

C_{EQO} = Equivalent capacitance of output buffers in pF

C_{EQCR} = Equivalent capacitance of routed array clock in pF

C_L = Output load capacitance in p

f_m = Average logic module switching rate in MHz

f_n = Average input buffer switching rate in MHz

f_p = Average output buffer switching rate in MHz

f_{q1} = Average first routed array clock rate in MHz

f_{q2} = Average second routed array clock rate in MHz

Fixed Capacitance Values for Actel FPGAs (pF)

Table 5.

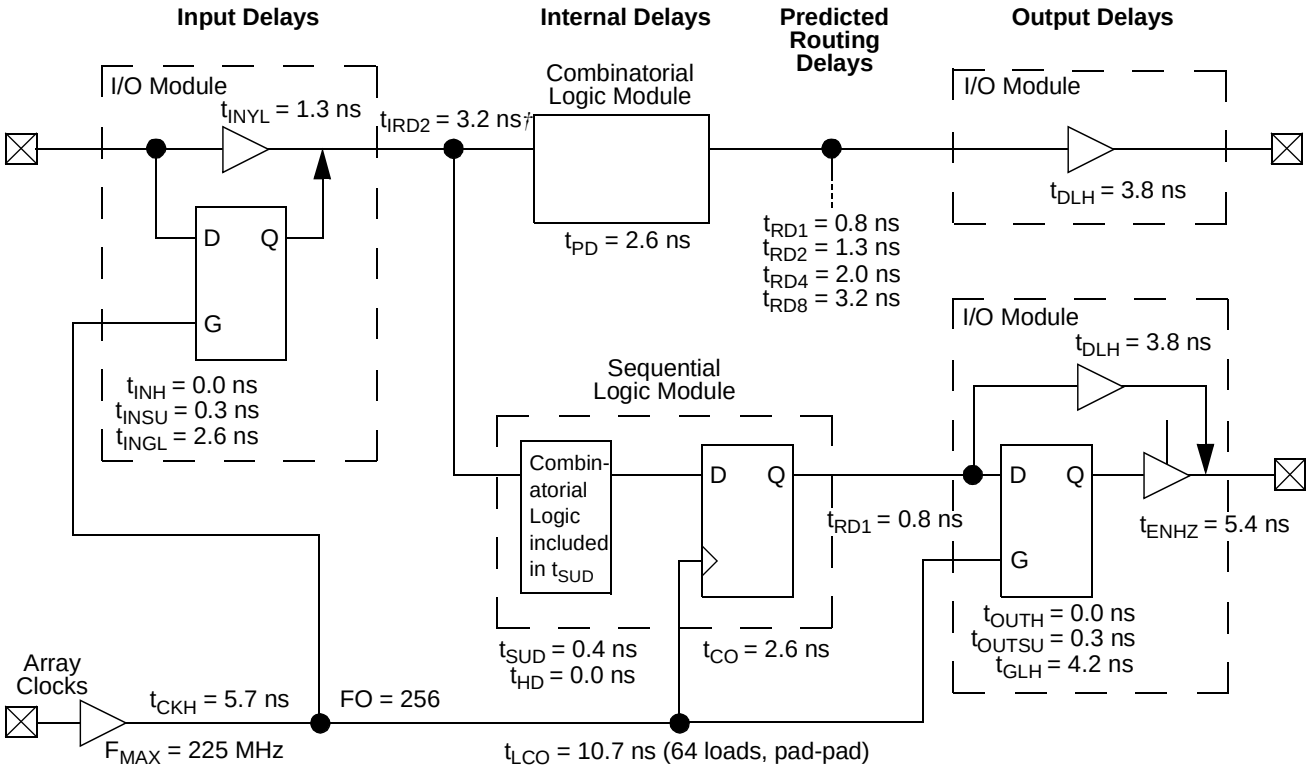
Device Type	r_1 routed_Clk1	r_2 routed_Clk2
A1225XL	106	106
A1240XL	134	134
A3265DX	158	158
A1280XL	168	168
A32100DX	178	178
A32140DX	190	190
A32200DX	230	230
A32300DX	285	285

Determining Average Switching Frequency

To determine the switching frequency for a design, the user must have a detailed understanding of the data input values to the circuit. The following guidelines represent worst-case scenarios; they can be generally used to predict the upper limits of power dissipation.

Logic Modules (m)	=	80% of Combinatorial Modules
Inputs Switching (n)	=	# of Inputs/4
Outputs Switching (p)	=	# Outputs/4
First Routed Array Clock Loads (q_1)	=	40% of Sequential Modules
Second Routed Array Clock Loads (q_2)	=	40% of Sequential Modules
Load Capacitance (C_L)	=	35 pF
Average Logic Module Switching Rate (f_m)	=	F/10
Average Input Switching Rate (f_n)	=	F/5
Average Output Switching Rate (f_p)	=	F/10
Average First Routed Array Clock Rate (f_{q1})	=	F
Average Second Routed Array Clock Rate (f_{q2})	=	F/2

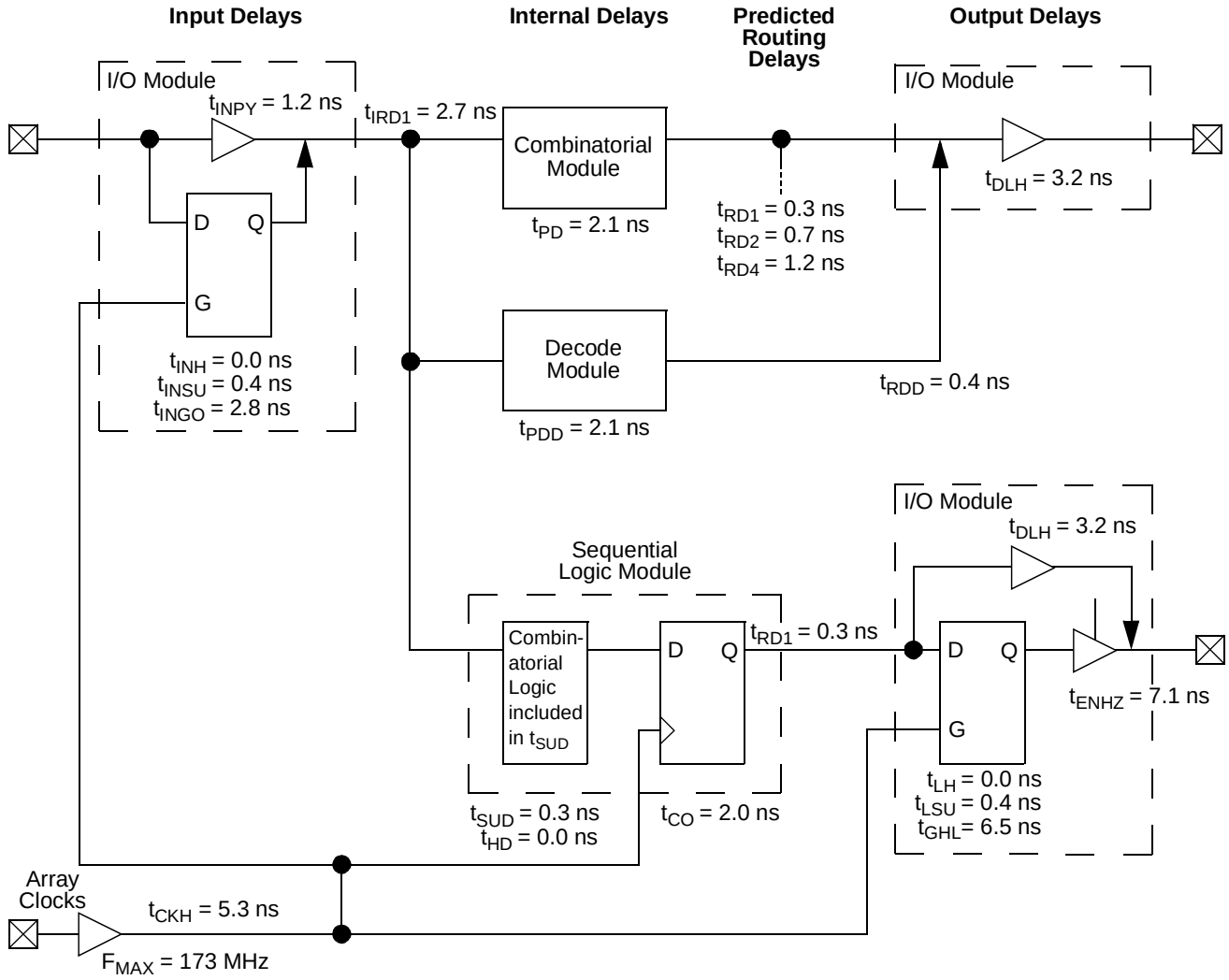
1200XL Timing Model*



Notes:

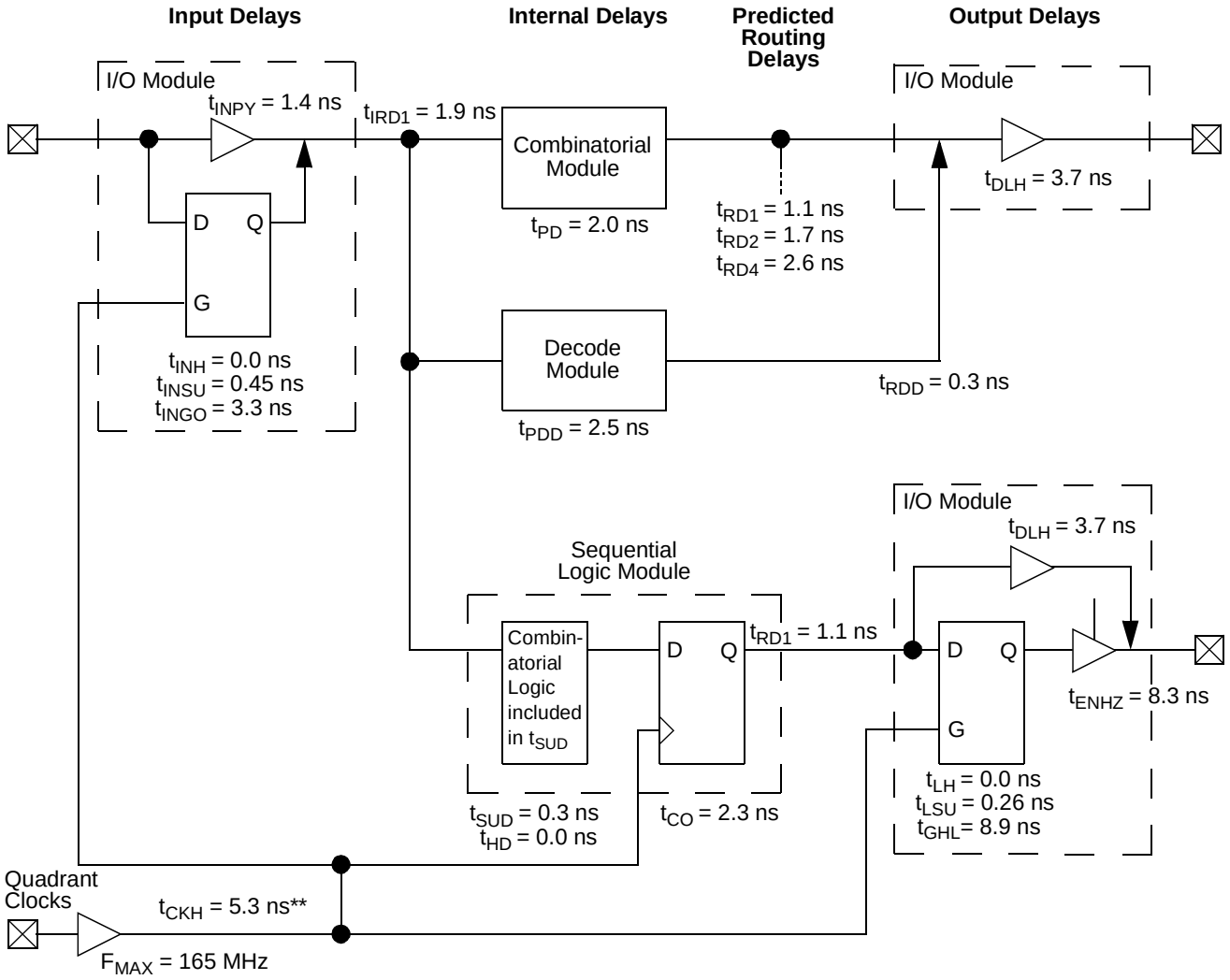
1. **Values shown for A1225XL-2 at worst-case commercial conditions.†*
2. *Input Module Predicted Routing Delay*

3200DX Timing Model (Logic Functions using Array Clocks)*



**Values shown for A3265DX-2 at worst-case commercial conditions.*

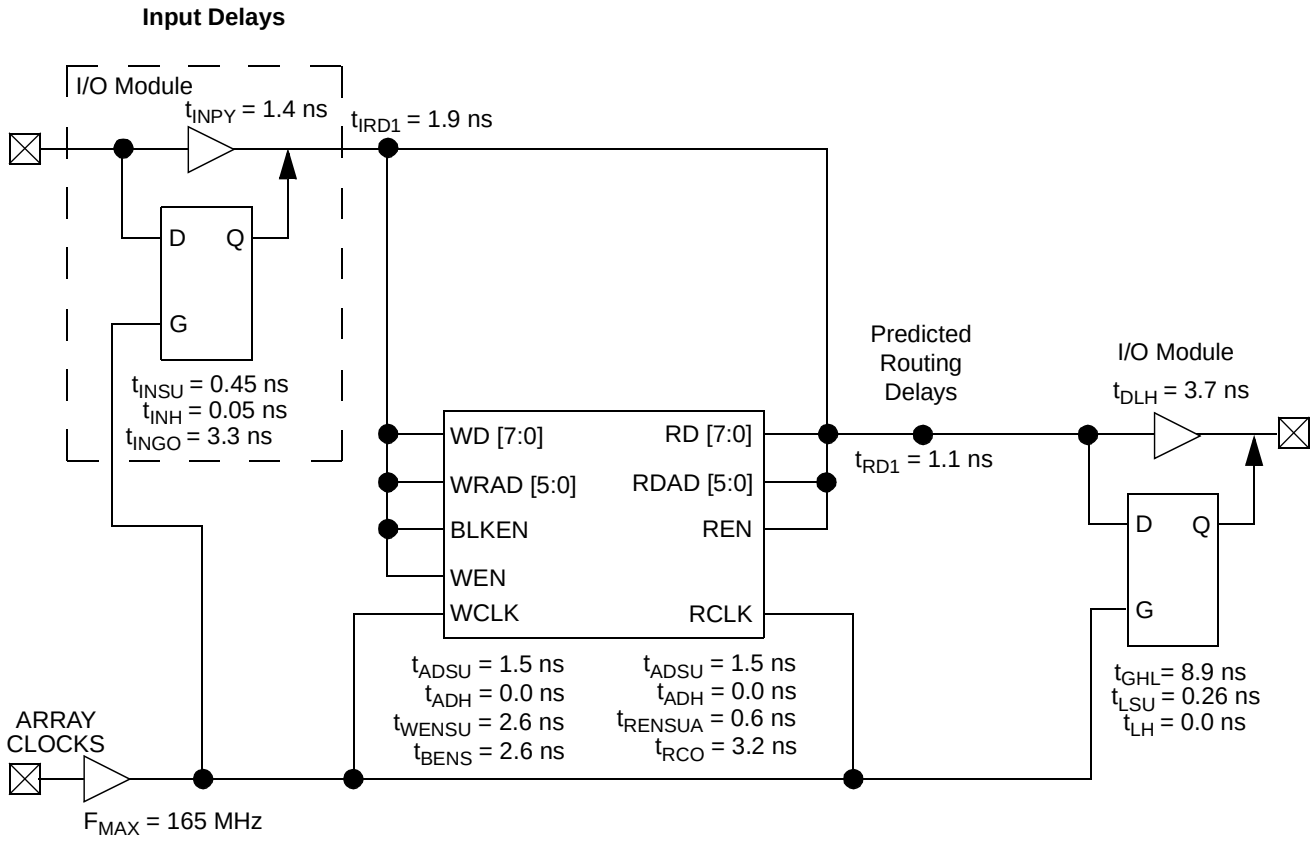
3200DX Timing Model (Logic Functions using Quadrant Clocks)*



** Preliminary values shown for A32200DX-3 at worst-case commercial conditions.*

*** Load-dependent.*

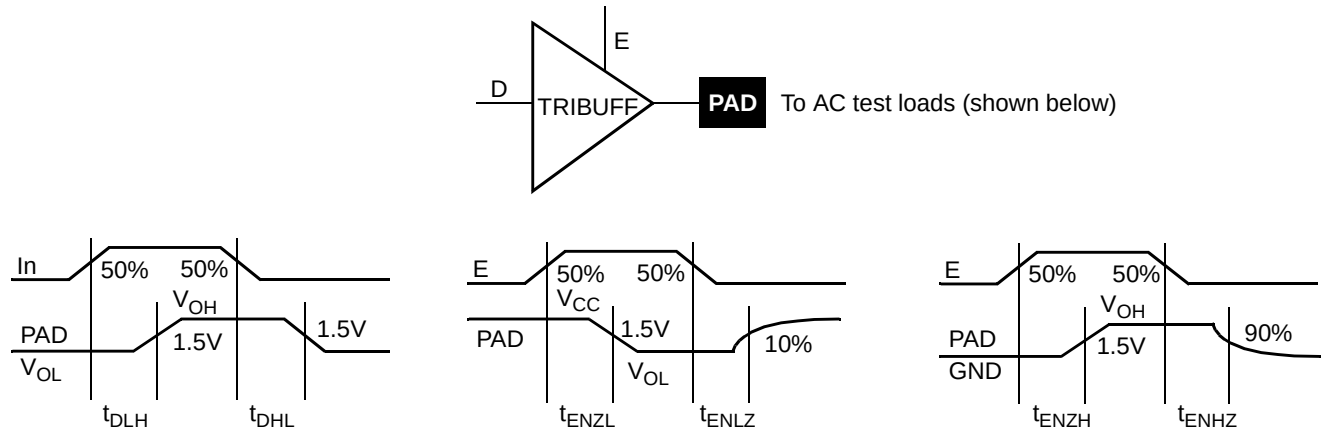
3200DX Timing Model (SRAM Functions)*



**Values shown for A32200DX-3 at worst-case commercial conditions.*

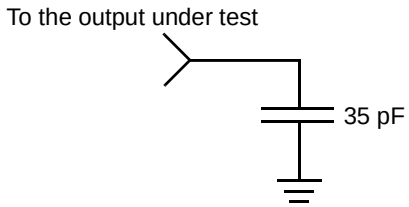
Parameter Measurement

Output Buffer Delays

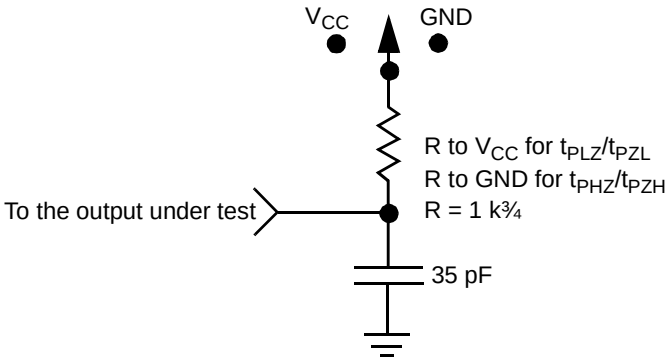


AC Test Loads

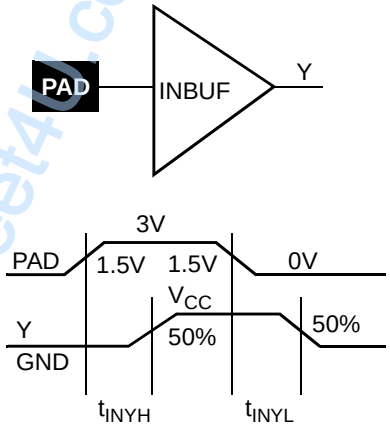
Load 1
(Used to measure propagation delay)



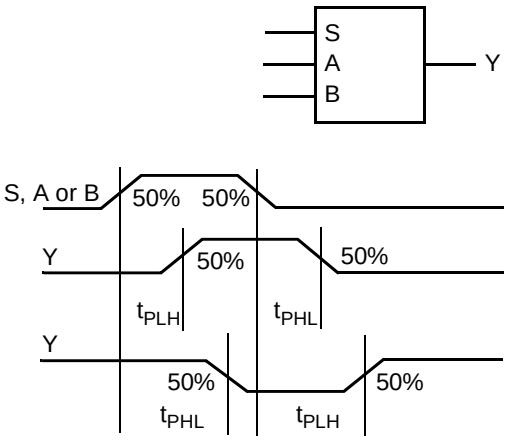
Load 2
(Used to measure rising/falling edges)



Input Buffer Delays

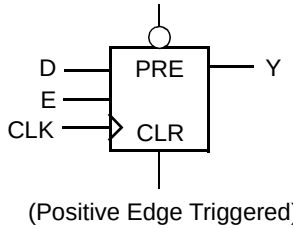


Module Delays

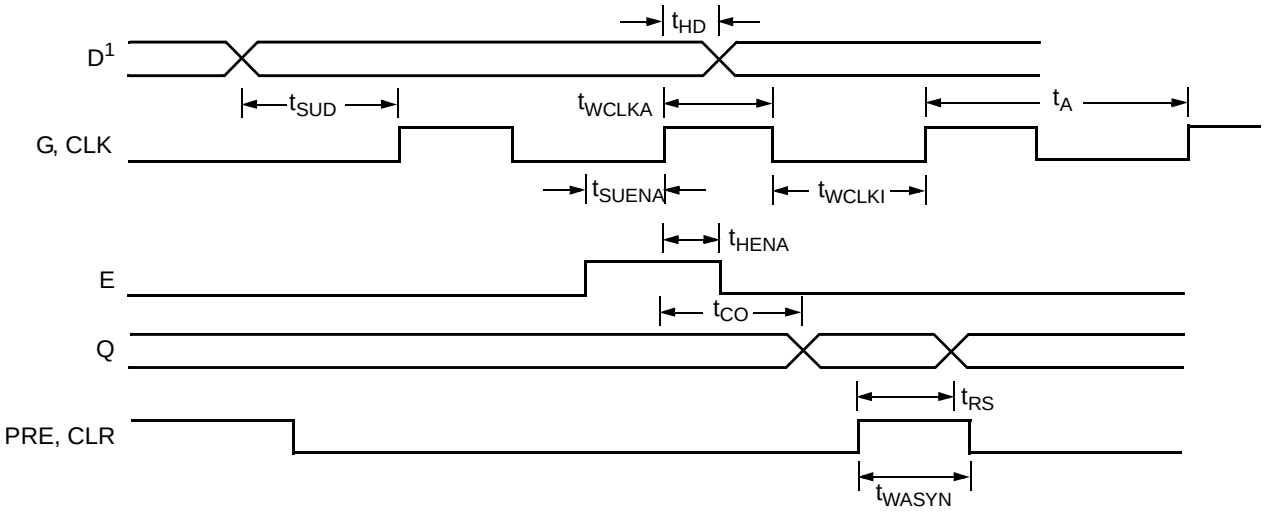


Sequential Module Timing Characteristics

Flip-Flops and Latches



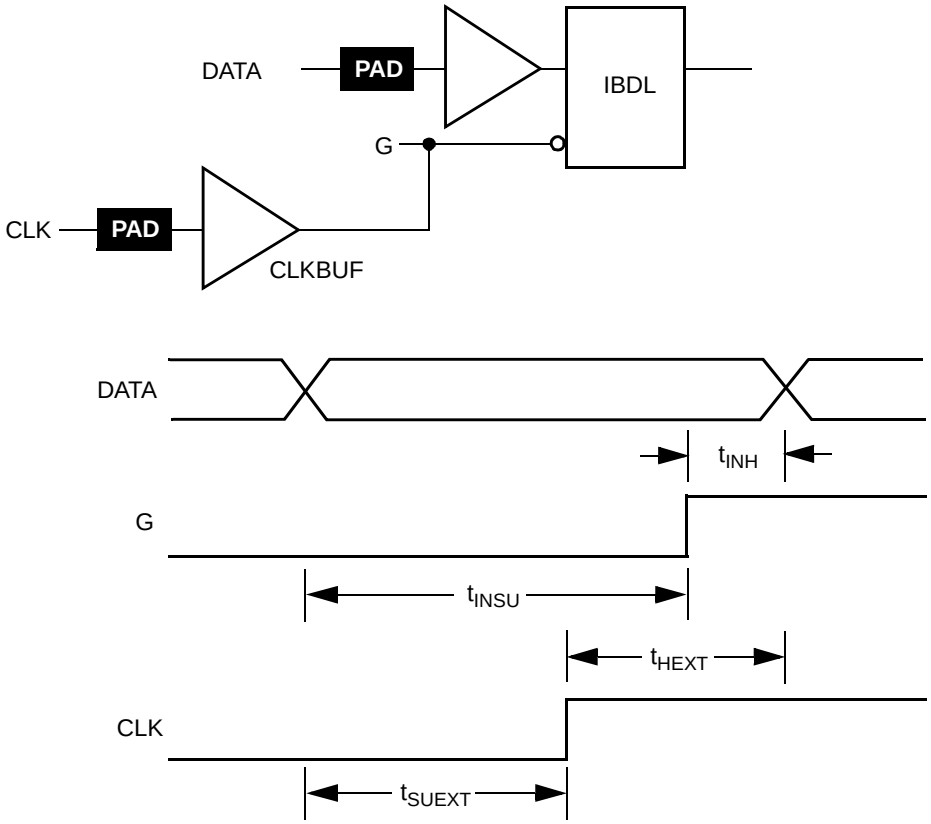
(Positive Edge Triggered)



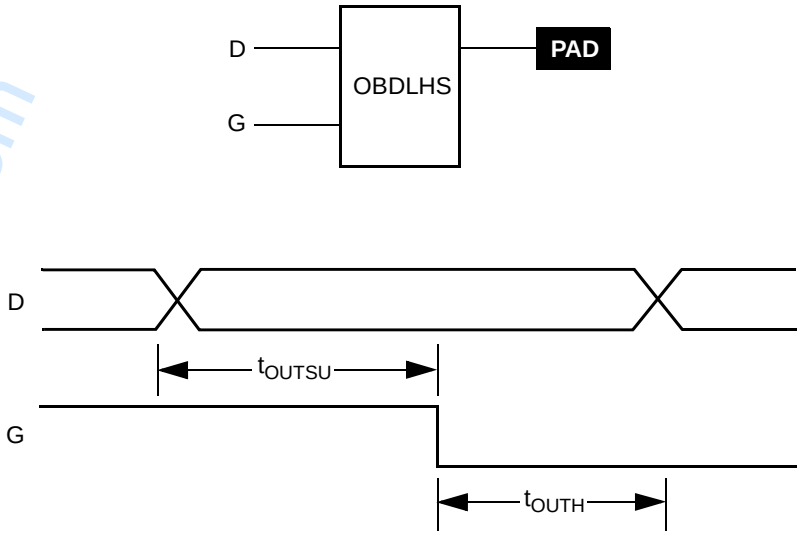
Note: *D represents all data functions involving A, B, and S for multiplexed flip-flops.*

Sequential Timing Characteristics (continued)

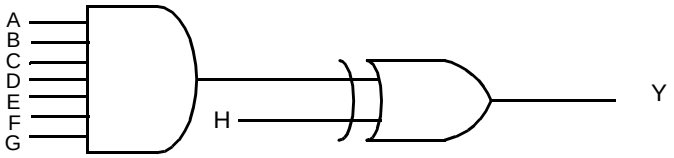
Input Buffer Latches

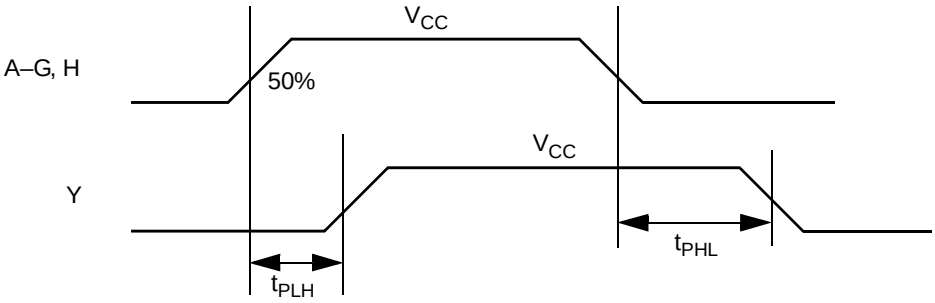


Output Buffer Latches

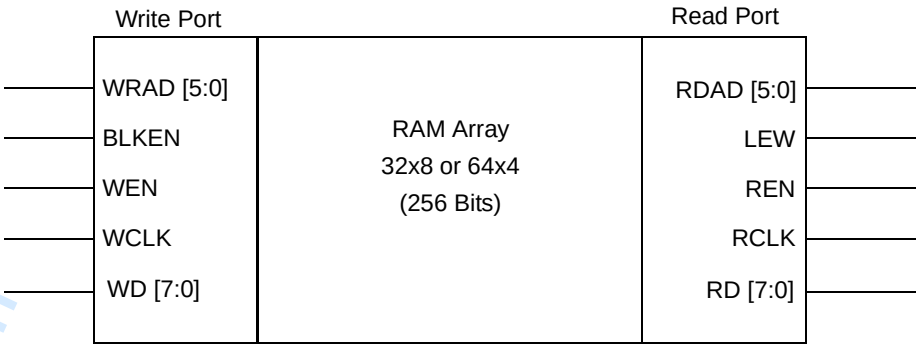


Decode Module Timing



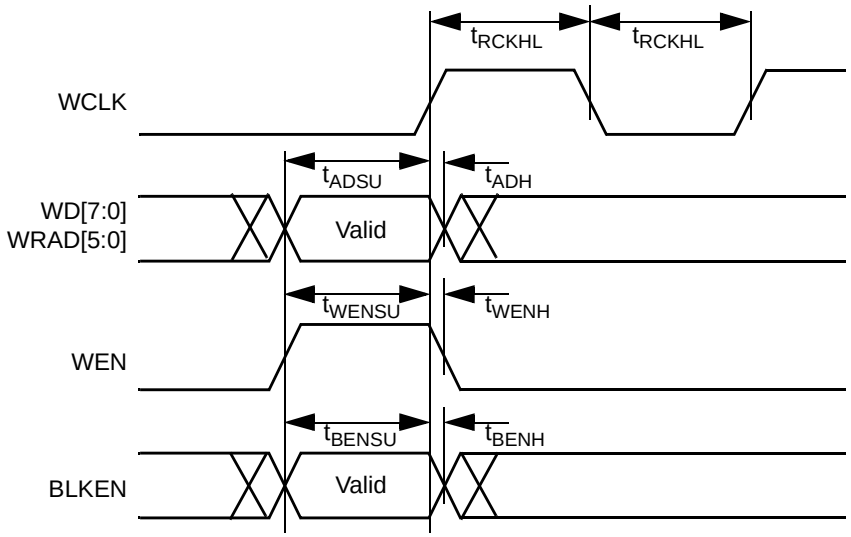


SRAM Timing Characteristics



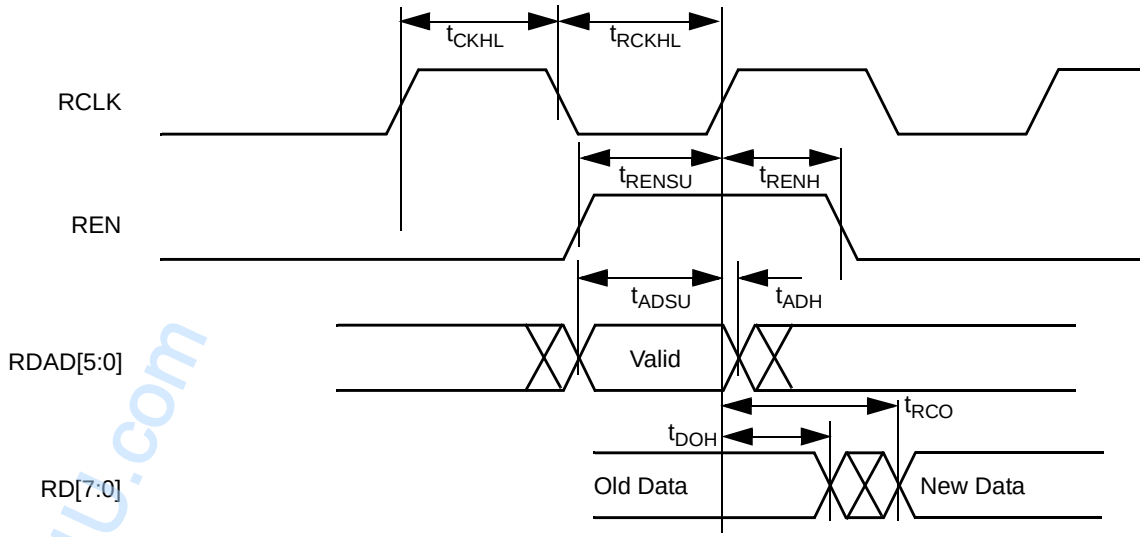
Dual-Port SRAM Timing Waveforms

3200DX SRAM Write Operation



Note: *Identical timing for falling-edge clock.*

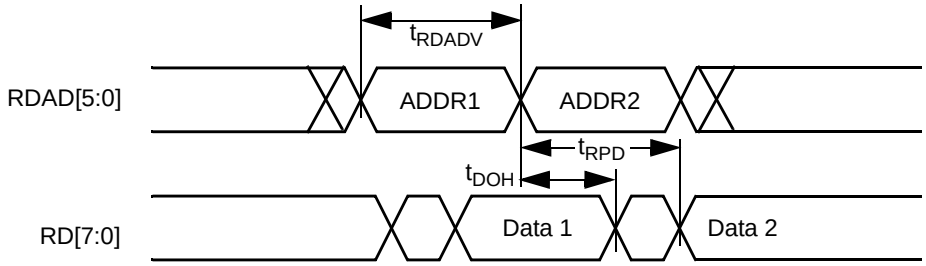
3200DX SRAM Synchronous Read Operation



Note: *Identical timing for falling-edge clock.*

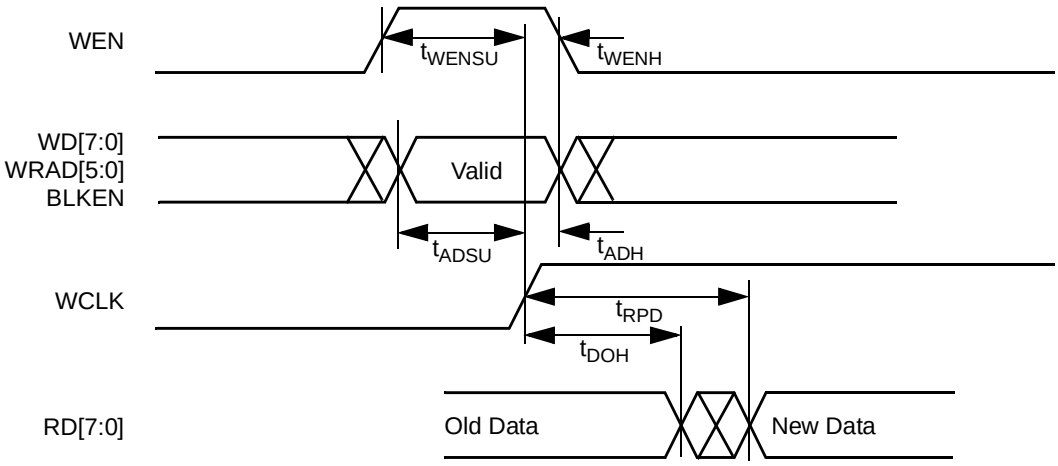
3200DX SRAM Asynchronous Read Operation—Type 1

(Read Address Controlled)



3200DX SRAM Asynchronous Read Operation—Type 2

(Write Address Controlled)



Predictable Performance: Tight Delay Distributions

Propagation delay between logic modules depends on the resistive and capacitive loading of the routing tracks, the interconnect elements, and the module inputs being driven. Propagation delay increases as the length of routing tracks, the number of interconnect elements, or the number of inputs increase.

From a design perspective, the propagation delay can be statistically correlated or modeled by the fanout (number of loads) driven by a module. Higher fanout usually requires some paths to have longer routing tracks.

The Integrator Series delivers a very tight fanout delay distribution. This tight distribution is achieved in two ways: by decreasing the delay of the interconnect elements and by decreasing the number of interconnect elements per path.

Actel's patented PLICE antifuse offers a very low resistive/capacitive interconnect. The antifuses, fabricated in 0.6 micron lithography, offer nominal levels of 100 ohms resistance and 7.0 femtofarad (fF) capacitance per antifuse.

The Integrator Series fanout distribution is also tight due to the low number of antifuses required for each interconnect path. The proprietary architecture limits the number of antifuses per path to a maximum of four, with 90% of interconnects using two antifuses.

Timing Characteristics

Timing characteristics for devices fall into three categories: family-dependent, device-dependent, and design-dependent. The input and output buffer characteristics are common to all Integrator Series members. Internal routing delays are device-dependent. Design dependency means actual delays are not determined until after placement and routing of the user's design is complete. Delay values may then be determined by using the Designer Series utility or performing simulation with post-layout delays.

Critical Nets and Typical Nets

Propagation delays in this data sheet apply to typical nets, which are used for initial design performance evaluation. The abundant routing resources in the Integrator Series architecture allows for deterministic timing. Using DirectTime, a timing-driven place and route tool in Actel's Designer Series development software, the designer may specify timing-critical nets and system clock frequency. Using these timing specifications, the place and route software optimize the design layout to meet the user's specifications.

Long Tracks

Some nets in the design use long tracks, which are special routing resources that span multiple rows, columns, or modules. Long tracks employ three and sometimes four antifuse connections. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6% of nets in a fully utilized device require long tracks. Long tracks contribute approximately 3 ns to 6 ns delay, which is represented statistically in higher fanout (FO=8) routing delays in the data sheet specifications section.

Timing Derating

A timing derating factor of 0.45 is used to reflect best-case processing. Note that this factor is relative to the "standard speed" timing parameters, and must be multiplied by the appropriate voltage and temperature derating factors for a given application.

Timing Derating Factor (Temperature and Voltage)

	Industrial		Military	
	Min.	Max.	Min.	Max.
(Commercial Specification) x	0.69	1.11	0.67	1.23

Timing Derating Factor for Designs at Typical Temperature (T_J = 25°C) and Voltage (5.0V)

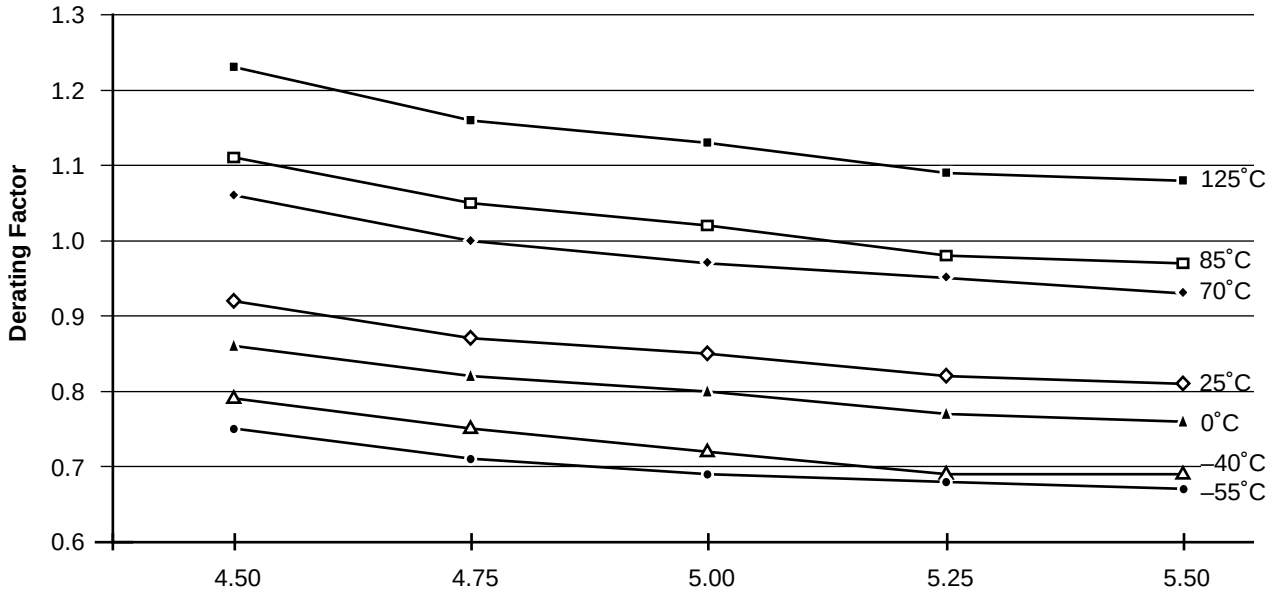
(Maximum Specification, Worst-Case Condition) x	0.85

Note: *This derating factor applies to all routing and propagation delays.*

Temperature and Voltage Derating Factors (Normalized to Worst-Case Commercial, T_J = 4.75V, 70°C)

	–55	–40	0	25	70	85	125
4.50	0.75	0.79	0.86	0.92	1.06	1.11	1.23
4.75	0.71	0.75	0.82	0.87	1.00	1.05	1.16
5.00	0.69	0.72	0.80	0.85	0.97	1.02	1.13
5.25	0.68	0.69	0.77	0.82	0.95	0.98	1.09
5.50	0.67	0.69	0.76	0.81	0.93	0.97	1.08

Junction Temperature and Voltage Derating Curves (Normalized to Worst-Case Commercial, T_J = 4.75V, 70°C)



Note: *This derating factor applies to all routing and propagation delays.*

A1225XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]												
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		0.8		0.9		1.1		1.57		1.3	ns
t_{RD2}	FO=2 Routing Delay		1.3		1.4		1.7		2.43		2.0	ns
t_{RD3}	FO=3 Routing Delay		1.7		1.8		2.2		3.15		2.6	ns
t_{RD4}	FO=4 Routing Delay		2.0		2.3		2.7		3.86		3.2	ns
t_{RD8}	FO=8 Routing Delay		3.2		3.5		4.2		6.00		5.0	ns
Sequential Timing Characteristics[3,4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.2		3.6		4.3		6.1		5.2		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.2		3.6		4.3		6.1		5.2		ns
t_A	Flip-Flop Clock Input Period	6.5		7.4		8.7		12.4		10.4		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		225		200		170		120		115	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*
5. *V_{CC} = 3.0V for 3.3V specifications.*

A1225XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad-to-Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G-to-Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G-to-Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.9		3.3		3.9		5.6		4.7	ns
t_{IRD2}	FO=2 Routing Delay			3.2		3.6		4.3		6.1		5.2	ns
t_{IRD3}	FO=3 Routing Delay			3.8		4.2		5.0		7.2		6.0	ns
t_{IRD4}	FO=4 Routing Delay			4.1		4.6		5.4		7.7		6.5	ns
t_{IRD8}	FO=8 Routing Delay			5.2		5.9		6.9		9.9		8.3	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32 FO = 256		5.1 5.7		5.8 6.5		6.8 7.6		9.7 10.9		8.2 9.1	ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		5.0 5.7		5.7 6.5		6.7 7.6		9.6 10.9		8.0 9.1	ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	2.6 2.7		3.0 3.1		3.5 3.6		5.0 5.1		4.2 4.3		ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	2.6 2.7		3.0 3.1		3.5 3.6		5.0 5.1		4.2 4.3		ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.8 0.8		0.9 0.9		1.0 1.0		1.4 1.4		1.2 1.2	ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	2.6 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.1 5.2		ns
t_P	Minimum Period	FO = 32 FO = 256	5.4 5.6		6.1 6.3		7.2 7.4		10.3 10.6		8.6 8.9		ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		225 200		200 180		170 155		120. 105		115 105	MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A1225XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std" Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data-to-Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.9		6.5	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		9.0		10.0		12.0		17.2		14.4	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		12.8		14.4		17.0		24.3		20.4	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data-to-Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		10.7		11.8		14.2		20.3		17.0	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		15.0		17.0		20.0		28.6		24.0	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Note:

1. Delays based on 35 pF loading.

A1240XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic ModulePropagation Delays[1]												
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		1.1		1.2		1.4		2.0		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.3		1.4		1.7		2.4		2.0	ns
t_{RD3}	FO=3 Routing Delay		1.7		1.9		2.2		3.1		2.6	ns
t_{RD4}	FO=4 Routing Delay		2.3		2.6		3.0		4.3		3.6	ns
t_{RD8}	FO=8 Routing Delay		3.4		3.8		4.5		6.4		5.4	ns
Sequential Timing Characteristics[3, 4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.4		3.8		4.5		6.4		5.4		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.4		3.8		4.5		6.4		5.4		ns
t_A	Flip-Flop Clock Input Period	6.8		7.7		9.1		13.0		10.9		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		215		190		160		110		105	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*
5. *V_{CC} = 3.0V for 3.3V specifications.*

A1240XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad-to-Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G-to-Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G-to-Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.9		3.3		3.9		5.6		4.7	ns
t_{IRD2}	FO=2 Routing Delay			3.4		3.8		4.5		6.4		5.4	ns
t_{IRD3}	FO=3 Routing Delay			3.8		4.3		5.1		7.3		6.1	ns
t_{IRD4}	FO=4 Routing Delay			4.1		4.7		5.5		7.9		6.6	ns
t_{IRD8}	FO=8 Routing Delay			5.6		6.3		7.4		10.6		8.9	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32 FO = 256		5.1 5.7		5.8 6.5		6.8 7.6		9.7 10.9		8.2 9.1	ns ns
t_{CKL}	Input High to Low	FO = 32 FO = 256		5.0 5.7		5.7 6.5		6.7 7.6		9.6 10.9		8.0 9.1	ns ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 256	2.7 2.9		3.1 3.3		3.6 3.9		5.1 5.6		4.3 4.7		ns ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 256	2.7 2.9		3.1 3.3		3.6 3.9		5.1 5.6		4.3 4.7		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 256		0.8 0.8		0.9 0.9		1.0 1.0		1.4 1.4		1.2 1.2	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 256	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 256	2.6 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.1 5.2		ns ns
t_P	Minimum Period	FO = 32 FO = 256	5.6 6.0		6.3 6.8		7.4 8.0		10.6 11.4		8.9 9.6		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 256		215 195		190 170		160 144		110 100		105 95	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A1240XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data-to-Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		9.2		10.5		12.3		17.6		14.8	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		12.9		14.6		17.2		24.6		20.6	ns
d_{TLH}	Capacity Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data-to-Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		10.9		12.4		14.5		20.7		17.4	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		15.2		17.2		20.3		29.0		24.4	ns
d_{TLH}	Capacity Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacity Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Note:

1. Delays based on 35 pF loading.

A3265DX Timing Characteristics

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic ModulePropagation Delays[1]												
Combinatorial Functions												
t_{PD}	Internal Array Module Delay		2.1		2.4		2.9		3.7		3.2	ns
t_{PDD}	Internal Decode Module Delay		2.5		2.8		3.4		4.4		3.7	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		0.3		0.4		0.5		0.6		0.5	ns
t_{RD2}	FO=2 Routing Delay		0.7		0.8		0.9		1.2		1.0	ns
t_{RD3}	FO=3 Routing Delay		1.0		1.2		1.4		1.8		1.6	ns
t_{RD4}	FO=4 Routing Delay		1.4		1.6		1.9		2.4		2.1	ns
t_{RD5}	FO=8 Routing Delay		2.7		3.2		3.7		4.9		4.1	ns
t_{RDD}	Decode-to-Output Routing Delay		0.46		0.5		0.62		0.8		0.7	ns
Sequential Timing Characteristics[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.3		2.7		3.1		4.1		3.5	ns
t_{GO}	Latch Gate-to-Output		2.1		2.4		2.9		3.7		3.2	ns
t_{SUD}	Flip-Flop (Latch) Set-Up Time	0.35		0.4		0.47		0.6		0.5		ns
t_{HD}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.3		2.7		3.1		4.1		3.5	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.75		0.9		1.0		1.3		1.1		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.7		4.2		4.9		6.4		5.5		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.9		5.5		6.5		8.4		7.1		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$ or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*
5. *V_{CC} = 3.0V for 3.3V specifications.*

A3265DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INPY}	Input Data Pad-to-Y			1.4		1.6		1.9		2.4		2.1	ns
t_{INGO}	Input Latch Gate-to-Output			3.3		3.7		4.4		5.7		4.8	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up		0.5		0.6		0.7		0.9		0.8		ns
t_{ILA}	Latch Active Pulse Width		5.1		5.9		6.9		9.0		7.7		ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			3.2		3.7		4.3		5.6		4.8	ns
t_{IRD2}	FO=2 Routing Delay			3.6		4.2		4.9		6.4		5.4	ns
t_{IRD3}	FO=3 Routing Delay			3.9		4.5		5.3		6.9		5.9	ns
t_{IRD4}	FO=4 Routing Delay			4.5		5.2		6.1		7.9		6.7	ns
t_{IRD5}	FO=8 Routing Delay			6.6		7.5		8.8		11.4		9.7	ns
t_{IRDD}	Decode-to-Output Routing Delay			0.37		0.4		0.5		0.7		0.6	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO=32 FO=256		6.3 7.4		7.1 8.4		8.4 9.9		10.9 12.8		9.2 10.9	ns ns
t_{CKL}	Input High to Low	FO=32 FO=256		5.9 6.4		6.6 7.3		7.8 8.6		10.1 11.2		8.6 9.5	ns ns
t_{PW}	Minimum Pulse Width	FO=32 FO=256	3.2 3.4		3.7 3.9		4.3 4.6		5.6 6.0		4.8 5.1		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=256		0.75 0.75		0.9 0.9		1.0 1.0		1.3 1.3		1.1 1.1	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=256	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=256	2.5 2.5		2.9 2.9		3.4 3.4		4.4 4.4		3.8 3.8		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=256	5.0 6.0		7.2 8.3		8.3 9.5		11.9 13.6		9.2 10.6		ns ns
f_{MAX}	Maximum Datapath Frequency	FO=32 FO=256		173 151		138 121		120 105		84 74		108 95	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A3265DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.8		4.3		5.0		6.5		5.5	ns
t_{DHL}	Data-to-Pad Low		4.6		5.2		6.1		7.9		6.7	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.4		6.4		8.3		7.1	ns
t_{ENZL}	Enable-Pad Z to Low		5.2		5.9		6.9		9.0		7.6	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.5		11.1		14.5		12.3	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.5		11.1		14.5		12.3	ns
t_{GLH}	G-to-Pad High		8.3		9.4		11.1		14.4		12.3	ns
t_{GHL}	G-to-Pad Low		7.7		8.7		10.2		13.3		11.3	ns
t_{LSU}	I/O Latch Output Set-Up	0.5		0.6		0.7		0.9		0.8		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.8		11.1		13.1		17.0		14.5	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad)32 I/O		13.9		15.7		18.5		24.1		20.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.037		0.04		0.05		0.071		0.06	ns/pF
d_{TLL}	Capacitive Loading, High to Low		0.05		0.03		0.07		0.1		0.08	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.3		0.4		0.5		0.7		0.6	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		4.6		5.2		6.1		7.9		6.7	ns
t_{DHL}	Data-to-Pad Low		3.8		4.3		5.0		6.5		5.5	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.5		6.4		8.4		7.1	ns
t_{ENZL}	Enable-Pad Z to Low		5.2		5.9		6.9		9.0		7.6	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.5		11.1		14.5		12.3	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.5		11.1		14.5		12.3	ns
t_{GLH}	G-to-Pad High		8.3		9.4		11.1		14.4		12.3	ns
t_{GHL}	G-to-Pad Low		9.0		10.2		12.0		15.6		13.3	ns
t_{LSU}	I/O Latch Set-Up	0.5		0.6		0.7		0.9		0.8		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		11.7		13.3		15.6		20.3		17.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		16.4		18.5		21.8		28.3		24.1	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.1		0.1	ns/pF
d_{TLL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.1		0.1	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.3		0.4		0.5		0.7		0.6	ns/pF

Note:

1. Delays based on 35pF loading.

A1280XL Timing Characteristics

(Worst-Case Commercial Conditions, V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic ModulePropagation Delays[1]												
t_{PD1}	Single Module		2.6		3.0		3.5		5.0		4.2	ns
t_{CO}	Sequential Clk-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{GO}	Latch G-to-Q		2.6		3.0		3.5		5.0		4.2	ns
t_{RS}	Flip-Flop (Latch) Reset-to-Q		2.6		3.0		3.5		5.0		4.2	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		1.3		1.4		1.7		2.4		2.0	ns
t_{RD2}	FO=2 Routing Delay		1.8		2.0		2.4		3.4		2.9	ns
t_{RD3}	FO=3 Routing Delay		2.2		2.5		2.9		4.1		3.5	ns
t_{RD4}	FO=4 Routing Delay		2.6		3.0		3.5		5.0		4.2	ns
t_{RD8}	FO=8 Routing Delay		5.0		5.7		6.7		9.6		8.0	ns
Sequential Timing Characteristics[3,4]												
t_{SUD}	Flip-Flop (Latch) Data Input Set-Up	0.4		0.4		0.5		0.7		0.6		ns
t_{HD}	Flip-Flop (Latch) Data Input Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.8		0.9		1.0		1.4		1.2		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.7		4.3		4.9		7.0		5.9		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.7		4.3		4.9		7.0		5.9		ns
t_A	Flip-Flop Clock Input Period	8.0		8.7		10.0		14.0		12.0		ns
t_{INH}	Input Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
t_{OUTH}	Output Buffer Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{OUTSU}	Output Buffer Latch Set-Up	0.3		0.4		0.4		0.6		0.5		ns
f_{MAX}	Flip-Flop (Latch) Clock Frequency		200		167		130		90		110	MHz

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDw}$, $t_{CO} + t_{RD1} + t_{PDw}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*
5. *V_{CC} = 3.0V for 3.3V specifications.*

A1280XL Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INYH}	Pad-to-Y High			1.1		1.2		1.4		2.0		1.7	ns
t_{INYL}	Pad-to-Y Low			1.3		1.4		1.7		2.4		2.0	ns
t_{INGH}	G-to-Y High			2.0		2.3		2.7		3.9		3.2	ns
t_{INGL}	G-to-Y Low			2.6		3.0		3.5		5.0		4.2	ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			3.2		3.7		4.3		6.1		5.2	ns
t_{IRD2}	FO=2 Routing Delay			3.7		4.2		4.9		7.0		5.9	ns
t_{IRD3}	FO=3 Routing Delay			4.0		4.5		5.3		7.6		6.4	ns
t_{IRD4}	FO=4 Routing Delay			4.6		5.2		6.1		8.7		7.3	ns
t_{IRD8}	FO=8 Routing Delay			6.6		7.5		8.8		12.6		10.6	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO = 32 FO = 384		5.1 5.7		5.8 6.5		6.8 7.6		9.7 10.9		8.2 9.1	ns ns
t_{CKL}	Input High to Low	FO = 32 FO = 384		5.0 5.7		5.7 6.5		6.7 7.6		9.6 10.9		8.0 9.1	ns ns
t_{PWH}	Minimum Pulse Width High	FO = 32 FO = 384	3.2 3.5		3.5 3.9		4.3 4.6		6.1 6.6		5.2 5.5		ns ns
t_{PWL}	Minimum Pulse Width Low	FO = 32 FO = 384	3.2 3.5		3.5 3.9		4.3 4.6		6.1 6.6		5.2 5.5		ns ns
t_{CKSW}	Maximum Skew	FO = 32 FO = 384		0.8 0.8		0.9 0.9		1.0 1.0		1.4 1.4		1.2 1.2	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO = 32 FO = 384	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO = 32 FO = 384	2.6 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.1 5.2		ns ns
t_P	Minimum Period	FO = 32 FO = 384	6.5 7.2		7.4 8.0		8.7 9.6		12.4 13.7		10.4 11.5		ns ns
f_{MAX}	Maximum Frequency	FO = 32 FO = 384		200 180		167 150		143 130		100 90		120 110	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A1280XL Timing Characteristics (continued)
(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.8		4.3		5.0		7.1		6.0	ns
t_{DHL}	Data-to-Pad Low		4.1		4.6		5.4		7.7		6.5	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.7		6.6	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		9.8		11.0		13.1		18.7		15.7	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		13.9		15.7		18.5		26.4		22.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.04		0.05		0.06		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.06		0.07		0.08		0.08	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		4.8		5.4		6.4		9.1		7.7	ns
t_{DHL}	Data-to-Pad Low		3.4		3.8		4.5		6.4		5.4	ns
t_{ENZH}	Enable-Pad Z to High		3.8		4.3		5.0		7.1		6.0	ns
t_{ENZL}	Enable-Pad Z to Low		4.1		4.7		5.5		7.9		6.6	ns
t_{ENHZ}	Enable-Pad High to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{ENLZ}	Enable-Pad Low to Z		5.4		6.1		7.2		10.3		8.6	ns
t_{GLH}	G-to-Pad High		4.2		4.8		5.6		8.0		6.7	ns
t_{GHL}	G-to-Pad Low		4.7		5.4		6.3		9.0		7.6	ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad), 64 Clock Loading		11.6		13.0		15.5		22.2		18.6	ns
t_{ACO}	Array Clock-Out (Pad-to-Pad), 64 Clock Loading		16.4		18.5		21.8		31.2		26.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.05		0.06		0.07		0.08		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.05		0.05		0.06		0.07		0.07	ns/pF

Note:

1. Delays based on 35 pF loading.

A32100DX Timing Characteristics

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic ModulePropagation Delays														
Combinatorial Functions														
t_{PD}	Internal Array Module Delay		2.2		2.6		3.0		3.5		5.2		4.1	ns
t_{PDD}	Internal Decode Module Delay		2.4		2.7		3.1		3.7		5.7		4.3	ns
Predicted Module Routing Delays														
t_{RD1}	FO=1 Routing Delay		1.0		1.1		1.3		1.5		3.3		1.7	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.7		1.9		2.2		4.3		2.5	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.1		2.5		2.9		5.2		3.4	ns
t_{RD4}	FO=4 Routing Delay		2.4		2.7		3.1		3.7		6.5		4.3	ns
t_{RD5}	FO=8 Routing Delay		4.2		5.0		5.6		6.6		10.0		7.7	ns
t_{RDD}	Decode-to-Output Routing Delay		0.3		0.37		0.4		0.5		0.4		0.6	ns
Sequential Timing Characteristics														
t_{CO}	Flip-Flop Clock-to-Output		2.2		2.6		3.0		3.5		5.0		4.1	ns
t_{GO}	Latch Gate-to-Output		2.2		2.6		3.0		3.5		5.0		4.1	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.3		0.37		0.4		0.5		0.7		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.2		2.6		3.0		3.5		5.0		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.75		0.9		1.0		1.4		0.85		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		3.7		4.2		4.9		7.0		5.7		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		4.8		5.4		6.4		7.0		7.5		ns

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Timing														
Synchronous SRAM Operations														
t_{RC}	Read Cycle Time	6.4		7.5		8.5		10.0		14.3		11.7		ns
t_{WC}	Write Cycle Time	6.4		7.5		8.5		10.0		14.3		11.7		ns
t_{RCKHL}	Clock High/Low Time	3.2		3.8		4.3		5.0		7.1		5.9		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		3.8		4.3		5.0		7.1		5.9	ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.3		1.0		ns
t_{RENH}	Read Enable Hold	3.2		3.8		4.3		5.0		7.1		5.9		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.7		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.6		3.1		3.5		4.1		5.8		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations														
t_{RPD}	Asynchronous Access Time		7.7		9.0		10.2		12.0		17.2		14.1	ns
t_{RDADV}	Read Address Valid	8.3		9.8		11.1		13.0		18.6		15.2		ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.57		0.7		0.8		0.9		1.3		1.0		ns
t_{RENHA}	Read Enable Hold	3.2		3.8		4.3		5.0		7.1		5.9		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.7		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.35		1.5		1.8		2.6		2.1	ns

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays															
t_{INPY}	Input Data Pad-to-Y			1.4		1.65		1.9		2.2		3.1		2.5	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.9		3.4		3.8		4.5		6.4		5.3	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up[1]		0.45		0.5		0.6		0.7		1.0		0.82		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		4.8		5.9		6.9		9.8		8.1		ns
Input Module Predicted Routing Delays															
t_{IRD1}	FO=1 Routing Delay			1.6		1.75		2.1		2.5		3.6		2.9	ns
t_{IRD2}	FO=2 Routing Delay			2.0		2.4		2.7		3.2		4.6		3.8	ns
t_{IRD3}	FO=3 Routing Delay			2.6		3.0		3.4		4.0		5.7		4.7	ns
t_{IRD4}	FO=4 Routing Delay			2.6		3.0		3.4		4.0		5.7		4.7	ns
t_{IRD8}	FO=8 Routing Delay			4.1		4.8		5.4		6.4		9.1		7.5	ns
Global Clock Network															
t_{CKH}	Input Low to High	FO=32 FO=635		4.7 5.7		5.6 6.75		6.3 7.7		7.4 9.0		10.5 12.8		8.7 10.5	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		4.8 6.4		5.6 7.5		6.4 8.5		7.5 10.0		10.7 14.2		8.8 11.7	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	2.5 2.7		2.9 3.2		3.3 3.7		3.9 4.3		5.6 6.1		4.5 5.0		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	2.5 2.7		2.9 3.2		3.3 3.7		3.9 4.3		5.5 6.1		4.5 5.0		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		0.6 0.6		0.75 0.75		0.9 0.9		1.0 1.0		1.4 1.4		1.8 1.8	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	2.2 2.7		2.5 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.0 6.1		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	5.0 5.5		6.0 6.4		7.4 8.2		7.9 8.6		12.4 13.7		9.3 10.1		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		183 167		159 145		146 133		127 116		89 81		108 99	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A32100DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		3.7		4.3		4.9		5.8		8.2		6.8	ns
t_{DHL}	Data-to-Pad Low		4.5		5.3		6.0		7.1		10.1		8.3	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		10.7		8.8	ns
t_{ENZL}	Enable-Pad Z to Low		5.1		6.0		6.8		8.0		11.4		9.4	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{GLH}	G-to-Pad High		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{GHL}	G-to-Pad Low		9.0		10.5		12.0		14.1		20.1		16.4	ns
t_{LSU}	I/O Latch Output Set-Up	0.26		0.3		0.34		0.4		0.6		0.6		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		9.8		11.1		13.1		18.7		15.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		13.8		15.7		18.5		26.5		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.037		0.04		0.05		0.07		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.07		0.10		0.08	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.04		0.045		0.05		0.06		0.09		0.07	ns
CMOS Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		4.5		5.3		6.0		7.1		10.1		8.3	ns
t_{DHL}	Data-to-Pad Low		3.7		4.3		4.9		5.8		8.2		6.8	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		10.7		8.8	ns
t_{ENZL}	Enable-Pad Z to Low		5.1		6.0		6.8		8.0		11.4		9.4	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{GLH}	G-to-Pad High		8.3		9.8		11.1		13.0		18.5		15.2	ns
t_{GHL}	G-to-Pad Low		9.0		10.5		12.0		14.1		20.0		16.4	ns
t_{LSU}	I/O Latch Set-Up	0.26		0.3		0.3		0.4		0.6		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		11.0		13.2		15.5		22.3		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		16.4		18.5		21.8		30.0		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.052		0.05		0.07		0.10		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.045		0.05		0.06		0.09		0.07	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.04		0.045		0.05		0.06		0.09		0.07	ns

Note:

1. Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.

A32140DX Timing Characteristics

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays[1]												
Combinatorial Functions												
t_{PD}	Internal Array Module Delay		1.8		2.3		2.8		3.6		3.2	ns
t_{PDD}	Internal Decode Module Delay		1.9		2.5		3.0		3.8		3.5	ns
Predicted Routing Delays[2]												
t_{RD1}	FO=1 Routing Delay		1.0		1.3		1.6		2.0		1.8	ns
t_{RD2}	FO=2 Routing Delay		1.4		1.9		2.2		2.8		2.5	ns
t_{RD3}	FO=3 Routing Delay		1.8		2.4		2.8		3.7		3.3	ns
t_{RD4}	FO=4 Routing Delay		2.2		2.9		3.4		4.5		4.0	ns
t_{RD5}	FO=8 Routing Delay		3.8		5.0		5.9		7.7		7.0	ns
t_{RDD}	Decode-to-Output Routing Delay		0.5		0.7		0.78		1.0		0.91	ns
Sequential Timing Characteristics[3, 4]												
t_{CO}	Flip-Flop Clock-to-Output		2.1		2.8		3.3		4.3		3.9	ns
t_{GO}	Latch Gate-to-Output		1.8		2.3		2.8		3.6		3.2	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.3		0.4		0.47		0.6		0.55		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.1		2.8		3.3		4.3		3.9	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.9		1.0		1.3		1.17		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	2.6		3.5		4.1		5.4		4.82		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		5.5		6.5		8.4		7.6		ns

Notes:

1. *For dual-module macros, use $t_{PD1} + t_{RD1} + t_{PDn}$, $t_{CO} + t_{RD1} + t_{PDn}$, or $t_{PD1} + t_{RD1} + t_{SUD}$, whichever is appropriate.*
2. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*
3. *Data applies to macros based on the S-module. Timing parameters for sequential macros constructed from C-modules can be obtained from the DirectTime Analyzer utility.*
4. *Set-Up and hold timing parameters for the input buffer latch are defined with respect to the PAD and the D input. External set-up/hold timing parameters must account for delay from an external PAD signal to the G inputs. Delay from an external PAD signal to the G input subtracts (adds) to the internal set-up (hold) time.*

A32140DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays													
t_{INPY}	Input Data Pad-to-Y			1.2		1.6		1.9		2.4		2.2	ns
t_{INGO}	Input Latch Gate-to-Output			2.3		3.1		3.7		4.7		4.3	ns
t_{INH}	Input Latch Hold		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up		0.3		0.4		0.47		0.6		0.55		ns
t_{ILA}	Latch Active Pulse Width		3.1		4.2		4.9		6.4		5.7		ns
Input Module Predicted Routing Delays[1]													
t_{IRD1}	FO=1 Routing Delay			2.7		3.7		4.3		5.6		5.0	ns
t_{IRD2}	FO=2 Routing Delay			3.1		4.2		4.9		6.4		5.7	ns
t_{IRD3}	FO=3 Routing Delay			3.4		4.5		5.3		6.9		6.2	ns
t_{IRD4}	FO=4 Routing Delay			3.9		5.2		6.1		7.9		7.1	ns
t_{IRD5}	FO=8 Routing Delay			5.6		7.5		8.8		11.4		10.3	ns
t_{IRDD}	Decode-to-Output Routing Delay			0.3		0.4		0.5		0.7		0.6	ns
Global Clock Network													
t_{CKH}	Input Low to High	FO=32 FO=486		6.2 6.8		8.3 9.1		9.7 10.7		12.7 13.9		11.4 12.5	ns ns
t_{CKL}	Input High to Low	FO=32 FO=486		6.12 6.7		8.2 8.9		9.6 10.5		12.5 13.6		11.3 12.3	ns ns
t_{PW}	Minimum Pulse Width	FO=32 FO=486	2.7 2.9		3.7 3.9		4.3 4.6		5.6 6.0		5.0 5.41		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=486		0.6 0.6		0.9 0.9		1.0 1.0		1.3 1.3		1.17 1.17	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=486	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=486	2.2 2.2		2.9 2.9		3.4 3.4		4.4 4.4		4.0 4.0		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=486	5.7 6.6		7.6 8.3		8.3 9.5		11.9 13.6		9.0 11.1		ns ns
f_{MAX}	Maximum Datapath Frequency	FO=32 FO=486		173 151		138 121		120 105		84 74		102 90	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A32140DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.3		4.4		5.1		6.7		6.0	ns
t_{DHL}	Data-to-Pad Low		3.5		4.6		5.4		7.1		6.3	ns
t_{ENZH}	Enable-Pad Z to High		4.1		5.5		6.4		8.4		7.5	ns
t_{ENZL}	Enable-Pad Z to Low		4.4		5.9		6.9		9.0		8.1	ns
t_{ENHZ}	Enable-Pad High to Z		7.1		9.5		11.1		14.5		13.0	ns
t_{ENLZ}	Enable-Pad Low to Z		7.1		9.5		11.1		14.5		13.0	ns
t_{GLH}	G-to-Pad High		6.5		8.7		10.2		13.3		12.0	ns
t_{GHL}	G-to-Pad Low		6.5		8.7		10.2		13.3		12.0	ns
t_{LSU}	I/O Latch Output Set-Up	0.4		0.6		0.7		0.9		0.82		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		11.1		13.1		17.0		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		15.7		18.5		24.1		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.04		0.05		0.07		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.02		0.03		0.07		0.1		0.08	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.03		0.04		0.05		0.07		0.06	ns/pF
CMOS Output Module Timing[1]												
t_{DLH}	Data-to-Pad High		3.5		4.6		5.4		7.1		6.0	ns
t_{DHL}	Data-to-Pad Low		3.3		4.4		5.1		6.7		6.3	ns
t_{ENZH}	Enable-Pad Z to High		4.1		5.5		6.4		8.4		7.5	ns
t_{ENZL}	Enable-Pad Z to Low		4.4		5.9		6.9		9.0		8.1	ns
t_{ENHZ}	Enable-Pad High to Z		7.1		9.5		11.1		14.5		13.0	ns
t_{ENLZ}	Enable-Pad Low to Z		7.1		9.5		11.1		14.5		13.0	ns
t_{GLH}	G-to-Pad High		6.5		8.7		10.2		13.3		12.0	ns
t_{GHL}	G-to-Pad Low		6.5		8.7		10.2		13.3		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.4		0.6		0.7		0.9		0.82		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		13.3		15.6		20.3		18.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		18.5		21.8		28.3		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.06		0.07		0.1		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.1		0.07	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.3		0.4		0.5		0.7		0.6	ns/pF

Note:

1. Delays based on 35 pF loading.

A32200DX Timing Characteristics

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays														
Combinatorial Functions														
t_{PD}	Internal Array Module Delay		2.0		2.4		2.7		3.2		4.5		3.7	ns
t_{PDD}	Internal Decode Module Delay		2.5		2.9		3.3		3.9		5.6		4.5	ns
Predicted Module Routing Delays														
t_{RD1}	FO=1 Routing Delay		1.1		1.35		1.5		1.8		2.6		2.1	ns
t_{RD2}	FO=2 Routing Delay		1.7		2.0		2.2		2.6		3.7		3.0	ns
t_{RD3}	FO=3 Routing Delay		2.1		2.4		2.8		3.3		4.7		3.8	ns
t_{RD4}	FO=4 Routing Delay		2.6		3.0		3.4		4.0		5.7		4.7	ns
t_{RD5}	FO=8 Routing Delay		4.5		5.3		6.0		7.0		10.0		8.2	ns
t_{RDD}	Decode-to-Output Routing Delay		0.6		0.67		0.8		0.9		1.3		1.0	ns
Sequential Timing Characteristics														
t_{CO}	Flip-Flop Clock-to-Output		2.3		2.7		3.1		3.6		5.1		4.2	ns
t_{GO}	Latch Gate-to-Output		2.0		2.4		2.7		3.2		4.5		3.7	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.3		0.35		0.4		0.47		0.7		0.55		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.3		2.7		3.1		3.6		5.1		4.2	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.75		0.9		1.0		1.4		1.17		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		3.7		4.2		4.9		7.0		5.7		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	4.1		4.9		5.5		6.5		9.2		7.6		ns

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Timing														
Synchronous SRAM Operations														
t_{RC}	Read Cycle Time	6.4		7.5		8.5		10.0		14.3		11.7		ns
t_{WC}	Write Cycle Time	6.4		7.5		8.5		10.0		14.3		11.7		ns
t_{RCKHL}	Clock High/Low Time	3.2		3.9		4.3		5.0		7.1		5.8		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		3.8		4.3		5.0		7.1		5.8	ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.7		0.8		0.9		1.4		1.0		ns
t_{RENH}	Read Enable Hold	3.2		3.8		4.3		5.0		7.0		5.8		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.4		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.6		3.1		3.5		4.1		5.6		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations														
t_{RPD}	Asynchronous Access Time		7.7		9.0		10.2		12.0		17.2		14.1	ns
t_{RDADV}	Read Address Valid	8.3		9.75		11.1		13.0		18.6		15.2		ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up to Address Valid	0.57		0.7		0.8		0.9		1.4		1.0		ns
t_{RENHA}	Read Enable Hold	3.2		3.8		4.3		5.0		7.1		5.8		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.4		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.3		1.5		1.8		2.6		2.1	ns

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays															
t_{INPY}	Input Data Pad-to-Y			1.4		1.65		1.9		2.2		2.9		2.5	ns
t_{INGO}	Input Latch Gate-to-Output[1]			3.3		3.2		4.3		5.1		7.3		6.0	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up[1]		0.45		0.52		0.6		0.7		1.0		0.8		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		5.2		5.9		6.9		9.8		8.1		ns
Input Module Predicted Routing Delays															
t_{IRD1}	FO=1 Routing Delay			1.9		2.2		2.6		3.0		4.2		3.5	ns
t_{IRD2}	FO=2 Routing Delay			2.5		2.9		3.3		3.9		5.5		4.5	ns
t_{IRD3}	FO=3 Routing Delay			3.3		3.9		4.4		5.2		7.6		6.1	ns
t_{IRD4}	FO=4 Routing Delay			3.9		4.5		5.2		6.1		8.7		7.1	ns
t_{IRD5}	FO=8 Routing Delay			5.0		6.0		6.7		7.9		11.2		9.3	ns
t_{IRDD}	Decode-to-Output Delay			0.3		0.37		0.4		0.5		0.7		0.6	ns
Global Clock Network															
t_{CKH}	Input Low to High	FO=32 FO=635		5.3 6.1		6.2 7.2		7.1 8.2		8.3 9.6		11.8 13.7		9.7 11.3	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		5.2 6.8		6.2 8.0		7.0 9.0		8.2 10.6		11.7 15.1		9.6 12.8	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	2.7 2.9		3.2 3.45		3.7 3.9		4.3 4.6		6.1 6.6		5.0 5.4		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	2.7 2.9		3.2 3.45		3.7 3.9		4.3 4.6		6.1 6.6		5.0 5.4		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		0.6 0.6		0.75 0.75		0.9 0.9		1.0 1.0		1.4 1.4		1.1 1.1	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	2.2 2.7		2.6 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.0 5.0		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	5.5 6.1		6.5 7.2		7.4 8.2		8.7 9.6		12.4 13.7		10.2 11.2		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		165 151		153. 140		132 121		115 105		80 73		98 90	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A32200DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		3.7		4.3		4.9		5.8		8.3		6.8	ns
t_{DHL}	Data-to-Pad Low		4.5		5.3		6.0		7.1		10.1		8.3	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		10.7		8.8	ns
t_{ENZL}	Enable-Pad Z to Low		5.2		6.0		6.9		8.1		11.5		9.5	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{GLH}	G-to-Pad High		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{GHL}	G-to-Pad Low		8.9		10.5		11.9		14.0		20.0		16.5	ns
t_{LSU}	I/O Latch Output Set-Up	0.26		0.3		0.3		0.4		0.6		0.5		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		9.8		11.1		13.1		18.7		15.4	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		13.9		15.7		18.5		26.5		21.7	ns
d_{TLH}	Capacitive Loading, Low to High		0.03		0.035		0.04		0.05		0.07		0.06	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.05		0.06		0.07		0.10		0.08	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.04		0.045		0.05		0.06		0.09		0.07	ns
CMOS Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		4.5		5.3		6.0		5.8		8.3		6.8	ns
t_{DHL}	Data-to-Pad Low		3.7		4.3		4.9		7.1		10.1		8.3	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		10.7		8.8	ns
t_{ENZL}	Enable-Pad Z to Low		5.2		6.0		6.9		8.1		11.5		9.5	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{GLH}	G-to-Pad High		8.3		9.7		11.1		13.0		18.5		15.2	ns
t_{GHL}	G-to-Pad Low		8.9		10.5		11.9		14.0		20.0		16.5	ns
t_{LSU}	I/O Latch Set-Up	0.26		0.3		0.3		0.4		0.6		0.5		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		11.6		13.2		15.5		22.3		18.2	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		16.3		18.5		21.8		31.2		25.6	ns
d_{TLH}	Capacitive Loading, Low to High		0.04		0.05		0.06		0.07		0.10		0.08	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.04		0.045		0.05		0.06		0.09		0.07	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.04		0.045		0.05		0.06		0.09		0.07	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A32300DX Timing Characteristics

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Propagation Delays														
Combinatorial Functions														
t_{PD}	Internal Array Module Delay		2.2		2.6		2.9		3.4		4.8		4.0	ns
t_{PDD}	Internal Decode Module Delay		2.5		2.9		3.3		3.9		5.6		4.5	ns
Predicted Module Routing Delays														
t_{RD1}	FO=1 Routing Delay		1.1		1.4		1.5		1.8		2.5		2.1	ns
t_{RD2}	FO=2 Routing Delay		1.7		2.0		2.3		2.7		3.8		3.2	ns
t_{RD3}	FO=3 Routing Delay		2.4		2.8		3.1		3.7		5.2		4.3	ns
t_{RD4}	FO=4 Routing Delay		2.9		3.6		3.9		4.6		6.5		5.4	ns
t_{RD5}	FO=8 Routing Delay		5.2		6.2		7.0		8.2		10.0		9.6	ns
t_{RDD}	Decode-to-Output Routing Delay		0.6		0.7		0.8		0.9		1.3		1.0	ns
Sequential Timing Characteristics														
t_{CO}	Flip-Flop Clock-to-Output		2.3		2.7		3.1		3.6		5.0		4.2	ns
t_{GO}	Latch Gate-to-Output		2.2		2.6		2.9		3.4		4.5		4.0	ns
t_{SU}	Flip-Flop (Latch) Set-Up Time	0.32		0.4		0.42		0.5		0.7		0.6		ns
t_{H}	Flip-Flop (Latch) Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RO}	Flip-Flop (Latch) Reset to Output		2.2		2.6		3.0		3.5		5.0		4.1	ns
t_{SUENA}	Flip-Flop (Latch) Enable Set-Up	0.6		0.75		0.9		1.0		1.4		1.1		ns
t_{HENA}	Flip-Flop (Latch) Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{WCLKA}	Flip-Flop (Latch) Clock Active Pulse Width	3.1		3.7		4.2		4.9		7.0		5.7		ns
t_{WASYN}	Flip-Flop (Latch) Asynchronous Pulse Width	3.5		4.1		4.7		5.5		7.9		6.4		ns

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3 Speed		'–2 Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Logic Module Timing														
Synchronous SRAM Operations														
t_{RC}	Read Cycle Time	6.4		7.5		8.5		10.0		14.3		11.6		ns
t_{WC}	Write Cycle Time	6.4		7.5		8.5		10.0		14.3		11.6		ns
t_{RCKHL}	Clock High/Low Time	3.2		3.75		4.3		5.0		7.1		5.8		ns
t_{RCO}	Data Valid After Clock High/Low		3.2		3.75		4.3		5.0		7.1		5.8	ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.82		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSU}	Read Enable Set-Up	0.6		0.68		0.8		0.9		1.3		1.05		ns
t_{RENH}	Read Enable Hold	3.2		3.75		4.3		5.0		7.1		5.8		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.7		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{BENS}	Block Enable Set-Up	2.6		2.3		3.5		4.1		5.9		4.8		ns
t_{BENH}	Block Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
Asynchronous SRAM Operations														
t_{RPD}	Asynchronous Access Time		7.7		9.0		10.2		12.0		17.2		14.1	ns
t_{RDADV}	Read Address Valid	8.3		9.6		11.1		13.0		18.6		15.2		ns
t_{ADSU}	Address/Data Set-Up Time	1.5		1.8		2.0		2.4		3.4		2.8		ns
t_{ADH}	Address/Data Hold Time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{RENSUA}	Read Enable Set-Up to Address Valid	0.57		0.68		0.8		0.9		1.3		1.05		ns
t_{RENHA}	Read Enable Hold	3.2		3.75		4.3		5.0		7.1		5.8		ns
t_{WENSU}	Write Enable Set-Up	2.6		3.0		3.4		4.0		5.7		4.7		ns
t_{WENH}	Write Enable Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{DOH}	Data Out Hold Time		1.1		1.35		1.5		1.8		2.6		2.1	ns

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

			'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**		**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
Input Module Propagation Delays															
t_{INPY}	Input Data Pad-to-Y			1.4		1.7		1.9		2.2		3.1		2.5	ns
t_{INGO}	Input Latch Gate-to-Output[1]			2.9		3.4		3.8		4.5		6.4		5.2	ns
t_{INH}	Input Latch Hold[1]		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{INSU}	Input Latch Set-Up[1]		0.45		0.5		0.6		0.7		1.0		0.82		ns
t_{ILA}	Latch Active Pulse Width[1]		4.4		5.2		5.9		6.9		9.8		8.1		ns
Input Module Predicted Routing Delays															
t_{IRD1}	FO=1 Routing Delay			1.9		2.3		2.6		3.0		4.2		3.5	ns
t_{IRD2}	FO=2 Routing Delay			2.5		2.9		3.3		3.9		5.5		4.6	ns
t_{IRD3}	FO=3 Routing Delay			3.3		3.9		4.4		5.2		7.4		6.1	ns
t_{IRD4}	FO=4 Routing Delay			3.9		4.6		5.2		6.1		8.7		7.2	ns
t_{IRD5}	FO=8 Routing Delay			5.0		6.0		6.7		7.9		11.2		9.2	ns
t_{RDD}	Decode-to-Output Routing Delay			0.6		0.67		0.8		0.9		1.3		1.05	ns
Global Clock Network															
t_{CKH}	Input Low to High	FO=32 FO=635		6.4 7.3		7.6 8.6		8.6 9.7		10.1 11.4		14.4 16.2		11.8 13.4	ns ns
t_{CKL}	Input High to Low	FO=32 FO=635		6.6 7.1		7.7 8.4		8.8 9.5		10.3 11.2		14.7 16.0		12.1 13.1	ns ns
t_{PWH}	Minimum Pulse Width High	FO=32 FO=635	3.0 3.3		3.5 3.8		4.0 4.3		4.7 5.1		6.7 7.2		5.5 6.0		ns ns
t_{PWL}	Minimum Pulse Width Low	FO=32 FO=635	3.0 3.3		3.8 3.8		4.0 4.3		4.7 5.1		6.7 7.2		5.5 6.0		ns ns
t_{CKSW}	Maximum Skew	FO=32 FO=635		0.6 0.6		0.75 0.75		0.9 0.9		1.0 1.0		1.4 1.4		1.17 1.17	ns ns
t_{SUEXT}	Input Latch External Set-Up	FO=32 FO=635	0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		0.0 0.0		ns ns
t_{HEXT}	Input Latch External Hold	FO=32 FO=635	2.2 2.7		2.6 3.2		2.9 3.7		3.4 4.3		4.9 6.1		4.0 5.0		ns ns
t_P	Minimum Period (1/fmax)	FO=32 FO=635	5.5 6.1		6.9 7.7		7.4 8.2		9.3 10.2		13.2 14.5		10.9 12.0		ns ns
f_{HMAX}	Maximum Datapath Frequency	FO=32 FO=635		154 141		142 130		123 113		107 98		75 69		91 83	MHz MHz

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

A32300DX Timing Characteristics (continued)

(Worst-Case Commercial Conditions V_{CC} = 4.75 V, T_J = 70°C)

		'–3' Speed		'–2' Speed		'–1' Speed		'Std' Speed		'–F' Speed		3.3V 'Std' Speed		
Parameter	**Description**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
TTL Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		3.7		4.3		4.9		5.8		7.7		8.2	ns
t_{DHL}	Data-to-Pad Low		4.4		5.2		5.9		6.9		8.1		9.8	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		8.8		10.7	ns
t_{ENZL}	Enable-Pad Z to Low		5.1		6.0		6.8		8.0		9.4		11.4	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.75		11.1		13.0		15.2		18.5	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.75		11.1		13.0		15.2		18.5	ns
t_{GLH}	G-to-Pad High		4.3		5.0		5.7		6.7		7.9		9.6	ns
t_{GHL}	G-to-Pad Low		5.4		6.3		7.1		8.4		7.9		12.0	ns
t_{LSU}	I/O Latch Output Set-Up	0.26		0.3		0.34		0.4		0.47		0.6		ns
t_{LH}	I/O Latch Output Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		8.4		9.7		11.1		13.1		15.4		18.7	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		11.8		13.9		15.7		18.5		21.8		26.5	ns
d_{TLH}	Capacitive Loading, Low to High		0.26		0.3		0.34		0.4		0.47		0.6	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.32		0.37		0.4		0.5		0.58		0.7	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.03		0.037		0.04		0.05		0.058		0.07	ns
CMOS Output Module Timing[1]														
t_{DLH}	Data-to-Pad High		4.4		5.2		5.9		6.9		8.1		8.2	ns
t_{DHL}	Data-to-Pad Low		3.7		4.3		4.9		5.8		7.7		9.8	ns
t_{ENZH}	Enable-Pad Z to High		4.8		5.6		6.4		7.5		8.8		10.7	ns
t_{ENZL}	Enable-Pad Z to Low		5.1		6.0		6.8		8.0		9.4		11.4	ns
t_{ENHZ}	Enable-Pad High to Z		8.3		9.75		11.1		13.0		15.2		18.5	ns
t_{ENLZ}	Enable-Pad Low to Z		8.3		9.75		11.1		13.0		15.2		18.5	ns
t_{GLH}	G-to-Pad High		4.3		5.0		5.7		6.7		7.9		9.6	ns
t_{GHL}	G-to-Pad Low		5.4		6.3		7.1		8.4		9.9		12.0	ns
t_{LSU}	I/O Latch Set-Up	0.26		0.3		0.34		0.4		0.47		0.6		ns
t_{LH}	I/O Latch Hold	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{LCO}	I/O Latch Clock-Out (Pad-to-Pad) 32 I/O		9.9		11.6		13.2		15.5		17.6		22.3	ns
t_{ACO}	Array Latch Clock-Out (Pad-to-Pad) 32 I/O		13.9		16.4		18.5		21.8		25.6		31.2	ns
d_{TLH}	Capacitive Loading, Low to High		0.32		0.37		0.4		0.5		0.6		0.10	ns/pF
d_{THL}	Capacitive Loading, High to Low		0.26		0.3		0.3		0.4		0.5		0.09	ns/pF
t_{WDO}	Hard-Wired Wide-Decode Output		0.03		0.037		0.04		0.05		0.06		0.09	ns

Note:

1. *Routing delays are for typical designs across worst-case operating conditions. These parameters should be used for estimating device performance. Post-route timing analysis or simulation is required to determine actual performance.*

Pin Descriptions

CLKA, CLKB Clock A and Clock B (Input)
TTL clock inputs for clock distribution networks. The clock input is buffered prior to clocking the logic modules. This pin can also be used as an I/O.

DCLK Diagnostic Clock (Input)
TTL clock input for diagnostic probe and device programming. DCLK is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

GND Ground (Input)
Input LOW supply voltage.

I/O Input/Output (Input, Output)
I/O pin functions as an input, output, three-state or bidirectional buffer. Input and output levels are compatible with standard TTL and CMOS specifications. Unused I/O pins are automatically driven LOW by the Designer Series software for XL devices and are automatically tristated for DX devices.

MODE Mode (Input)
The MODE pin controls the use of multi-function pins (DCLK, PRA, PRB, SDI, TDO). When the MODE pin is HIGH, the special functions are active. To provide ActionProbe capability, the MODE pin should be terminated to GND through a 10K resistor so the MODE pin can be pulled HIGH when required.

NC No Connection
This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

PRA, I/O Probe A (Output)
The Probe A pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe B pin to allow real-time diagnostic output of any signal path within the device. The Probe A pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRA is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

PRB, I/O Probe B (Output)
The Probe B pin is used to output data from any user-defined design node within the device. This independent diagnostic pin is used in conjunction with the Probe A pin to allow real-time diagnostic output of any signal path within the device. The Probe B pin can be used as a user-defined I/O when debugging has been completed. The pin's probe capabilities can be permanently disabled to protect programmed design confidentiality. PRB is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

QCLKA,B,C,D Quadrant Clock (Input/Output)
These four pins are the quadrant clock inputs. When not used as a register control signal, these pins can function as general purpose I/O.

SDO Serial Data (Output)
Serial data output for diagnostic probe and device programming. SDO is active when the MODE pin is HIGH. This pin functions as an I/O when MODE pin is LOW.

SDI Serial Data Input (Input)
Serial data input for diagnostic probe and device programming. SDI is active when the MODE pin is HIGH. This pin functions as an I/O when the MODE pin is LOW.

TCK Test Clock
Clock signal to shift the JTAG data into the device. This pin functions as an I/O when the JTAG fuse is not programmed.

TDI Test Data In
Serial data input for JTAG instructions and data. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

TDO Test Data Out
Serial data output for JTAG instructions and test data. This pin functions as an I/O when the JTAG fuse is not programmed.

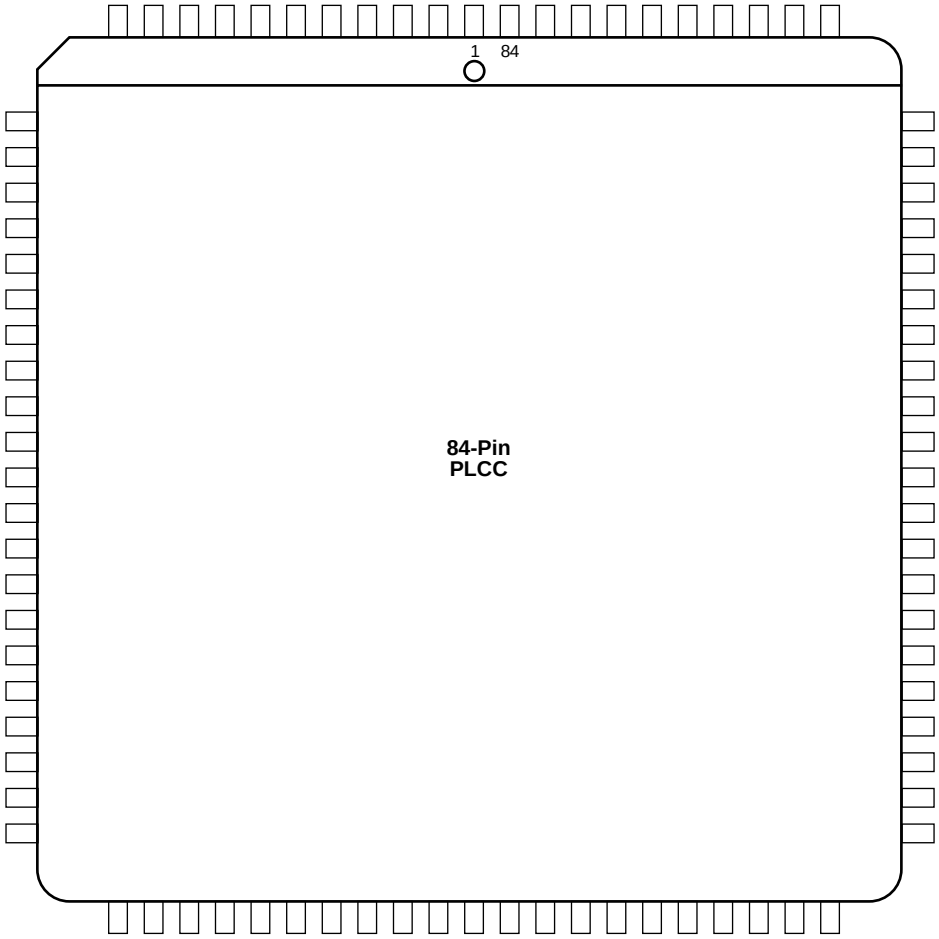
TMS Test Mode Select
Serial data input for JTAG test mode. Data is shifted in on the rising edge of TCLK. This pin functions as an I/O when the JTAG fuse is not programmed.

V_{CC} Supply Voltage (Input)
Input HIGH supply voltage.

Note: *TCK, TDI, TDO, TMS are only available on devices containing JTAG circuitry.*

Package Pin Assignments

84-Pin PLCC Package (Top View)



84-Pin PLCC Package

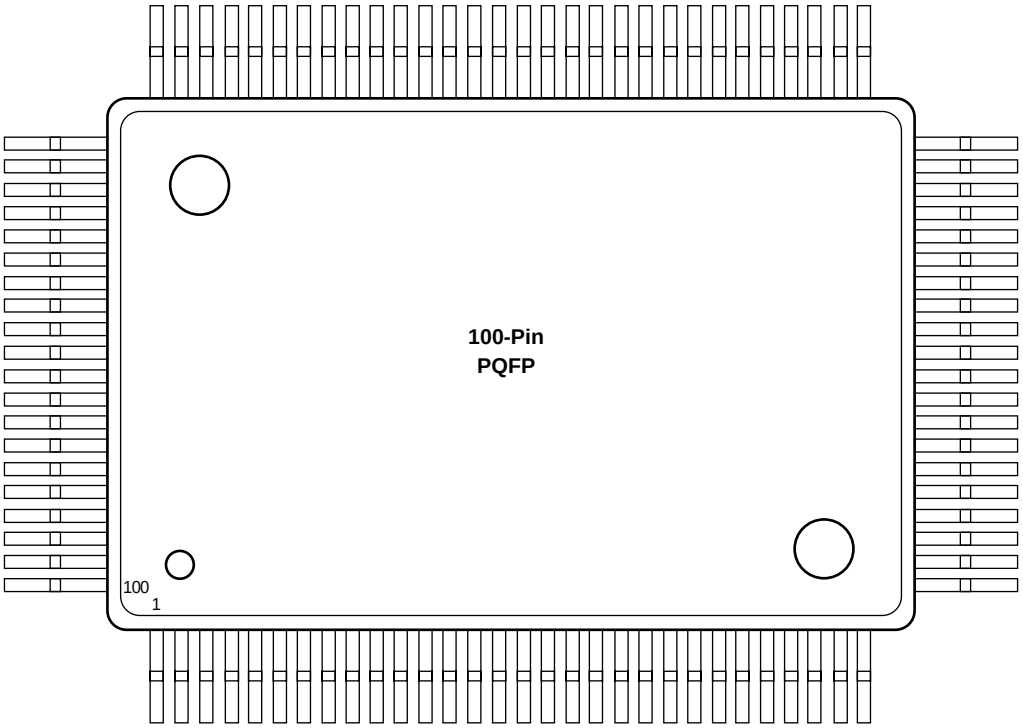
Pin Number	A1225XL Function	A1240XL Function	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
2	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
4	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
5	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
6	GND	GND	GND	GND	GND	GND
7	I/O	I/O	I/O	I/O	QCLKC, I/O	I/O
8	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
9	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
10	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O
12	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)
22	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
23	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
28	GND	GND	GND	GND	GND	GND
34	I/O	I/O	I/O	I/O	TMS, I/O	TMS, I/O
35	I/O	I/O	I/O	I/O	TDI, I/O	TDI, I/O
36	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
37	I/O	I/O	I/O	I/O	QCLKA, I/O	I/O
38	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
39	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
43	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
44	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
45	I/O	I/O	I/O	I/O	QCLKB, I/O	I/O (WD)
46	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
47	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
49	GND	GND	GND	GND	GND	GND
50	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
51	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
52	I/O	I/O	I/O	I/O	SDO, TDO, I/O	SDO, TDO, I/O
53	I/O	I/O	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O	TCK, I/O	TCK, I/O
63	GND	GND	GND	GND	GND	GND
64	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
65	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
70	GND	GND	GND	GND	GND	GND
76	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O
78	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
79	I/O	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
80	I/O	I/O	I/O (WD)	I/O	QCLKD, I/O	I/O (WD)
81	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
83	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O
84	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}

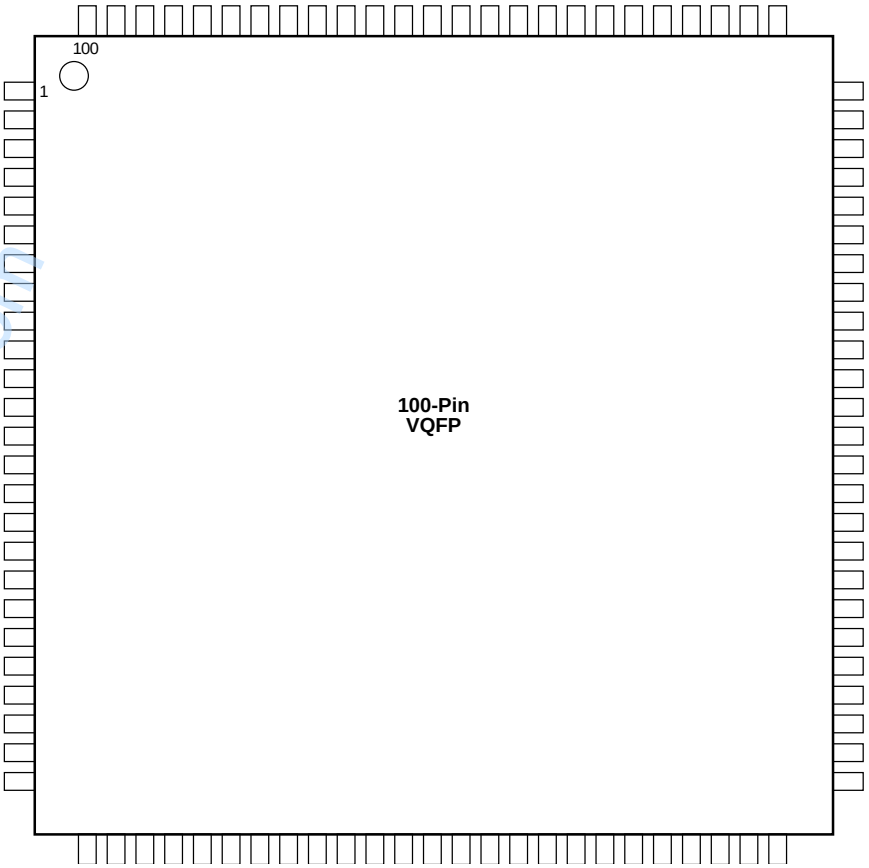
Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module*
2. *Wide-decode I/O (WD) can also be general purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/O's.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

100-Pin PQFP Package, 100-Pin VQFP Package (Top View)





100-Pin PQFP Package, 100-Pin VQFP Package

Pin Number	A1225XL-PQ100 Function	A1225XL-VQ100 Function	A1240XL-PQ100 Function	A3265DX PQ100 Function
2	DCLK, I/O	MODE (GND)	DCLK, I/O	DCLK, I/O
4	MODE (GND)	I/O	MODE (GND)	MODE (GND)
7	I/O	GND	I/O	I/O
9	GND	I/O	GND	GND
14	I/O	V_{CC}	I/O	I/O
15	I/O	V_{CC}	I/O	I/O
16	V_{CC}	I/O	V_{CC}	V_{CC}
17	V_{CC}	I/O	V_{CC}	V_{CC}
20	I/O	GND	I/O	I/O
22	GND	I/O	GND	GND
32	I/O	GND	I/O	I/O
34	GND	I/O	GND	GND
35	I/O	I/O	I/O	I/O (WD)
36	I/O	I/O	I/O	I/O (WD)
37	I/O	I/O	I/O	I/O (WD)
38	I/O	V_{CC}	I/O	I/O (WD)
40	V_{CC}	I/O	V_{CC}	V_{CC}
41	I/O	I/O	I/O	I/O (WD)
42	I/O	I/O	I/O	I/O (WD)
44	I/O	GND	I/O	I/O (WD)
45	I/O	I/O	I/O	I/O (WD)
46	GND	I/O	GND	GND
47	I/O	I/O	I/O	I/O (WD)
48	I/O	I/O	I/O	I/O (WD)
50	I/O	SDO, I/O	I/O	I/O
52	SDO, I/O	I/O	SDO, I/O	SDO, I/O
55	I/O	GND	I/O	I/O
57	GND	I/O	GND	GND
62	I/O	GND	I/O	I/O
63	I/O	V_{CC}	I/O	I/O
64	GND	V_{CC}	GND	GND
65	V_{CC}	V_{CC}	V_{CC}	V_{CC}
66	V_{CC}	I/O	V_{CC}	V_{CC}
67	V_{CC}	I/O	V_{CC}	V_{CC}
70	I/O	GND	I/O	I/O
72	GND	I/O	GND	GND
77	I/O	SDI, I/O	I/O	I/O
79	SDI, I/O	I/O	SDI, I/O	SDI, I/O
81	I/O	I/O	I/O	I/O (WD)
82	I/O	GND	I/O	I/O (WD)
83	I/O	I/O	I/O	I/O (WD)
84	GND	I/O	GND	GND
85	I/O	PRA, I/O	I/O	I/O (WD)
86	I/O	I/O	I/O	I/O (WD)

100-Pin PQFP Package, 100-Pin VQFP Package (Continued)

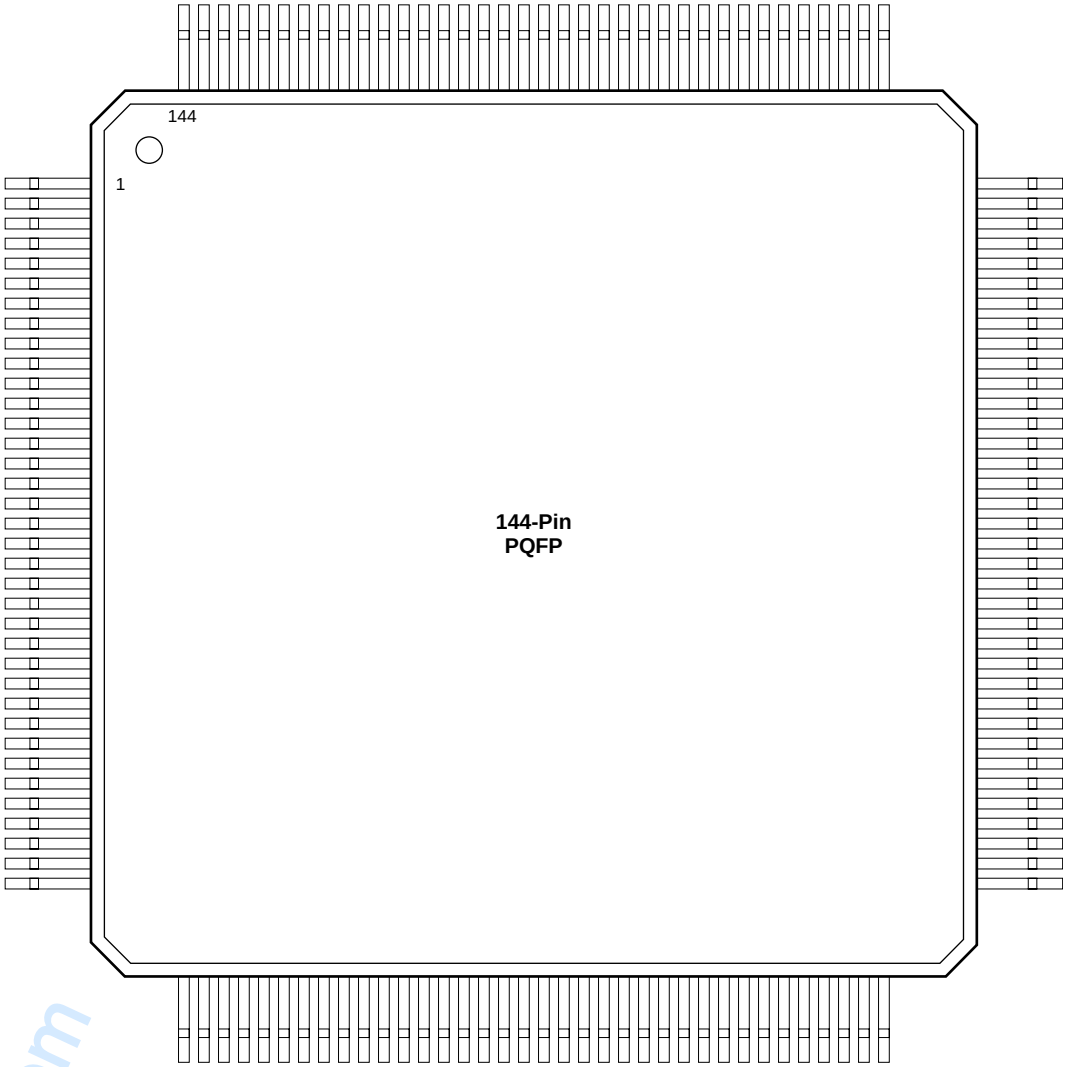
Pin Number	A1225XL-PQ100 Function	A1225XL-VQ100 Function	A1240XL-PQ100 Function	A3265DX PQ100 Function
87	PRA, I/O	CLKA, I/O	PRA, I/O	PRA, I/O
88	I/O	V_{CC}	I/O	I/O
89	CLKA, I/O	I/O	CLKA, I/O	CLKA, I/O
90	V_{CC}	CLKB, I/O	V_{CC}	V_{CC}
92	CLKB, I/O	PRB, I/O	CLKB, I/O	CLKB, I/O
94	PRB, I/O	GND	PRB, I/O	PRB, I/O
95	I/O	I/O	I/O	I/O (WD)
96	GND	I/O	GND	GND
99	I/O	I/O	I/O	I/O (WD)
100	I/O	DCLK, I/O	I/O	I/O (WD)

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/O's.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*
4. *I/O (WD): Denotes I/O pin with an associated Wide-Decode Module*

Package Pin Assignments (continued)

144-Pin PQFP Package (Top View)



144-Pin PQFP Package

Pin Number	A1240XL Function
2	MODE (GND)
9	GND
10	GND
11	GND
18	V_{CC}
19	V_{CC}
20	V_{CC}
21	V_{CC}
28	GND
29	GND
30	GND
44	GND
45	GND
46	GND
54	V_{CC}
55	V_{CC}
56	V_{CC}
64	GND
65	GND
79	GND
80	GND
81	GND
88	GND

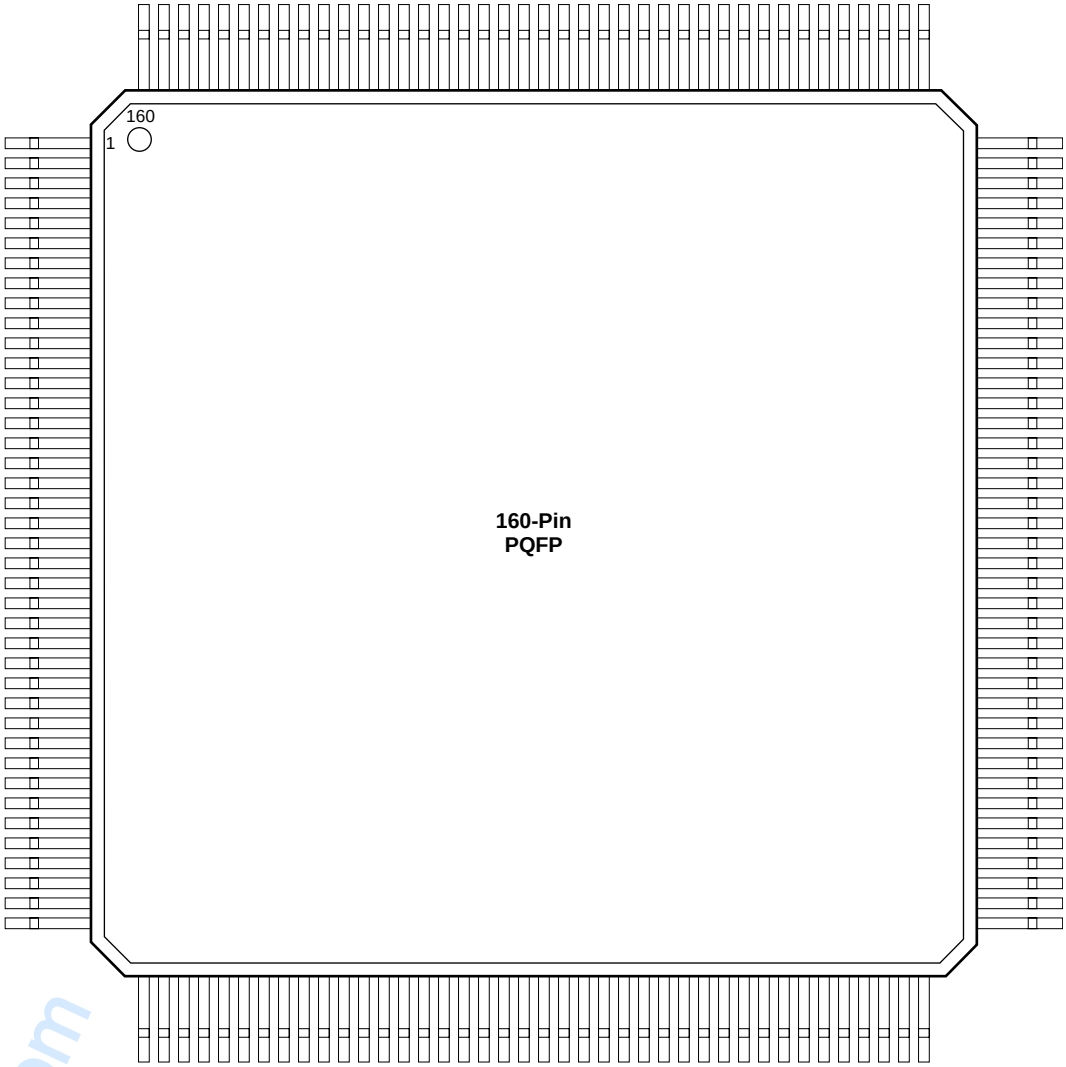
Pin Number	A1240XL Function
89	V_{CC}
90	V_{CC}
91	V_{CC}
92	V_{CC}
93	V_{CC}
100	GND
101	GND
102	GND
110	SDI, I/O
116	GND
117	GND
118	GND
123	PRA, I/O
125	CLKA, I/O
126	V_{CC}
127	V_{CC}
128	V_{CC}
130	CLKB, I/O
132	PRB, I/O
136	GND
137	GND
138	GND
144	DCLK, I/O

Notes:

1. *NC: Denotes 'No Connection'.*
2. *All unlisted pin numbers are user I/O's.*
3. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*

Package Pin Assignments (continued)

160-Pin PQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module*
2. *Wide-Decode I/O (WD) can also be general-purpose user I/O.*
3. *NC Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/O's.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*

160-Pin PQFP Package

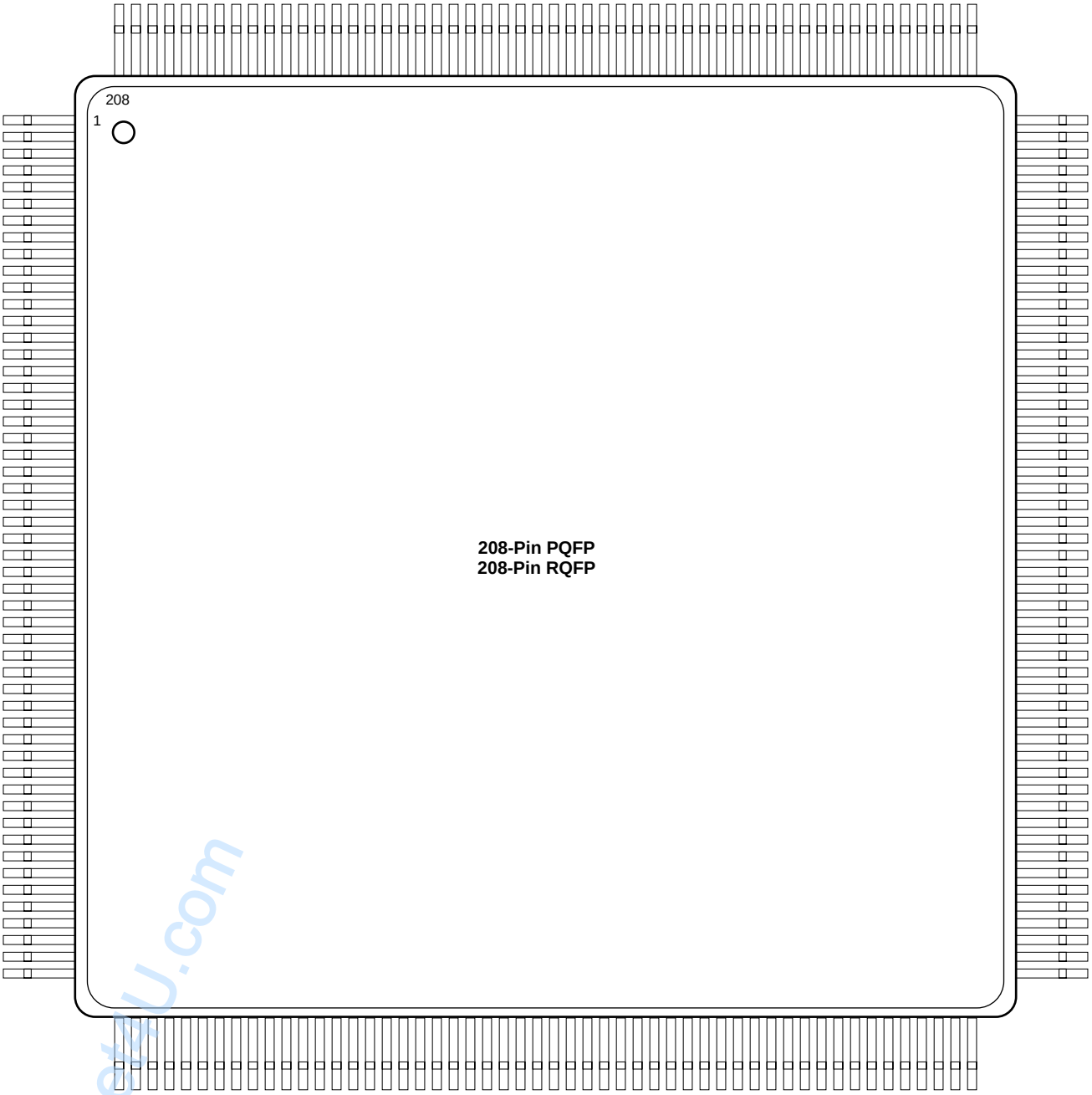
Pin Number	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
2	DCLK, I/O	DCLK, I/O	DCLK	DCLK, I/O
4	I/O	I/O	I/O (WD)	I/O (WD)
5	I/O (WD)	I/O	I/O (WD)	I/O (WD)
6	V_{CC}	V_{CC}	V_{CC}	V_{CC}
7	I/O (WD)	I/O	I/O	I/O
11	GND	GND	GND	GND
12	I/O	I/O	QCLKC, I/O	I/O
13	I/O (WD)	I/O	I/O (WD)	I/O (WD)
14	I/O (WD)	I/O	I/O (WD)	I/O (WD)
16	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O
18	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
20	V_{CC}	V_{CC}	V_{CC}	V_{CC}
21	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O
23	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
24	I/O	I/O	I/O (WD)	I/O (WD)
25	I/O (WD)	I/O	I/O (WD)	I/O (WD)
26	I/O (WD)	I/O	I/O	I/O
28	I/O	I/O	QCLKD	I/O
29	I/O (WD)	I/O	I/O (WD)	I/O (WD)
30	GND	GND	GND	GND
31	I/O (WD)	I/O	I/O (WD)	I/O (WD)
33	I/O	I/O	NC	I/O
34	I/O (WD)	I/O	NC	I/O
35	V_{CC}	V_{CC}	V_{CC}	V_{CC}
36	I/O (WD)	I/O	I/O (WD)	I/O (WD)
37	I/O	I/O	I/O (WD)	I/O (WD)
38	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O
40	GND	GND	GND	GND
44	GND	GND	GND	GND
49	GND	GND	GND	GND
54	V_{CC}	V_{CC}	V_{CC}	V_{CC}
57	V_{CC}	V_{CC}	V_{CC}	V_{CC}
58	V_{CC}	V_{CC}	V_{CC}	V_{CC}
59	GND	GND	GND	GND
60	V_{CC}	V_{CC}	V_{CC}	V_{CC}
61	GND	GND	GND	GND
62	I/O	I/O	TCK, I/O	TCK, I/O
64	GND	GND	GND	GND
69	GND	GND	GND	GND
80	GND	GND	GND	GND
82	I/O	I/O	SDO, I/O	SDO, TDO, I/O
83	I/O	I/O	I/O (WD)	I/O (WD)
84	I/O	I/O	I/O (WD)	I/O (WD)
86	V_{CC}	V_{CC}	V_{CC}	V_{CC}
87	I/O (WD)	I/O	I/O	I/O
88	I/O (WD)	I/O	I/O (WD)	I/O (WD)
89	GND	GND	GND	GND
90	I/O	I/O	I/O (WD)	I/O

160-Pin PQFP Package (Continued)

Pin Number	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
91	I/O	I/O	QCLKB, I/O	I/O
92	I/O (WD)	I/O	I/O	I/O
93	I/O (WD)	I/O	I/O	I/O
95	I/O	I/O	I/O (WD)	I/O
96	I/O (WD)	I/O	I/O (WD)	I/O (WD)
97	I/O (WD)	I/O	I/O	I/O
98	V_{CC}	V_{CC}	V_{CC}	V_{CC}
99	GND	GND	GND	GND
106	I/O (WD)	I/O	I/O (WD)	I/O (WD)
107	I/O (WD)	I/O	I/O (WD)	I/O (WD)
109	GND	GND	GND	GND
110	I/O	I/O	QCLKA, I/O	I/O
111	I/O (WD)	I/O	I/O	I/O (WD)
112	I/O (WD)	I/O	I/O	I/O (WD)
114	V_{CC}	V_{CC}	V_{CC}	V_{CC}
115	I/O	I/O	I/O (WD)	I/O (WD)
116	I/O	I/O	I/O (WD)	I/O (WD)
118	I/O	I/O	TDI, I/O	TDI, I/O
119	I/O	I/O	TMS, I/O	TMS, I/O
120	GND	GND	GND	GND
125	GND	GND	GND	GND
130	GND	GND	GND	GND
135	V_{CC}	V_{CC}	V_{CC}	V_{CC}
138	V_{CC}	V_{CC}	V_{CC}	V_{CC}
139	V_{CC}	V_{CC}	V_{CC}	V_{CC}
140	GND	GND	GND	GND
145	GND	GND	GND	GND
150	V_{CC}	V_{CC}	V_{CC}	V_{CC}
155	GND	GND	GND	GND
159	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)
160	GND	GND	GND	GND

Package Pin Assignments (continued)

208-Pin PQFP Package, 208-Pin RQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-Decode I/O (WD) can also be general purpose user I/O.*
3. *NC: Denotes 'No Connection'.*
4. *All unlisted pin numbers are user I/O's.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heat sink on the top surface.*

208-Pin PQFP Package, 208-Pin RQFP Package

Pin Number	A1280XL Function	A32100DX Function	A32140DX Function	A32200DX-PQ208 Function	A32200DX-RQ208 Function	A32300DX Function
1	GND	GND	GND	GND	I/O	I/O
2	NC	V_{CC}	V_{CC}	V_{CC}	DCLK, I/O	DCLK, I/O
3	MODE (GND)	MODE (GND)	MODE (GND)	MODE (GND)	I/O	I/O
5	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
6	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
7	I/O	I/O	I/O	I/O	V_{CC}	V_{CC}
9	NC	NC	I/O	I/O	I/O	I/O
10	NC	NC	I/O	I/O	I/O	I/O
11	NC	NC	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O	QCLKC, I/O	QCLKC, I/O
15	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
16	NC	NC	I/O	I/O	I/O (WD)	I/O (WD)
17	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
19	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
20	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
22	GND	GND	GND	GND	PRB, I/O	PRB, I/O
24	I/O	I/O	I/O	I/O	CLKB, I/O	CLKB, I/O
26	I/O	I/O	I/O	I/O	GND	GND
27	GND	GND	GND	GND	V_{CC}	V_{CC}
28	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
29	V_{CC}	V_{CC}	V_{CC}	V_{CC}	CLKA, I/O	CLKA, I/O
30	I/O	I/O	I/O	I/O	PRA, I/O	PRA, I/O
32	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O (WD)	I/O (WD)
33	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
38	I/O	I/O	I/O	I/O	QCLKD, I/O	QCLKD, I/O
40	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
41	NC	NC	I/O	I/O	I/O (WD)	I/O (WD)
42	NC	NC	I/O	I/O	I/O	I/O
43	NC	NC	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O	V_{CC}	V_{CC}
47	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
48	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
50	NC	NC	I/O	I/O	SDI, I/O	SDI, I/O
51	NC	NC	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND	GND	GND
53	GND	GND	GND	GND	I/O	I/O
54	I/O	TMS, I/O	TMS, I/O	TMS, I/O	I/O	I/O
55	I/O	TDI, I/O	TDI, I/O	TDI, I/O	I/O	I/O
57	I/O	I/O	I/O (WD)	I/O (WD)	I/O	I/O
58	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
59	I/O	I/O (WD)	I/O	I/O	GND	GND
60	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
61	NC	I/O	I/O	I/O	I/O	I/O
62	NC	I/O	I/O	I/O	I/O	I/O
65	I/O	QCLKA, I/O	I/O	QCLKA, I/O	I/O	I/O
66	I/O	I/O	I/O (WD)	I/O (WD)	I/O	I/O
67	NC	NC	I/O (WD)	I/O (WD)	I/O	I/O
68	NC	I/O	I/O	I/O	I/O	I/O
70	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
71	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
74	I/O	I/O	I/O	I/O	V_{CC}	V_{CC}
77	I/O	I/O	I/O	I/O	V_{CC}	V_{CC}
78	GND	GND	GND	GND	V_{CC}	V_{CC}

208-Pin PQFP Package, 208-Pin RQFP Package (Continued)

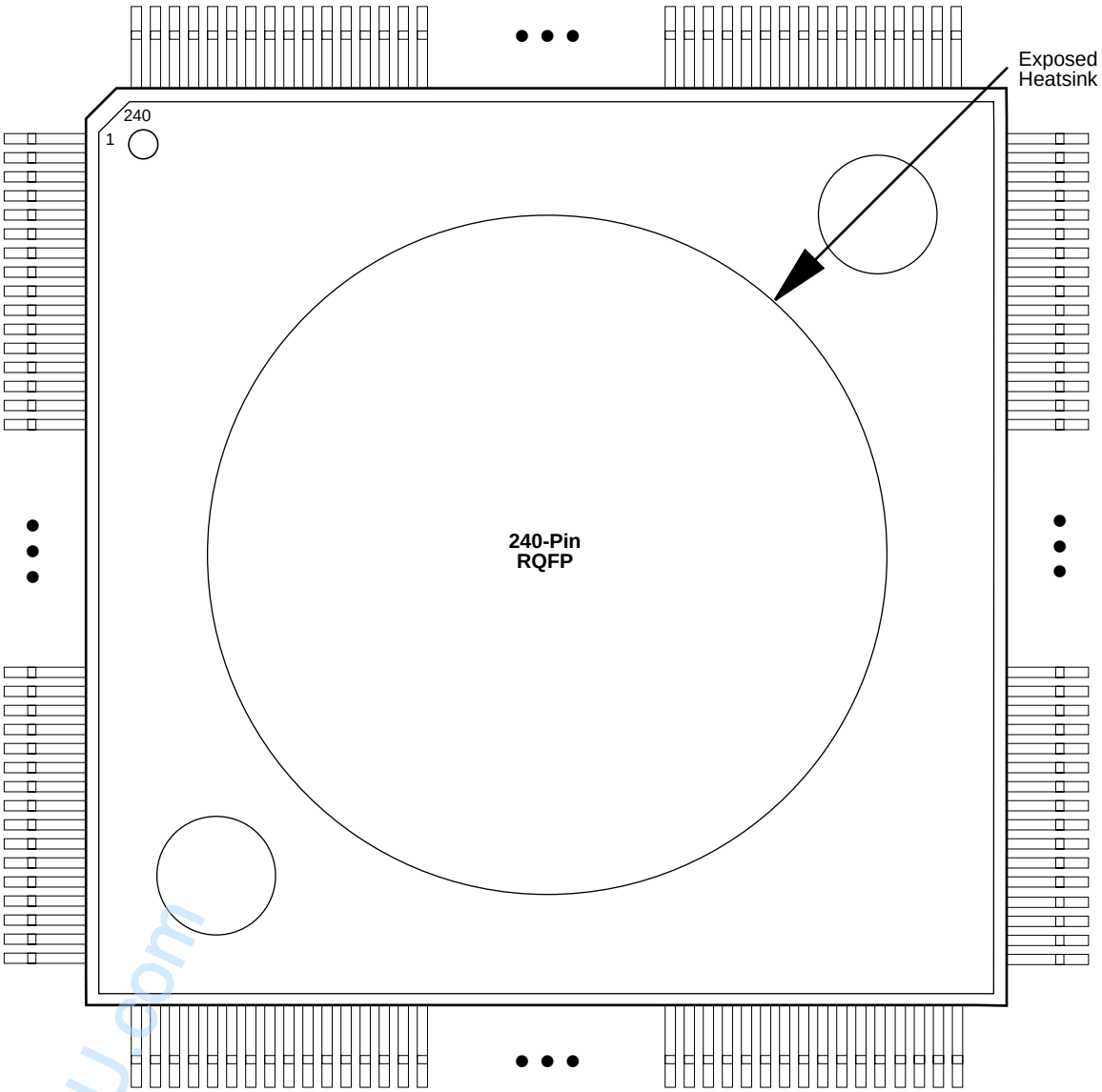
Pin Number	A1280XL Function	A32100DX Function	A32140DX Function	A32200DX-PQ208 Function	A32200DX-RQ208 Function	A32300DX Function
79	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
80	NC	V_{CC}	V_{CC}	V_{CC}	GND	GND
81	I/O	I/O	I/O	I/O	TCK, I/O	TCK, I/O
83	I/O	I/O	I/O	I/O	GND	GND
85	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
86	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
89	NC	I/O	I/O	I/O	I/O	I/O
90	NC	I/O	I/O	I/O	I/O	I/O
91	I/O	QCLKB, I/O	I/O	QCLKB, I/O	I/O	I/O
93	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
94	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
95	NC	I/O	I/O	I/O	I/O	I/O
96	NC	NC	I/O	I/O	I/O	I/O
97	NC	NC	I/O	I/O	I/O	I/O
98	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
100	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
101	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
103	I/O	SDO, I/O	SDO, TDO, I/O	SDO, TDO, I/O	V_{CC}	V_{CC}
104	I/O	I/O	I/O	I/O	GND	GND
105	GND	GND	GND	GND	I/O	I/O
106	NC	V_{CC}	V_{CC}	V_{CC}	SDO, TDO, I/O	SDO, TDO, I/O
107	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
108	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
110	I/O	I/O	I/O	I/O	V_{CC}	V_{CC}
112	NC	NC	I/O	I/O	I/O	I/O
113	NC	NC	I/O	I/O	I/O	I/O
114	NC	NC	I/O	I/O	I/O (WD)	I/O (WD)
115	NC	NC	I/O	I/O	I/O (WD)	I/O (WD)
117	I/O	I/O	I/O	I/O	QCLKB, I/O	QCLKB, I/O
121	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
122	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
126	GND	GND	GND	GND	I/O	I/O (WD)
127	I/O	I/O	I/O	I/O	I/O	I/O (WD)
128	I/O	TCK, I/O	TCK, I/O	TCK, I/O	I/O	I/O
129	GND	GND	GND	GND	V_{CC}	V_{CC}
130	V_{CC}	V_{CC}	V_{CC}	V_{CC}	GND	GND
131	GND	GND	GND	GND	I/O	I/O
132	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
133	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
136	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
137	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
138	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
141	NC	I/O	I/O	I/O	I/O (WD)	I/O (WD)
142	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
144	I/O	I/O	I/O	I/O	QCLKA, I/O	QCLKA, I/O
146	NC	NC	I/O	I/O	I/O	I/O
147	NC	NC	I/O	I/O	I/O	I/O
148	NC	NC	I/O	I/O	I/O	I/O
149	NC	NC	I/O	I/O	V_{CC}	V_{CC}
150	GND	GND	GND	GND	I/O	I/O
151	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
152	I/O	I/O	I/O	I/O	I/O (WD)	I/O (WD)
154	I/O	I/O	I/O	I/O	TDI, I/O	TDI, I/O

208-Pin PQFP Package, 208-Pin RQFP Package (Continued)

Pin Number	A1280XL Function	A32100DX Function	A32140DX Function	A32200DX-PQ208 Function	A32200DX-RQ208 Function	A32300DX Function
155	I/O	I/O	I/O	I/O	TMS, I/O	TMS, I/O
156	I/O	I/O	I/O	I/O	GND	GND
157	GND	GND	GND	GND	V_{CC}	V_{CC}
159	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O	I/O	I/O
161	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
162	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
164	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
165	NC	NC	I/O	I/O	I/O	I/O
166	NC	NC	I/O	I/O	I/O	I/O
168	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
169	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
171	NC	QCLKD, I/O	I/O	QCLKD, I/O	I/O	I/O
176	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
177	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
178	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O	V_{CC}	V_{CC}
180	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O	I/O	I/O
181	NC	I/O	I/O	I/O	V_{CC}	V_{CC}
182	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
183	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
184	GND	GND	GND	GND	I/O	I/O
186	CLKB, I/O	CLKB	CLKB, I/O	CLKB, I/O	I/O	I/O
187	I/O	I/O	I/O	I/O	GND	GND
188	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O	I/O	I/O
190	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
191	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
193	NC	I/O	I/O	I/O	I/O	I/O
194	NC	NC	I/O (WD)	I/O (WD)	I/O	I/O
195	NC	I/O	I/O (WD)	I/O (WD)	I/O	I/O
196	I/O	QCLKC, I/O	I/O	QCLKC, I/O	I/O	I/O
197	NC	NC	I/O	I/O	I/O	I/O
201	NC	I/O	I/O	I/O	I/O	I/O
202	V_{CC}	V_{CC}	V_{CC}	V_{CC}	I/O	I/O
203	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
204	I/O	I/O (WD)	I/O (WD)	I/O (WD)	I/O	I/O
206	I/O	I/O	I/O	I/O	MODE	MODE (GND)
207	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O	V_{CC}	V_{CC}
208	I/O	I/O	I/O	I/O	GND	GND

Package Pin Assignments (continued)

240-Pin RQFP Package (Top View)



Notes:

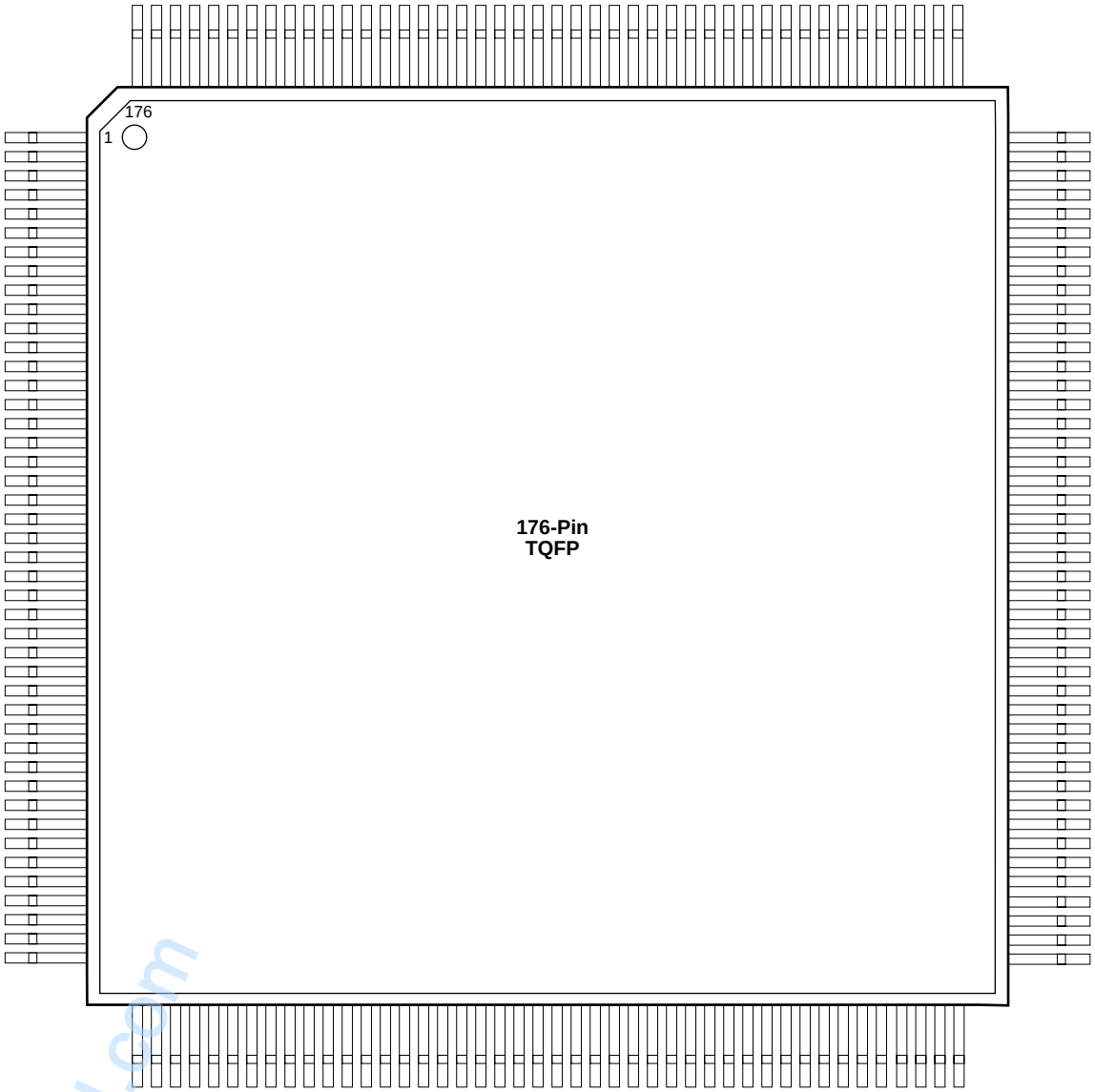
1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-Decode I/O (WD) can also be general purpose user I/O.*
3. *NC: Denotes 'No Connection.'*
4. *All unlisted pin numbers are user I/O's.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*
6. *RQFP has an exposed circular metal heat sink on the top surface.*

240-Pin RQFP Package

Pin Number	A32200DX Function	A32300DX Function
2	DCLK, I/O	DCLK, I/O
6	I/O (WD)	I/O (WD)
7	I/O (WD)	I/O (WD)
8	V_{CC}	V_{CC}
15	QCLKC, I/O	QCLKC, I/O
17	I/O (WD)	I/O (WD)
18	I/O (WD)	I/O (WD)
21	I/O (WD)	I/O (WD)
22	I/O (WD)	I/O (WD)
24	PRB, I/O	PRB, I/O
26	CLKB, I/O	CLKB, I/O
28	GND	GND
29	V_{CC}	V_{CC}
30	V_{CC}	V_{CC}
32	CLKA, I/O	CLKA, I/O
33	I/O	I/O (WD)
34	PRA, I/O	PRA, I/O
37	I/O (WD)	I/O (WD)
38	I/O (WD)	I/O (WD)
45	QCLKD, I/O	QCLKD, I/O
47	I/O (WD)	I/O (WD)
48	I/O (WD)	I/O (WD)
52	V_{CC}	V_{CC}
54	I/O (WD)	I/O (WD)
55	I/O (WD)	I/O (WD)
57	SDI, I/O	SDI, I/O
59	V_{CC}	V_{CC}
60	GND	GND
61	GND	GND
71	V_{CC}	V_{CC}
85	V_{CC}	V_{CC}
88	V_{CC}	V_{CC}
89	V_{CC}	V_{CC}
90	V_{CC}	V_{CC}
91	GND	GND
92	TCK, I/O	TCK, I/O
94	GND	GND
108	V_{CC}	V_{CC}
118	V_{CC}	V_{CC}
119	GND	GND
120	GND	GND
121	GND	GND
123	SDO, TDO, I/O	SDO, TDO, I/O
125	I/O (WD)	I/O (WD)
126	I/O (WD)	I/O (WD)
128	V_{CC}	V_{CC}
132	I/O (WD)	I/O (WD)
133	I/O (WD)	I/O (WD)
135	QCLKB, I/O	QCLKB, I/O
142	I/O (WD)	I/O (WD)
143	I/O (WD)	I/O (WD)
147	I/O	I/O (WD)
148	I/O	I/O (WD)
150	V_{CC}	V_{CC}
151	V_{CC}	V_{CC}
152	GND	GND
159	I/O (WD)	I/O (WD)
160	I/O (WD)	I/O (WD)
163	I/O (WD)	I/O (WD)
164	I/O (WD)	I/O (WD)
166	QCLKA, I/O	QCLKA, I/O
172	V_{CC}	V_{CC}
174	I/O (WD)	I/O (WD)
175	I/O (WD)	I/O (WD)
178	TDI, I/O	TDI, I/O
179	TMS, I/O	TMS, I/O
180	GND	GND
181	V_{CC}	V_{CC}
182	GND	GND
192	V_{CC}	V_{CC}
206	V_{CC}	V_{CC}
209	V_{CC}	V_{CC}
210	V_{CC}	V_{CC}
219	V_{CC}	V_{CC}
227	V_{CC}	V_{CC}
237	GND	GND
238	MODE (GND)	MODE (GND)
239	V_{CC}	V_{CC}
240	GND	GND

Package Pin Assignments (continued)

176-Pin TQFP Package (Top View)



Notes:

1. *I/O (WD): Denotes I/O pin with an associated wide-decode module.*
2. *Wide-Decode I/O (WD) can also be general-purpose user I/O.*
3. *NC: Denotes 'No Connection.'*
4. *All unlisted pin numbers are user I/O's.*
5. *MODE should be terminated to GND through a 10K resistor to enable ActionProbe usage; otherwise it can be terminated directly to GND.*

176-pin TQFP Package

Pin Number	A1240XL Function	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
1	GND	GND	GND	GND	GND
2	MODE	MODE	MODE	MODE	MODE
8	NC	NC	NC	NC	I/O
10	NC	NC	I/O	I/O	I/O
11	NC	NC	I/O	I/O	I/O
13	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
18	GND	GND	GND	GND	GND
19	NC	I/O	I/O	I/O	I/O
20	NC	I/O	I/O	I/O	I/O
22	NC	I/O	I/O	I/O	I/O
23	GND	GND	GND	GND	GND
24	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
25	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
26	NC	I/O	I/O	I/O	I/O
27	NC	I/O	I/O	I/O	I/O
28	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
29	NC	NC	I/O	I/O	I/O
33	NC	NC	NC	NC	I/O
37	NC	NC	I/O	I/O	I/O
38	NC	NC	NC	NC	I/O
45	GND	GND	GND	GND	GND
46	I/O	I/O	I/O	TMS, I/O	TMS, I/O
47	I/O	I/O	I/O	TDI, I/O	TDI, I/O
48	I/O	NC	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O	I/O (WD)
50	I/O	I/O	I/O	I/O (WD)	I/O (WD)
51	I/O	I/O	I/O	I/O (WD)	I/O
52	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
54	NC	I/O (WD)	I/O	I/O	I/O
55	NC	I/O (WD)	I/O	I/O	I/O (WD)
56	I/O	I/O	I/O	I/O	I/O (WD)
57	NC	NC	NC	QCLKA, I/O	I/O
59	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
60	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
61	NC	I/O	I/O	I/O	I/O
64	NC	I/O	I/O	I/O	I/O
66	NC	I/O	I/O	I/O	I/O
67	GND	GND	GND	GND	GND
68	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
69	I/O	I/O (WD)	I/O	I/O	I/O (WD)
70	I/O	I/O (WD)	I/O	I/O	I/O (WD)
72	I/O	I/O	I/O	I/O (WD)	I/O
73	I/O	I/O (WD)	I/O	I/O (WD)	I/O
74	NC	NC	I/O	I/O	I/O
75	I/O	I/O (WD)	I/O	I/O	I/O
76	I/O	I/O	I/O	QCLKB, I/O	I/O
77	NC	NC	NC	I/O	I/O (WD)
78	NC	NC	I/O	I/O (WD)	I/O (WD)
79	I/O	I/O	I/O	I/O (WD)	I/O
80	NC	I/O (WD)	I/O	NC	I/O

176-pin TQFP Package (Continued)

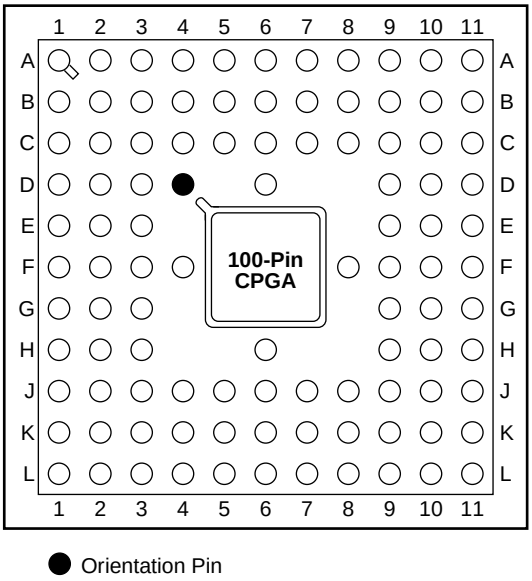
Pin Number	A1240XL Function	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
81	I/O	I/O (WD)	I/O	I/O	I/O
82	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
84	I/O	I/O	I/O	I/O (WD)	I/O (WD)
85	I/O	I/O	I/O	I/O (WD)	I/O (WD)
86	NC	NC	I/O	I/O	I/O
87	I/O	I/O	I/O	SDO, TDO, I/O	SDO, TDO, I/O
89	GND	GND	GND	GND	GND
96	NC	NC	I/O	I/O	I/O
97	NC	I/O	I/O	I/O	I/O
101	NC	NC	NC	NC	I/O
103	NC	I/O	I/O	I/O	I/O
106	GND	GND	GND	GND	GND
107	NC	I/O	I/O	I/O	I/O
108	NC	I/O	I/O	TCK, I/O	TCK, I/O
109	GND	GND	GND	GND	GND
110	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
111	GND	GND	GND	GND	GND
112	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
113	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
114	NC	I/O	I/O	I/O	I/O
115	NC	I/O	I/O	I/O	I/O
116	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
117	I/O	NC	I/O	I/O	I/O
121	NC	NC	NC	I/O	I/O
124	NC	NC	I/O	I/O	I/O
125	NC	NC	I/O	I/O	I/O
126	NC	NC	NC	NC	I/O
133	GND	GND	GND	GND	GND
135	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O	SDI, I/O
136	NC	NC	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O (WD)	I/O (WD)
138	I/O	I/O	I/O	I/O (WD)	I/O (WD)
139	I/O	I/O (WD)	I/O	I/O	I/O
140	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
141	I/O	I/O (WD)	I/O	I/O	I/O
142	I/O	I/O	I/O	I/O (WD)	I/O
143	NC	I/O	I/O	I/O (WD)	I/O
144	NC	I/O (WD)	I/O	I/O	I/O (WD)
145	NC	NC	NC	NC	I/O (WD)
146	I/O	I/O (WD)	I/O	QCLKD, I/O	I/O
147	NC	I/O	I/O	I/O	I/O
149	I/O	I/O (WD)	I/O	I/O	I/O
150	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
151	NC	I/O	I/O	I/O (WD)	I/O (WD)
152	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O	PRA, I/O
154	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O	CLKA, I/O
155	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
156	GND	GND	GND	GND	GND
158	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O	CLKB, I/O
160	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O	PRB, I/O

176-pin TQFP Package (Continued)

Pin Number	A1240XL Function	A3265DX Function	A1280XL Function	A32100DX Function	A32140DX Function
161	NC	I/O	I/O	I/O (WD)	I/O (WD)
162	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
163	I/O	I/O (WD)	I/O	I/O	I/O
164	I/O	I/O	I/O	QCLKC, I/O	I/O
165	NC	NC	NC	NC	I/O (WD)
166	NC	I/O	I/O	I/O	I/O (WD)
168	NC	I/O	I/O	I/O	I/O
169	I/O	I/O (WD)	I/O	I/O	I/O
170	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
171	I/O	I/O (WD)	I/O	I/O (WD)	I/O (WD)
172	I/O	I/O	I/O	I/O (WD)	I/O (WD)
173	NC	NC	I/O	I/O	I/O
175	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O	DCLK, I/O

Package Pin Assignments (continued)

100-Pin CPGA (Top View)



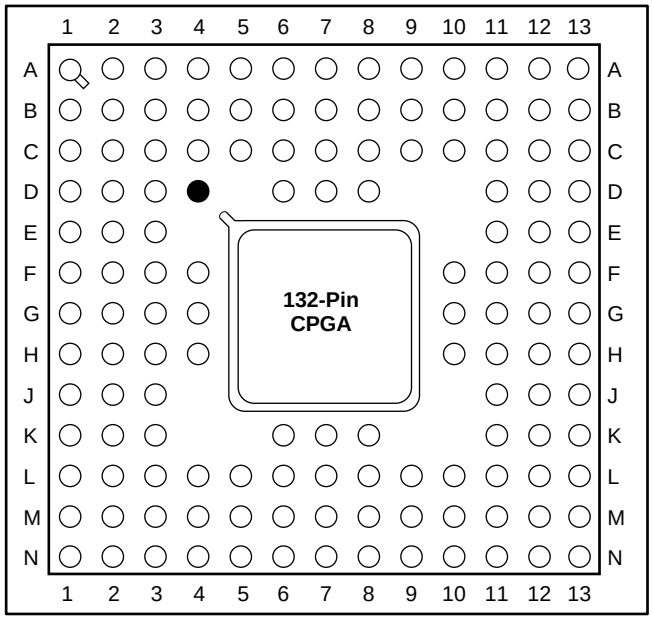
Signal	Pad Number	Location
PRA or I/O	85	A7
PRB or I/O	92	A4
MODE	2	C2
SDI or I/O	77	C8
DCLK or I/O	100	C3
CLKA or I/O	87	C6
CLKB or I/O	90	D6
GND	7, 20, 32, 44, 55, 70, 82, 94	E3, G3, J5, J7, G9, F11, D10, C7, C5
V_{CC}	15, 38, 64, 88	F3, G1, K6, F9, F10, E11, B6

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

132-Pin CPGA (Top View)



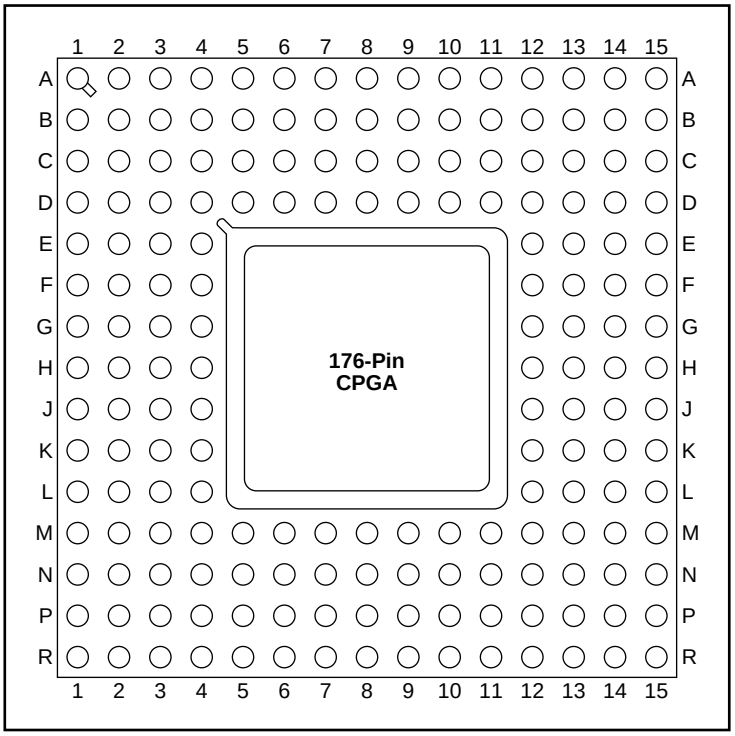
Signal	Pad Number	Location
PRA or I/O	113	B8
PRB or I/O	121	C6
MODE	2	A1
SDI or I/O	101	B12
DCLK or I/O	132	C3
CLKA or I/O	115	B7
CLKB or I/O	119	B6
GND	9, 10, 26, 27, 41, 58, 59, 73, 74, 92, 93, 107, 108, 125, 126	E3, F4, J2, J3, L5, L9, M9, K12, J11, H13, E12, E11, C9, B9, B5, C5
V_{CC}	18, 19, 49, 50, 83, 84, 116, 117	G3, G2, G4, L7, K7, G10, G11, G12, G13, D7, C7

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

176-Pin CPGA (Top View)



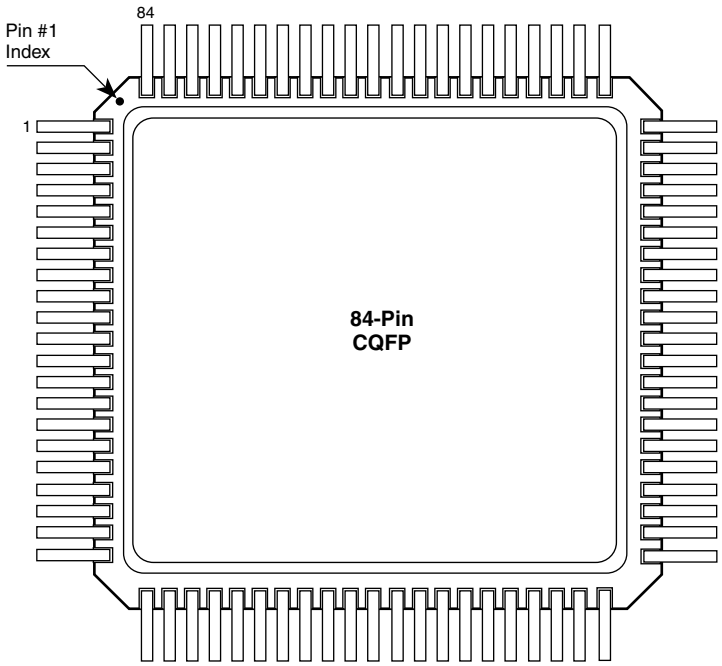
Signal	Pad Number	Location
PRA or I/O	152	C9
PRB or I/O	160	D7
MODE	2	C3
SDI or I/O	135	B14
DCLK or I/O	175	B3
CLKA or I/O	154	A9
CLKB or I/O	158	B8
GND	1, 8, 18, 23, 33, 38, 45, 57, 67, 77, 89 101, 106, 111, 121, 126, 133, 145, 156, 165	D4, E4, G4, H4, K4, L4, M4, M6, M8, M10, M12 K12, J12, J13, H12, F12, E12, D12, D10, C8, D6
V_{CC}	13, 24, 28, 52, 68, 82, 112, 116, 140, 155, 170	F4, H2, H3, J4, M5, N8, M11, J14, H13, H14, G12, D11, D8, D5

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

Package Pin Assignments (continued)

84-Pin CQFP



Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

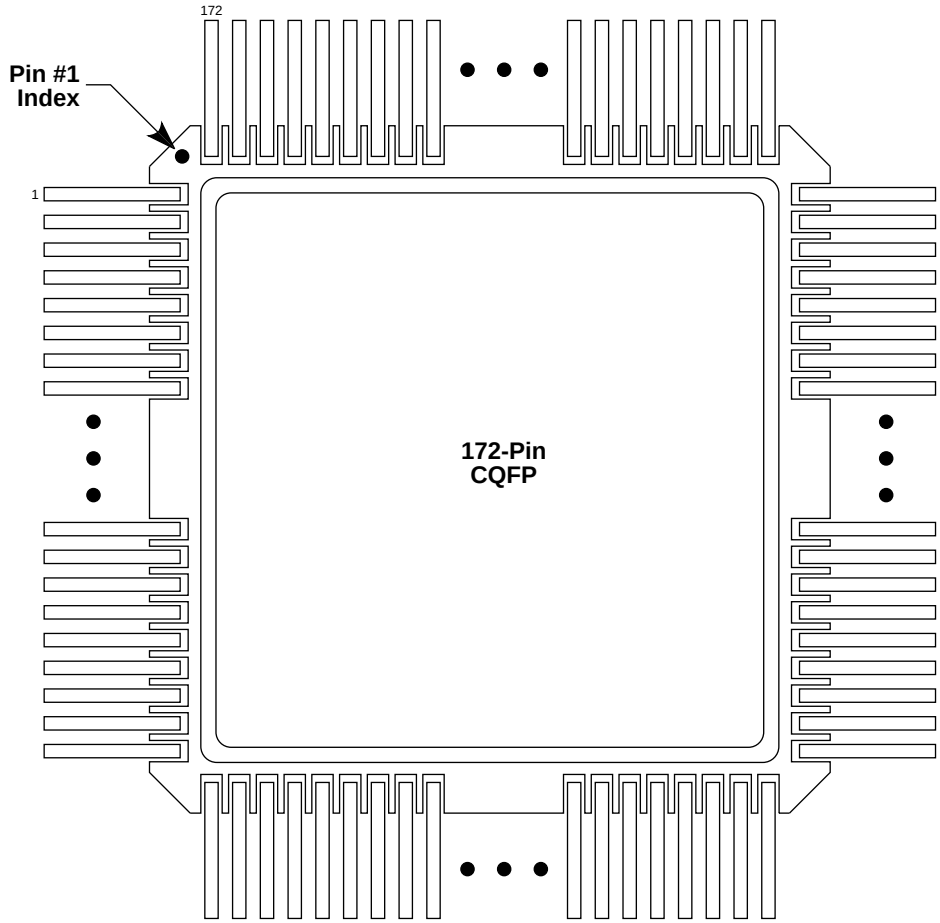
84-pin CQFP Package

Pin Number	A32100DX Function
1	GND
2	MODE (GND)
7	V_{CC}
10	GND
11	V_{CC}
12	V_{SV} (V_{CC})
17	GND
22	GND
23	TMS, I/O
24	TDI, I/O
25	I/O (WD)
26	I/O (WD)
28	QCLKA, I/O
30	I/O (WD)
32	GND
33	V_{CC}
34	I/O (WD)
35	I/O (WD)
36	QCLKB, I/O
37	I/O (WD)
38	GND
39	I/O (WD)
40	I/O (WD)
41	I/O (WD)
42	SDO, I/O
43	GND
50	GND

Pin Number	A32100DX Function
51	TCK, I/O
52	VKS (GND)
53	V_{PP} (V_{CC})
55	V_{SV} (V_{CC})
56	V_{CC}
59	GND
63	GND
64	SDI
65	I/O (WD)
66	I/O (WD)
67	I/O (WD)
68	I/O (WD)
69	QCLKD, I/O
70	I/O (WD)
71	I/O (WD)
72	PRA, I/O
73	CLKA, I/O
74	V_{CC}
76	CLKB, I/O
77	PRB, I/O
78	I/O (WD)
79	I/O (WD)
80	QCLKC, I/O
81	GND
82	I/O (WD)
83	I/O (WD)
84	DCLK, I/O

Package Pin Assignments (continued)

172-Pin CQFP



Signal	Pad Number
CLKA or I/O	150
CLKB or I/O	154
DCLK or I/O	171
GND	7, 17, 22, 32, 37, 55, 65, 75, 98, 103, 106, 118, 123, 141, 152, 161
MODE	1
PRA or I/O	148
PRB or I/O	156
SDI or I/O	131
V_{CC}	12, 23, 24, 27, 50, 66, 80, 107, 109, 110, 113, 136, 151, 166

Notes:

1. *Unused I/O pins are designated as outputs by ALS and are driven LOW.*
2. *All unassigned pins are available for use as I/Os.*
3. *MODE = GND, except during device programming or debugging.*

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v3.0)	Page
Unspecified	Because the changes in this data sheet are extensive and technical in nature—due to the elimination of 32400DX product—this should be viewed as a new document. Please read it as you would a data sheet that is published for the first time. Note that the "Package and Mechanical Drawings" section has been eliminated from the data sheet and can now be found on the Actel web site. Note that the "Package Characteristics and Mechanical Drawings" section has been eliminated from the data sheet. The mechanical drawings are now contained in a separate document, "Package Characteristics and Mechanical Drawings," available on the Actel web site.	ALL

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as "Advanced" or Preliminary" data sheets. The definition of these categories are as follows:

Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

The data sheet contains information that is considered to be final.

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