



Product Specification

A150XN01 V0

AU OPTRONICS CORPORATION

(V) Preliminary Specification

() Final Specification

Module	15" XGA TFT-LCD Semi-Module
Model Name	A150XN01 V0

Customer	Date
_____	_____
Approved by	
_____	_____
Note: This Specification is subject to change without notice.	

Checked & Approved by	Date
<i>FY Gan</i>	03/18/2008
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Audio-Video Display Business Unit / AU Optronics corporation	



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Record of Revision

Version and Date	Page	Old description	New Description
0.1 2007/04/19	All	First Draft	All
0.2 2007/04/25	9 18	4.1 Absolute Ratings of TFT LCD module: Logic LCD drive voltage VDD 0.3(min), 3.6(Max) --	4.1 Absolute Ratings of TFT LCD module: Logic LCD drive voltage VDD -0.3(min), 4.0(Max) Add 6.5 Color Input Data Reference
0.3 2007/09/27	5 6 10 11 12 22 23	2.1 Cell transmittance, Power consumption, Weight : TBD 2.2 Cell transmittance: TBD 4.3 Absolute Ratings of Environment TOP, TST TBD 5.1.1 IDD, Irush, PDD TBD 5.1.2 VID, VICM spec 9. Outline Drawing 10. Packing Form	2.1 Cell transmittance: (8.8), Power consumption: 2.5, Weight: 315 2.2 Cell transmittance: (8.8) 4.3 Absolute Ratings of Environment TOP 65C, TST 80C 5.1.1 IDD: 750, Irush:930, PDD: 2.5 5.1.2 VID: 250(min), 350(typ), 450(Max). VICM: 1.0(min), 1.25(typ), 2(Max) 9. Update Outline Drawing 10. Update Packing Form
0.4 2008/02/27	22	9. outline drawing	9. update outline drawing
0.5 2008/03/18	11 12,13	VDD current =750mA ---	Updated VDD current =600mA Add LVDS Setup/Hold time Add Cycle Jitter Add Clock Cycle Rate of Change
0.6 2008/	6	Transmittance min.: NA	Transmittance min.: 7.8%



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Handling Precautions

- 1) Since front polarizer is easily damaged, pay attention not to scratch it.
- 2) Be sure to turn off power supply when inserting or disconnecting from input connector.
- 3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- 4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
- 5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
- 6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
- 7) Do not open or modify the Module Assembly.
- 8) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
- 9) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.



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2. General Description

This specification applies to the 15 inch Color TFT-LCD Semi-Module A150XN01 V0

The display supports the XGA (1024(H) x 768(V)) screen format and 16.2M colors. All input signals are 1 Channel LVDS interface compatible.

This module does not contain the backlight.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

Items	Unit	Specifications
Active Area	[mm]	304.128 (H) x 228.096
Pixels H x V		1024(x3) x 768
Pixel Pitch	[mm]	0.297 (per one triad) x 0.297
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		TN mode, Normally White
Cell Transmittance	[%]	(8.8)
Contrast Ratio		500:1
Optical ResponseTime	[msec]	12 (Typ, on/off)
Nominal Input Voltage VDD	[Volt]	+3.3 (Typ)
Power Consumption(Black Pattern)	[Watt]	2.5 (Typ)
Weight	[Grams]	315 (Typ)
Physical Size (H x V x D)	[mm]	316.23(W) x 242.55(H) x 1.9(D) (Typ)
Electrical Interface		one Channel LVDS
Surface Treatment		Glare type, Hardness 3H
Support Colors		16.2M colors (RGB 6-bits+FRC)
RoHS Compliance		RoHS Compliance



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2.2 Optical Characteristics

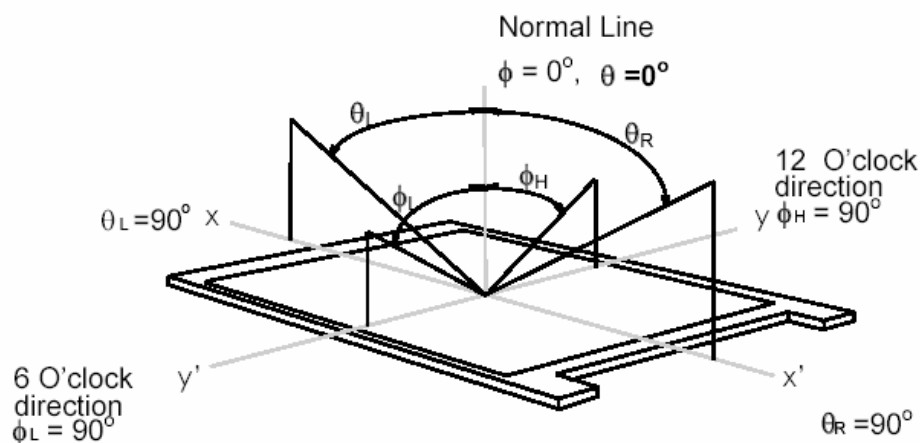
The optical characteristics are measured under stable conditions at 25°C (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree]	Horizontal (Right)		80	-	1
		CR > 10 (Left)		80		
		Vertical (Up)		80	-	
CR > 10 (Down)		80				
Optical Response Time	[msec]	Rising + Falling		12		3
Color / Chromaticity Coordinates (CIE 1931)		White x		0.310		2
		White y		0.330		
Cell Transmittance (At CCFL= mA)	[%]		(7.8)	(8.8)	-	2
Contrast Ratio				500:1	-	4

Optical Equipment: BM-5A, BM-7, PR880, or equivalent

Note 1: Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10 , at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.



Note 2: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change

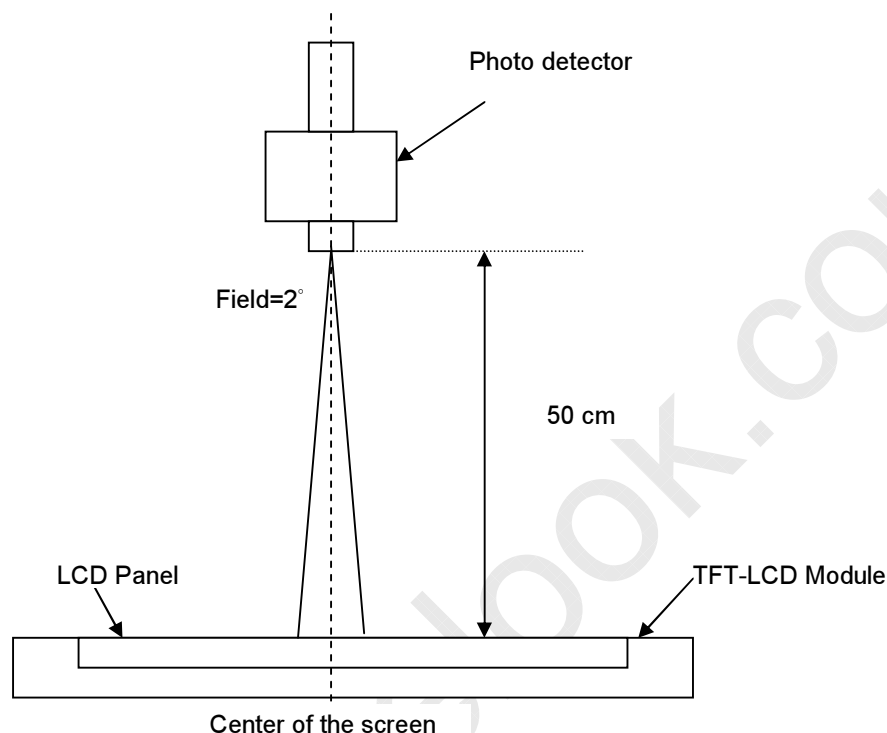


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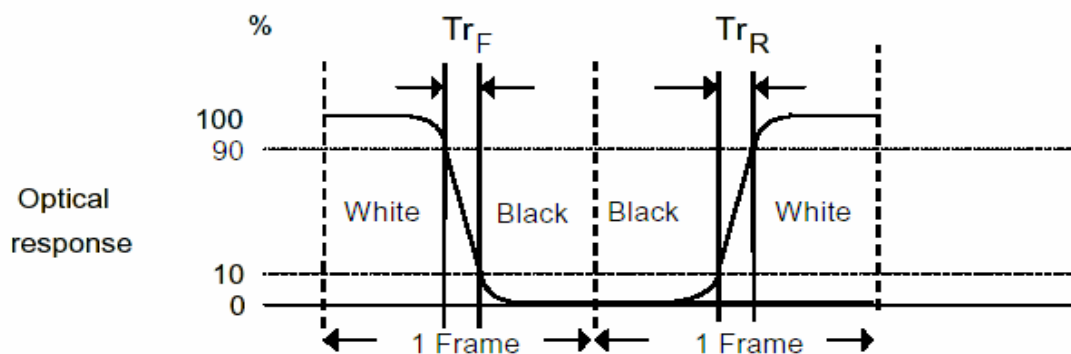
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during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room. Based on backlight chromaticity ($W_x:0.30$, $W_y:0.31$), backlight luminance 3600nit.



Note 3: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from "Full Black" to "Full White" (rising time), and from "Full White" to "Full Black" (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.





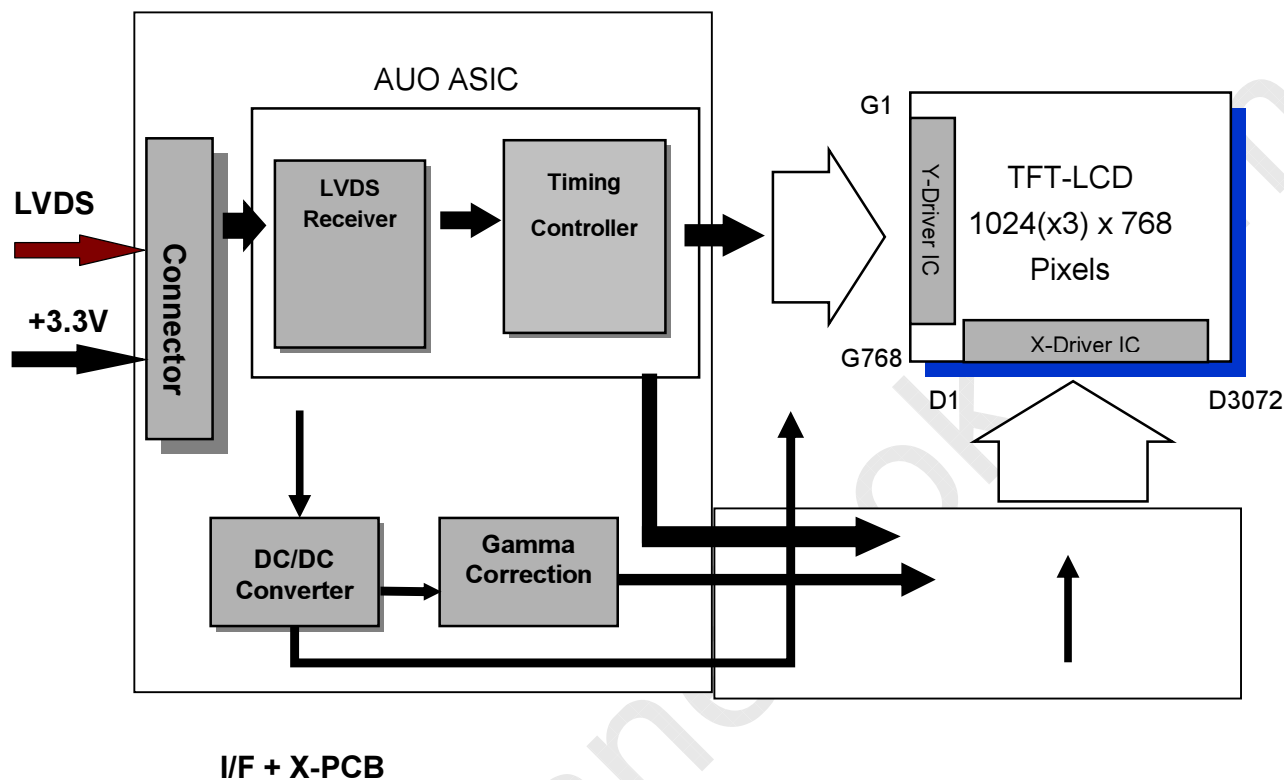
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3. Functional Block Diagram

The following diagram shows the functional block of the 15.0 inches wide Color TFT-LCD Module:





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4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min.	Max.	Unit	Conditions
Logic/LCD Drive Voltage	VDD	-0.3	+4.0	[Volt]	<i>Note 1,2</i>

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min.	Max.	Unit	Conditions
CCFL Current	ICFL	-	8.5	[mA] rms	<i>Note 1,2</i>



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4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	65	[°C]	Note 3
Operating Humidity	HOP	8	90	[%RH]	
Storage Temperature	TST	-20	80	[°C]	
Storage Humidity	HST	8	90	[%RH]	

Note 1: With in Ta= 25°C

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS (Incoming Inspection Standard).



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5. Electrical characteristics

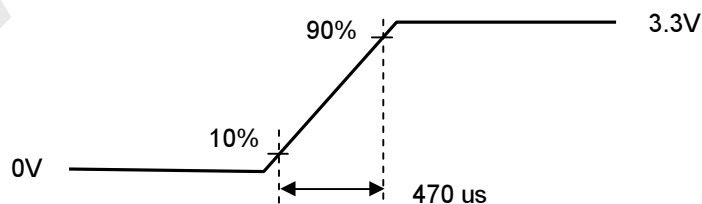
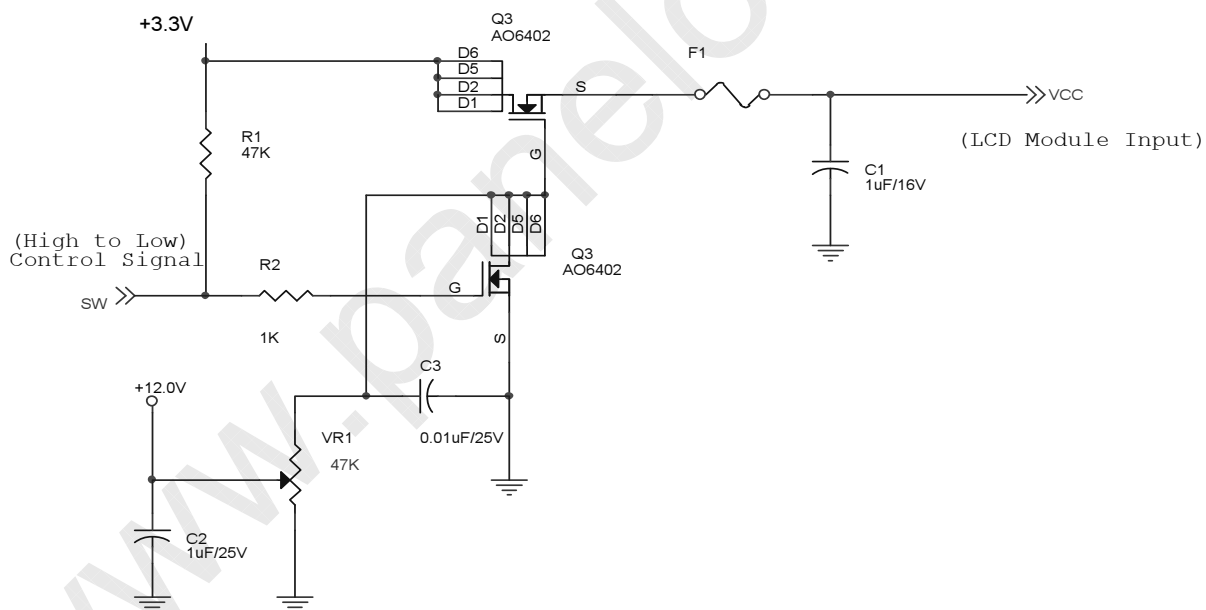
5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows:

Symble	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	±10%
IDD	VDD current	-	600	-	[mA]	Vin=3.3V , Black Pattern, at 60Hz
Irush	LCD Inrush Current	-	930	-	[mA]	Vin rising time = 470us
PDD	VDD Power		2.5	-	[Watt]	Vin=3.3V , Black Pattern, at 60Hz

Note: Measurement conditions:



Vin rising time



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5.1.2 Signal Electrical Characteristics

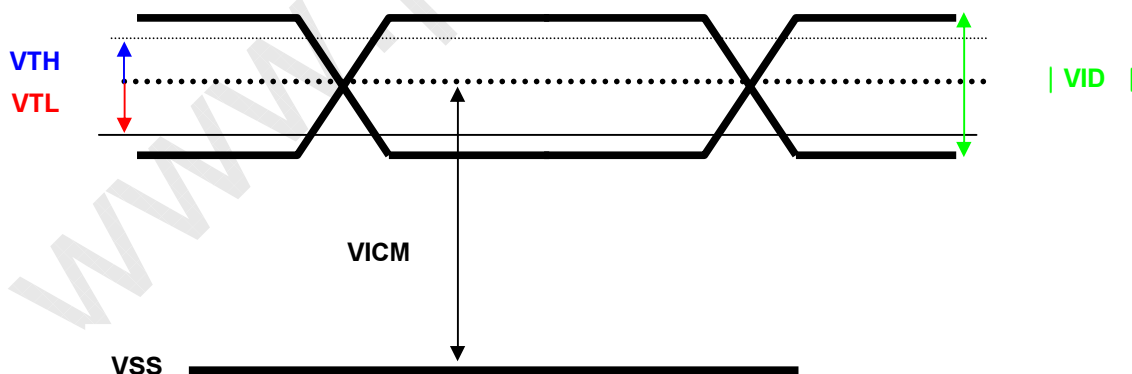
Input signals shall be low or Hi-Z state when V_{in} is off

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Each signal characteristics are as follows;

Symbol	Parameter	Min	Typ	Max	Units	Condition
VTH	Differential Input High Threshold	-	-	100	[mV]	$V_{ICM} = 1.2V$ Note1
VTL	Differential Input Low Threshold	-100	-	-	[mV]	$V_{ICM} = 1.2V$ Note1
VID	Input Differential Voltage	250	350	450	[mV]	Note1
VICM	Differential Input Common Mode Voltage	1.0	1.25	2	[V]	$V_{TH}/V_{TL} = \pm 100mV$ Note1
tsu	Data setup time	400	--	--	ps	$V_{DD}=3.3\pm 0.3V$, $TOP=-10\sim 85\text{ }^{\circ}C$ $T_{clk}=15ns$, $V_{cm}=1.25V$ Note2
thd	Data hold time	400	--	--	ps	$V_{DD}=3.3\pm 0.3V$, $TOP=-10\sim 85\text{ }^{\circ}C$ $T_{clk}=15ns$, $V_{cm}=1.25V$ Note2
Tcj1	Cycle Jitter	--	--	250	ps	
Tcj2	Clock Cycle Rate of Change	--	--	20	ps/cycle	

Note1: LVDS Signal Waveform



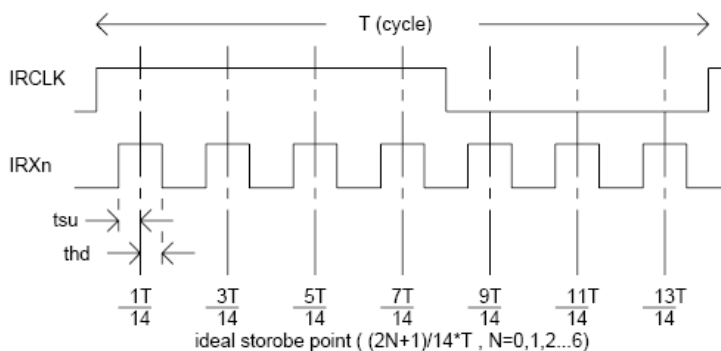


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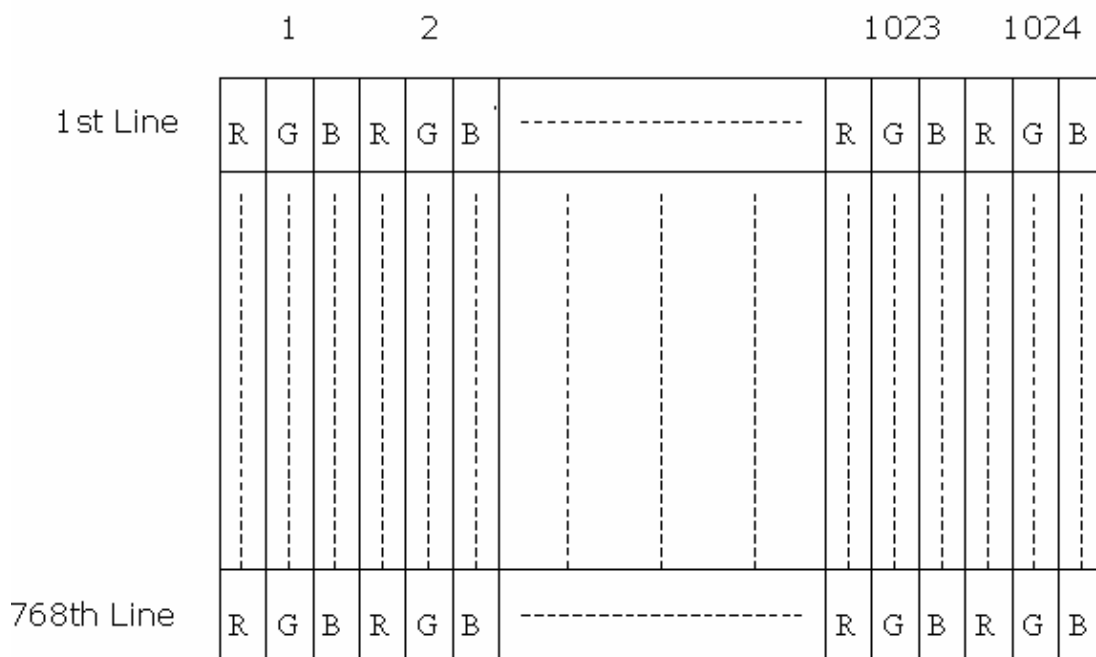
Note2: LVDS Input Signal For Timing Specification



6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



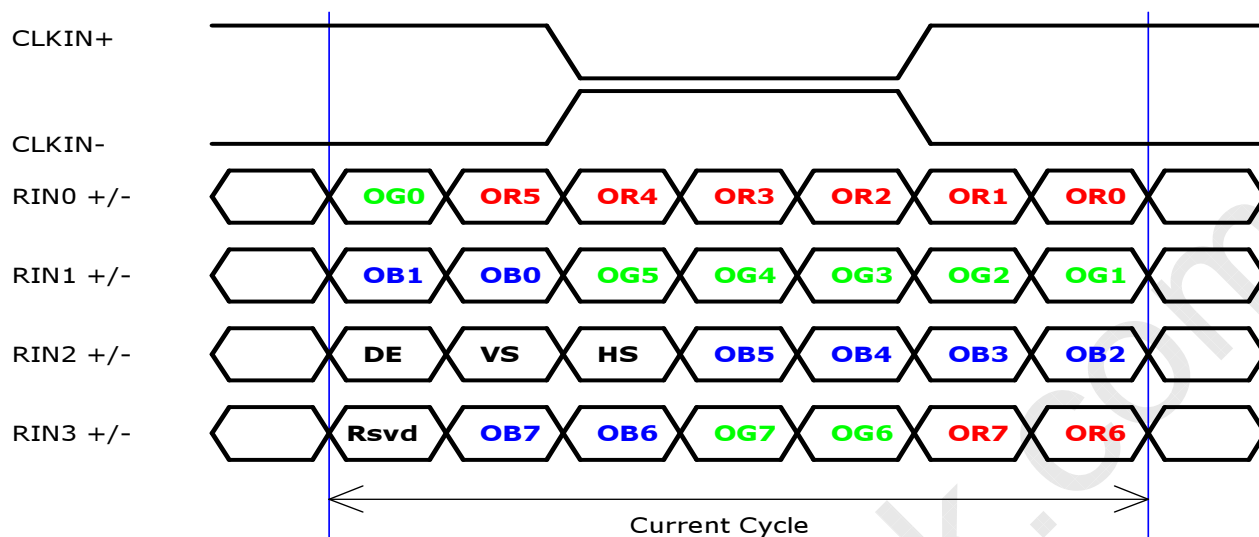


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6.2 The Input Data Format



Note1: Please follow PSWG.

Note2: 8-bit in

Note3: R/G/B data 7:MSB, R/G/B data 0:LSB



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6.3 Signal Description

The module using a pair of LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

DF14A-20P-1.25H (HIROSE)		
Pin No.	Symbol	Description
1	VDD	Power Supply, 3.3V (typical)
2	VDD	Power Supply, 3.3V (typical)
3	VSS	Ground
4	VSS	Ground
5	Rin0-	- LVDS differential data input (R0-R5, G0)
6	Rin0+	+ LVDS differential data input (R0-R5, G0)
7	VSS	Ground
8	Rin1-	- LVDS differential data input (G1-G5, B0-B1)
9	Rin1+	+ LVDS differential data input (G1-G5, B0-B1)
10	VSS	Ground
11	Rin2-	- LVDS differential data input (B2-B5, HS, VS, DE)
12	Rin2+	+ LVDS differential data input (B2-B5, HS, VS, DE)
13	VSS	Ground
14	ClKIN-	- LVDS differential clock input
15	ClKIN+	+ LVDS differential clock input
16	VSS	Ground
17	Rin3-	- LVDS differential data input (R6-R7, G6-G7, B6-B7)
18	Rin3+	+ LVDS differential data input (R6-R7, G6-G7, B6-B7)
19	VSS	Ground
20	VSS	Ground



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6.4 Interface Timing

6.4.1 Timing Characteristics

Signal	Item	Symbol	Min	Typ	Max	Unit
Clock Timing	Clock frequency	Tclk	50	65	81	MHz
Hsync Timing	Horizontal active	Tdisp(h)	1024	1024	1024	Tclk
	Horizontal blanking	Tblk(h)	30	320	1024	Tclk
	Horizontal period	Th	1054	1344	2048	Tck
Vsync Timing	Vertical active	Tdisp(v)	768	768	768	Th
	Vertical blanking	Tblk(v)	8	38	256	Th
	Vertical period	Tv	776	806	1024	Th

Note: DE mode only

Note: Typical value refer to VESA STANDARD

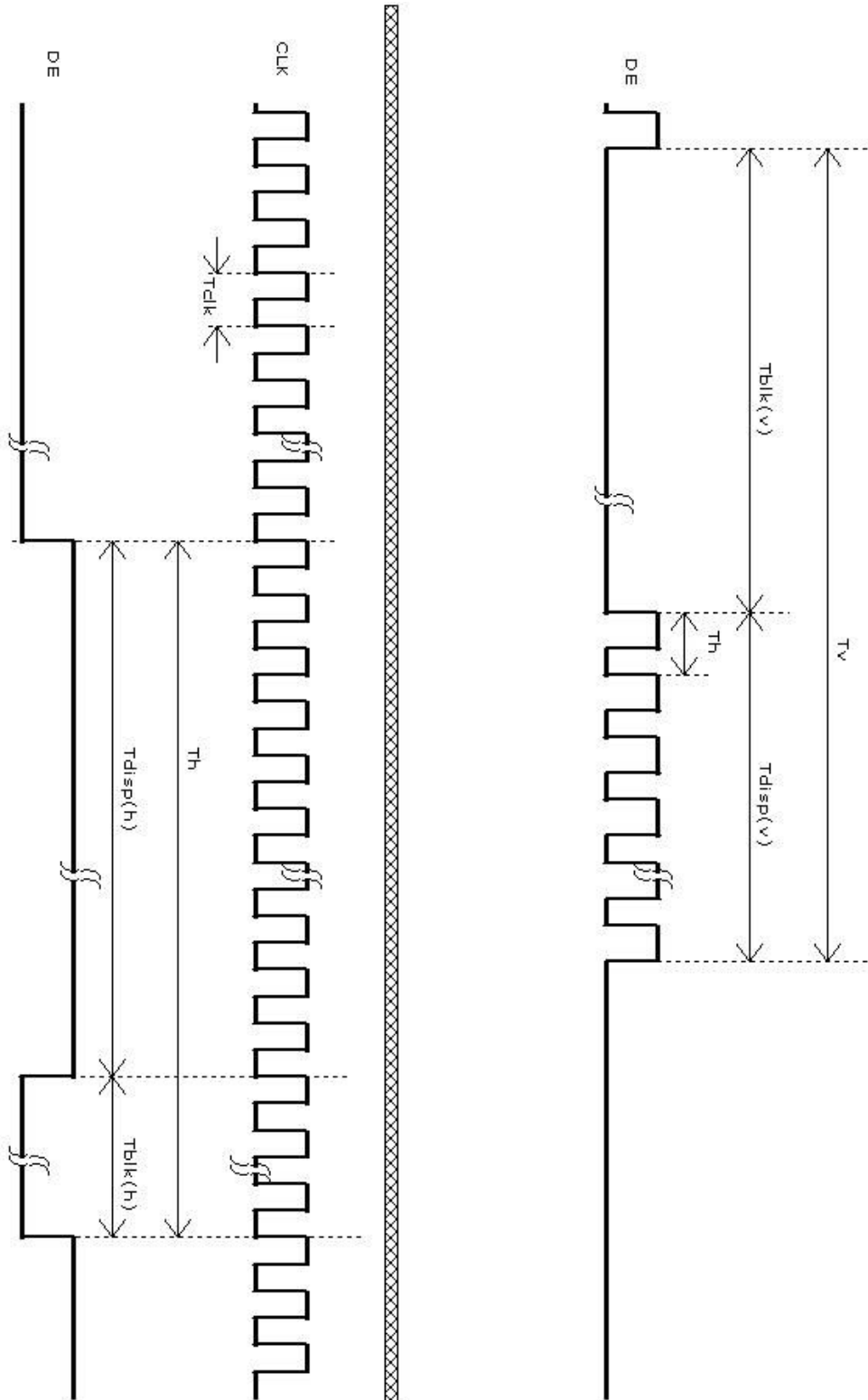


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6.4.2 Timing Diagram





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6.5 Color Input Data Reference

Color Data Reference

Color		Input Color Data																						
		RED							GREEN							BLUE								
		R7 (M)	R6	R5	R4	R3	R2	R1	R0 (L)	R7 (M)	R6	R5	R4	R3	R2	R1	R0 (L)	R7 (M)	R6	R5	R4	R3	R2	R1
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	RED (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED (001)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	—																							
	RED (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	RED (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
GREEN	GREEN (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	GREEN (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	
	—																							
	GREEN (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	GREEN (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
BLUE	BLUE (000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	BLUE (001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	—																							
	BLUE (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	BLUE (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	



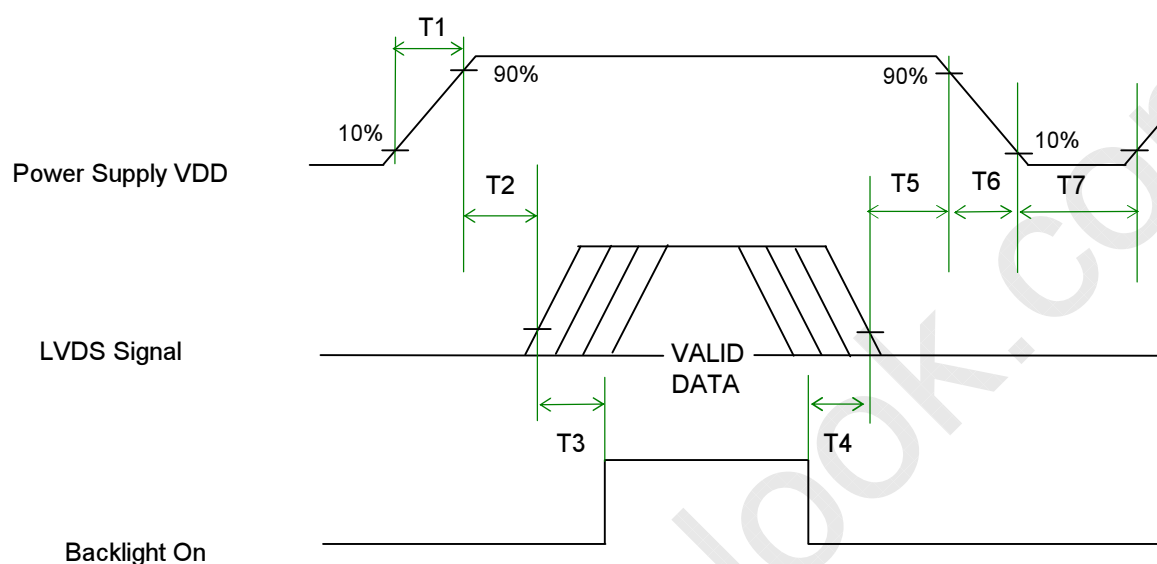
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6.6 Power ON/OFF Sequence

Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.



Power Sequence Timing

Parameter	Value			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	[ms]
T2	30	40	50	[ms]
T3	200	-	-	[ms]
T4	100	-	-	[ms]
T5	0	16	50	[ms]
T6	-	-	10	[ms]
T7	1000	-	-	[ms]



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7. Connector & Pin Assignment

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

7.1.1 Connector

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	HIROSE
Type Part Number	HRS DF14A-20P-1.25H(56)

7.1.2 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	VDD	2	VDD
3	VSS	4	VSS
5	Rin0-	6	Rin0+
7	VSS	8	Rin1-
9	Rin1+	10	VSS
11	Rin2-	12	Rin2+
13	VSS	14	ClkIN-
15	ClkIN+	16	VSS
17	Rin3-	18	Rin3+
19	VSS	20	VSS



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8. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C, 80%RH, 240hours	
High Temperature Operation (HTO)	Ta= 65°C, 240hours	
Low Temperature Operation (LTO)	Ta= 0°C, 240hours	
High Temperature Storage (HTS)	Ta= 80°C, 240hours	
Low Temperature Storage (LTS)	Ta= -10°C, 240hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-10°C/30min, 80°C/30min, 100 cycles	1
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 8 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -10°C to 80°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

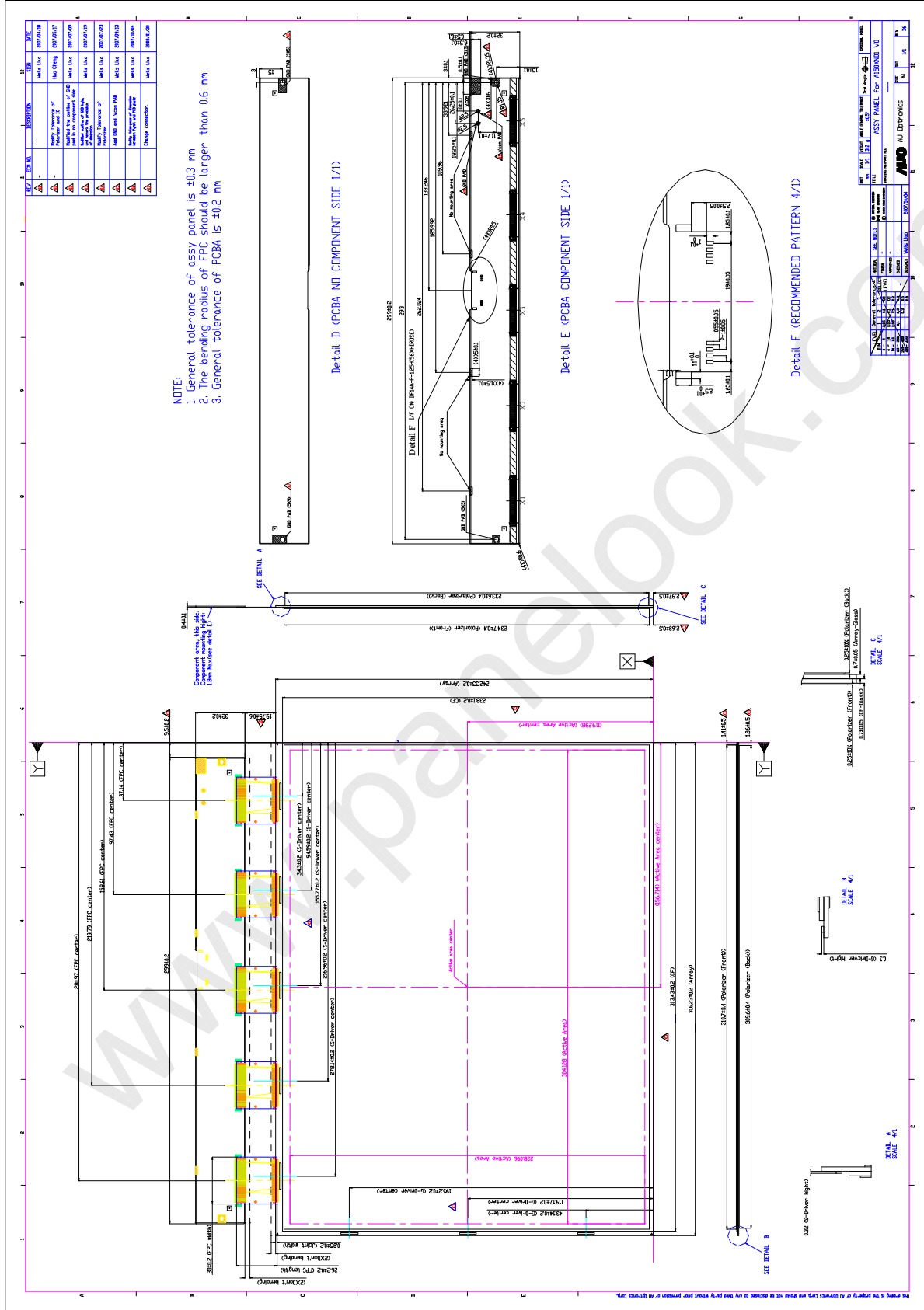


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9. Outline Drawing



NOTE:

1. General tolerance of assy panel is ± 0.3 mm
2. The bending radius of FPC should be larger than 0.6 mm
3. General tolerance of PCBA is ± 0.2 mm

REV	NO.	DATE	DESCRIPTION
1	1	2011/07/07	Initial drawing of
2	1	2011/07/07	Modified the width of AO
3	1	2011/07/07	Modified the width of AO
4	1	2011/07/07	Modified the width of AO
5	1	2011/07/07	Modified the width of AO
6	1	2011/07/07	Modified the width of AO
7	1	2011/07/07	Modified the width of AO
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9	1	2011/07/07	Modified the width of AO
10	1	2011/07/07	Modified the width of AO
11	1	2011/07/07	Modified the width of AO
12	1	2011/07/07	Modified the width of AO
13	1	2011/07/07	Modified the width of AO
14	1	2011/07/07	Modified the width of AO
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18	1	2011/07/07	Modified the width of AO
19	1	2011/07/07	Modified the width of AO
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21	1	2011/07/07	Modified the width of AO
22	1	2011/07/07	Modified the width of AO
23	1	2011/07/07	Modified the width of AO
24	1	2011/07/07	Modified the width of AO
25	1	2011/07/07	Modified the width of AO
26	1	2011/07/07	Modified the width of AO
27	1	2011/07/07	Modified the width of AO
28	1	2011/07/07	Modified the width of AO
29	1	2011/07/07	Modified the width of AO
30	1	2011/07/07	Modified the width of AO



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10. Packing Form

