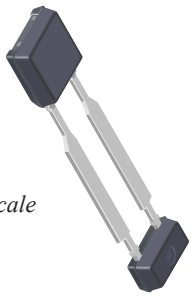
A1688

Two-Wire, True Zero-Speed, High Accuracy Sensor IC

FEATURES AND BENEFITS

- Integrated capacitor reduces need for external EMI protection components
- Wide leads facilitate ease of assembly
- True zero-speed operation
- Automatic Gain Control (AGC) for air gap independent switch points
- Automatic Offset Adjustment (AOA) for signal processing optimization
- Large operating air gap range
- Internal current regulator for two-wire operation
- Undervoltage lockout
- Single chip sensing IC for high reliability
- On-chip voltage regulator with wide operating voltage range and stability in the presence of a variety of complex load impedances
- Fully synchronous digital logic with Scan and IDDQ testing

PACKAGE: 2-pin SIP (suffix UB)



Not to scale

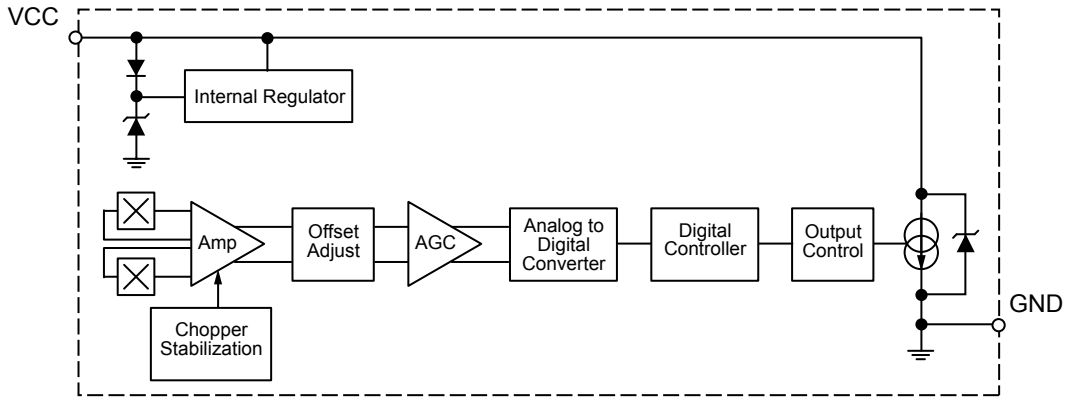
DESCRIPTION

The A1688 is a Hall-effect-based integrated circuit (IC) that provides a user-friendly solution for true zero-speed digital ring magnet and gear tooth sensing in two-wire applications. The A1688 is offered in the UB package, which integrates the IC and a high temperature ceramic capacitor in a single overmolded SIP package. The integrated capacitor provides enhanced EMC performance with reduced external components.

The integrated circuit incorporates a dual-element Hall-effect circuit and signal processing that switches in response to differential magnetic signals created by magnetic encoders, or, when properly back-biased with a magnet, from ferromagnetic targets. The device contains a sophisticated digital circuit that reduces magnet and system offsets, calibrates the gain for air gap independent switch points, and provides true zero-speed operation.

Signal optimization occurs at power-up through the combination of offset and gain-adjust and is maintained throughout operation with the use of a running-mode calibration scheme. Running-mode calibration provides immunity from environmental effects such as micro-oscillations of the sensed target or sudden air gap changes.

The regulated current output is configured for two-wire interface circuitry and is ideally suited for obtaining speed information in wheel speed applications. The Hall element spacing is optimized for high resolution, small diameter targets. The package is lead (Pb) free, with 100% matte-tin leadframe plating.



Functional Block Diagram

SPECIFICATIONS

SELECTION GUIDE

Part Number	Packing*	Power-On State
A1688LUBTN–L–T	4000 pieces per 13-in. reel	$I_{CC(LOW)}$
A1688LUBTN–H–T	4000 pieces per 13-in. reel	$I_{CC(HIGH)}$

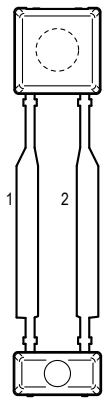
*Contact Allegro™ for additional packing options.

ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		28	V
Reverse Supply Voltage	V_{RCC}		–18	V
Operating Ambient Temperature	T_A	L temperature range	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Internal Discrete Capacitor Ratings

Characteristic	Symbol	Test Conditions*	Value (Typ.)	Unit
Nominal Capacitance	C_{SUPPLY}	Connected between VCC and GND	2200	pF



UB Package, 2-Pin SIP Pinout Diagram

Terminal List Table

Name	Number	Function
VCC	1	Supply Voltage
GND	2	Ground

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OPERATING CHARACTERISTICS: Valid throughout full operating and temperature ranges; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
ELECTRICAL CHARACTERISTICS						
Supply Voltage[2]	V_{CC}	Operating, $T_J < T_J$(max)	4	–	24	V
Undervoltage Lockout	$V_{CC(UV)}$	V_{CC} transitioning from 0 → 5 V or 5 → 0 V	–	3.6	3.95	V
Reverse Supply Current[3]	I_{RCC}	$V_{CC} = V_{RCC}$(max)	–	–	–10	mA
Supply Zener Clamp Voltage	$V_{ZSUPPLY}$	$I_{CC} = I_{CC}$(max) + 3 mA, T_A = 25ºC	28	–	–	V
Supply Zener Current	$I_{ZSUPPLY}$	T_A = 25°C, V_{CC} = 28 V	–	–	19	mA
OUTPUT						
Power-On State	POS	-H variant	–	$I_{CC(HIGH)}$	–	–
		-L variant	–	$I_{CC(LOW)}$	–	–
Supply Current	$I_{CC(LOW)}$	Low-current state	5.9	–	8.4	mA
	$I_{CC(HIGH)}$	High-current state	12	–	16	mA
Supply Current Ratio	$I_{CC(HIGH)} / I_{CC(LOW)}$	Measured as ratio of high current to low current (isothermal)	1.9	–	–	–
Output Rise Time	t_r	Corresponds to measured output slew rate with C_{SUPPLY}; R_{LOAD} = 100 Ω	0	–	1.5	µs
Output Fall Time	t_f	Corresponds to measured output slew rate with C_{SUPPLY}; R_{LOAD} = 100 Ω	0	–	1.5	µs
OPERATING CHARACTERISTICS						
Operate Point	B_{OP}	% of peak-to-peak IC-processed magnetic signal	–	60	–	%
Release Point	B_{RP}	% of peak-to-peak IC-processed magnetic signal	–	40	–	%
Operating Frequency	f_{FWD}		0	–	5	kHz

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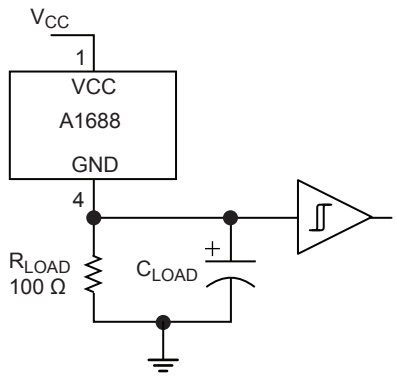

Figure 1: Typical Application Circuit

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OPERATING CHARACTERISTICS (continued): Valid throughout full operating and temperature ranges; unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Unit
OPERATING CHARACTERISTICS (continued)						
Input Signal	B_{SIG}	Differential signal, measured peak-to-peak	20	–	1200	G
Allowable User-Induced Differential Offset	B_{SIGEXT}	External differential signal bias (DC), operating within specification	–300	–	300	G
Sensitivity Temperature Coefficient[4]	TC		–	+0.2	–	%/°C
Total Pitch Deviation		For constant B_{SIG}, sine wave	–	–	±2	%
Maximum Sudden Signal Amplitude Change	$B_{SEQ(n+1)}$ / $B_{SEQ(n)}$	No missed output edge. Instantaneous symmetric magnetic signal amplitude change, measured as a percentage of peak-to-peak B_{SIG} (see figure 2)	–	0.6	–	–
Maximum Total Signal Amplitude Change	$B_{SEQ(max)}$ / $B_{SEQ(min)}$	Overall symmetric magnetic signal amplitude change, measured as a percentage of peak-to-peak B_{SIG}	–	0.2	–	–
Front-End Chopping Frequency			–	400	–	kHz

[1] Typical values are at T_A = 25°C and V_{CC} = 12 V. Performance may vary for individual units, within the specified maximum and minimum limits.
[2] Maximum voltage must be adjusted for power dissipation and junction temperature; see representative discussions in Power Derating section.
[3] Negative current is defined as conventional current coming out of (sourced from) the specified device terminal.
[4] Ring magnets decrease strength with rising temperature. Device compensates. Note that B_{SIG} requirement is not influenced by this.

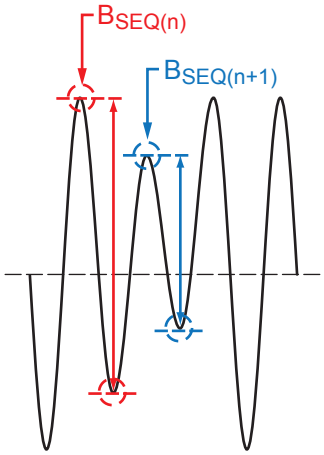

Figure 2: Differential Signal Variation

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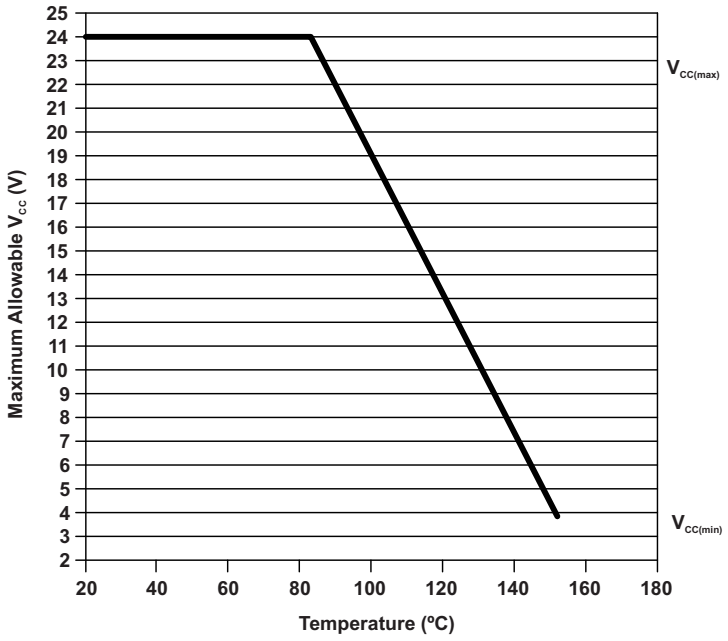
THERMAL CHARACTERISTICS

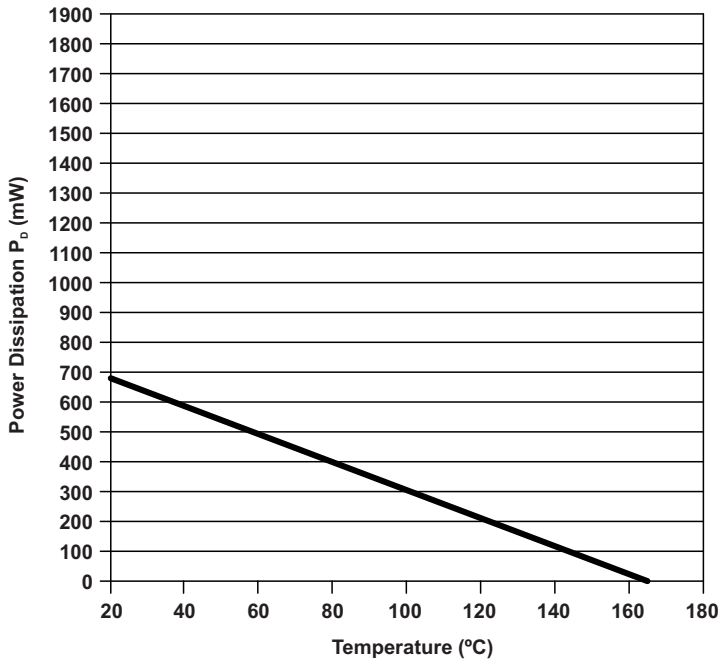
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	Single-layer PCB with copper limited to solder pads	213	°C/W

*Additional thermal information is available on the Allegro website.

Power Derating Curve



Power Dissipation versus Ambient Temperature



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FUNCTIONAL DESCRIPTION

Hall Technology

This single-chip differential Hall-effect sensor IC contains two Hall elements as shown in Figure 5, which simultaneously sense the magnetic profile of the ring magnet or gear target. The magnetic fields are sensed at different points (spaced at a 1.75 mm pitch), generating a differential internal analog voltage, V_{PROC}, that is processed for precise switching of the digital output signal.

The Hall IC is self-calibrating and also possesses a temperature-compensated amplifier and offset cancellation circuitry. Its voltage regulator provides supply noise rejection throughout the operating voltage range. Changes in temperature do not greatly affect this device due to the stable amplifier design and the offset rejection circuitry. The Hall transducers and signal processing electronics are integrated on the same silicon substrate, using a proprietary BiCMOS process.

Target Profiling During Operation

An operating device is capable of providing digital information that is representative of the mechanical features of a rotating gear or ring magnet. The waveform diagram in Figure 5 presents the automatic translation of the mechanical profile, through the magnetic profile that it induces, to the digital output signal of the A1688. No additional optimization is needed, and minimal processing circuitry is required. This ease of use reduces design time and incremental assembly costs for most applications.

Determining Output Signal Polarity

In Figure 5, the top panel, labeled *Mechanical Position*, represents the mechanical features of the ring magnet or gear target and orientation to the device. The bottom panel, labeled *Device Output Signal*, displays the square waveform corresponding to the digital output signal that results from a rotating target configured as shown in Figure 4. That direction of rotation (of the target side adjacent to the package face) is: perpendicular to the leads, across the face of the device, from the pin 1 side to the pin 2 side. This results in the device output switching from high to low output state as a north magnetic pole passes the device face. In this configuration, the device output voltage switches to its high polarity when a south pole is the target feature nearest to the device. If the direction of rotation is reversed or if a part of type A1688LUBxx-L-x is used, then the output polarity inverts (see Table 1).

Table 1: Output Polarity when a South Pole Passes the Package Face in the Indicated Rotation Direction

Rotation Direction	Part Type	
	A1688LUBxx-H-x	A1688LUBxx-L-x
Pin 1 → Pin 2	$I_{CC(HIGH)}$	$I_{CC(LOW)}$
Pin 2 → Pin 1	$I_{CC(LOW)}$	$I_{CC(HIGH)}$

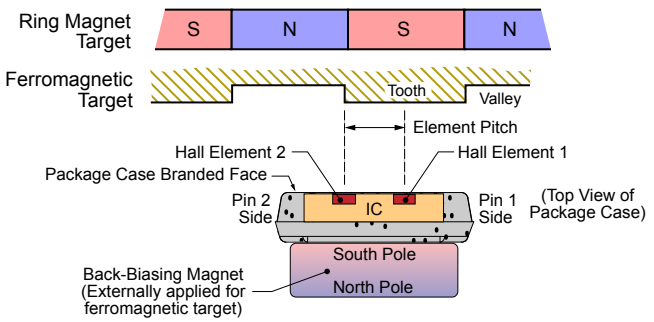

Figure 3: Relative Motion of the Target
Relative Motion of the Target is detected by the dual Hall elements mounted on the Hall IC.

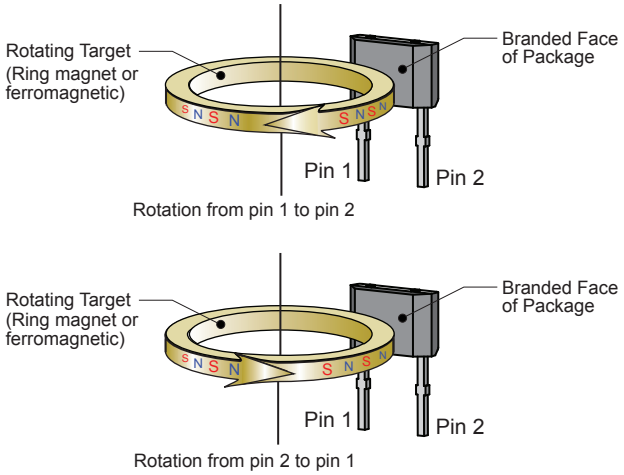

Figure 4: Target Orientation Relative to Device (ring magnet shown).

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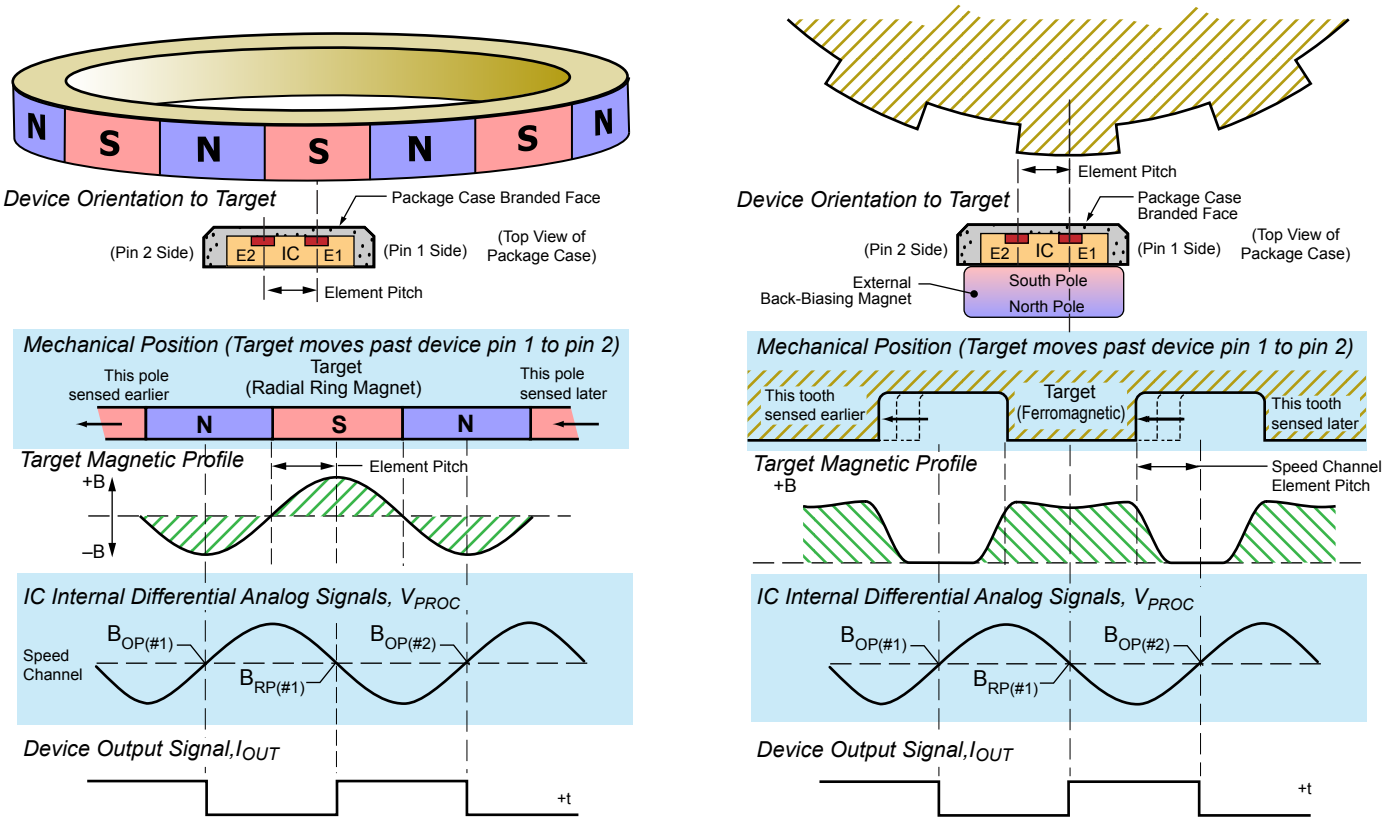

Figure 5: Basic Operation

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POWER DERATING

The device must be operated below the maximum junction temperature of the device, $T_{J(max)}$. Under certain combinations of peak conditions, reliable operation may require derating supplied power or improving the heat dissipation properties of the application. This section presents a procedure for correlating factors affecting operating T_J. (Thermal data is also available on the Allegro MicroSystems website.)

The Package Thermal Resistance, $R_{\theta JA}$, is a figure of merit summarizing the ability of the application and the device to dissipate heat from the junction (die), through all paths to the ambient air. Its primary component is the Effective Thermal Conductivity, K, of the printed circuit board, including adjacent devices and traces. Radiation from the die through the device case, $R_{\theta JC}$, is relatively small component of $R_{\theta JA}$. Ambient air temperature, T_A, and air motion are significant external factors, damped by overmolding.

The effect of varying power levels (Power Dissipation, P_D), can be estimated. The following formulas represent the fundamental relationships used to estimate T_J, at P_D.

$$P_D = V_{IN} \times I_{IN} \quad (1)$$

$$\Delta T = P_D \times R_{\theta JA} \quad (2)$$

$$T_J = T_A + \Delta T \quad (3)$$

For example, given common conditions such as: T_A= 25°C, V_{CC} = 12 V, I_{CC} = 14 mA, and $R_{\theta JA}$ = 213 °C/W, then:

$$P_D = V_{CC} \times I_{CC} = 12\ V \times 14\ mA = 168\ mW$$

$$\Delta T = P_D \times R_{\theta JA} = 168\ mW \times 213\ °C/W = 38.8°C$$

$$T_J = T_A + \Delta T = 25°C + 38.8°C = 63.8°C$$

A worst-case estimate, $P_{D(max)}$, represents the maximum allowable power level ($V_{CC(max)}$, $I_{CC(max)}$), without exceeding $T_{J(max)}$, at a selected $R_{\theta JA}$ and T_A.

Example: Reliability for V_{CC} at T_A=150°C, package UB, using minimum-K PCB.

Observe the worst-case ratings for the device, specifically: $R_{\theta JA}$=213°C/W, $T_{J(max)}$ =165°C, $V_{CC(max)}$= 24 V, and $I_{CC(max)}$ = 16 mA.

Calculate the maximum allowable power level, $P_{D(max)}$. First, invert equation 3:

$$\Delta T_{max} = T_{J(max)} - T_A = 165\,°C - 150\,°C = 15\,°C$$

This provides the allowable increase to T_J resulting from internal power dissipation. Then, invert equation 2:

$$P_{D(max)} = \Delta T_{max} \div R_{\theta JA} = 15°C \div 213\ °C/W = 64.9\,mW$$

Finally, invert equation 1 with respect to voltage:

$$V_{CC(est)} = P_{D(max)} \div I_{CC(max)} = 64.9\,mW \div 16.0\,mA = 4.05\ V$$

The result indicates that, at T_A, the application and device can dissipate adequate amounts of heat at voltages ≤$V_{CC(est)}$.

Compare $V_{CC(est)}$ to $V_{CC(max)}$. If $V_{CC(est)} \leq V_{CC(max)}$, then reliable operation between $V_{CC(est)}$ and $V_{CC(max)}$ requires enhanced $R_{\theta JA}$. If $V_{CC(est)} \geq V_{CC(max)}$, then operation between $V_{CC(est)}$ and $V_{CC(max)}$ is reliable under these conditions.

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PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000408, Rev. 3)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

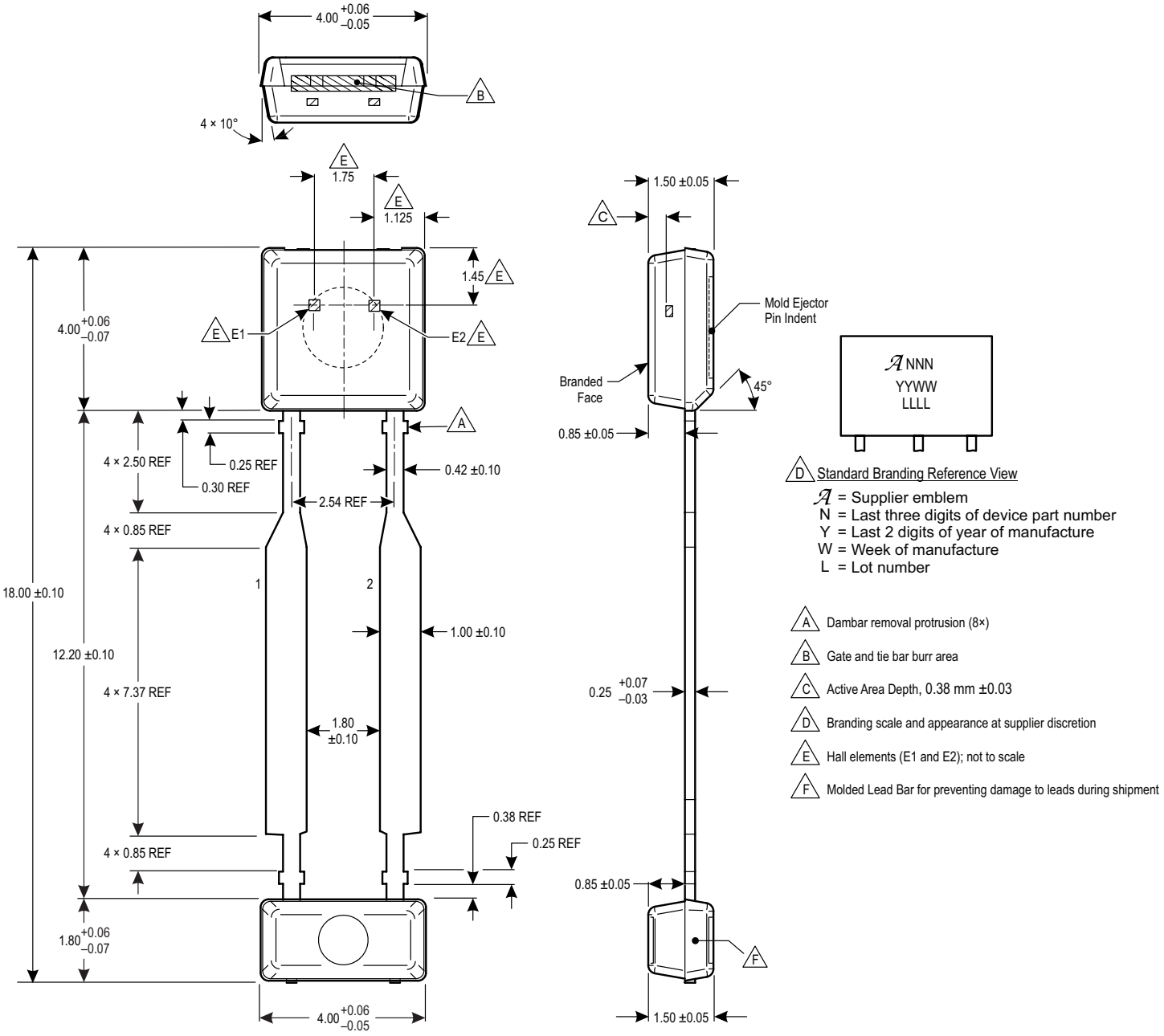

Figure 6: Package UB, 2-Pin SIP

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Revision History

Number	Date	Description
–	March 18, 2014	Initial release. No change from Preliminary Rev. 2.6
1	October 1, 2014	Revised Package Outline Drawing and reformatted datasheet
2	November 10, 2014	Deleted redundant Thermal Characteristics table from page 2
3	December 15, 2014	Corrected error on Package Outline Drawing
4	March 24, 2015	Updated branding on Package Outline Drawing
5	July 10, 2015	Removed bulk options from Selection Guide on page 2
6	March 1, 2016	Updated Internal Discrete Capacitor Ratings table and Package Outline Drawing
7	March 29, 2019	Minor editorial updates
8	April 9, 2020	Minor editorial updates
9	April 30, 2021	Updated Package Outline Drawing (page 9)
10	October 1, 2022	Change product status: Not for new design

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