CHI MEI OPTOELECTRONICS CORP.

DOC No.:
Issued Date: Jan. 18, 2008
Model No.: A190A2-001
**Approval**

# Specifications

## Model No : A190A2-001

## (CR 700:1)

Customer :_____

Approved by : _____

Note :

| Liquid Crystal Display Division | |
|---|---|
| QRA Division. | OA Head Division. |
| Approval | Approval |
| | |



**Version 3.0**

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## REVISION HISTORY

| | Date | Section | Description |
|---|---|---|---|
| 3.0 | Jan, 18, 08' | | A190A2-001 S-ISM Approval Specifications was first issued. |

# 1. GENERAL DESCRIPTION

## 1.1 OVERVIEW

A190A2-001 is a 19" wide TFT Liquid Crystal Display module with 4 CCFL Backlight unit and RSDS interface. This module supports 1440 x 900 WXGA+ mode and can display 16.2M colors.

## 1.2 FEATURES

- Super Wide viewing angle.
- Super High contrast ratio
- Super fast response time
- High color saturation
- WXGA+ (1440 x 900 pixels) resolution
- DE (Data Enable) only mode
- RSDS (reduced swing differential signaling ) interface
- RoHS Compliance

## 1.3 APPLICATION

- TFT LCD Monitor

## 1.4 GENERAL SPECIFICATI0NS

| Item | Specification | Unit | Note |
|---|---|---|---|
| Diagonal Size | 481.4 (19.05" diagonal) | mm | |
| Active Area | 410.4 (H) x 256.5 (V) | mm | (1) |
| Bezel Opening Area | 414.36 x 260.45 | mm | |
| Driver Element | a-si TFT active matrix | - | - |
| Pixel Number | 1440 x R.G.B. x 900 | pixel | - |
| Pixel Pitch | 0.285 (H) x 0.285 (V) | mm | - |
| Pixel Arrangement | RGB vertical stripe | - | - |
| Display Colors | 16.2M | color | - |
| Transmissive Mode | Normally White | - | - |
| Surface Treatment | Hard coating (3H) | - | - |

## 1.5 MECHANICAL SPECIFICATIONS

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Module Size | Horizontal(H) | 425.5 | 425.7 | 425.9 | mm | (1) |
| | Vertical(V) | 275.7 | 275.9 | 276.1 | mm | |
| | Depth(D) | - | 16.4 | 16.6 | mm | |
| Weight | | - | - | 2000 | g | - |

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

## 2. ABSOLUTE MAXIMUM RATINGS

### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

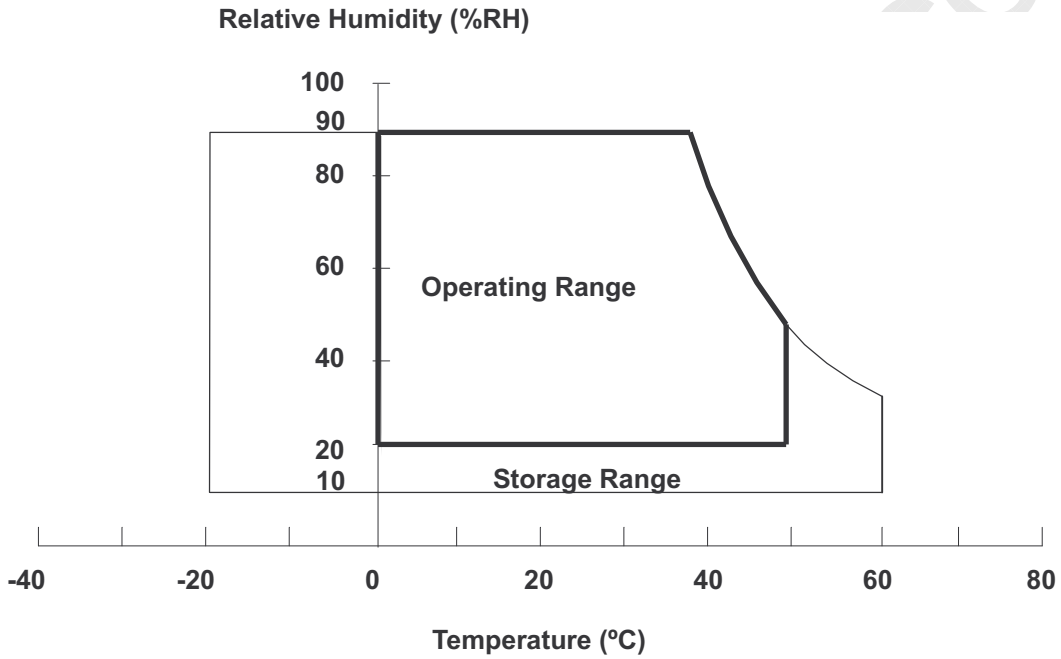
| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Storage Temperature | $T_{ST}$ | -20 | +60 | ºC | (1) |
| Operating Ambient Temperature | $T_{OP}$ | 0 | +50 | ºC | (1), (2) |
| Shock (Non-Operating) | $S_{NOP}$ | - | 50 | G | (3), (5) |
| Vibration (Non-Operating) | $V_{NOP}$ | - | 1.5 | G | (4), (5) |

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

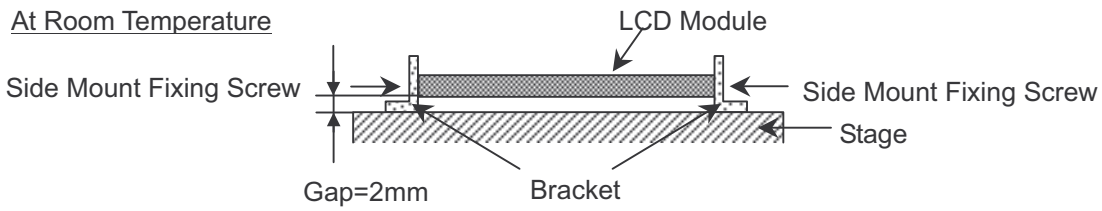



Note (2) The temperature of panel display surface area should be 0 ºC Min. and 60 ºC Max.

Note (3) 11ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 300 Hz, 10min/cycle, 3 cycles each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 ELECTRICAL ABSOLUTE RATINGS

### 2.2.1 TFT LCD MODULE

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Power Supply Voltage for LCD | Vin | 12.42 | 15.18 | V | (1) |
| Logic Input Voltage | V5A | -0.3 | 6 | V | |
| Logic Input Voltage | VDD | -0.3 | 4 | V | |

### 2.2.2 BACKLIGHT UNIT

| Item | Symbol | Value | | Unit | Note |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Lamp Voltage | $V_L$ | - | 1.71K | $V_{RMS}$ | (1), (2), $I_L$ = 7.0mA |
| Lamp Current | $I_L$ | - | 7.5 | $mA_{RMS}$ | (1), (2) |
| Lamp Frequency | $F_L$ | 46 | 52 | KHz | |

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for lamp (Refer to 3.2 for further information).

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## 3. ELECTRICAL CHARACTERISTICS

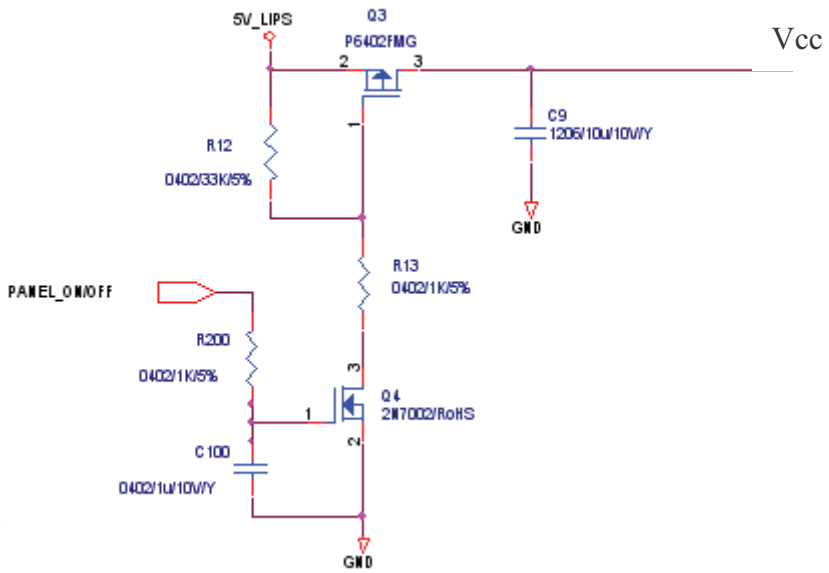
### 3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

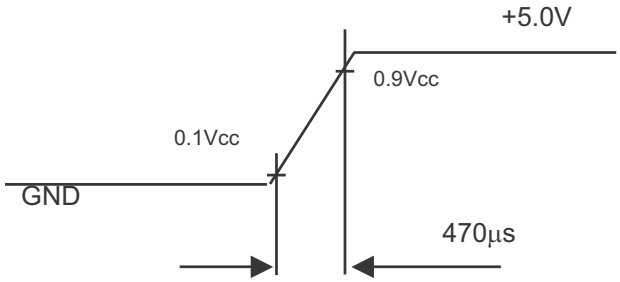
| Parameter | | SYMBOL | Value | | | UNIT | Note |
|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | |
| Logic Input Voltage | | V5A | 4.75 | 5 | 5.25 | V | |
| Logic Input Current | | I5A | | 0.64 | | A | |
| Driver Logic Input Voltage | | VDD | 3.135 | 3.3 | 3.465 | V | |
| Driver Logic Input Current | | IDD | | 60 | | mA | |
| Differential Impendence | | Zm | | 100 | | Ω | |
| Logic Input Voltage | High | VIH | 0.8VDD | - | VDD | V | |
| | Low | VIL | 0 | - | VDD | V | |
| LCD Inrush Current | | Irush | | 3 | | A | (2) |
| Power Consumption | | P | | 5 | | W | |
| PANEL On | High | PANEL_ON | 2.5 | 3.3 | | V | MAX=3.6 is ok |
| | Low | | | | 0.6 | V | |
| DCDC On | High | DCDC_ ON | 2.5 | 3.3 | | V | MAX=3.6 is ok |
| | Low | | | | 0.6 | V | |
| VCOM PWM | High | VCOM_PWM | 2.5 | | | V | MAX=5.45 is ok |
| | Low | | | | 0.6 | V | |
| VCOM PWM Frequency | | VCOM_PWM | | 27 | | KHz | Adjustable Duty Cycle |

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



**Vcc rising time is 470µs**




Note (3) The specified power supply current is under the conditions at Vcc = 5.0 V, Ta = 25 ± 2 ºC, $f_v$ = 60 Hz, whereas a power dissipation check pattern below is displayed.

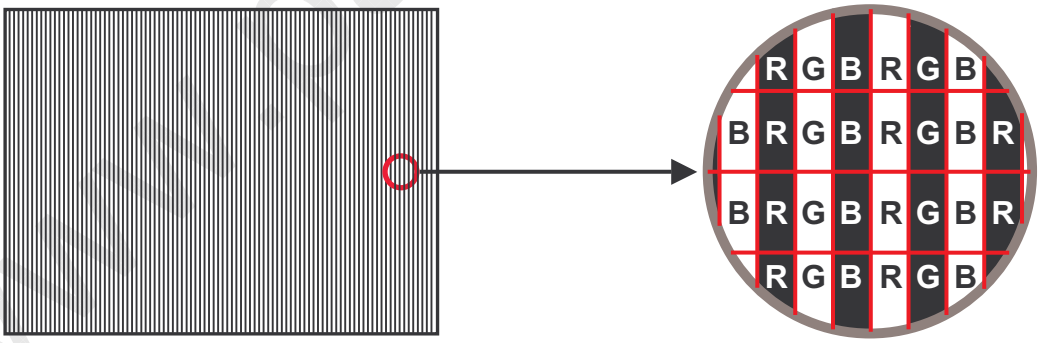
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



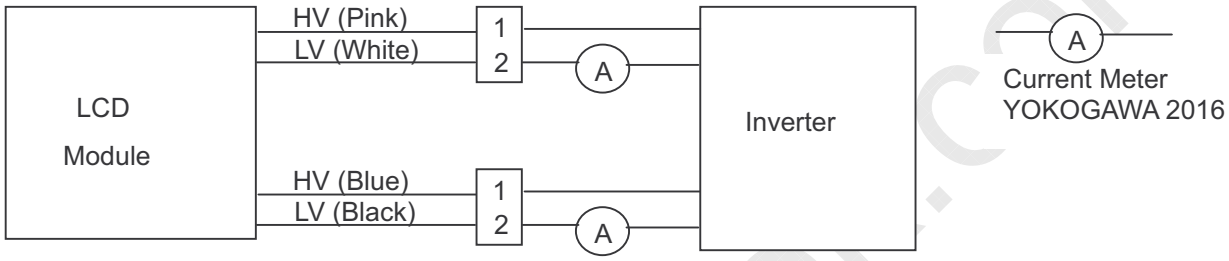

Active Area

3.2 BACKLIGHT UNIT

Ta = 25 ± 2 ºC

| Parameter | Symbol | Value | | | Unit | Note |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Lamp Input Voltage | $V_L$ | - | 780 | - | $V_{RMS}$ | $I_L$ = 7.0 mA |
| Lamp Current | $I_L$ | 6.5 | 7.0 | 7.5 | $mA_{RMS}$ | (1) |
| Lamp Turn On Voltage | $V_S$ | --- | --- | 1500(25℃) | $V_{RMS}$ | (2) |
| | | --- | --- | 1710(0℃) | $V_{RMS}$ | (2) |
| Operating Frequency | $F_L$ | 40 | 60 | 80 | KHz | (3) |
| Lamp Life Time | $L_{BL}$ | 40000 | 50000 | --- | Hrs | (5) |
| Power Consumption | $P_L$ | --- | 16.9 | --- | W | (4), $I_L$ = 7.0 mA |

Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:




Note (2) The voltage that must be larger than Vs should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency from the display, and this may cause line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) $P_L = I_L \times V_L \times$ 4 CCFLs

Note (5) The lifetime of lamp can be defined as the time in which it continues to operate under the condition **Ta = 25 ±2 °C and $I_L$ = 7.0 mA rms** until one of the following events occurs:

(a) When the brightness becomes or lower than 50% of its original value.

(b) When the effective ignition length becomes or lower than 80% of its original value. (Effective ignition length is defined as an area that has less than 70% brightness compared to the brightness in the center point.)

Note (6) The waveform of the voltage output of inverter must be area-symmetric and the design of the inverter must have specifications for the modularized lamp. The performance of the Backlight, such as lifetime or brightness, is greatly influenced by the characteristics of the DC-AC inverter for the lamp. All the parameters of an inverter should be carefully designed to avoid producing too much current leakage from high voltage output of the inverter. When designing or ordering the inverter please make sure that a poor lighting caused by the mismatch of the Backlight and the inverter (miss-lighting, flicker, etc.) never occurs. If the above situation is confirmed, the module should be operated in the same manners when it is installed in your instrument.

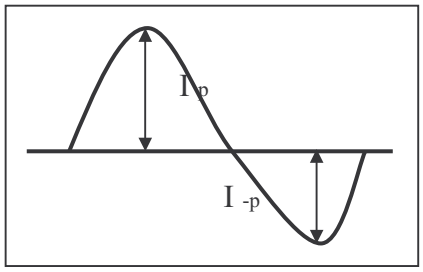
The output of the inverter must have symmetrical (negative and positive) voltage waveform and symmetrical current waveform.(Unsymmetrical ratio is less than 10%) Please do not use the inverter which has unsymmetrical voltage and unsymmetrical current and spike wave. Lamp frequency may produce interface with horizontal synchronous frequency and as a result this may cause beat on the display. Therefore lamp frequency shall be as away possible from the horizontal synchronous frequency and from its harmonics in order to prevent interference.

Requirements for a system inverter design, which is intended to have a better display performance, a better power efficiency and a more reliable lamp. It shall help increase the lamp lifetime and reduce its leakage current.

a. The asymmetry rate of the inverter waveform should be 10% below;

b. The distortion rate of the waveform should be within $\sqrt{2} \pm 10\%$;

c. The ideal sine wave form shall be symmetric in positive and negative polarities.




* Asymmetry rate:

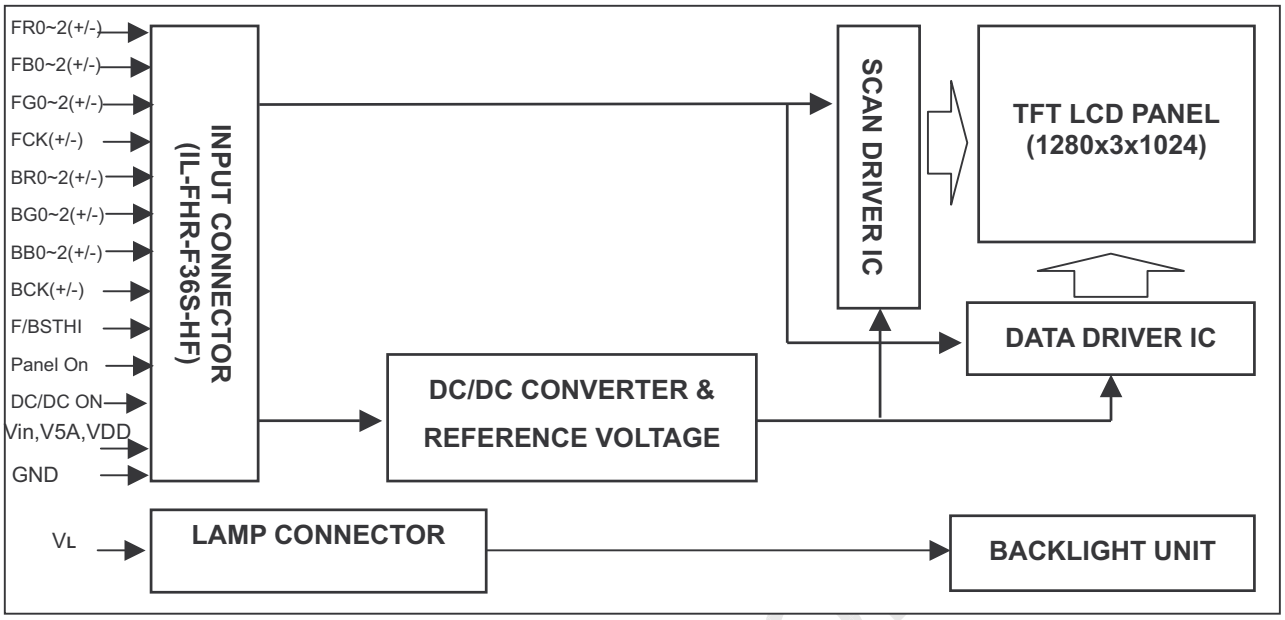
$$| I_p - I_{-p} | / I_{rms} * 100\%$$

* Distortion rate

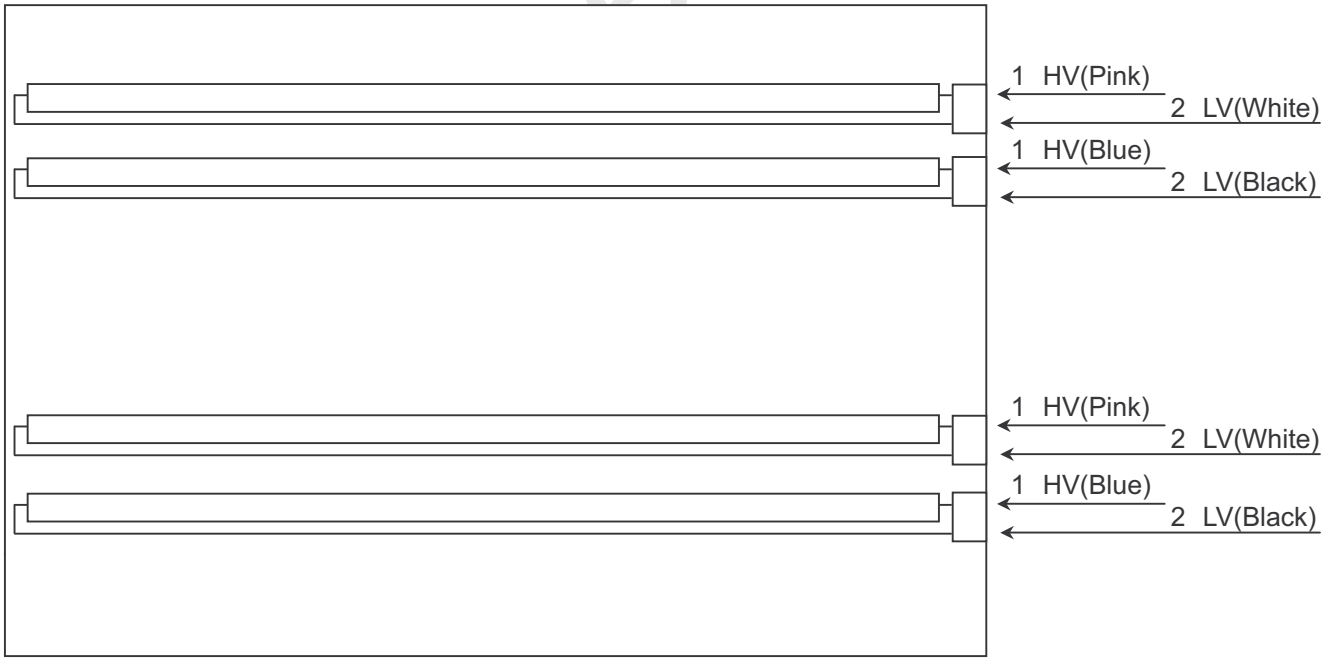
$$I_p \text{ (or } I_{-p}) / I_{rms}$$

# 4. BLOCK DIAGRAM

## 4.1 TFT LCD MODULE




## 4.2 BACKLIGHT UNIT



# 5. INPUT TERMINAL PIN ASSIGNMENT

## 5.1 TFT LCD MODULE

(1)CN1 (Panel Interface)

| Pin | Name | Description |
|---|---|---|
| 1 | Vin | Driver Power Input Voltage |
| 2 | Vin | Driver Power Input Voltage |
| 3 | V5A | Logic Input Voltage +5V |
| 4 | PANEL_ON | This pin is used to control the driver Logic Input Voltage VDD. When PANEL_ON input is “H”, VDD will be to driver. |
| 5 | DCDC_ON | This pin is used to control the PWM IC. When DCDC_ON input is “H”, it enable PWM IC. |
| 6 | VCM_PWM | This pin is used to generate common voltage for panel. Adjust pulse width could be changed common voltage. |
| 7 | GVOFF | Gate driver high voltage switch timing control. |
| 8 | NC | No connect |
| 9 | GND | Ground |
| 10 | BSTHI | Data driver start pulse input(Back) |
| 11 | GND | Ground |
| 12 | BR0N | Negative RSDS differential data input. Channel R0(Back) |
| 13 | BR0P | Positive RSDS differential data input. Channel R0(Back) |
| 14 | BR1N | Negative RSDS differential data input. Channel R1(Back) |
| 15 | BR1P | Positive RSDS differential data input. Channel R1(Back) |
| 16 | BR2N | Negative RSDS differential data input. Channel R2(Back) |
| 17 | BR2P | Positive RSDS differential data input. Channel R2(Back) |
| 18 | GND | Ground |
| 19 | BCKN | Negative RSDS differential clock input. (Back) |
| 20 | BCKP | Positive RSDS differential clock input. (Back) |
| 21 | GND | Ground |
| 22 | BG0N | Negative RSDS differential data input. Channel G0(Back) |
| 23 | BG0P | Positive RSDS differential data input. Channel G0(Back) |
| 24 | BG1N | Negative RSDS differential data input. Channel G1(Back) |
| 25 | BG1P | Positive RSDS differential data input. Channel G1(Back) |
| 26 | BG2N | Negative RSDS differential data input. Channel G2(Back) |
| 27 | BG2P | Positive RSDS differential data input. Channel G2(Back) |
| 28 | GND | Ground |
| 29 | BB0N | Negative RSDS differential data input. Channel B0(Back) |
| 30 | BB0P | Positive RSDS differential data input. Channel B0(Back) |
| 31 | BB1N | Negative RSDS differential data input. Channel B1(Back) |
| 32 | BB1P | Positive RSDS differential data input. Channel B1(Back) |
| 33 | BB2N | Negative RSDS differential data input. Channel B2(Back) |
| 34 | BB2P | Positive RSDS differential data input. Channel B2(Back) |
| 35 | GND | Ground |
| 36 | GND | Ground |

(2)CN1 (Panel Interface)

| Pin | Name | Description |
|---|---|---|
| 1 | VDD | Driver Logic Input Voltage |
| 2 | VDD | Driver Logic Input Voltage |
| 3 | XAO | When /XAO input pin is low, all the Gate driver output pins are forced to VGH level. Note that this pin has higher priority than OE. |
| 4 | STV | Gate driver start pulse is read at the rising edge of CKV and a scan signal is output from the gate driver output pin. |
| 5 | CKV | Gate driver shift clock |
| 6 | OE | This pin is used to control the Gate driver output. When OE input is “H”, gate driver output is fixed to VGL level regardless CKV. |
| 7 | GND | Ground |
| 8 | FR0N | Negative RSDS differential data input. Channel R0(Front) |
| 9 | FR0P | Positive RSDS differential data input. Channel R0(Front) |
| 10 | FR1N | Negative RSDS differential data input. Channel R1(Front) |
| 11 | FR1P | Positive RSDS differential data input. Channel R1(Front) |
| 12 | FR2N | Negative RSDS differential data input. Channel R2(Front) |
| 13 | FR2P | Positive RSDS differential data input. Channel R2(Front) |
| 14 | GND | Ground |
| 15 | POL | Data driver polarity inverting input |
| 16 | STB | The contents of the data driver register are transferred to the latch circuit at the rising edge of STB. Then the gray scale voltage is output from the device at the falling edge of STB. |
| 17 | GND | Ground |
| 18 | FCKN | Negative RSDS differential clock input. (Front) |
| 19 | FCKP | Positive RSDS differential clock input. (Front) |
| 20 | GND | Ground |
| 21 | FG0N | Negative RSDS differential data input. Channel G0(Front) |
| 22 | FG0P | Positive RSDS differential data input. Channel G0(Front) |
| 23 | FG1N | Negative RSDS differential data input. Channel G1(Front) |
| 24 | FG1P | Positive RSDS differential data input. Channel G1(Front) |
| 25 | FG2N | Negative RSDS differential data input. Channel G2(Front) |
| 26 | FG2P | Positive RSDS differential data input. Channel G2(Front) |
| 27 | GND | Ground |
| 28 | FB0N | Negative RSDS differential data input. Channel B0(Front) |
| 29 | FB0P | Positive RSDS differential data input. Channel B0(Front) |
| 30 | FB1N | Negative RSDS differential data input. Channel B1(Front) |
| 31 | FB1P | Positive RSDS differential data input. Channel B1(Front) |
| 32 | FB2N | Negative RSDS differential data input. Channel B2(Front) |
| 33 | FB2P | Positive RSDS differential data input. Channel B2(Front) |
| 34 | FSTHI | Data driver start pulse input(Front) |
| 35 | GND | Ground |
| 36 | GND | Ground |

Note (1) Connector Part No.: IL-FHR-F36S-HF.

## 5.2 BACKLIGHT UNIT

| Pin | Symbol | Description | Remark |
|---|---|---|---|
| 1 | HV | High Voltage | Pink |
| 2 | LV | Low Voltage | White |
| 1 | HV | High Voltage | Blue |
| 2 | LV | Low Voltage | Black |

Note (1) Connector Part No.: JST-BHSR-02VS-1 or equivalent

Note (2) User's connector Part No.: JST-SM02B-BHSS-1-TB (JST) or equivalent

## 5.3 COLOR DATA INPUT ASSIGNMENT

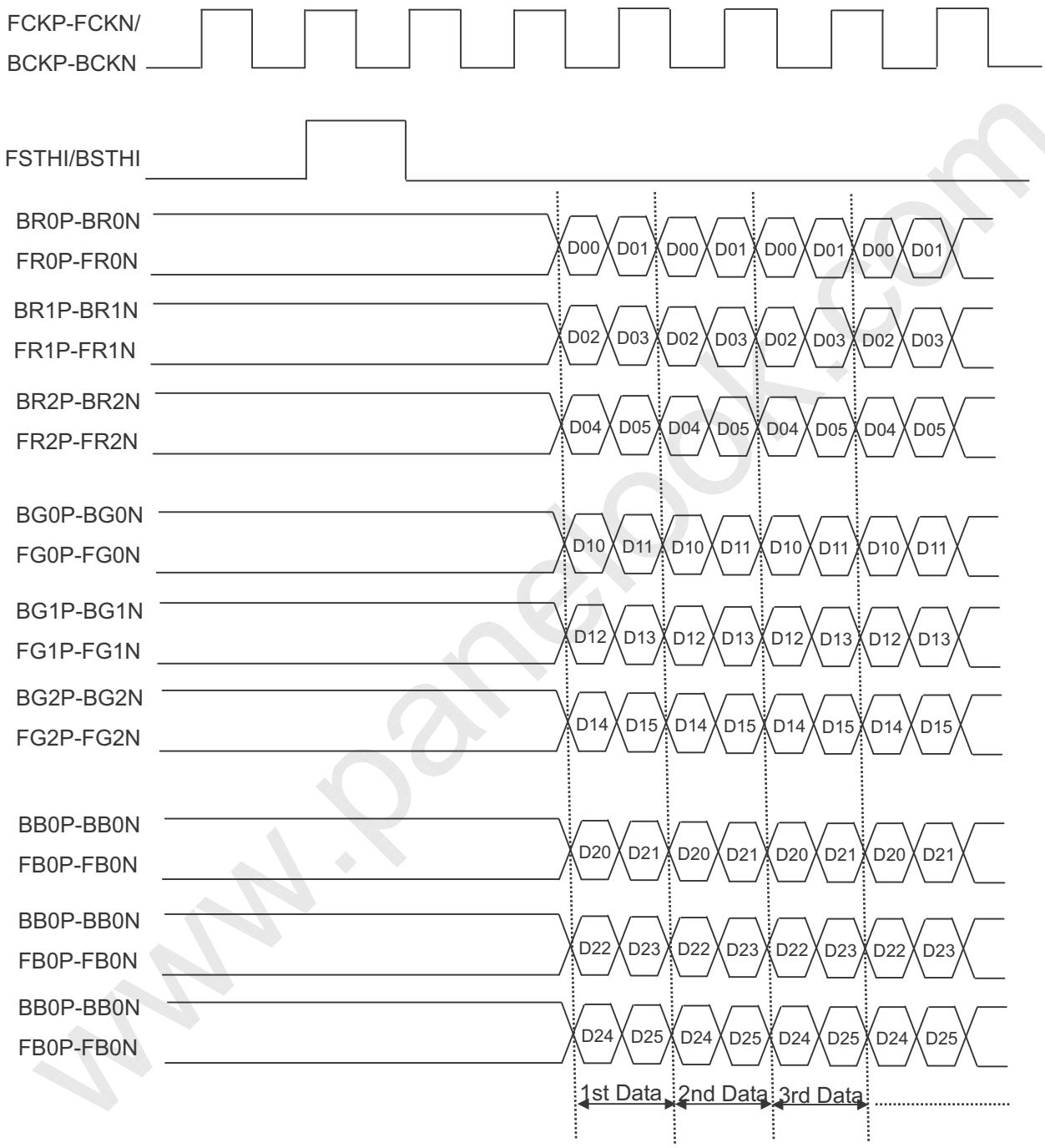
The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

| Color | | Data Signal | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Red | | | | | | | | Green | | | | | | | | Blue | | | | | | | |
| | | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | R7 | R6 | G5 | G4 | G3 | G2 | G1 | G0 | R7 | R6 | B5 | B4 | B3 | B2 | B1 | B0 |
| Basic Colors | Black | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Cyan | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Magenta | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Yellow | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | White | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Gray Scale Of Red | Red(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(2) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Red(253) | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(254) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Red(255) | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Green | Green(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Green(253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Green(255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Gray Scale Of Blue | Blue(0) / Dark | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Blue(1) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| | Blue(2) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : | : |
| | Blue(253) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| | Blue(254) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | Blue(255) | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Note (1) 0: Low Level Voltage, 1: High Level Voltage

# 6. INTERFACE TIMING

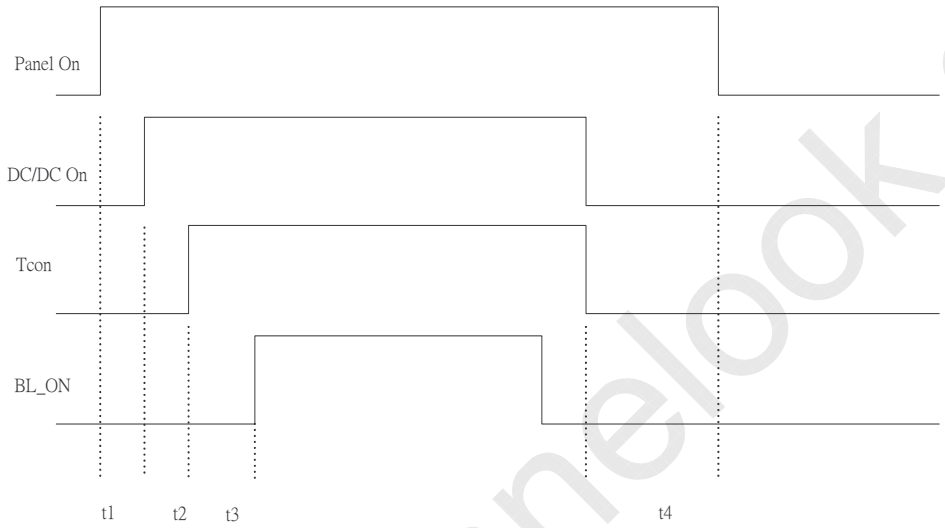
## 6.1 INPUT SIGNAL TIMING SPECIFICATIONS



## 6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.

| Parameter | Symbol | Condition | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Panel On to DC/DC On | $t_1$ | - | 10 | - | - | mS |
| DC/DC On to RSDS Data | $t_2$ | - | 40 | 50 | 60 | |
| RSDS Data to BL_On | $t_3$ | - | 100 | 200 | - | |
| RSDS Data Off to Panel Off | $t_4$ | - | 80 | 100 | 120 | |



## 7. Driver DC Characteristics

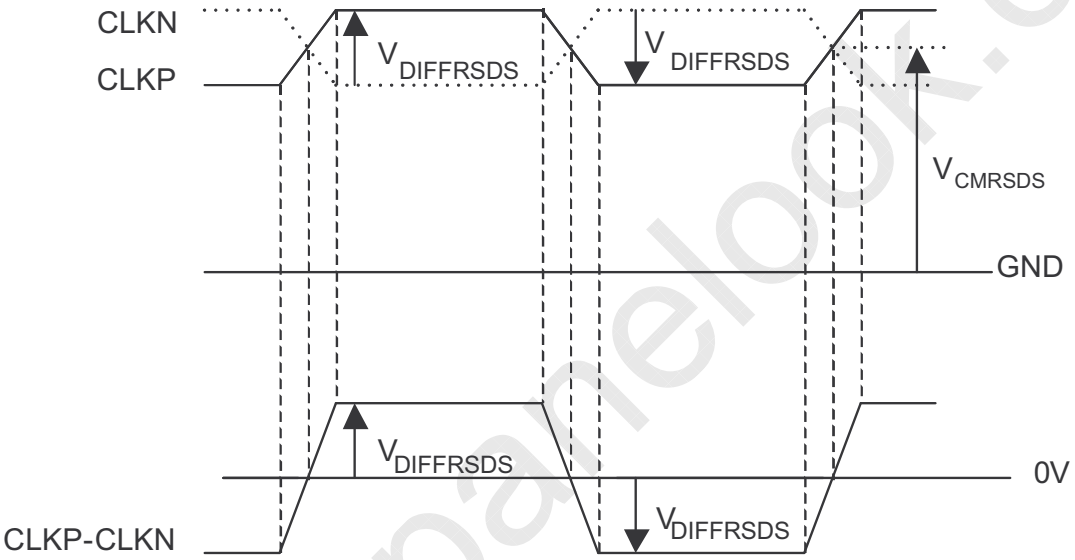
### 7.1 RSDS CHARACTERISTICS

(Ta = - 10 to +85 °C, VDD = 2.3 to 3.6 V, VDDA = 8.0 to 13.5 V, VSSD = VSSA = 0V)

| Parameter | Symbol | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| RSDS high input voltage | $V_{DIFFRSDS}$ | $V_{CMRSDS}$ = + 1.2 V (1) | 100 | 200 | - | mV |
| RSDS low input voltage | $V_{DIFFRSDS}$ | $V_{CMRSDS}$ = + 1.2 V (1) | - | -200 | - 100 | |
| RSDS common mode input voltage range | $V_{CMRSDS}$ | $V_{DIFFRSDS}$ = + 200 mV (2) | VSSD + 0.1 | - | VDDD - 1.2 | V |
| RSDS input leakage current | IDL | DxxP, DxxN, CLKP, CLKN | -10 | - | 10 | μA |

**Note:** (1) $V_{CMRSDS}$ = (VCLKP + VCLKN) / 2 or $V_{CMRSDS}$ = (VDxxP + VDxxN) / 2

(2) $V_{DIFFRSDS}$ = VCLKP - VCLKN or $V_{DIFFRSDS}$ = VDxxP – VDxxN



7.2 Electrical Characteristics (VSSD=VSSA=0V)

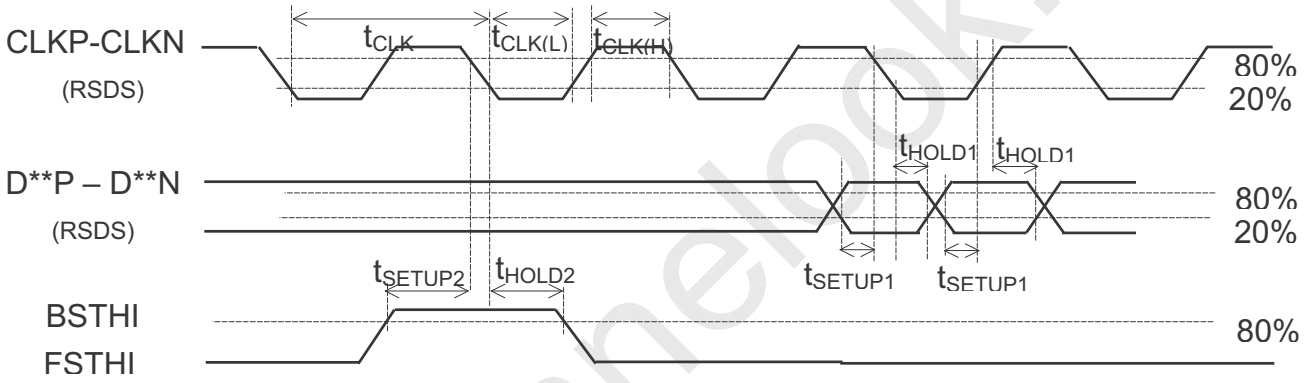
| Parameter | Symbol | Condition | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| RSDS input "Low" Voltage | $V_{DIFFRSDS}$ | DX[2:0]P,DX[2:0]N, CLKP,CLKN | - | -200 | - | mV |
| RSDS input "High" Voltage | $V_{DIFFRSDS}$ | | - | 200 | - | mV |
| RSDS reference voltage | $V_{CMRSDS}$ | | VSSD+0.1 | 1.2 | VDDD-1.2 | V |
| Input "Low" voltage | $V_{IL}$ | EIO1,EIO2,DIR,TP1, POL | 0 | - | 0.2VDDD | V |
| Input "High" voltage | $V_{IH}$ | | 0.8VDDD | - | VDDD | V |
| Input leak current | IL | | 1 | - | 1 | μA |
| Supply current (In operation mode) | $I_{CCD1}$ | VDDD=3.6V | - | 32.3 | | mA |
| Supply current (In operation mode) | $I_{CCA1}$ | VDDA=13.5V | - | 308 | | mA |
| Output current | $I_{VOH}$ | Vout=V γ 1-1V | - | - | -100 | μA |
| | $I_{VOL}$ | Vout=V γ 10+1V | - | - | 100 | μA |
| Output Voltage range | Vout | OUT1~OUT432 | VSSA+0.1 | - | VDDA-0.1 | V |
| Output Voltage deviation | Vcho-dev | VDDA=13.5V Dxx=0 to 63 Gray | - | ±5 | ±10 | mV |
| Gamma impedance | Rr | V γ 1~V γ 5,V γ 6~V γ 10 | 0.7Typ | 11270 | 1.3Typ | Ω |

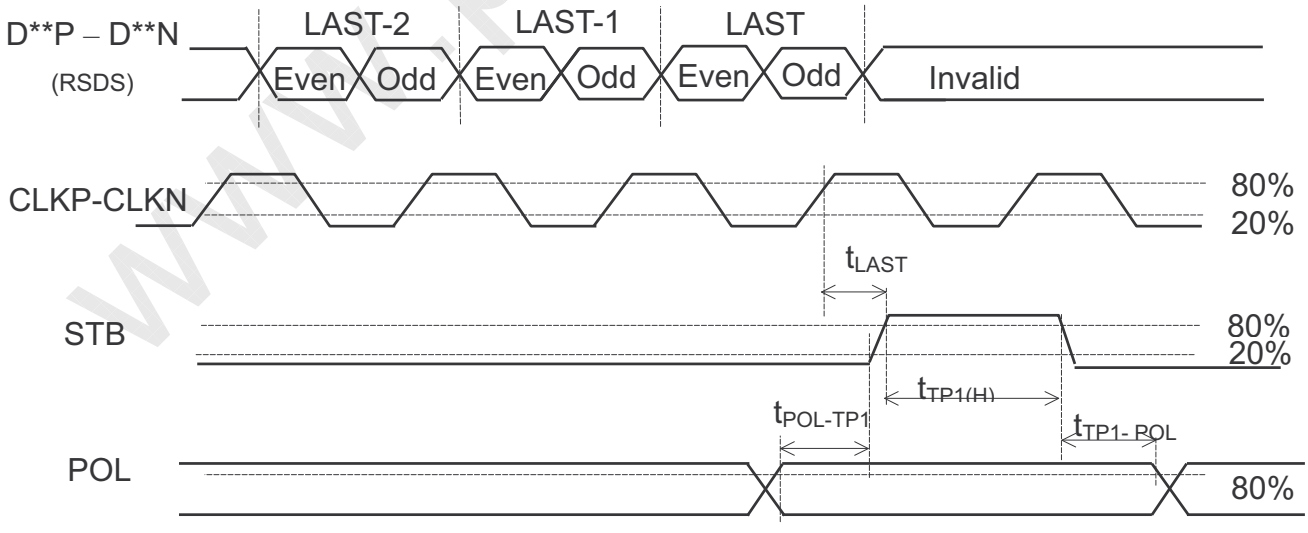
**Note:** (1) Test condition: TP1= 20μs, CLK =54MHz, data pattern =1010….checkerboard pattern, Ta=25℃

(2) No load condition

## 8.Driver AC Characteristics

| Parameter | Symbol | Condition | Spec | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Clock pulse width | $t_{CLK}$ | - | 11 | - | - | ns |
| Clock pulse low period | $t_{CLK(L)}$ | - | 5 | - | - | ns |
| Clock pulse high period | $t_{CLK(H)}$ | - | 5 | - | - | ns |
| Data setup time | $t_{SETUP1}$ | - | 2 | - | - | ns |
| Data hold time | $t_{HOLD1}$ | - | 0 | - | - | ns |
| Start pulse setup time | $t_{SETUP2}$ | - | 1 | - | - | ns |
| Start pulse hold time | $t_{HOLD2}$ | - | 2 | - | - | ns |
| TP1 high period | $t_{TP1(H)}$ | - | 1 | - | - | CLKP |
| Last data CLK to TP1 high | $t_{LAST}$ | - | 0 | - | - | CLKP |
| TP1 high to EIOn high | $t_{NEXT}$ | - | 6 | - | - | CLKP |
| POL to TP1 setup time | $t_{POL-TP1}$ | POL toggle to TP1 rising | 3 | - | - | ns |
| TP1 to POL hold time | $t_{TP1-POL}$ | TP1 falling to POL toggle | 2 | - | - | ns |



## 9.Vertical Timing

| Parameter | Symbol | Condition | Spec | | | Unit | Remark |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| CKV period | $t_{CKV}$ | - | 5 | - | - | μs | |
| CKV pulse width | $t_{CKVH}$, $t_{CKVL}$ | 50% duty cycle | 2.5 | - | - | μs | |
| OE pulse width | $t_{OE}$ | - | 1 | - | 3.5 | μs | Note2 |
| /XAO pulse width | $t_{WXAO}$ | - | 6 | - | - | μs | |
| Data setup time | $t_{SU}$ | - | 700 | - | - | ns | |
| Data hold time | $t_{HD}$ | - | 700 | - | - | ns | |
| OE to CKV time | $t_{OE-CKV}$ | | | 0.5 | | μs | |
| STB to CKV | $t_{STB-CKV}$ | | 0 | 0 | 0 | μs | |
| STB Pulse Width | $t_{STB}$ | | | 0.5 | | μs | |
| CKV to GVOFF | $t_{CKV-GVOFF}$ | | | -0.5 | | μs | |
| GVOFF Pulse width | $t_{GVOFF}$ | | | 12.8 | | μs | Note1 |

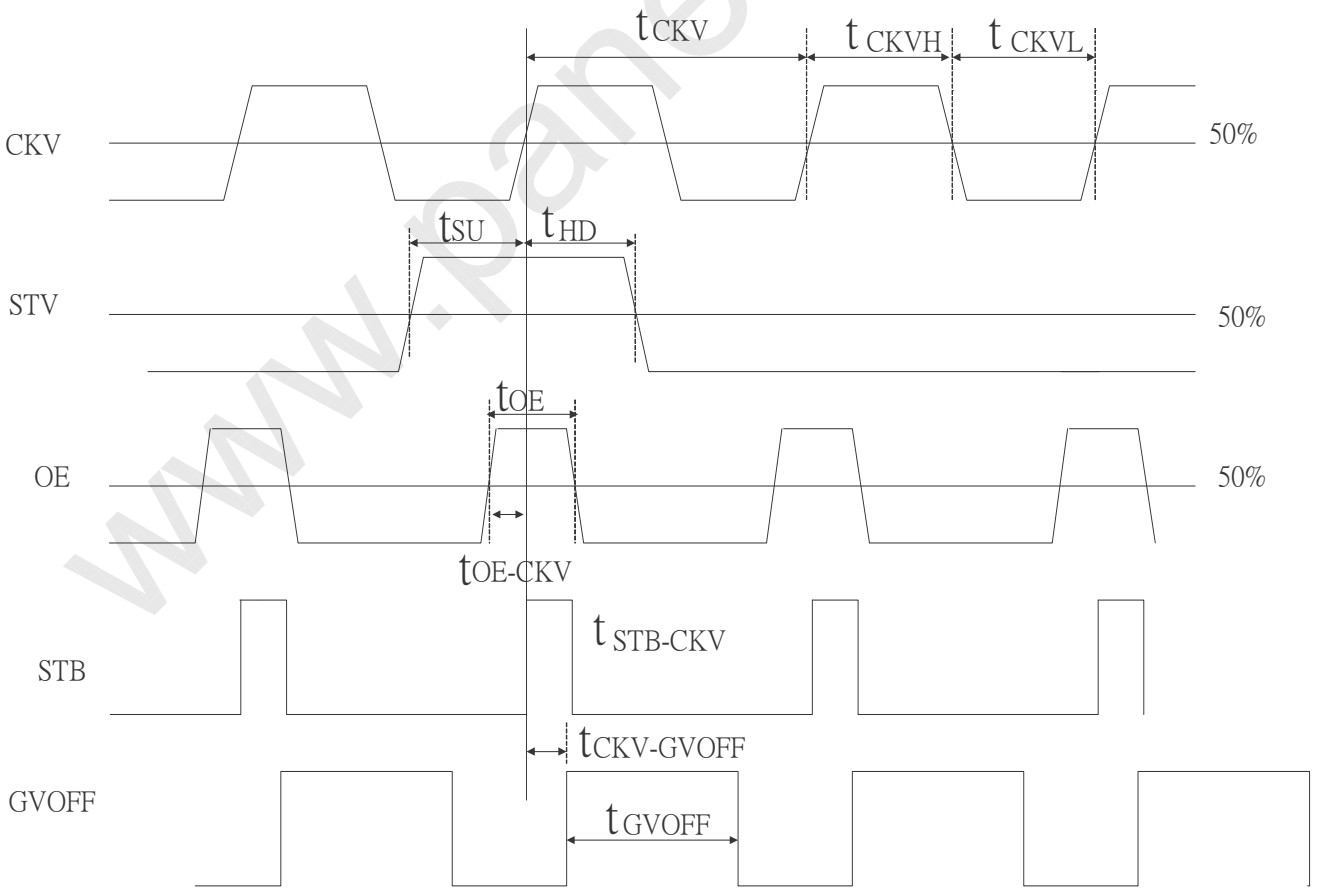
Note 1:GVOFF,OE,STB frequency same as CKV

Note 2:Width of OE pulse should be according to vertical frequency.

Ex:2.4 μs with 75Hz V-Sync ; 3.0μs with 60Hz V-Sync.

Note 3 : GVOff is used to make 3-step wave form to avoid V-Through on panel.

Note 4 : OE is used to control VGH_P output to panel. When OE is “H” , VGH_P output to panel is fixed to “L” regardless CKV.



# 10. OPTICAL CHARACTERISTICS

## 10.1 TEST CONDITIONS

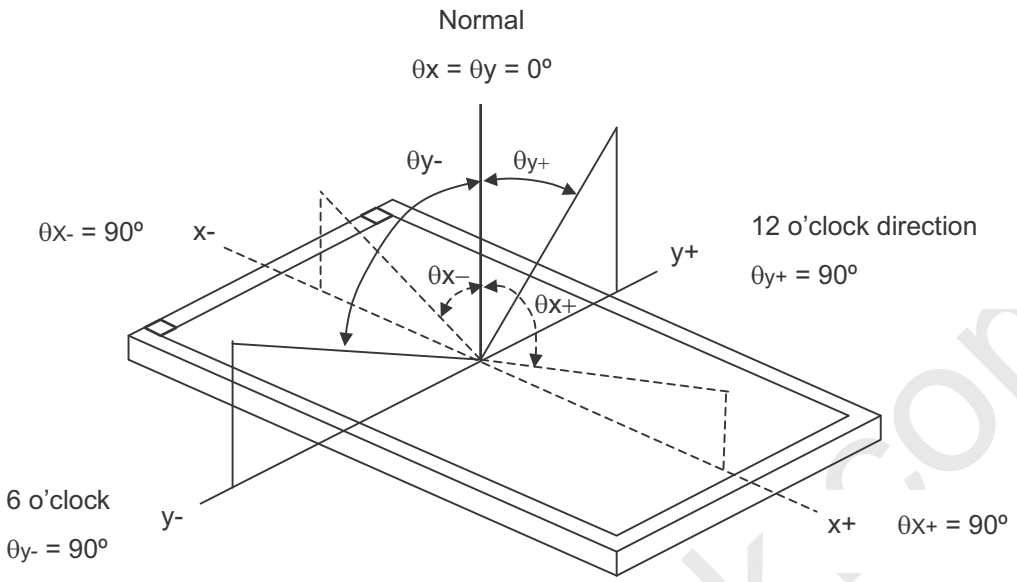
| Item | Symbol | Value | Unit |
|---|---|---|---|
| Ambient Temperature | Ta | 25±2 | °C |
| Ambient Humidity | Ha | 50±10 | %RH |
| Supply Voltage | $V_{CC}$ | 5.0 | V |
| Input Signal | According to typical value in "3. ELECTRICAL CHARACTERISTICS" | | |
| Lamp Current | $I_L$ | 7.0 | mA |
| Inverter Operating Frequency | $F_L$ | 61 | KHz |

## 10.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|---|---|
| Color Chromaticity | Red | Rx | $\theta_x$=0°, $\theta_Y$ =0° CS-1000T | Typ – 0.03 | 0.640 | Typ + 0.03 | | (1), (5) |
| | | Ry | | | 0.334 | | | |
| | Green | Gx | | | 0.286 | | | |
| | | Gy | | | 0.599 | | | |
| | Blue | Bx | | | 0.154 | | | |
| | | By | | | 0.077 | | | |
| | White | Wx | | | 0.313 | | | |
| | | Wy | | | 0.329 | | | |
| Center Luminance of White | | $L_C$ | | 230 | 300 | --- | $cd/m^2$ | (4), (5) |
| Contrast Ratio | | CR | | 500 | 700 | --- | - | (2), (5) |
| Response Time | | $T_R$ | $\theta_x$=0°, $\theta_Y$ =0° | --- | 1.5 | 6.5 | ms | (3) |
| | | $T_F$ | | --- | 3.5 | 8.5 | ms | |
| White Variation | | δW | $\theta_x$=0°, $\theta_Y$ =0° | --- | 1.3 | 1.5 | - | (5), (6) |
| Viewing Angle | Horizontal | $\theta_x$+ | CR ≧ 10 | 75 | 85 | --- | Deg. | (1), (5) |
| | | $\theta_x$- | | 75 | 85 | --- | | |
| | Vertical | $\theta_Y$+ | | 70 | 80 | --- | | |
| | | $\theta_Y$- | | 70 | 80 | --- | | |

Note (1) Definition of Viewing Angle (θx, θy):




Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

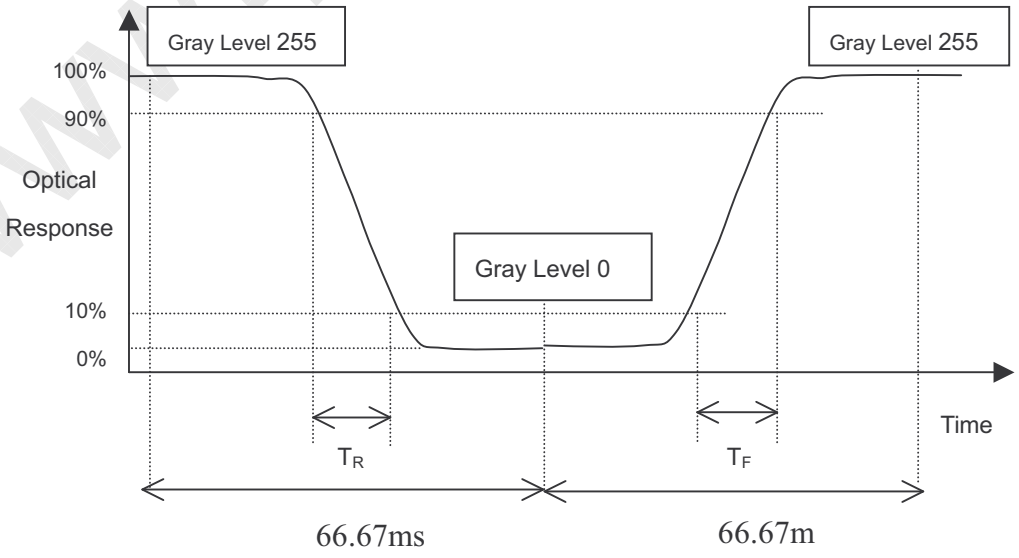
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1)

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (3) Definition of Response Time ($T_R$, $T_F$):



Note (4) Definition of Luminance of White ($L_C$):

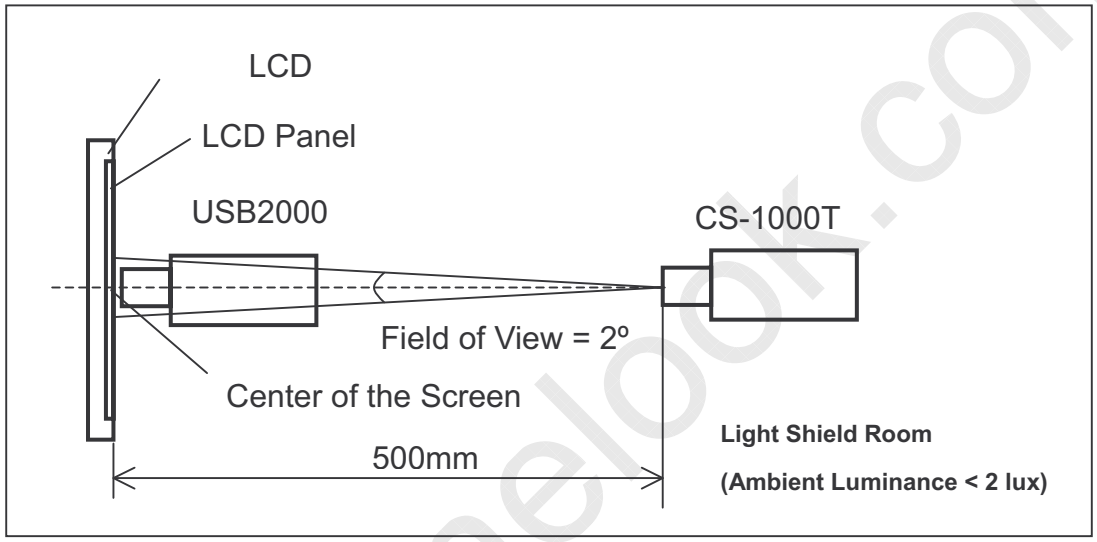
Measure the luminance of gray level 255 at center point

$L_C$ = L (1)

L (x) is corresponding to the luminance of the point X at Figure in Note (6).

Note (5) Measurement Setup:

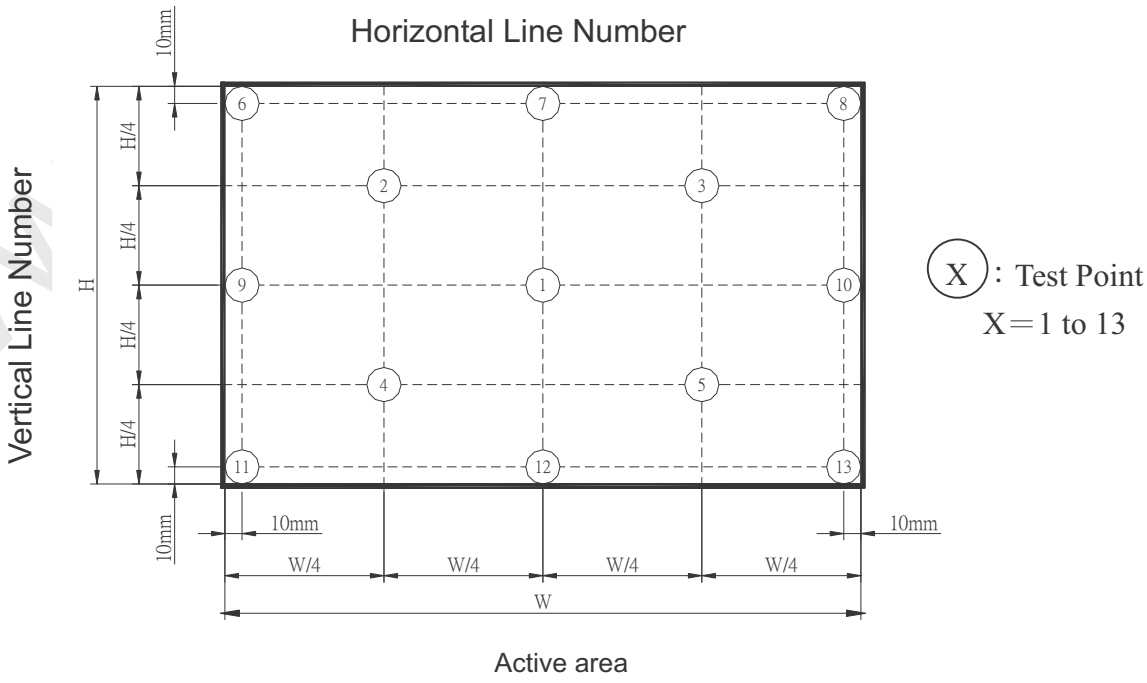
The LCD module should be stabilized at given temperature for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 15 minutes in a windless room.




Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 13 points

δW = Maximum [L (1), L (2) ……L (4), L (13)] / Minimum [L (1), L (2) …… L (4), L (13)]




Active area

# 11. PACKAGING

## 11.1 PACKING SPECIFICATIONS

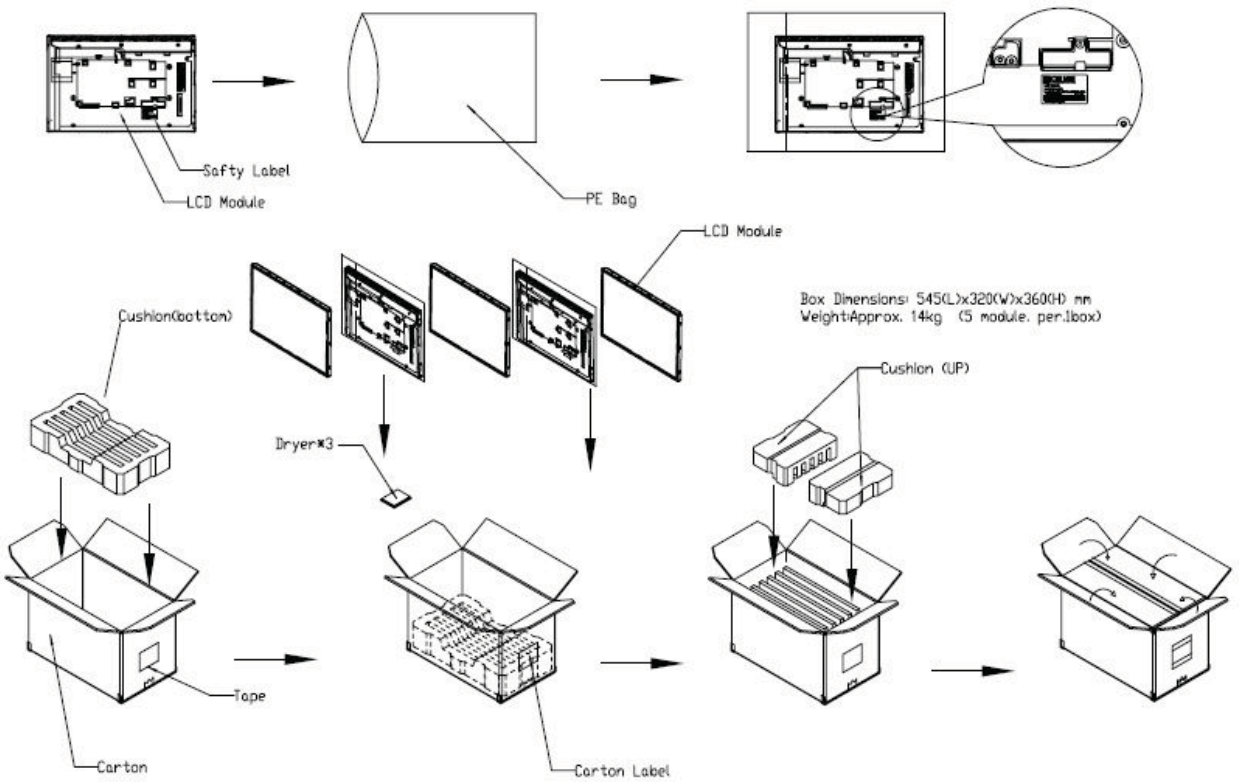
(1) 5 pcs LCD modules / 1 Box

(2) Box dimensions: 545mm(L) x 320mm (W) x 360mm (H)

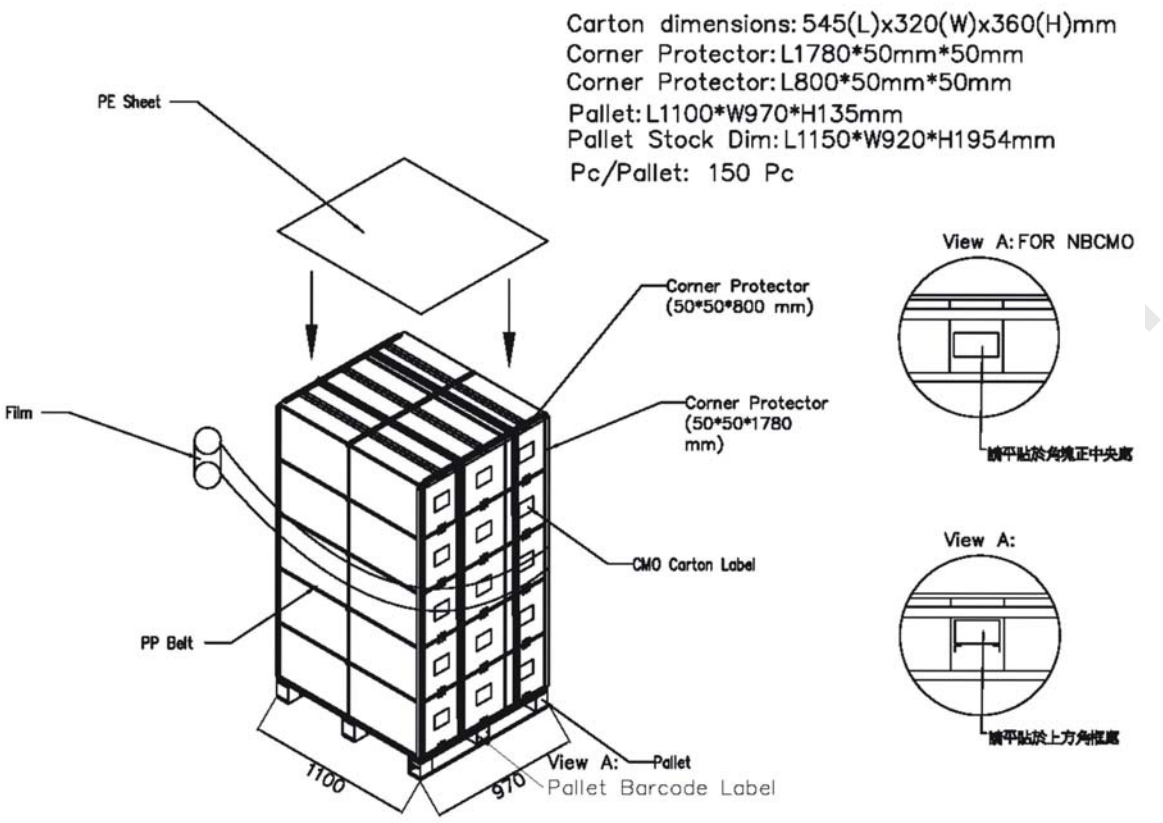
(3) Weight: approximately 13.69Kg (gloss)

## 11.2 PACKING METHOD

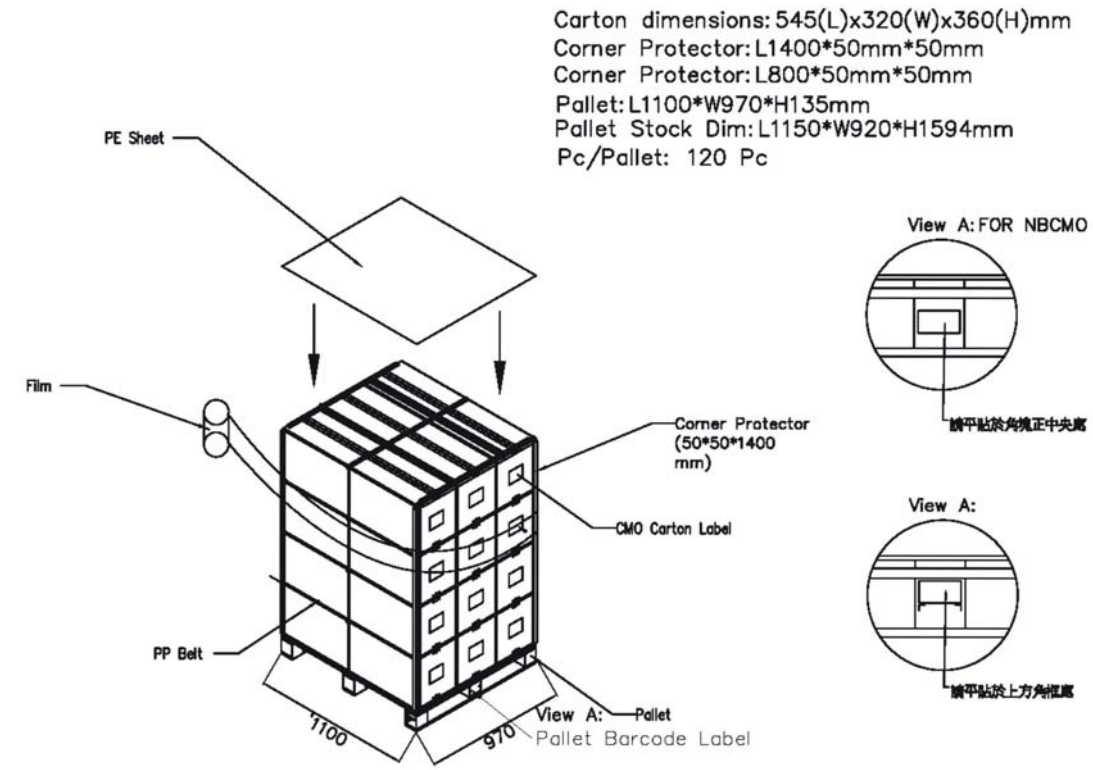
| Test Item | Test Conditions | Note |
|---|---|---|
| Vibration | ISTA STANDARD<br>Random, Frequency Range: 1 – 200 Hz<br>Top & Bottom: 30 minutes (+Z), 10 min (-Z),<br>Right & Left: 10 minutes (X)<br>Back & Forth 10 minutes (Y) | Non Operation |
| Dropping Test | 1 Angle, 3 Edge, 6 Face, 60cm | Non Operation |



## By sea




## By air

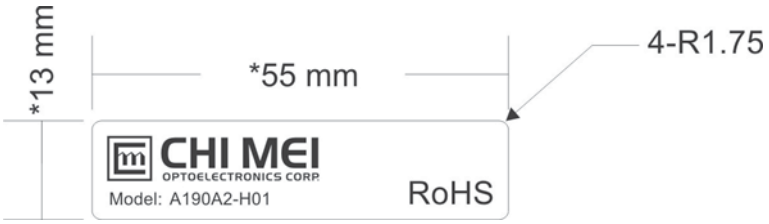


# 12. DEFINITION OF LABELS

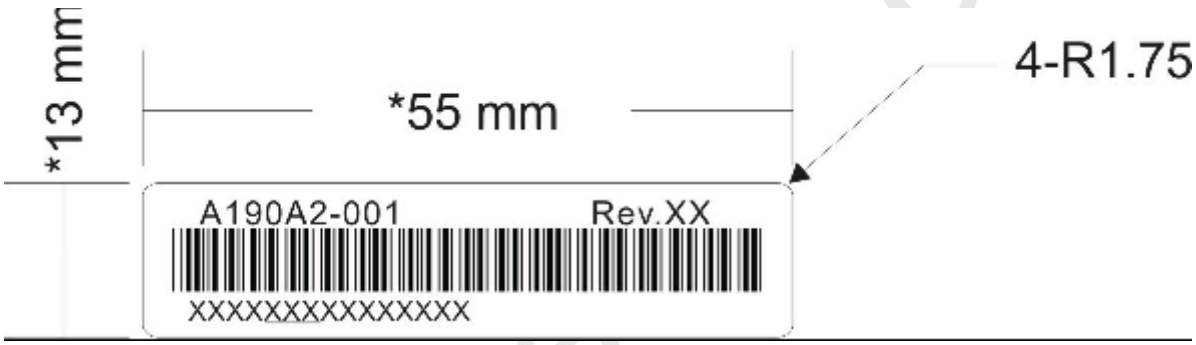
## 12.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

(a) GP label:




(b) S/N label:




1. Model Name: A190A2-001
2. Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.
3. CMO barcode definition:

   Serial ID: XX-XX-X-XX-XXX-X-XXXX

| Code | Meaning | Description |
|---|---|---|
| XX | CMO internal use | - |
| XX | Revision | Cover all the change |
| X | CMO internal use | - |
| XX | CMO internal use | - |
| XXX | Year, month, day | Year: 2001=1, 2002=2, 2003=3, 2004=4…<br>Month: 1~12=1, 2, 3, ~, 9, A, B, C<br>Day: 1~31=1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U. |
| X | Product line # | Line 1=1, Line 2=2, Line 3=3, … |
| XXXX | Serial number | Manufacturing sequence of product |

# 13. PRECAUTIONS

## 13.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) To assemble or install module into user's system can be only in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) It's not permitted to have pressure or impulse on the module because the LCD panel and Backlight will be damaged.

(4) Always follow the correct power sequence when LCD module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.

(5) Do not pull the I/F connector in or out while the module is operating.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) It is dangerous that moisture come into or contacted the LCD module, because moisture may damage LCD module when it is operating.

(9) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(10) When ambient temperature is lower than 10ºC may reduce the display quality. For example, the response time will become slowly, and the starting voltage of CCFL will be higher than room temperature.

## 13.2 SAFETY PRECAUTIONS

(1) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.