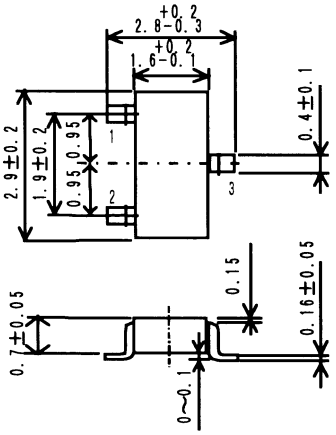
TOSHIBA Transistor Silicon PNP Epitaxial Type

# 2SA2061

High-Speed Switching Applications
DC-DC Converter Applications
Strobe Applications

- High DC current gain: $h_{FE}$ = 200 to 500 ($I_C$ = −0.5 A)
- Low collector-emitter saturation voltage: $V_{CE\ (sat)}$ = −0.19 V (max)
- High-speed switching: $t_f$ = 40 ns (typ.)

Unit: mm




| | |
|---|---|
| JEDEC | — |
| JEITA | — |
| TOSHIBA | 2-3S1C |

Weight: 0.01 g (typ.)

## Absolute Maximum Ratings (Ta = 25°C)

| Characteristics | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Collector-base voltage | | $V_{CBO}$ | −20 | V |
| Collector-emitter voltage | | $V_{CEO}$ | −20 | V |
| Emitter-base voltage | | $V_{EBO}$ | −7 | V |
| Collector current | DC | $I_C$ | −2.5 | A |
| | Pulse | $I_{CP}$ | −4 | |
| Base current | | $I_B$ | −250 | mA |
| Collector power dissipation | t = 10 s | $P_C$ (Note 1) | 1 | W |
| | DC | | 0.625 | |
| Junction temperature | | $T_j$ | 150 | °C |
| Storage temperature range | | $T_{stg}$ | −55 to 150 | °C |

Note 1: Mounted on an FR4 board (glass epoxy, 1.6 mm thick, Cu area: 645 $mm^2$)

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Electrical Characteristics (Ta = 25°C)

| Characteristics | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Collector cut-off current | | $I_{CBO}$ | $V_{CB}$ = −20 V, $I_E$ = 0 | — | — | −100 | nA |
| Emitter cut-off current | | $I_{EBO}$ | $V_{EB}$ = −7 V, $I_C$ = 0 | — | — | −100 | nA |
| Collector-emitter breakdown voltage | | $V_{(BR)\ CEO}$ | $I_C$ = −10 mA, $I_B$ = 0 | −20 | — | — | V |
| DC current gain | | $h_{FE}$ (1) | $V_{CE}$ = −2 V, $I_C$ = −0.5 A | 200 | — | 500 | |
| | | $h_{FE}$ (2) | $V_{CE}$ = −2 V, $I_C$ = −1.6 A | 100 | — | — | |
| Collector-emitter saturation voltage | | $V_{CE\ (sat)}$ | $I_C$ = −1.6 A, $I_B$ = −53 mA | — | — | −0.19 | V |
| Base-emitter saturation voltage | | $V_{BE\ (sat)}$ | $I_C$ = −1.6 A, $I_B$ = −53 mA | — | — | −1.1 | V |
| Collector output capacitance | | $C_{ob}$ | $V_{CB}$ = −10 V, $I_E$ = 0, f = 1 MHz | — | 28 | — | pF |
| Switching time | Rise time | $t_r$ | See Figure 1 circuit diagram. | — | 70 | — | ns |
| | Storage time | $t_{stg}$ | $V_{CC}$ ≈ −12 V, $R_L$ = 7.5 Ω | — | 150 | — | |
| | Fall time | $t_f$ | $I_{B1}$ = 53 mA, $I_{B2}$ = 53 mA | — | 40 | — | |

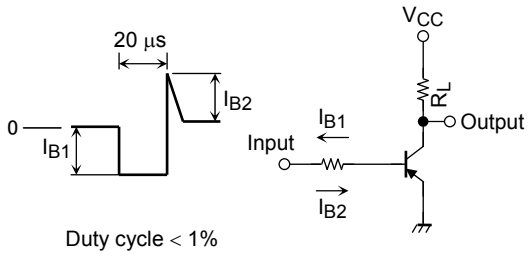
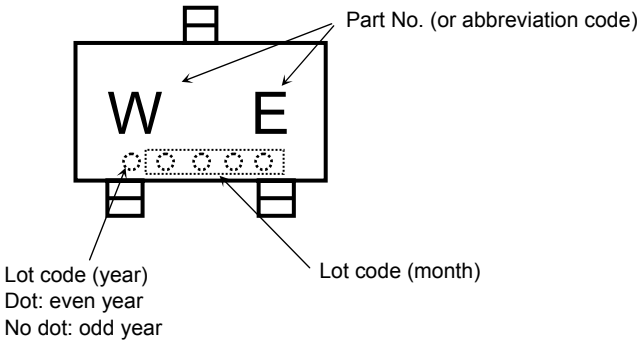
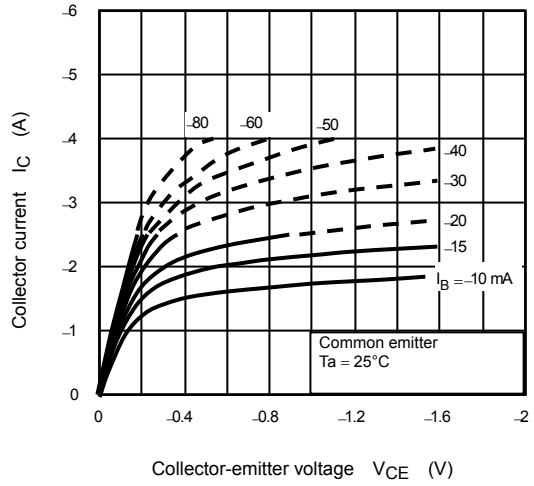



**Figure 1 Switching Time Test Circuit & Timing Chart**

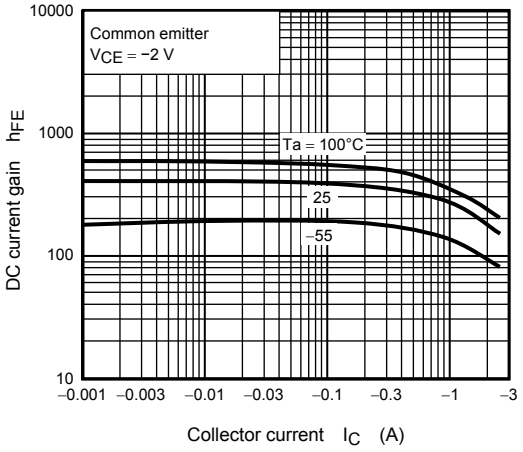
### Marking



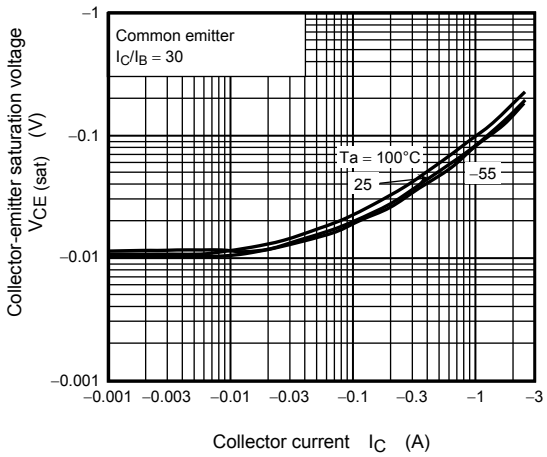
$I_C - V_{CE}$



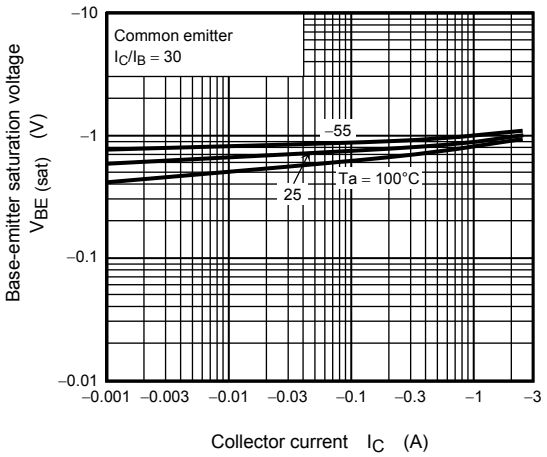

$h_{FE} - I_C$



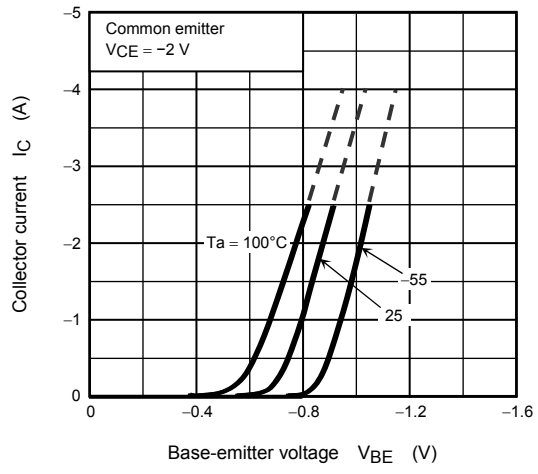

$V_{CE\ (sat)} - I_C$



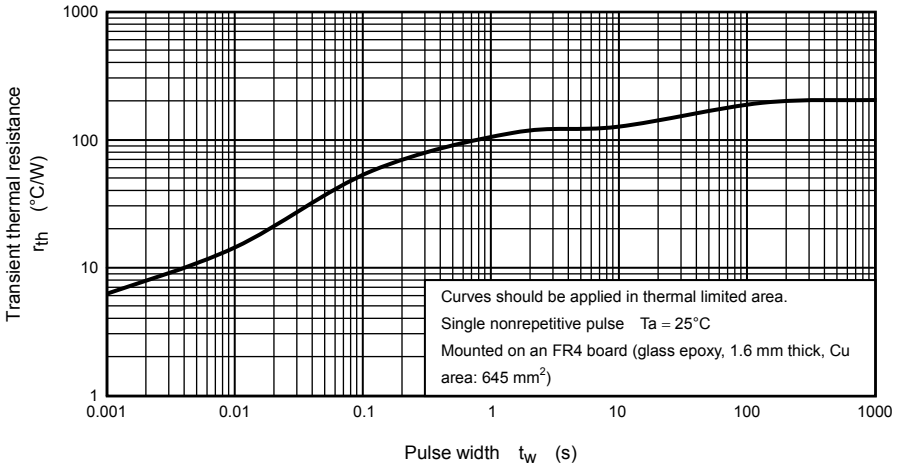

$V_{BE\ (sat)} - I_C$



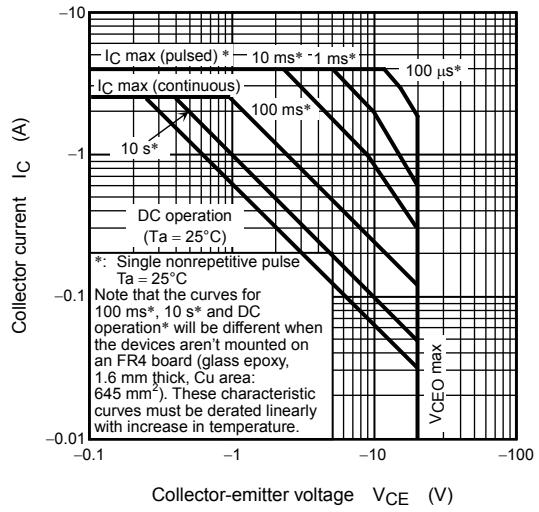

$I_C - V_{BE}$



$r_{th} - t_w$




Safe Operating Area



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