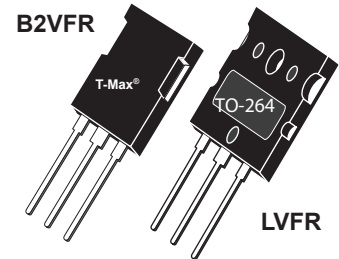
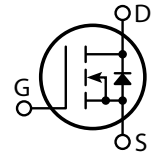


## POWER MOS V<sup>®</sup> FREDFET

Power MOS V<sup>®</sup> is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V<sup>®</sup> also achieves faster switching speeds through optimized gate layout.



- T-MAX™ or TO-264 Package
- Avalanche Energy Rated
- Faster Switching
- Lower Leakage
- **FAST RECOVERY BODY DIODE**



### MAXIMUM RATINGS

All Ratings:  $T_C = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	APT20M18B2VFR_LVFR	UNIT
$V_{DSS}$	Drain-Source Voltage	200	Volts
$I_D$	Continuous Drain Current <sup>⑥</sup> @ $T_C = 25^\circ\text{C}$	100	Amps
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	400	
$V_{GS}$	Gate-Source Voltage Continuous	$\pm 30$	Volts
$V_{GSM}$	Gate-Source Voltage Transient	$\pm 40$	
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	625	Watts
	Linear Derating Factor	5.00	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
$T_L$	Lead Temperature: 0.063" from Case for 10 Sec.	300	
$I_{AR}$	Avalanche Current <sup>①</sup> (Repetitive and Non-Repetitive)	100	Amps
$E_{AR}$	Repetitive Avalanche Energy <sup>①</sup>	50	mJ
$E_{AS}$	Single Pulse Avalanche Energy <sup>④</sup>	3000	

### STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-Source Breakdown Voltage ( $V_{GS} = 0V, I_D = 250\mu\text{A}$ )	200			Volts
$R_{DS(on)}$	Drain-Source On-State Resistance <sup>②</sup> ( $V_{GS} = 15V, I_D = 50A$ )			0.018	Ohms
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{DS} = 200V, V_{GS} = 0V$ )			250	$\mu\text{A}$
	Zero Gate Voltage Drain Current ( $V_{DS} = 160V, V_{GS} = 0V, T_C = 125^\circ\text{C}$ )			1000	
$I_{GSS}$	Gate-Source Leakage Current ( $V_{GS} = \pm 30V, V_{DS} = 0V$ )			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 2.5mA$ )	2		4	Volts

 CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

**DYNAMIC CHARACTERISTICS**

**APT20M18B2VFR\_LVFR**

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C <sub>iss</sub>	Input Capacitance	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1 MHz		9880		pF
C <sub>oss</sub>	Output Capacitance			2320		
C <sub>rss</sub>	Reverse Transfer Capacitance			700		
Q <sub>g</sub>	Total Gate Charge <sup>③</sup>	V <sub>GS</sub> = 10V V <sub>DD</sub> = 150V I <sub>D</sub> = 100A @ 25°C		330		nC
Q <sub>gs</sub>	Gate-Source Charge			55		
Q <sub>gd</sub>	Gate-Drain ("Miller") Charge			145		
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>GS</sub> = 15V V <sub>DD</sub> = 150V I <sub>D</sub> = 100A @ 25°C R <sub>G</sub> = 0.6Ω		18		ns
t <sub>r</sub>	Rise Time			27		
t <sub>d(off)</sub>	Turn-off Delay Time			55		
t <sub>f</sub>	Fall Time			6		

**SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS**

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I <sub>S</sub>	Continuous Source Current (Body Diode)			100	Amps
I <sub>SM</sub>	Pulsed Source Current <sup>①</sup> (Body Diode)			400	Amps
V <sub>SD</sub>	Diode Forward Voltage <sup>②</sup> (V <sub>GS</sub> = 0V, I <sub>S</sub> = -100A)			1.3	Volts
dv <sub>i</sub> /dt	Peak Diode Recovery <sup>⑤</sup> dv <sub>i</sub> /dt			8	V/ns
t <sub>rr</sub>	Reverse Recovery Time (I <sub>S</sub> = -100A, di <sub>i</sub> /dt = 100A/μs)	T <sub>j</sub> = 25°C		230	ns
		T <sub>j</sub> = 125°C		450	
Q <sub>rr</sub>	Reverse Recovery Charge (I <sub>S</sub> = -100A, di <sub>i</sub> /dt ≤ 100A/μs)	T <sub>j</sub> = 25°C	0.9		μC
		T <sub>j</sub> = 125°C	3.4		
I <sub>R</sub>	Peak Recovery Current (I <sub>S</sub> = -100A, di <sub>i</sub> /dt = 100A/μs)	T <sub>j</sub> = 25°C	11		Amps
		T <sub>j</sub> = 125°C	20		

**THERMAL CHARACTERISTICS**

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction to Case			0.20	°C/W
R <sub>θJA</sub>	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting T<sub>j</sub> = +25°C, L = 600μH, R<sub>G</sub> = 25Ω, Peak I<sub>L</sub> = 100A

⑤ dv<sub>i</sub>/dt numbers reflect the limitations of the test circuit rather than the device itself. I<sub>S</sub> ≤ -I<sub>D</sub>100A di<sub>i</sub>/dt ≤ 200A/μs V<sub>R</sub> ≤ 200V T<sub>j</sub> ≤ 150°C

⑥ The maximum current is limited by lead temperature.

Microsemi reserves the right to change, without notice, the specifications and information contained herein.

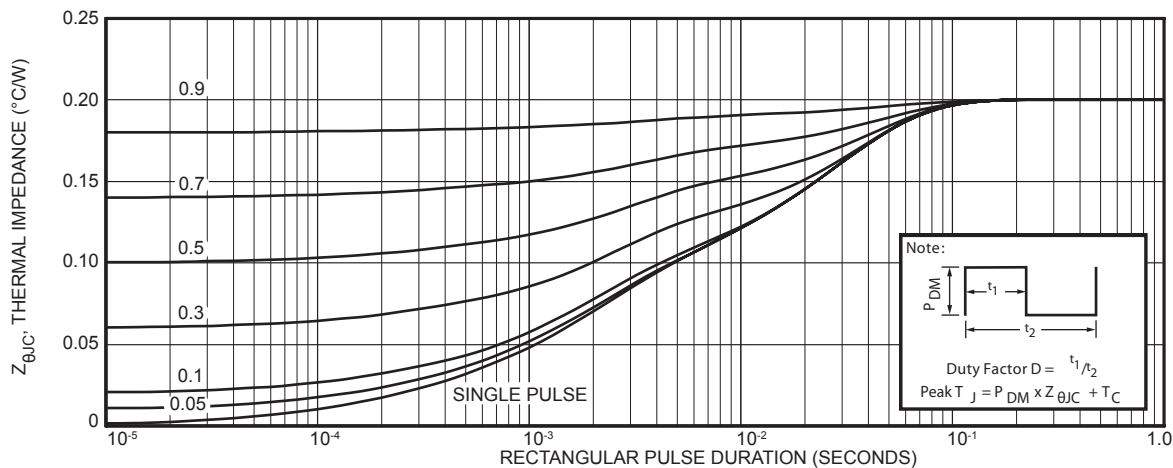


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

# Typical Performance Curves

APT20M18B2VFR\_LVFR

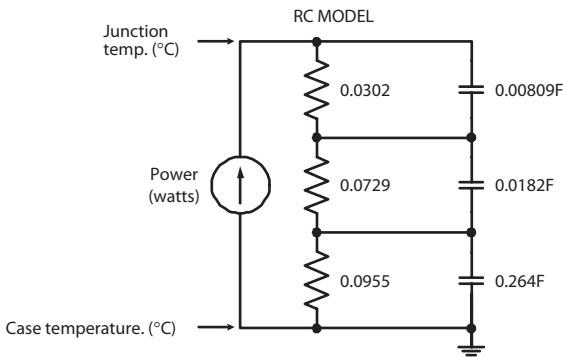


FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL

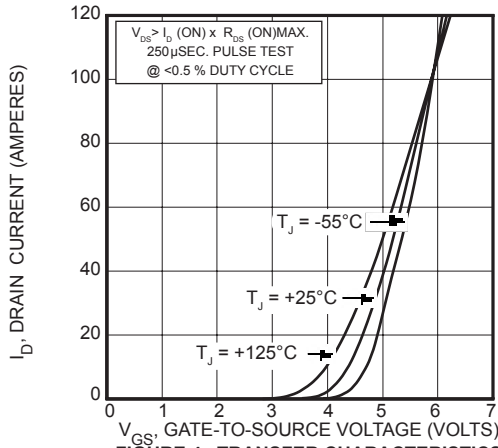


FIGURE 4, TRANSFER CHARACTERISTICS

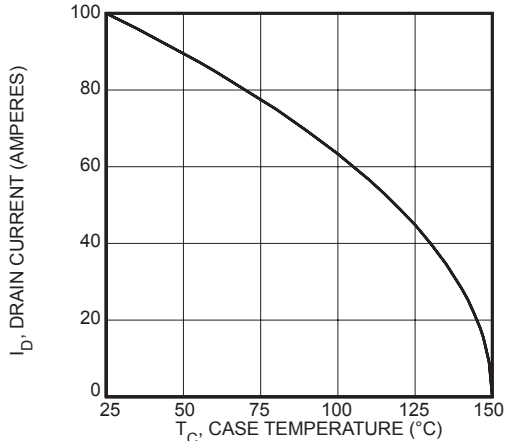


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

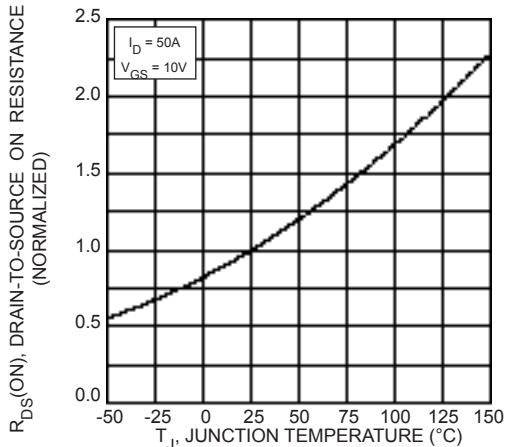


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

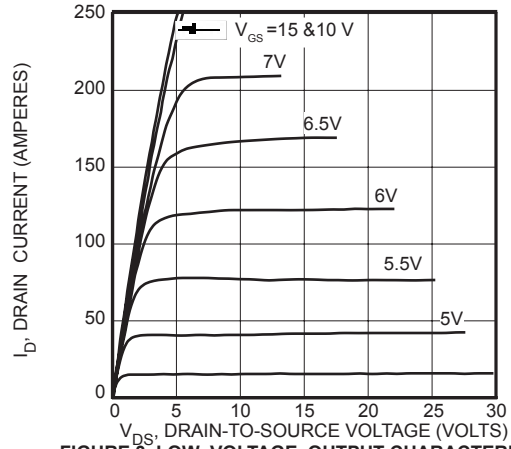


FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS

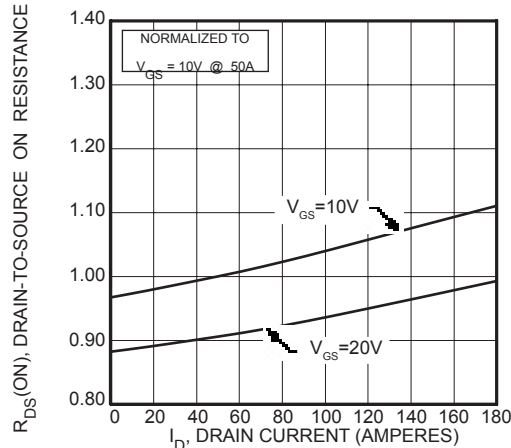


FIGURE 5,  $R_{DS(\text{ON})}$  vs DRAIN CURRENT

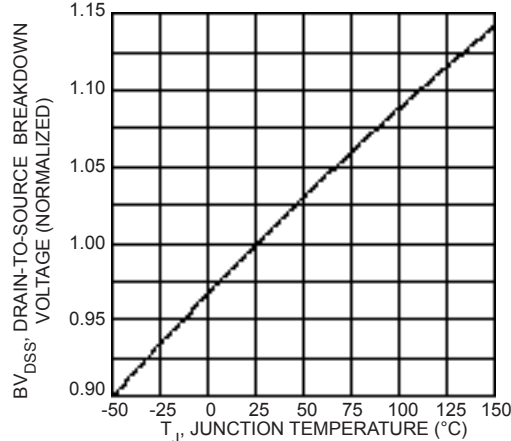


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

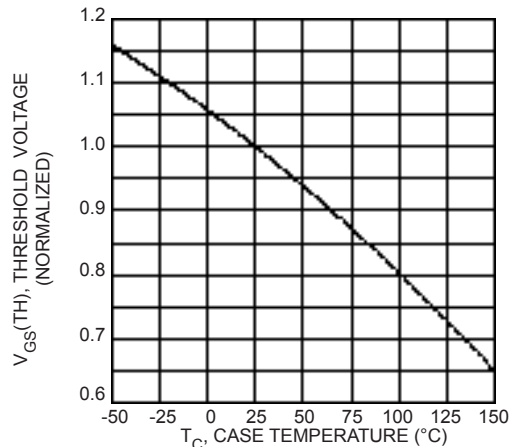


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

# Typical Performance Curves

APT20M18B2VFR\_LVFR

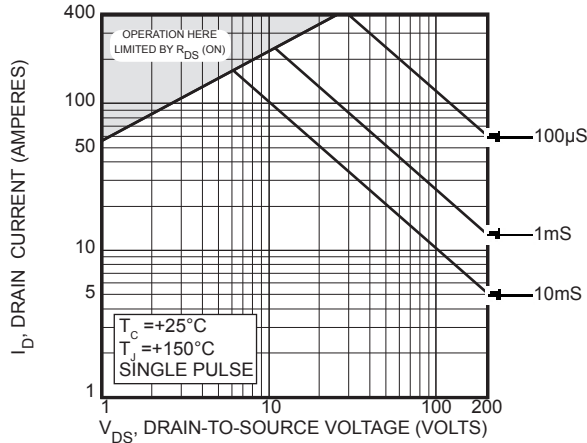


FIGURE 10, MAXIMUM SAFE OPERATING AREA

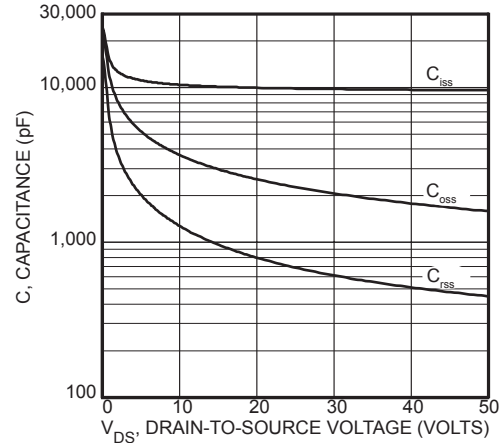


FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

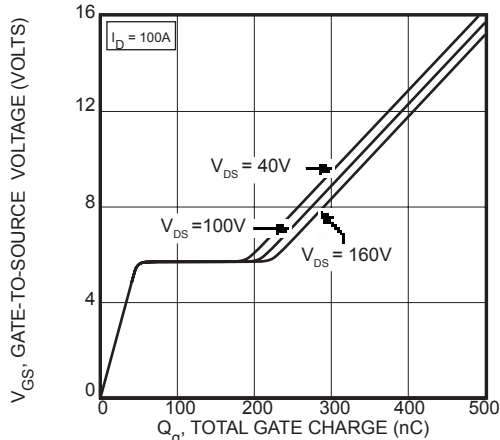


FIGURE 12, GATE CHARGE vs GATE-TO-SOURCE VOLTAGE

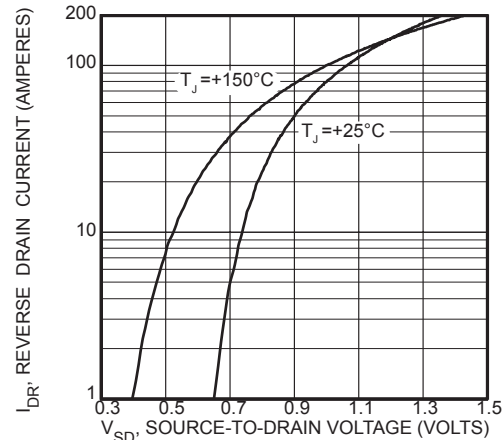
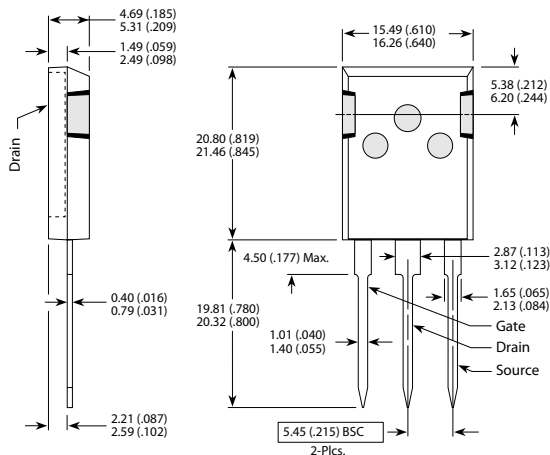
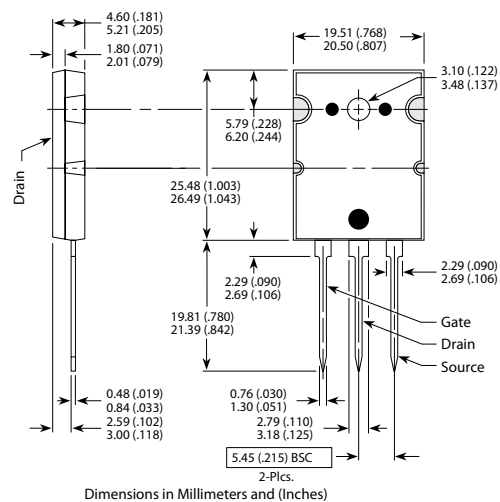


FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

## T-MAX™ (B2) Package Outline (B2VFR)



## TO-264 (L) Package Outline (LVFR)



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