DESCRIPTION

The A2232 is a stereo audio power amplifier that drives 3W/channel of continuous RMS power into a 3Ω load. Advanced DC volume control minimizes external components and allows BTL (speaker) volume control and SE (headphone) volume control. Notebook and pocket PCs benefit from the integrated feature set that minimizes external components without sacrificing functionality.

To simplify design, the speaker volume level is adjusted by applying a DC voltage to the VOLUME terminal. Likewise, the delta between speaker volume and headphone volume can be adjusted by applying a DC voltage to the SEDIFF terminal. To avoid an unexpected high volume level through the headphones, a third terminal, SEMAX, limits the headphone volume level when a DC voltage is applied. Finally, to ensure a smooth transition between active and shutdown modes, a fade mode ramps the volume up and down.

The A2232 is available in P-TSSOP24 package.

ORDERING INFORMATION

Package Type	Part Number	
P-TSSOP24	TMXP24	A2232TMXP24R
		A2232TMXP24VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products Suffix " V " means Halogen free Package		

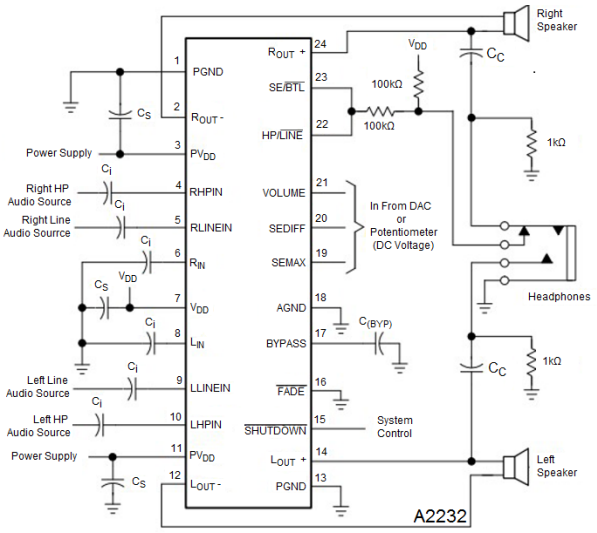
FEATURES

- Advanced DC Volume Control With 2-dB Steps, From -40 dB to 20 dB
  - -Fade Mode
  - -Maximum Volume Setting for SE Mode
  - -Adjustable SE Volume Control
- Referenced to BTL Volume Control
- 3 W Into 3Ω Speakers
- Stereo Input MUX
- Differential Inputs
- Available in P-TSSOP24 Package

APPLICATION

- Notebook PC
- LCD Monitors
- Pocket PC

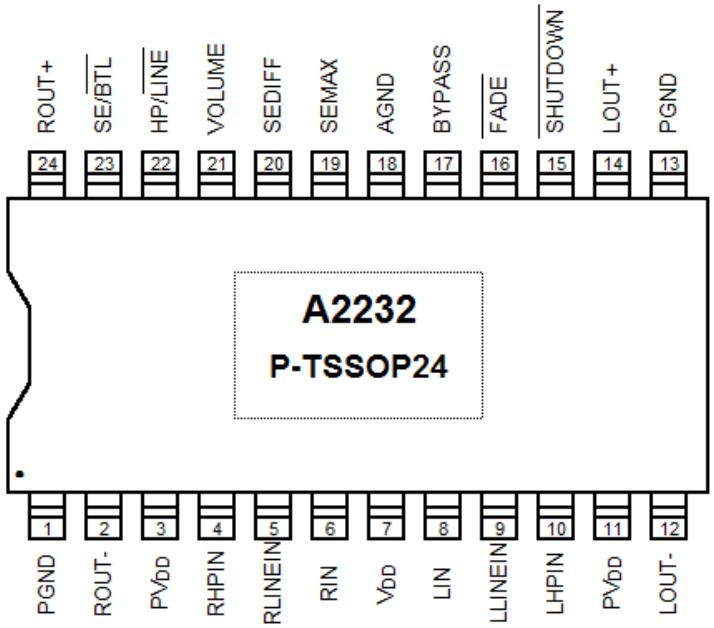
TYPICAL APPLICATION



Typical A2232 application Circuit Using

Single-Ended Inputs And Input MUX

PIN DESCRIPTION



Top View

Pin #	Symbol	I/O	Functions
1,13	PGND	-	Power ground
2	R_{OUT-}	O	Right channel negative audio output
3,11	PV_{DD}	-	Supply voltage terminal for power stage
4	RHPIN	I	Right channel headphone input, selected when HP/$\overline{LINE}$ is held high
5	RLINEIN	I	Right channel line input, selected when HP/$\overline{LINE}$ is held low
6	RIN	I	Common right channel input for fully differential input. AC ground for single-ended inputs.
7	V_{DD}	-	Supply voltage terminal
8	LIN	I	Common left channel input for fully differential input. AC ground for single-ended inputs.
9	LLINEIN	I	Left channel line input, selected when HP/$\overline{LINE}$ is held low
10	LHPIN	I	Left channel headphone input, selected when HP/$\overline{LINE}$ is held light
12	L_{OUT-}	O	Left channel negative audio output

Pin #	Symbol	I/O	Functions
14	L_{OUT}+	O	Left channel positive audio output
15	$\overline{SHUTDOWN}$	I	Places the amplifier in shutdown mode if a TTL logic low is placed on this terminal
16	$\overline{FADE}$	I	Places the amplifier in fade mode if a logic low is placed on this terminal; normal operation if a logic placed on this terminal
17	BYPASS	I	Tap to voltage divider for internal midsupply bias generator used for analog reference
18	AGND	-	Analog power supply ground
19	SEMAX	I	Sets the maximum volume for single ended operation. DC voltage range is 0 to V_{DD}
20	SEDIFF	I	Sets the difference between BTL volume and SE volume. DC voltage range is 0 to V_{DD}
21	VOLUME	I	Terminal for dc volume control. DC voltage range is 0 to V_{DD}
22	HP/$\overline{LINE}$	I	Input MUX control. When logic high, RHPIN and LHPIN inputs are selected. When logic low, RLINEIN and LLINEIN inputs are selected
23	SE/$\overline{BTL}$	I	Output MUX control. When this terminal is high, SE outputs are selected. When this terminal is low, BTL outputs are selected
24	R_{OUT}+	O	Right channel positive audio output.

ABSOLUTE MAXIMUM RATINGS

V_{DD}, Supply Voltage	-0.3V ~ 6.0V
V_{IN}, Input Voltage	-0.3V ~ V_{DD}+0.3V
T_A, Operating Temperature	-40℃ ~ 85℃
Junction Temperature	-45℃ ~ 150℃
T_{STG}, Storage Temperature	-65℃ ~ 150℃
ESD Susceptibility	2000V

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, Unless otherwise specified. Limits apply for T_A = 25°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Offset Voltage	$\|V_{OO}\|$	V_{DD}=5.5V, Gain=0dB, SE/$\overline{BTL}$=0V	-	-	30	mV
		V_{DD}=5.5V, Gain=20dB, SE /$\overline{BTL}$=0V			50	
Power Supply Rejection Ratio	PSRR	V_{DD}=PV_{DD} = 4.0V to 5.5V	-42	-70	-	dB
High-level input current	$\|I_{IH}\|$	V_{DD} = PV_{DD} = 5.5V, V_I = V_{DD} = PV_{DD}	-	-	1	µA
Low-level input current	$\|I_{IL}\|$	V_{DD} = PV_{DD} = 5.5V, V_I = 0V	-	-	1	µA
Shutdown Current	$I_{(SD)}$	$\overline{SHUTDOWN}$ = 0V	-	1	20	µA
Supply current, no load	I_{DD}	V_{DD}=PV_{DD}=5.5V, SE/$\overline{BTL}$= 0V, $\overline{SHUTDOWN}$ = 2V	6.0	7.5	9.0	mA
		V_{DD}=PV_{DD}=5.5V, SE/$\overline{BTL}$=5.5V, $\overline{SHUTDOWN}$ =2V	3.0	5	6	
Supply current, max power into a 3Ω load	I_{DD}	V_{DD}=PV_{DD}=5.5V,SE/$\overline{BTL}$=0V, $V_{\overline{SHUTDOWN}}$ =2V,R_L=3Ω	-	1.5	-	A_{RMS}

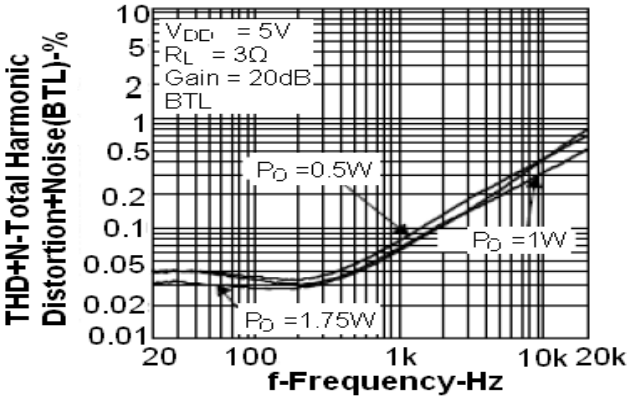
OPERATING RECOMMENDATION

V_{DD} = 5V, GAIN = 2V/V, R_L = 8Ω. Unless otherwise specified. Limits apply for T_A = 25°C

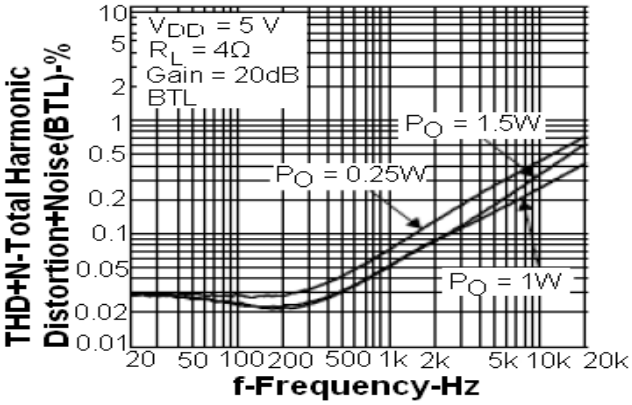
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Power	P_O	THD = 1%, f = 1kHz	-	2	-	W
		THD = 10%, f = 1kHz, V_{DD} = 5.5 V		3		
Total Harmonic Distortion + Noise	THD+N	P_O = 1W, R_L = 8Ω , f = 20 Hz to 20 kHz	-	< 0.4%	-	-
High-level output voltage	V_{OH}	R_L = 8 Ω, Measured between output and V_{DD}	-	-	700	mV
Low-level output voltage	V_{OL}	R_L = 8 Ω, Measured between output and GND	-	-	400	mV

TYPICAL PERFORMANCE CHARACTERISTICS

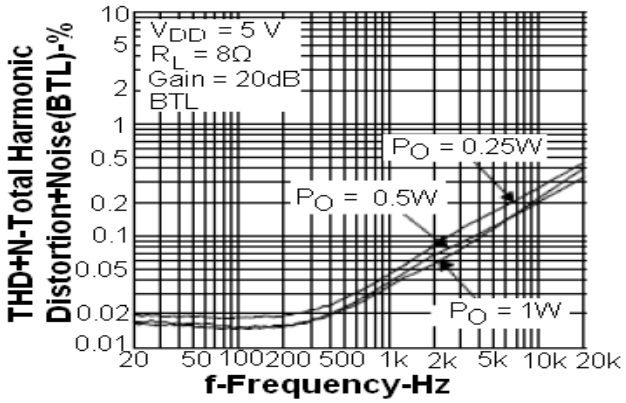
1. Total Harmonic Distortion + Noise(BTL) VS Frequency



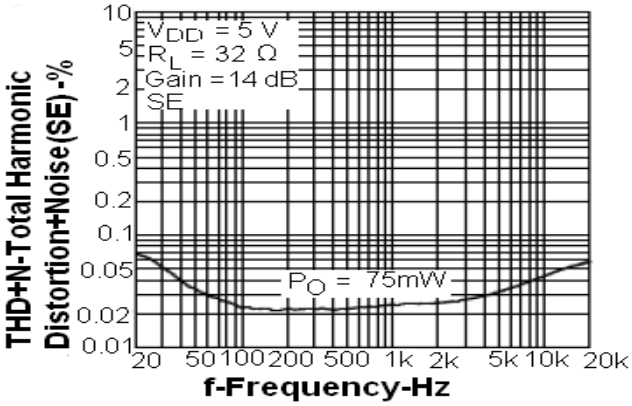
2. Total Harmonic Distortion + Noise(BTL) VS Frequency



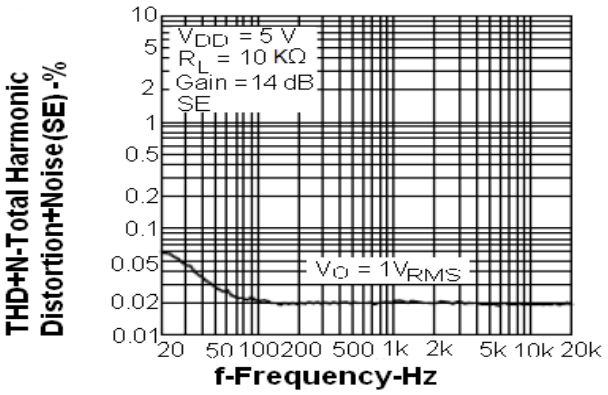
3. Total Harmonic Distortion + Noise(BTL) VS Frequency



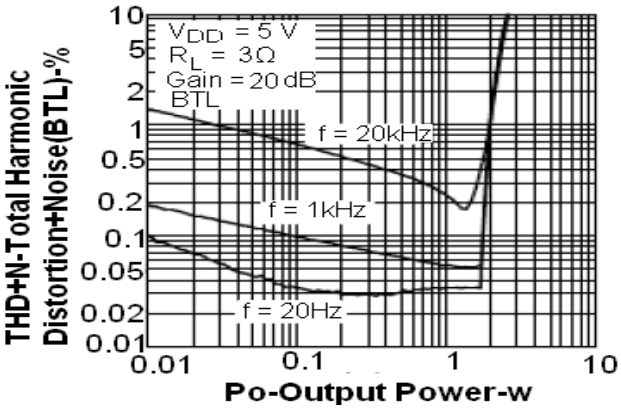
4. Total Harmonic Distortion + Noise(SE) VS Frequency



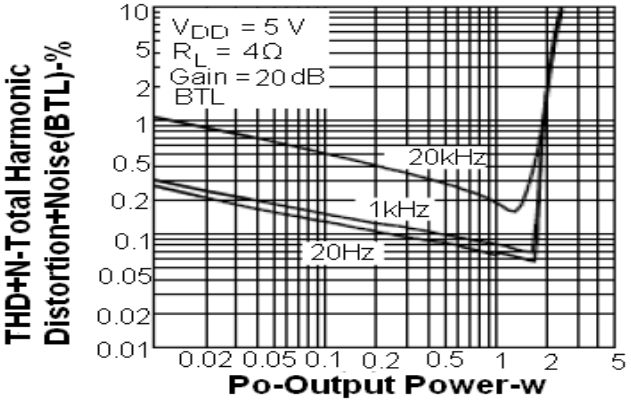
5. Total Harmonic Distortion + Noise(SE) VS Frequency



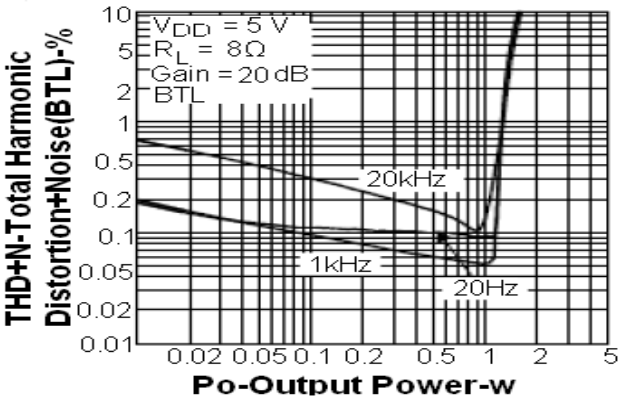
6. Total Harmonic Distortion + Noise(BTL) VS Output Power



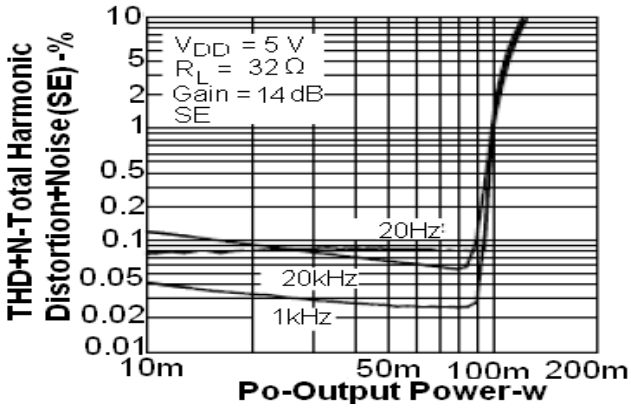
7. Total Harmonic Distortion + Noise(BTL) VS Output Power



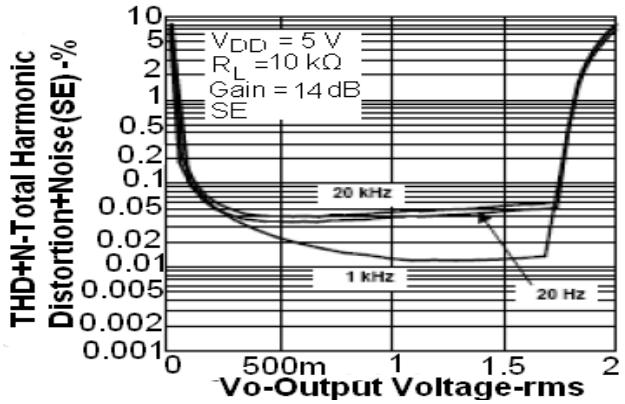
8. Total Harmonic Distortion + Noise(BTL) VS Output Power



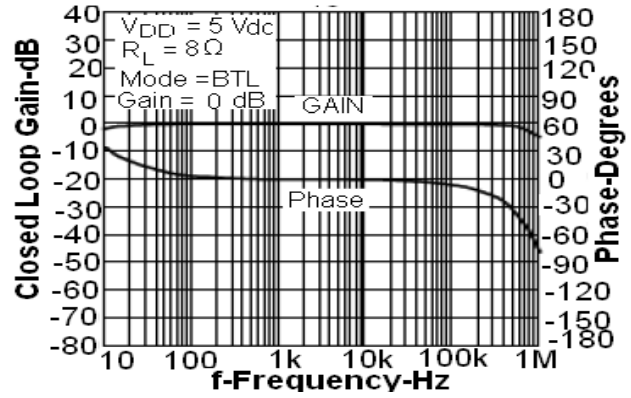
9. Total Harmonic Distortion + Noise(SE) VS Output Power



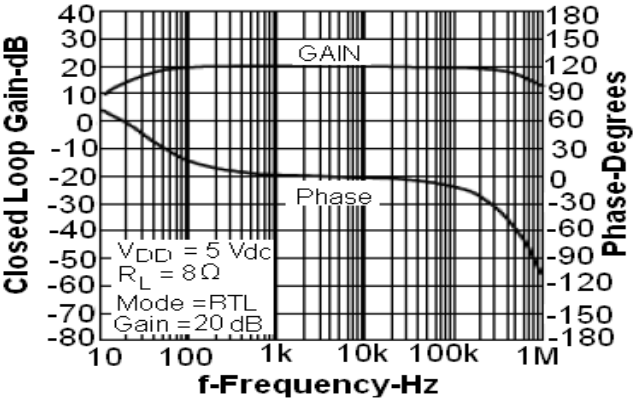
10. Total Harmonic Distortion + Noise(SE) VS Output Voltage



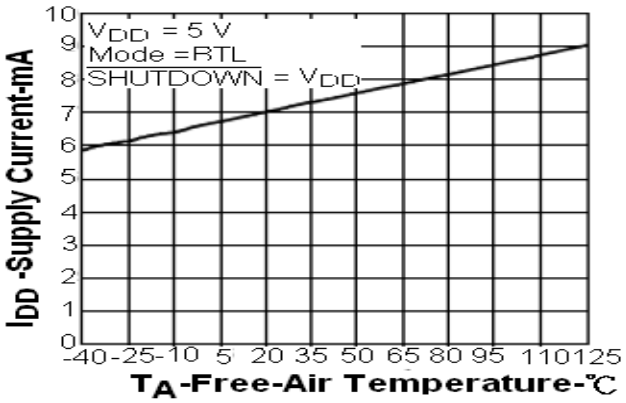
11. Closed Loop Response



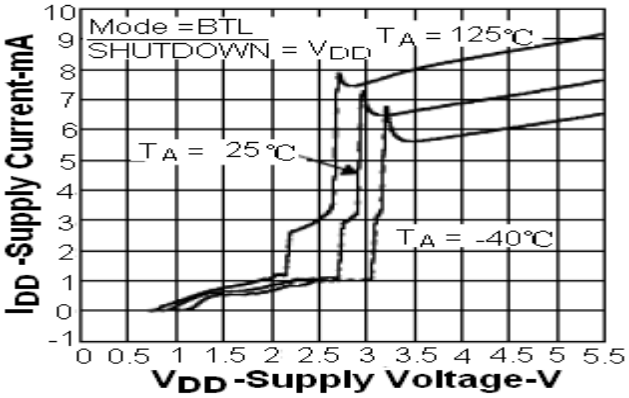
12. Closed Loop Response



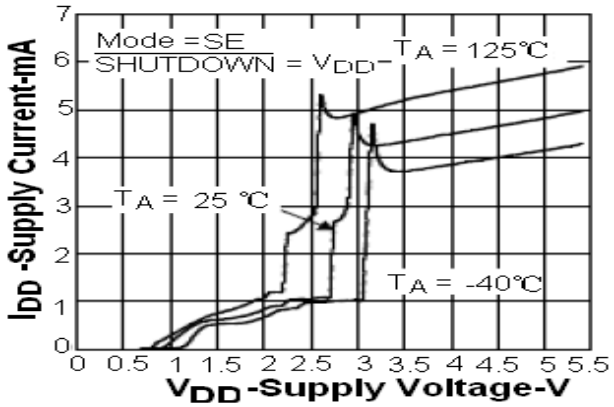
13. Supply Current VS Free-AIR Temperature



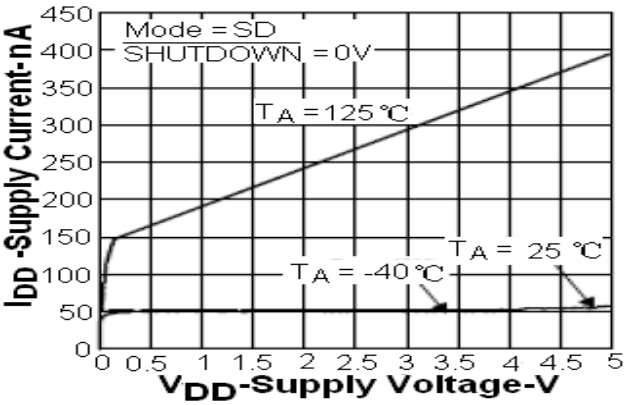
14. Supply Current VS Supply Voltage



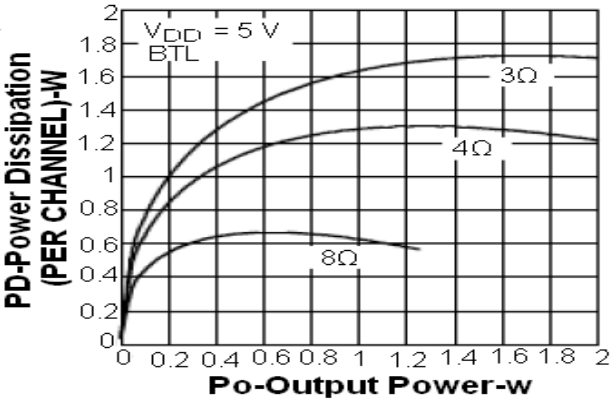
15. Supply Current VS Supply Voltage



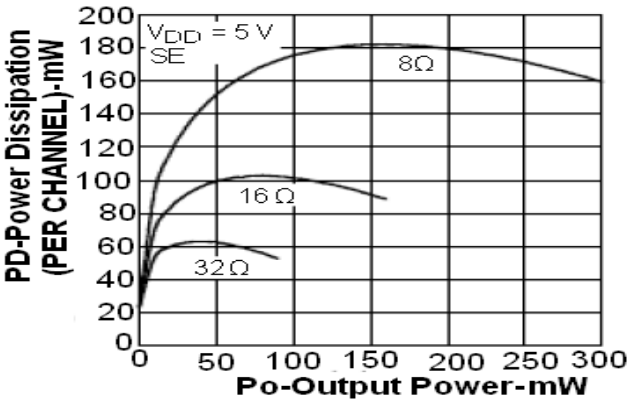
16. Supply Current VS Supply Voltage



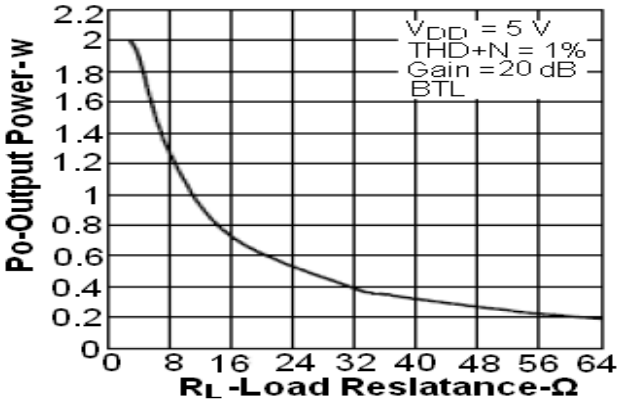
17. Power Dissipation (PER CHANNEL) VS Output Power



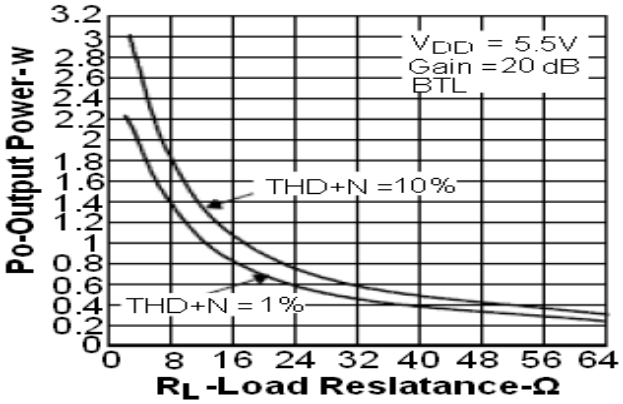
18. Power Dissipation (PER CHANNEL) VS Output Power



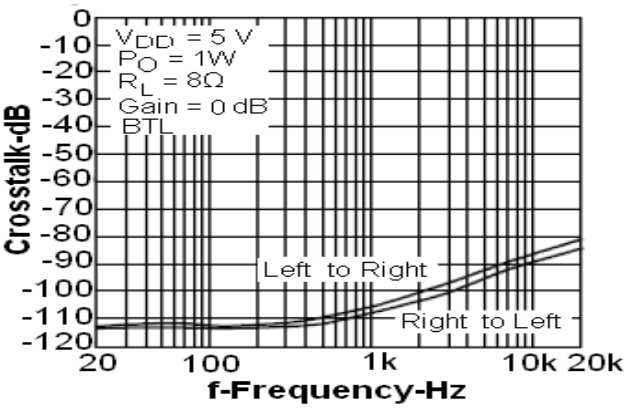
19. Output Power VS Load Resistance



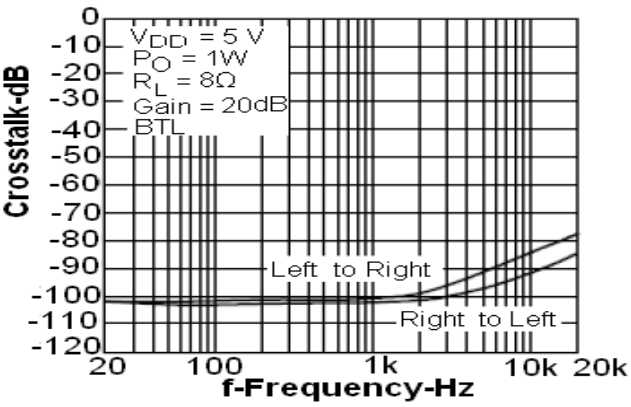
20. Output Power VS Load Resistance



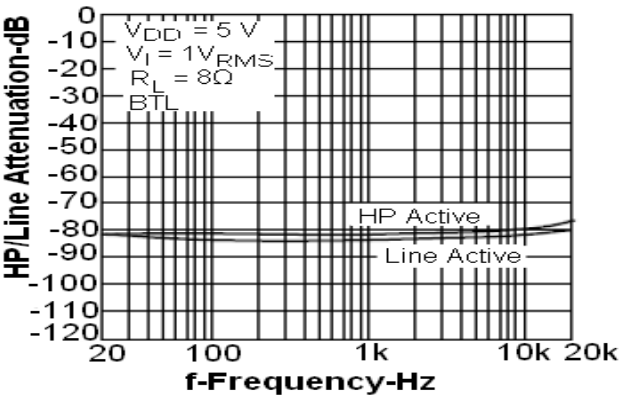
21. Crosstalk VS Frequency



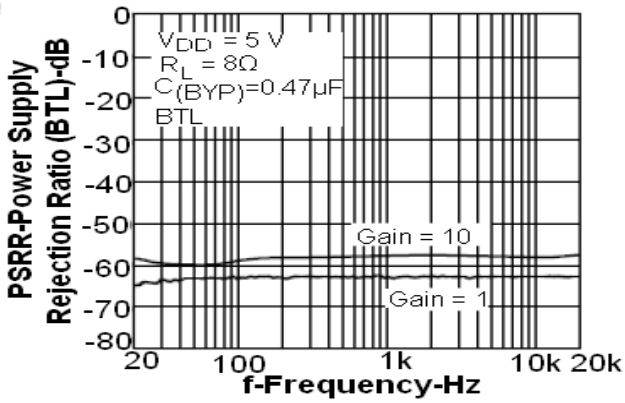
22. Crosstalk VS Frequency



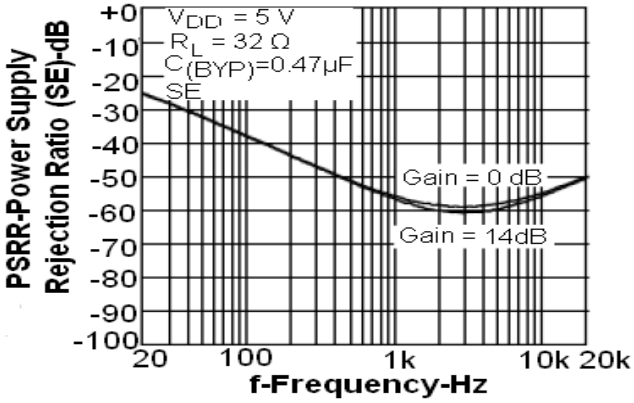
23. HP/LINE Attenuation VS Frequency



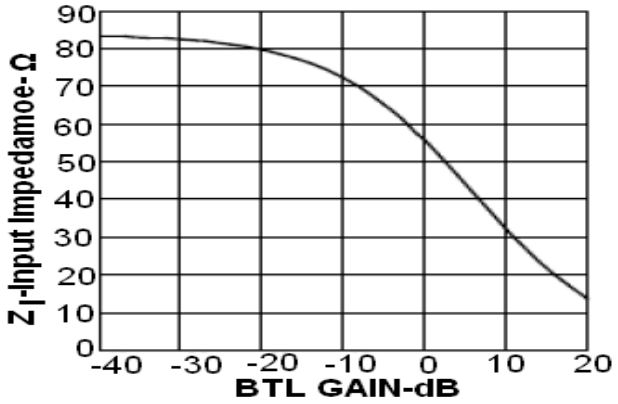
24. Power Supply Rejection ratio(BTL) VS Frequency



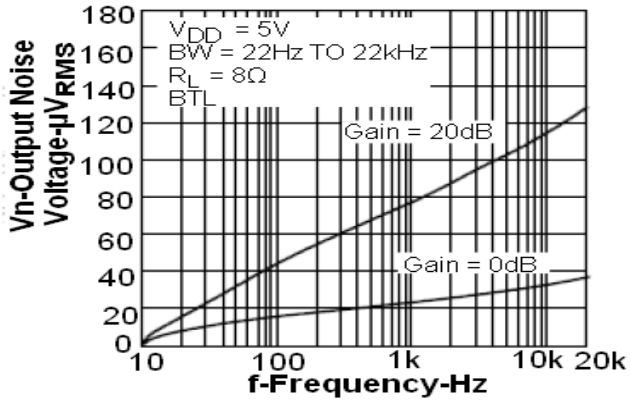
25. Power Supply Rejection ratio(SE) VS Frequency



26. Input Impedance VS BTL GAIN

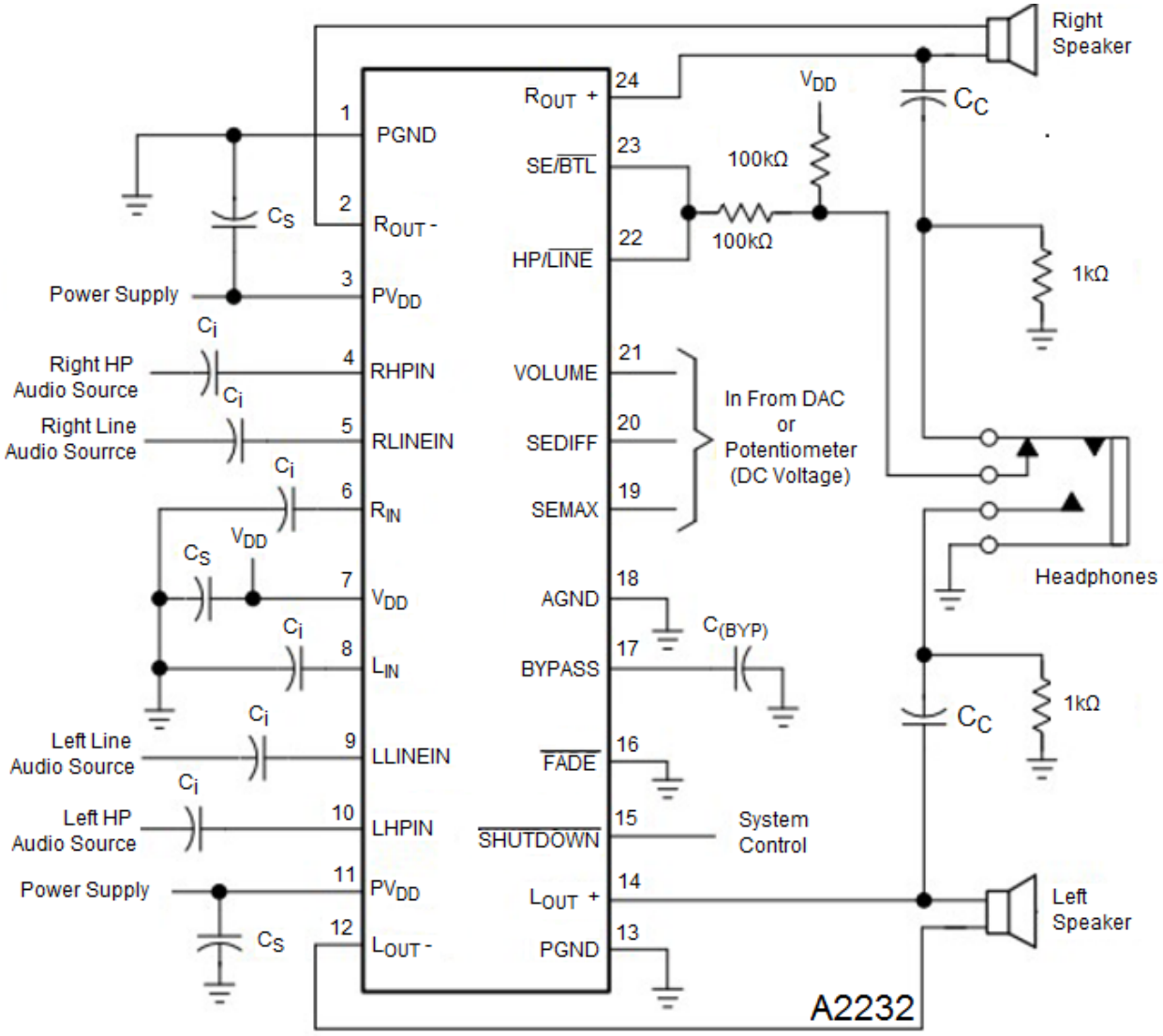


27. Output Noise Voltage VS Frequency



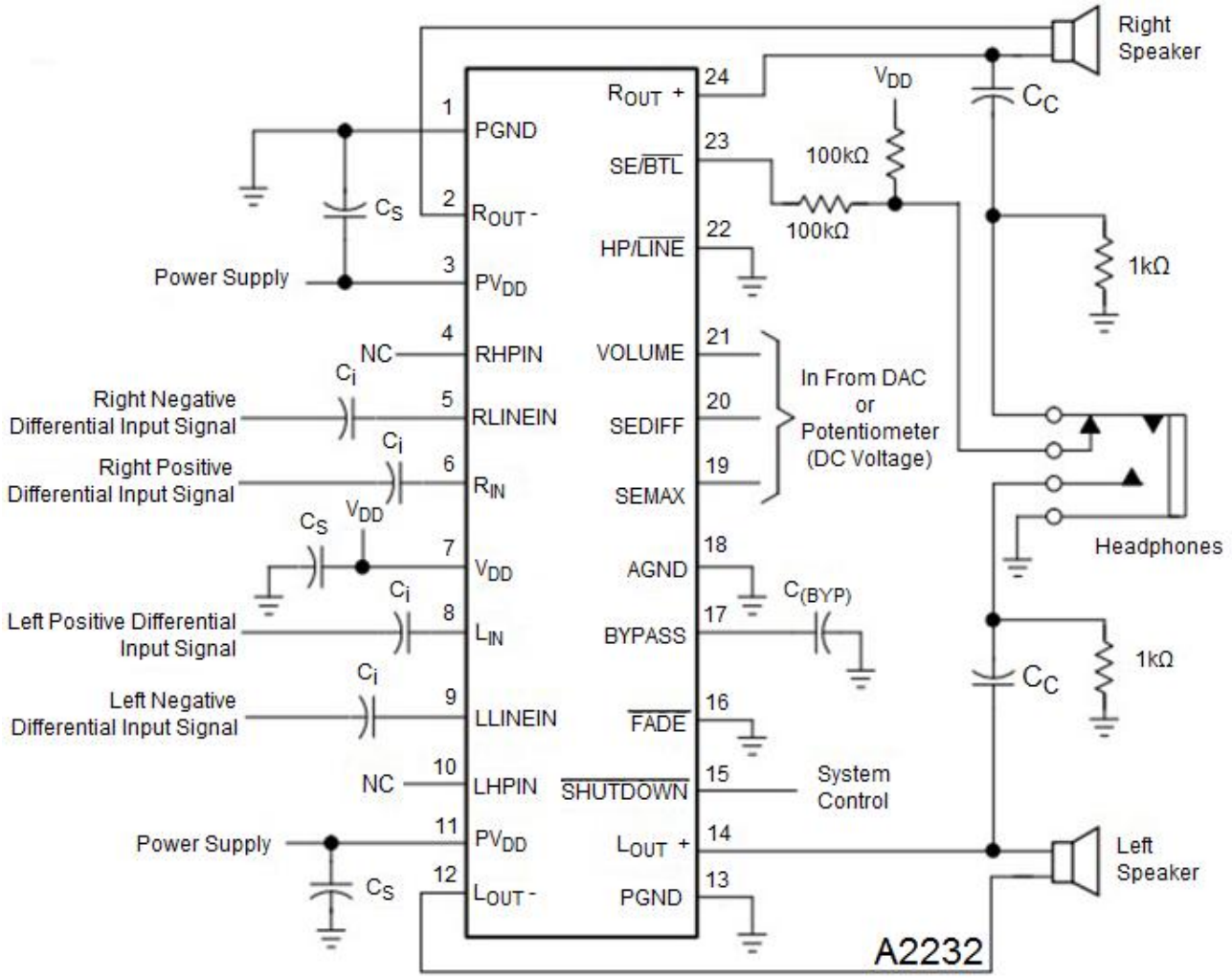
TEST CIRCUIT

Figure 1. Typical A2232 application Circuit Using Single-Ended Inputs And Input MUX



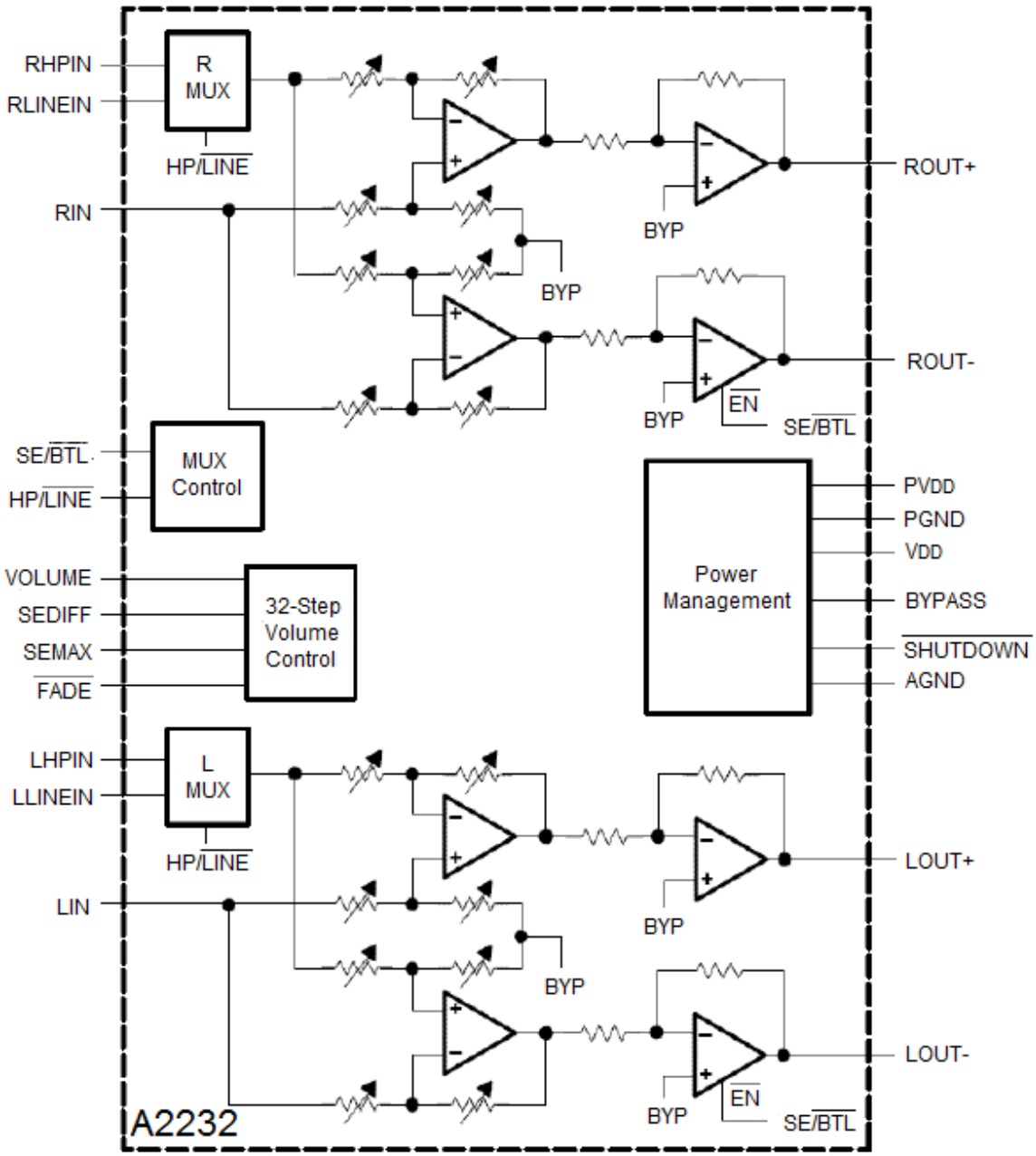
NOTE: 0.1μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10μF or greater should be placed near the audio power amplifier.

Figure 2. Typical A2232 Application Circuit Using Differential Inputs



NOTE: 0.1μF ceramic capacitor should be placed as close as possible to the IC. For filtering lower-frequency noise signals, a larger electrolytic capacitor of 10μF or greater should be placed near the audio power amplifier.

BLOCK DIAGRAM



DETAILED INFORMATION

Table 1 : DC volume control corresponding to the table (BTL output mode V_{DD}=5V)[NOTE1]

VOLUME (PIN5)		Gain Of Amplifier
From (V)	To (V)	(Typ)
0.00	0.26	-85[NOTE2]
0.33	0.37	-40
0.44	0.48	-38
0.56	0.59	-36
0.67	0.70	-34
0.78	0.82	-32
0.89	0.93	-30
1.01	1.04	-28
1.12	1.16	-26
1.23	1.27	-24
1.35	1.38	-22
1.46	1.49	-20
1.57	1.60	-18
1.68	1.72	-16
1.79	1.83	-14
1.91	1.94	-12
2.02	2.06	-10
2.13	2.17	-8
2.25	2.28	-6 [NOTE2]
2.36	2.39	-4
2.47	2.50	-2
2.58	2.61	0
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20 [NOTE2]

NOTE1: For other values of V_{DD}, scale the voltage values in the table by a factor of V_{DD} /5.

NOTE2: Tested in production. Remaining gain steps are specified by design.

Table 2 : DC volume control corresponding to the table (SE output mode V_{DD}=5V)[NOTE1]

SE_VOLUME=VOLUME or SEMAX		Gain Of Amplifier (Typ.)
From (V)	To (V)	
0.00	0.26	-85 [NOTE2]
0.33	0.37	-40
0.44	0.48	-38
0.56	0.59	-36
0.67	0.70	-34
0.78	0.82	-32
0.89	0.93	-30
1.01	1.04	-28
1.12	1.16	-26
1.23	1.27	-24
1.35	1.38	-22
1.46	1.49	-20
1.57	1.60	-18
1.68	1.72	-16
1.79	1.83	-14
1.91	1.94	-12
2.02	2.06	-10
2.13	2.17	-8
2.25	2.28	-6 [NOTE2]
2.36	2.39	-4
2.47	2.50	-2
2.58	2.61	0 [NOTE2]
2.70	2.73	2
2.81	2.83	4
2.92	2.95	6 [NOTE2]
3.04	3.06	8
3.15	3.17	10
3.26	3.29	12
3.38	3.40	14
3.49	3.51	16
3.60	3.63	18
3.71	5.00	20

NOTE2: Tested in production. Remaining gain steps are specified by design

Application Information

SE/BTL Operation

The ability of the A2232 to easily switch between BTL and SE modes is one of its most important cost saving features. This feature eliminates the requirement for an additional headphone amplifier in applications where internal stereo speakers are driven in BTL mode but external headphone or speakers must be accommodated. Internal to the A2232, two separate amplifiers drive OUT+ and OUT-. The SE/$\overline{\text{BTL}}$ input controls the operation of the follower amplifier that drives LOUT- and ROUT-. When SE/$\overline{\text{BTL}}$ is held low, the amplifier is on and the A2232 is in the BTL mode. When is SE/$\overline{\text{BTL}}$ is held high, the OUT- amplifiers are in a high output impedance state, which configures the A2232 as an SE driver from LOUT+ and ROUT+. I_{DD} is reduced by approximately one-third in SE mode. Control of the SE/$\overline{\text{BTL}}$ input can be from a logic-level CMOS source or, more typically, from a resistor divider network as shown in the Figure below. The trip level for the SE/$\overline{\text{BTL}}$ input can be found in the recommended operating conditions table.

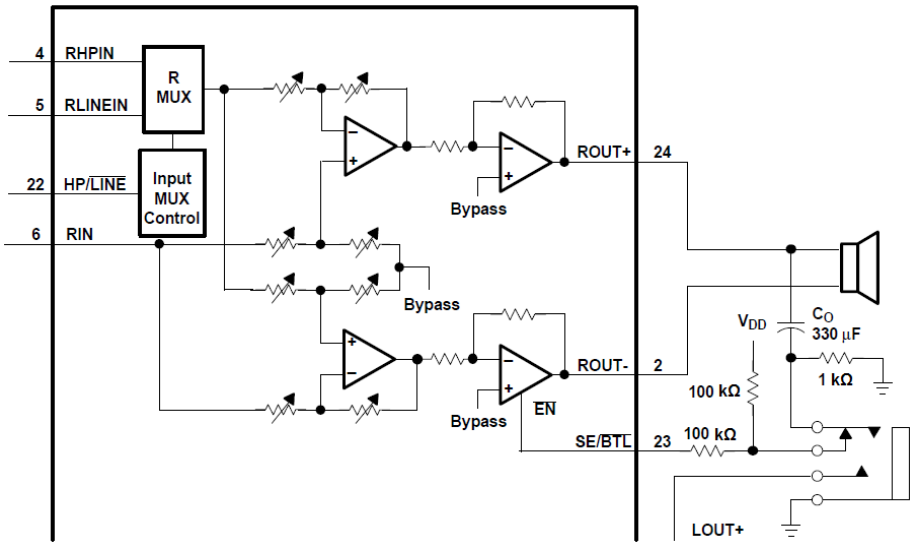


Figure 3 A2232 Resistor Divider Network Circuit

Using a 1/8-in. (3.5 mm) stereo headphone jack, the control switch is closed when no plug is inserted. When closed the 100kΩ/1kΩ divider pulls the SE/$\overline{\text{BTL}}$ input low. When a plug is inserted, the 1kΩ resistor is disconnected and the SE/$\overline{\text{BTL}}$ input is pulled high. When the input goes high, the OUT- amplifier is shut down causing the speaker to mute (open-circuits the speaker). The OUT+ amplifier then drives through the output capacitor (C_O) into the headphone jack.

HP/LINE Operation

The HP/$\overline{\text{LINE}}$ input controls the internal input multiplexer (MUX). Refer to the block diagram in Figure3. This allows the device to switch between two separate stereo inputs to the amplifier. For design flexibility, the

HP/$\overline{\text{LINE}}$ control is independent of the output mode, SE or BTL, which is controlled by the aforementioned SE/$\overline{\text{BTL}}$ pin. To allow the amplifier to switch from the LINE inputs to the HP inputs when the output switches from BTL mode to SE mode, simply connect the SE/$\overline{\text{BTL}}$ control input to the HP/$\overline{\text{LINE}}$ input.

When this input is logic high, the RHPIN and LHPIN inputs are selected. When this terminal is logic low, the RLINEIN and LLINEIN inputs are selected. This operation is also detailed in Table 1 and the trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the recommended operating conditions table.

SHUTDOWN Modes

The A2232 employs a shutdown mode of operation designed to reduce supply current (I_{DD}) to the absolute minimum level during periods of nonuse for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, I_{DD}=20μA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected because amplifier operation would be unpredictable.

Table 3 HP/$\overline{\text{LINE}}$, SE/$\overline{\text{BTL}}$, and $\overline{\text{SHUTDOWN}}$ Functions

Input[NOTE3]			Amplifier State	
HP/$\overline{\text{LINE}}$	SE/$\overline{\text{BTL}}$	$\overline{\text{SHUTDOWN}}$	Input	Output
X	X	Low	X	Mute
Low	Low	High	Line	BTL
Low	High	High	Line	SE
High	Low	High	HP	BTL
High	High	High	HP	SE

NOTE3: Inputs should never be left unconnected.

Fade Operation

For design flexibility, a fade mode is provided to slowly ramp up the amplifier gain when coming out of shutdown mode and conversely ramp the gain down when going into shutdown. This mode provides a smooth transition between the active and shutdown states and virtually eliminates any pops or clicks on the outputs.

When the $\overline{\text{FADE}}$ input is a logic low, the device is placed into fade-on mode. A logic high on this pin places the amplifier in the fade-off mode. The voltage trip levels for a logic low (V_{IL}) or logic high (V_{IH}) can be found in the recommended operating conditions table.

When a logic low is applied to the $\overline{FADE}$ pin and a logic low is then applied on the $\overline{SHUTDOWN}$ pin, the channel gain steps down from gain step to gain step at a rate of two clock cycles per step. With a nominal internal clock frequency of 58 Hz, this equates to 34ms (1/24 Hz) per step. The gain steps down until the lowest gain step is reached. The time it takes to reach this step depends on the gain setting prior to placing the device in shutdown. For example, if the amplifier is in the highest gain mode of 20 dB, the time it takes to ramp down the channel gain is 1.05 seconds. This number is calculated by taking the number of steps to reach the lowest gain from the highest gain, or 31 steps, and multiplying by the time per step, or 34ms.

After the channel gain is stepped down to the lowest gain, the amplifier begins discharging the bypass capacitor from the nominal voltage of $V_{DD}/2$ to ground. This time is dependent on the value of the bypass capacitor. For a 0.47µF capacitor that is used in the application diagram in Figure 1, the time is approximately 500ms. This time scales linearly with the value of bypass capacitor. For example, if a 1µF capacitor is used for bypass, the time period to discharge the capacitor to ground is twice that of the 0.47µF capacitor, or 1 second. Figure 3 below is a waveform captured at the output during the shutdown sequence when the part is in fade-on mode. The gain is set to the highest level and the output is at V_{DD} when the amplifier is shut down.

When a logic high is placed on the $\overline{SHUTDOWN}$ pin and the $\overline{FADE}$ pin is still held low, the device begins the start-up process. The bypass capacitor will begin charging. Once the bypass voltage reaches the final value of $V_{DD}/2$, the gain increases in 2dB steps from the lowest gain level to the gain level set by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

In the fade-off mode, the amplifier stores the gain value prior to starting the shutdown sequence. The output of the amplifier immediately drops to $V_{DD}/2$ and the bypass capacitor begins a smooth discharge to ground. When shutdown is released, the bypass capacitor charges up to $V_{DD}/2$ and the channel gain returns immediately to the value stored in memory. Figure 4 below is a waveform captured at the output during the shutdown sequence when the part is in the fade-off mode. The gain is set to the highest level, and the output is at V_{DD} when the amplifier is shut down.

The power-up sequence is different from the shutdown sequence and the voltage on the $\overline{FADE}$ pin does not change the power-up sequence. Upon a power-up condition, the A2232 begins in the lowest gain setting and steps up 2dB every 2 clock cycles until the final value is reached as determined by the dc voltage applied to the VOLUME, SEDIFF, and SEMAX pins.

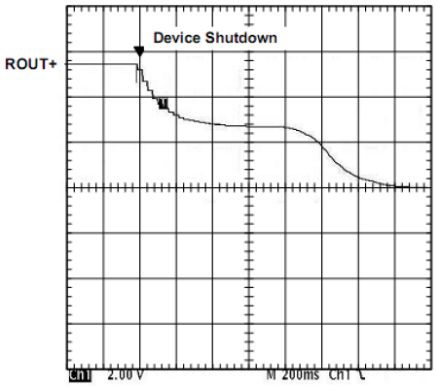


Figure 4 Shutdown Sequence in the Fade-on Mode

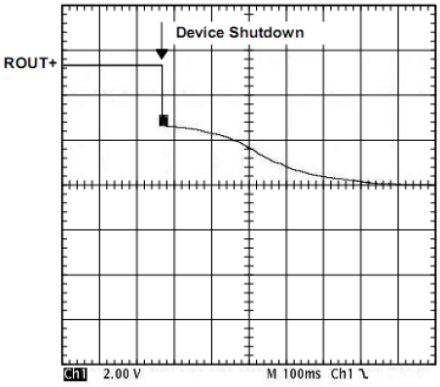


Figure 5 Shutdown Sequence in the Fade-off Mode

VOLUME, SEDIFF, and SEMAX Operation

Three pins labeled VOLUME, SEDIFF, and SEMAX control the BTL volume when driving speakers and the SE volume when driving headphones. All of these pins are controlled with a dc voltage, which should not exceed V_{DD}.

When driving speakers in BTL mode, the VOLUME pin is the only pin that controls the gain. Table 1 shows the gain for the BTL mode. The voltages listed in the table are for V_{DD}=5V. For a different V_{DD}, the values in the table scale linearly. If V_{DD}=4V, multiply all the voltages in the table by 4V/5V, or 0.8.

The A2232 allows the user to specify a difference between BTL gain and SE gain. This is desirable to avoid any listening discomfort when plugging in headphones. When switching to SE mode, the SEDIFF and SEMAX pins control the singe-ended gain proportional to the gain set by the voltage on the VOLUME pin. When SEDIFF=0V, the difference between the BTL gain and the SE gain is 6 dB. Refer to the section labeled bridged-tied load versus single-ended load for an explanation on why the gain in BTL mode is 2x that of single-ended mode, or 6dB greater. As the voltage on the SEDIFF terminal is increased, the gain in SE mode decreases. The voltage on the SEDIFF terminal is subtracted from the voltage on the VOLUME terminal and this value is used to determine the SE gain.

Some audio systems require that the gain be limited in the single-ended mode to a level that is comfortable for headphone listening. Most volume control devices only have one terminal for setting the gain. For example, if the speaker gain is 20dB, the gain in the headphone channel is fixed at 14dB. This level of gain could cause discomfort to listeners and the SEMAX pin allows the designer to limit this discomfort when plugging in headphones. The SEMAX terminal controls the maximum gain for single-ended mode.

The functionality of the SEDIFF and SEMAX pin are combined to set the SE gain. A block diagram of the combined functionality is shown in Figure 6. The value obtained from the block diagram for SE_VOLUME is a dc voltage that can be used in conjunction with Table 2 to determine the SE gain. Again, the voltages listed in the table are for V_{DD}=5V. The values must be scaled for other values of V_{DD}.

Table 1 and Table 2 show a range of voltages for each gain step. There is a gap in the voltage between each gain step. This gap represents the hysteresis about each trip point in the internal comparator. The hysteresis ensures that the gain control is monotonic and does not oscillate from one gain step to another. If a potentiometer is used to adjust the voltage on the control terminals, the gain increases as the potentiometer is turned in one direction and decreases as it is turned back the other direction. The trip point, where the gain actually changes, is different depending on whether the voltage is increased or decreased as a result of the hysteresis about each trip point. The gaps in Table 1 and Table 2 can also be thought of as indeterminate states where the gain could be in the next higher gain step or the lower gain step depending on the direction the voltage is changing. If using a DAC to control the volume, set the voltage in the middle of each range to ensure that the desired gain is achieved.

A pictorial representation of the volume control can be found in Figure 7. The graph focuses on three gain steps with the trip points defined in Table 1 for BTL gain. The dotted line represents the hysteresis about each gain step.

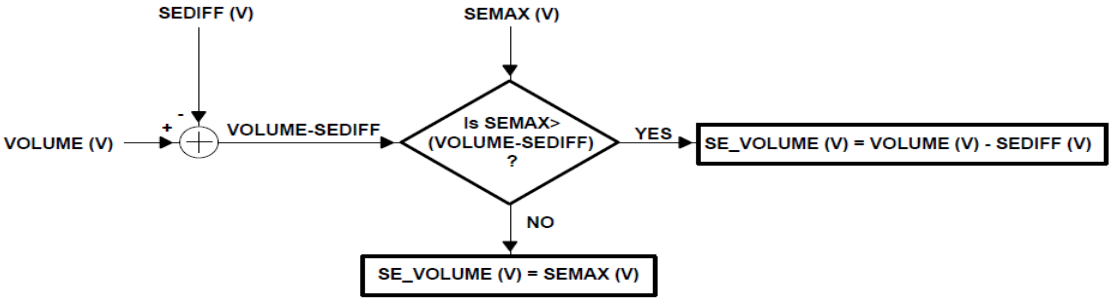


Figure 6 Block Diagram of SE Volume Control

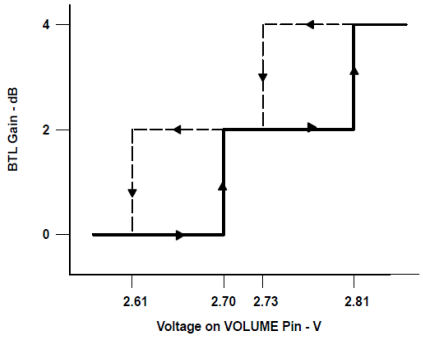


Figure 7 DC Volume Control Operation

Input Resistance

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3dB or cutoff frequency also changes by over six times.

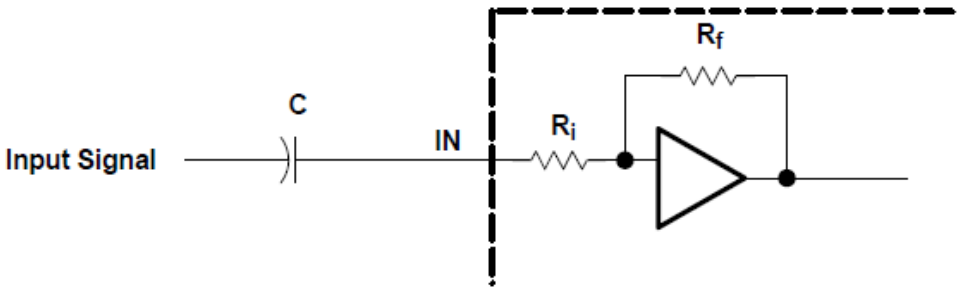


Figure 8 Resistor on Input for Cut-Off Frequency

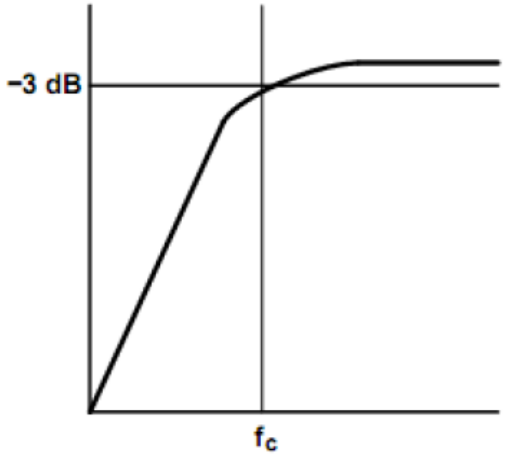
The -3dB frequency can be calculated using Equation 1.

$$f_{-3dB} = \frac{1}{2\pi CRi}$$

Input CAPACITOR, C_I

In the typical application an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (R_i) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_{c(highpass)} = \frac{1}{2\pi RiCi}$$



The value of C_i is important to consider as it directly affects the bass (low frequency) performance of the circuit. Consider the example where R_i is 70 kΩ and the specification calls for a flat-bass response down to 40Hz.Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi R_i f_c}$$

In this example, C_i is 56.8nF, so one would likely choose a value in the range of 56nF to 1μF. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at $V_{DD}/2$, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling, $C_{(S)}$

The A2232 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device V_{DD} lead, works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

Midrail Bypass Capacitor, $C_{(BYP)}$

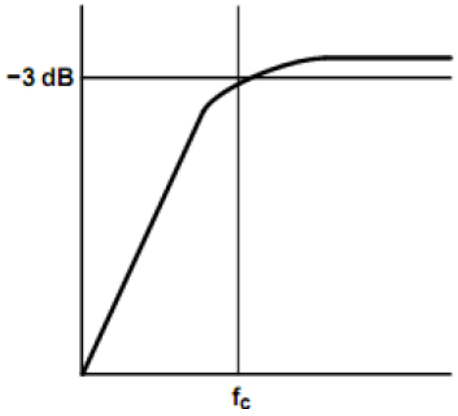
The midrail bypass capacitor ($C_{(BYP)}$) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, $C_{(BYP)}$ determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor ($C_{(BYP)}$) values of 0.47μF to 1μF ceramic or tantalum low-ESR capacitors are recommended for the best THD and noise performance. For the best pop performance, choose a value for $C_{(BYP)}$ that is equal to or greater than the value chosen for C_I. This ensures that the input capacitors are charged up to the midrail voltage before $C_{(BYP)}$ is fully charged to the midrail voltage.

Output Coupling capacitor, $C_{(C)}$

In the typical single-supply SE configuration, an output coupling capacitor ($C_{(C)}$) is required to block the dc bias at the output of the amplifier, thus preventing dc currents in the load. As with the input coupling capacitor, the output coupling capacitor and impedance of the load form a high-pass filter governed by Equation 4.

$$f_{c(high)} = \frac{1}{2\pi R_L C_{(C)}}$$



The main disadvantage, from a performance standpoint, is the load impedances are typically small, which drives the low-frequency corner higher, degrading the bass response. Large values of $C_{(C)}$ are required to pass low frequencies into the load. Consider the example where a $C_{(C)}$ of 330µF is chosen and loads vary from 3Ω, 4Ω, 8Ω, 32Ω, 10kΩ , and 47kΩ. Table 4 summarizes the frequency response characteristics of each configuration.

Table 4 Common Load Impedances vs Low Frequency Output Characteristics in SE Mode

R_L	$C_{(C)}$	Lowest Frequency
3Ω	330µF	161Hz
4Ω	330µF	120Hz
8Ω	330µF	60Hz
32Ω	330µF	15Hz
10,000Ω	330µF	0.05Hz
47,000Ω	330µF	0.01Hz

As Table 4 indicates, most of the bass response is attenuated into a 4Ω load, an 8Ω load is adequate, headphone response is good, and drive into line level inputs (a home stereo for example) is exceptional.

Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

Bridged-Tied Load VS Single-ended Load

Figure 9 shows a Class-AB audio power amplifier (APA) in a BTL configuration. The A2232 BTL amplifier consists of two Class-AB amplifiers driving both ends of the load. There are several potential benefits to this differential drive configuration, but, initially consider power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance (see Equation 5).

$$V_{(rms)} = \frac{Vo(pp)}{2\sqrt{2}} \qquad Power = \frac{V_{(rms)}^2}{R_L}$$

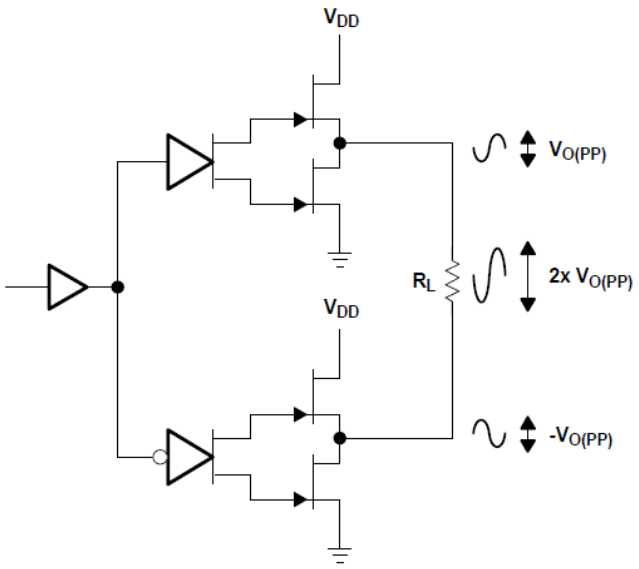


Figure 9 Bridge-Tied Load Configuration

In a typical computer sound channel operating at 5V, bridging raises the power into an 8Ω speaker from a singled-ended (SE, ground reference) limit of 250mW to 1W. In sound power that is a 6dB improvement, which is loudness that can be heard. In addition to increased power there are frequency response concerns. Consider the single-supply SE configuration shown in Figure10. A coupling capacitor is required to block the

dc offset voltage from reaching the load. These capacitors can be quite large (approximately 33μF to 1000μF), so they tend to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance of the system. This frequency limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance and is calculated with Equation 6.

$$f_{(c)} = \frac{1}{2\pi R_L C_C}$$

For example, a 68μ F capacitor with an 8Ω speaker would attenuate low frequencies below 293Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

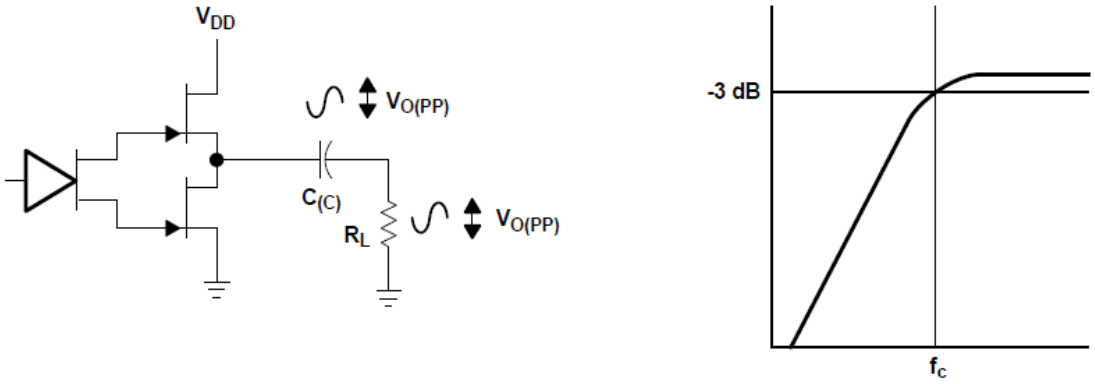


Figure 10 Single-Ended Configuration and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration. Internal dissipation versus output power is discussed further in the crest factor and thermal considerations section.

Single-ended operation

In SE mode (see Figure10), the load is driven from the primary amplifier output for each channel (OUT+). The amplifier switches single-ended operation when the SE/$\overline{\text{BTL}}$ terminal is held high. This puts the negative outputs in a high-impedance state, and effectively reduces the amplifier's gain by 6dB.

BTL Amplifier Efficiency

Class-AB amplifiers are inefficient. The primary cause of these inefficiencies is voltage drop across the output stage transistors. There are two components of the internal voltage drop. One is the headroom or dc voltage

drop that varies inversely to output power. The second component is due to the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the RMS value of the supply current (I_{DD} rms) determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 11).

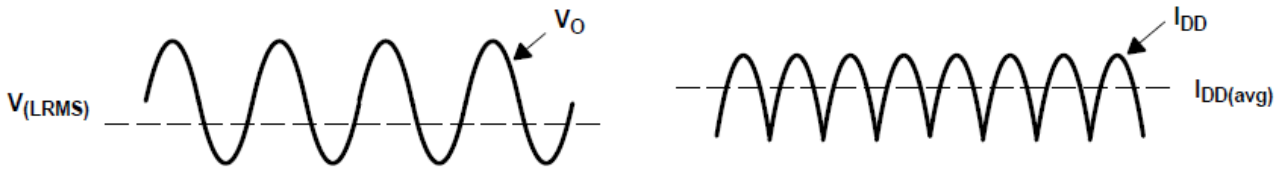


Figure11. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore }, P_L = \frac{V_P{}^2}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD} I_{DD} avg \text{ and } I_{DD}\,avg = \frac{1}{\pi}\int_0^{\pi} \frac{Vp}{R_L}\sin(t)dt = \frac{1}{\pi} \times \frac{Vp}{R_L}\left[\cos(t)\right]_0^{\pi} = \frac{2Vp}{\pi R_L}$$

$$\text{Therefore, } P_{SUP} = \frac{2V_{DD}Vp}{\pi RL}$$

Substituting PL and PSUP into Equation 7

$$\text{Efficiency of a BTL amplifier} = \frac{\frac{Vp^2}{2R_L}}{\frac{2V_{DD}Vp}{\pi R_L}} = \frac{\pi Vp}{4V_{DD}}$$

$$\text{Where : } Vp = \sqrt{2PLRL} \quad \text{Therefore } \eta_{BTL} \quad \frac{\pi\sqrt{2P_L R_L}}{4V_{DD}}$$

P_L=Power delivered to load

V_P=Peak voltage on BTL load

P_{SUP}=Power drawn from power supply

I_{DD}avg=Average current drawn from the power supply

V_{LRMS}=RMS voltage on BTL load

V_{DD}=Power supply voltage

R_L=Load resistance

η_{BTI}=Efficiency of a BTL amplifier

Table 5 employs Equation 8 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a stereo 1W audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 3.25 W.

Table 5 Efficiency VS Output Power in 5V, 8

Output Power(W)	Efficiency(%)	Peak Voltage(V)	Internal DIsspation(W)
0.25	31.4	2.00	0.55
0.50	44.4	2.83	0.62
1.00	62.8	4.00	0.59
1.25	70.2	4.47NOTE4	0.53

NOTE4: High peak voltage cause the THD to increase.

A final point to remember about Class-AB amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation 8, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

Crest Factor And Thermal Considerations

Class-AB power amplifiers dissipate a significant amount of heat in the package under normal operating conditions. A typical music CD requires 12dB to 15dB of dynamic range, or headroom above the average power output, to pass the loudest portions of the signal without distortion. In other words, music typically has a crest factor between 12dB and 15dB. When determining the optimal ambient operating temperature, the internal dissipated power at the average output power level must be used. From the A2232 data sheet, one can see that when the A2232 is operating from a 5V supply into a 3Ω speaker, that 4W peaks are available. Use equation 9 to convert watts to dB.

$$P_{dB} = 10Log\frac{P_W}{P_{ref}} = 10Log\frac{4W}{1W} = 6dB$$

Subtracting the headroom restriction to obtain the average listening level without distortion yields:

- 6 dB - 15 dB = -9 dB (15dB crest factor)
- 6 dB - 12 dB = -6 dB (12dB crest factor)
- 6 dB - 9 dB = -3 dB (9dB crest factor)
- 6 dB - 6 dB = 0 dB (6dB crest factor)
- 6 dB - 3 dB = 3 dB (3dB crest factor)

To convert dB back into watts use equation 10.

$$P_W = 10^{PdB/10} \times P_{REF}$$

=63mW (18dB crest factor)
=125mW (15dB crest factor)
=250mW (12dB crest factor)
=500mW (9dB crest factor)
=1000mW (6dB crest factor)
=2000mW (3dB crest factor)

This is valuable information to consider when attempting to estimate the heat dissipation requirements for the amplifier system. Comparing the worst case, which is 2W of continuous power output with a 3dB crest factor, against 12dB and 15dB applications significantly affects maximum ambient temperature ratings for the system. Using the power dissipation curves for a 5V, 3Ω system, the internal dissipation in the A2232 and maximum ambient temperatures is shown in Table 6.

Table 6 A2232 Power Rating, 5V, 3Ω Stereo

Peak output Power (W)	Average Output Power	Power dissipation (W/Channel)	Maximum Ambient Temperature
4	2 W (3dB)	1.7	-3℃
4	1 W (6dB)	1.6	6℃
4	500 mW (9dB)	1.4	24℃
4	250 mW (12dB)	1.1	51℃
4	125 mW (15dB)	0.8	78℃
4	63 mW (18dB)	0.6	96℃

Table 7 A2232 Power Rating, 5V, 8Ω Stereo

Peak output Power (W)	Average Output Power	Power dissipation (W/Channel)	Maximum Ambient Temperature
2.5	1250mW (3dB crest factor)	0.55	100℃
2.5	1000mW (4dB crest factor)	0.62	94℃
2.5	500mW (7dB crest factor)	0.59	97℃
2.5	250mW (10dB crest factor)	0.53	102℃

The maximum dissipated power ($P_{D(MAX)}$) is reached at a much lower output power level for an 8Ω load than for a 3Ω load. As a result, this simple formula for calculating $P_{D(MAX)}$ may be used for an 8Ω application.

$$P_{D(max)} = \frac{2V^2_{DD}}{\pi^2 R_L}$$

However, in the case of a 3Ω load, the $P_{D(MAX)}$) occurs at a point well above the normal operating power level. The amplifier may therefore be operated at a higher ambient temperature than required by the $P_{D(MAX)}$ formula for a 3Ω load.

The maximum ambient temperature depends on the heat-sinking ability of the PCB system. The derating factor for the PWP package is shown in the dissipation rating table. Use equation 12 to convert this to θ_{JA}.

$$\theta_{JA} = \frac{1}{\text{DeratingFactor}} = \frac{1}{0.022} = 45\ ℃/W$$

To calculate maximum ambient temperatures, first consider that the numbers from the dissipation graphs are per channel, so the dissipated power needs to be doubled for two channel operation. Given θ_{JA} , the maximum allowable junction temperature, and the total internal dissipation, the maximum ambient temperature can be calculated using Equation 13 . The maximum recommended junction temperature for the A2232 is 150°C.The internal dissipation figures are taken from the Power Dissipation VS Output Power graphs.

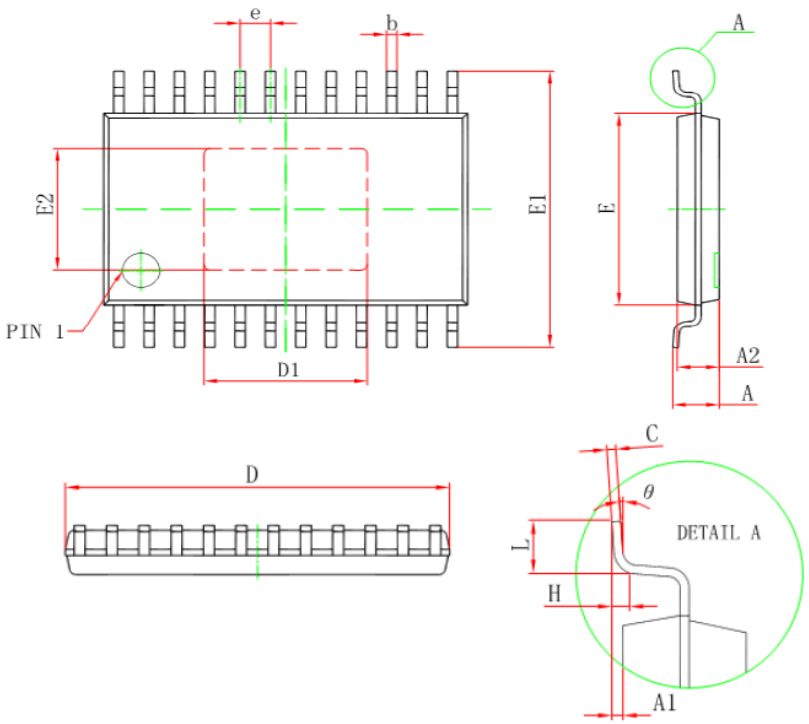
$$T_{AMAX}=T_{JMAX}-\theta_{JA}P_D=150-45(0.6\times2)=96℃(15\ dB\ crest\ factor)$$

NOTE: Internal dissipation of 0.6 W is estimated for a 2W system with 15dB crest factor per channel.

Table 6 and Table 7 show that some applications require no airflow to keep junction temperatures in the specified range. The A2232 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. Table 6 and Table 7 were calculated for maximum listening volume without distortion. When the output level is reduced the numbers in the table change significantly. Also, using 8Ω speakers increases the thermal performance by increasing amplifier efficiency.

PACKAGE INFORMATION

Dimension in P-TSSOP24 (Unit: mm)



Symbol	Min	Max
D	7.700	7.900
D1	3.400	3.600
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A	-	1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65 (BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°

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