DESCRIPTION

The A2410 is a 10W (per channel), efficient, class-D audio power amplifier for driving stereo speakers in a single-ended configuration; or a mono speaker in a bridge-tied-load configuration. The gain can be selected to 20, 26, 32, and 36 dB utilizing the GAIN0 and GAIN1 gain select pins.

The efficiency of the A2410 eliminates the need for an external heat sink when playing music.

The A2410 is available in P-TSSOP24 package.

ORDERING INFORMATION

Package Type	Part Number	
P-TSSOP24	TMXP24	A2410TMXP24R
		A2410TMXP24VR
Note	V: Halogen free Package R: Tape & Reel	
AiT provides all RoHS products Suffix " V " means Halogen free Package		

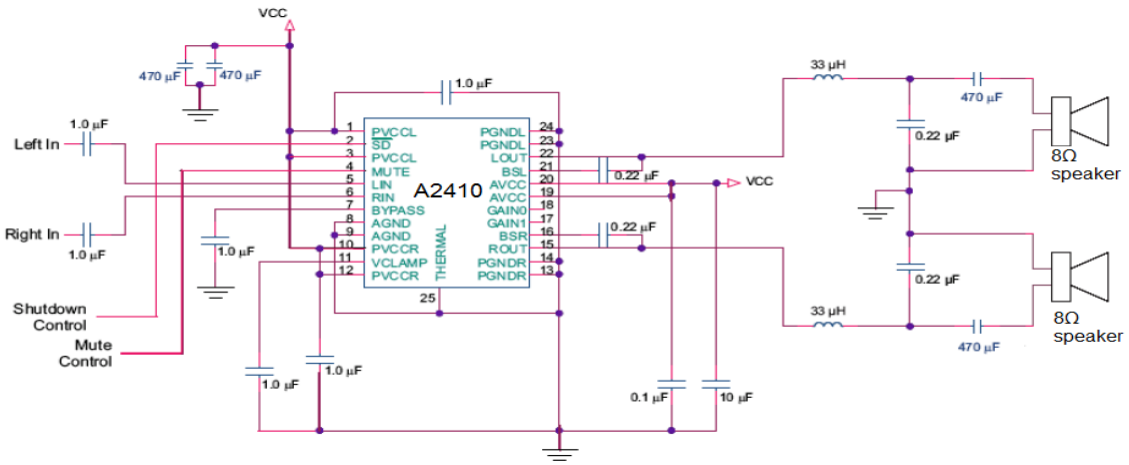
FEATURES

- Maximum Output
  10W/ch (V_{CC}=24V, R_L=8Ω, THD+N=10%)
- Low THD+N
  (0.06% @ V_{CC} = 24V, R_L=8Ω, P_O=4W, 1kHz)
- Wide Supply Voltage Range : 10V~26V
- Four Selectable, Fixed-Gain Settings
  (20dB, 26dB, 32dB, 36dB)
- High Efficiency (86%@R_L=8Ω,P_O=4W)
- Over-current and Thermal Protection Function
- Under-voltage & Over-voltage Protection Function
- Operation Temperature Range: -40℃~85℃
- Single-Ended Analog Inputs
- Available in P-TSSOP24 Package

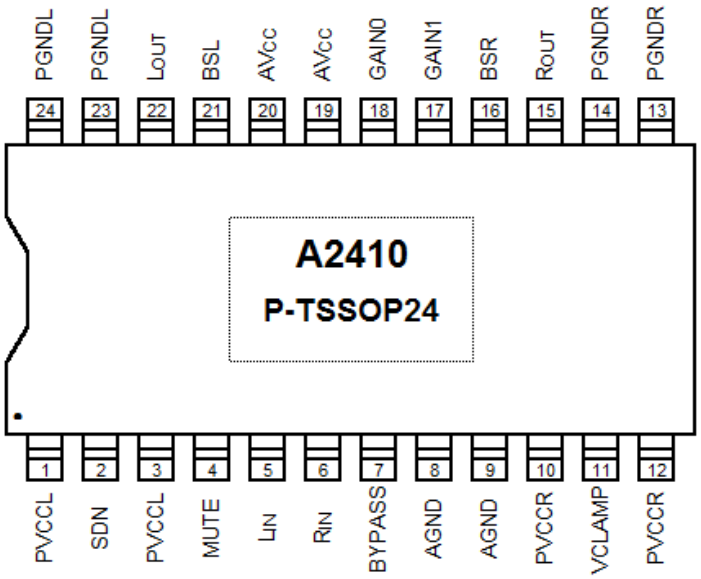
APPLICATION

- Flat Panel Televisions
- Notebook PC
- Powered Speakers

TYPICAL APPLICATION



PIN DESCRIPTION



Top View

Pin #	Symbol	I/O/P	Function
1,3	PVCCL	P	Power supply for left-channel H-bridge, not internally connected to PVCCR or AV_{CC}
2	SDN	I	Shutdown signal for IC (low=disabled, high=operational). TTL logic levels with compliance to AV_{CC}
4	MUTE	I	Mute signal for quick disable/enable of outputs (high=mute, low=outputs enabled). TTL logic levels with compliance to AV_{CC}
5	L_{IN}	I	Audio input for left channel
6	R_{IN}	I	Audio input for right channel
7	BYPASS	O	Reference for preamplifier inputs. Nominally equal to $AV_{CC}/8$
8,9	AGND	P	Analog ground
10,12	PVCCR	P	Power supply for right-channel H-bridge, not connected to PVCCL or AV_{CC}
11	VCLAMP	P	Internally generated voltage supply for bootstrap capacitors
13,14	PGNDR	P	Power ground for right-channel H-bridge.
15	R_{OUT}	O	Class-D H-bridge negative output for right channel
16	BSR	I/O	Bootstrap I/O for right channel
17	GAIN1	I	Gain select most-significant bit. TTL logic levels with compliance to

			AV_{CC}
18	GAIN0	I	Gain select least-significant bit. TTL logic levels with compliance to AV_{CC}
19,20	AV_{CC}	P	Analog ground
21	BSL	I/O	Bootstrap I/O for left channel
22	L_{OUT}	O	Class-D H-bridge positive output for left channel
23.24	PGNDL	P	Power ground for left-channel H-bridge
Thermal pad	Die pad	-	Connect to ground.

ABSOLUTE MAXIMUM RATINGS

V_{CC}, AV_{CC}, PV_{CC}, Power supply terminal voltage range	-0.3V to 30V
V_L, SDN, MUTE, GAIN0,GAIN1, Input logic terminal voltage range	-0.3V to AV_{CC}+0.3V
V_{IN}, R_{IN}, L_{IN}, Input analog terminal voltage range	-0.3 to 7
P_{D25}, Allowable dissipation(T_A=25℃)	4.17W
P_{D85}, Allowable dissipation(T_A=85℃)	2.16W
T_A, Operating free-air temperature range	-40℃ to 85℃
T_J, Junction temperature range	-40℃ to 150℃
T_{STG}, Storage temperature range	-65 to 150℃
$R_{L(SE)}$, Speaker impedance	3.5Ω
$R_{L(BTL)}$, Speaker impedance	7Ω
HM,ESD	±2KV
CDM, ESD	±500V

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	MAX	Units
Power supply terminal voltage range (V_{CC})	AV_{CC} , PV_{CC}	10	26	V
Input logic terminal voltage range(V_L)	SDN, MUTE, GAIN0, GAIN1	2	AV_{CC}	V
Input analog terminal voltage range(V_{IN})	SDN, MUTE, GAIN0, GAIN1	0	0.8	V
Operating Temperature Range	T_A	-40	85	°C

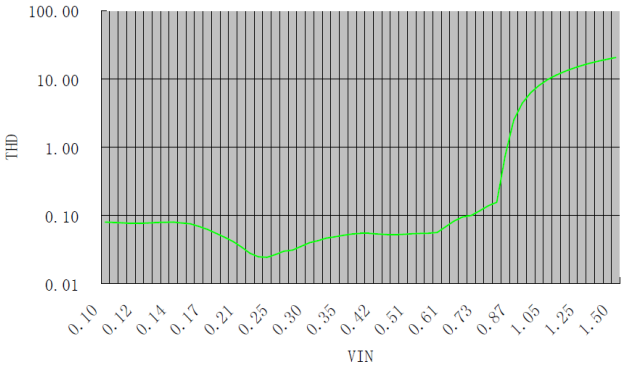
ELECTRICAL CHARACTERISTICS

All specifications below are at V_{CC}=24V, R_L=8Ω, T_A=25℃, unless otherwise noted.

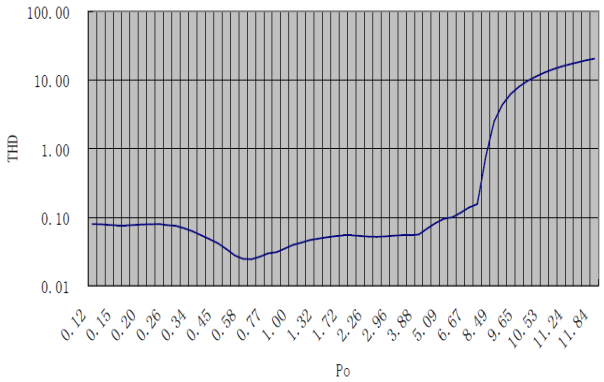
Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
AC CHARACTERISTICS							
Maximum Output power	P_O	THD+N=1%	V_{CC} = 24V		8		W
		THD+N=10%	f=1kHz		10		
Total Harmonic Distortion Rate	THD+N	P_O=4W, f=lkHz			0.06		%
Power supply rejection ratio	PSRR	V_{RIPPLE}=200mV_{PP}	100Hz		-48		dB
		Gain=20dB	1kHz		-52		
Signal/Noise Ratio (BW:20kHz A-Filter)	SNR	Gain=20dB, Max output at THD+N < 1%, f=1kHz			-92		dB
Output integrated noise floor	V_N	20Hz to 22kHz, A-weighted filter, Gain=20dB			125		μV
					-78		dBV
Crosstalk	$C_{ROSSTALK}$	P_O=1W, f=1kHz, Gain=20dB			-70		dB
Oscillator frequency	F_{SW}			250	300	350	KHz
Mute delay	Δt mute	Time from mute input switches high until outputs muted			30		μs
Unmute delay	Δt nmute	Time from mute input switches low until outputs unmated			120		ms
DC CHARACTERISTICS							
Output offset voltage	V_{OS}	V_{IN}=0V, A_V=36dB (measured differentially in BTL)		-50	±7.5	+50	mV
Gain	GAIN	GAIN1=L, GAIN0=L		18	20	22	dB
		GAIN1=L, GAIN0=H		24	26	28	
		GAIN1=H, GAIN0=L		30	32	34	
		GAIN1=H, GAIN0=H		34	36	38	
Quiescent supply current	I_{CC}	SDN=H, MUTE=L, no load			16	30	mA
Quiescent supply current in mute mode	I_{MUTE}	SDN=H, MUTE=H, no load			16		mA
Quiescent supply current in shutdown mode	I_{SD}	SDN=L, no load			0.5	1	mA
Drain-source on-state resistance	$R_{DS(ON)}$				210	450	mΩ

TYPICAL PERFORMANCE CHARACTERISTICS

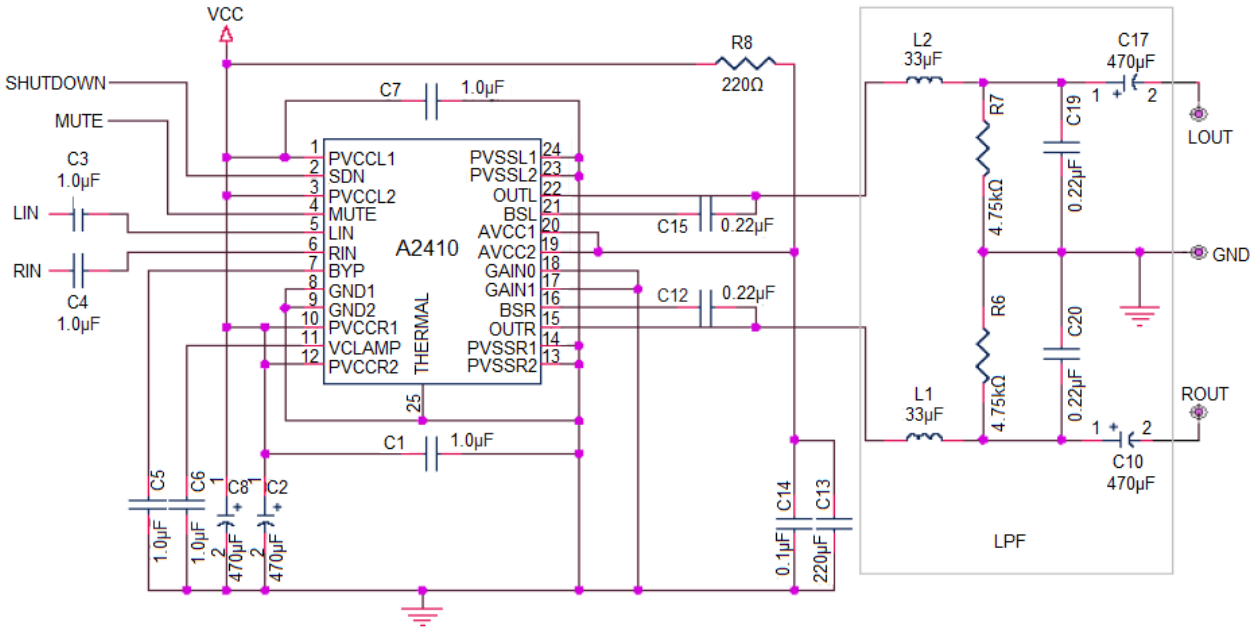
1. THD+N VS V_{IN} @ V_{CC}=24V, R_L=8Ω



2. THD+N VS P_O @ V_{CC}=24V, R_L=8Ω



TEST CIRCUIT

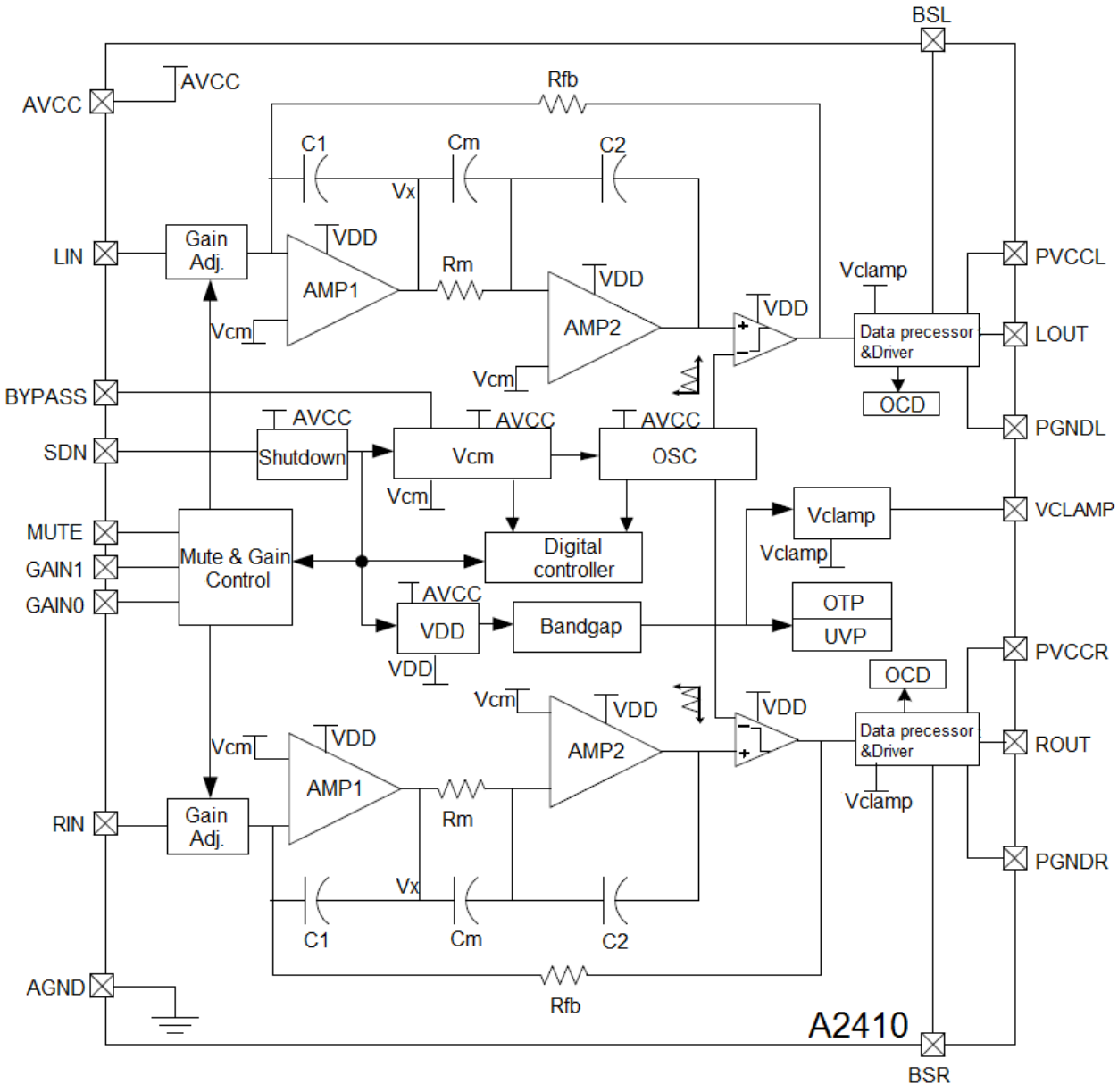


NOTE1: The LPF (shown in figure) is required even if the analyzer has an internal LPF

NOTE2: Capacitors should be placed as close as possible to the pad of the device.

NOTE3: Except for ISD, the test of other parameters should wait the end of start up. The start up time is approximately 180ms.

BLOCK DIAGRAM



DETAILED INFORMATION

Description of operating functions

The A2410 is a 10W (per channel), efficient, class-D audio power amplifier for driving stereo speakers in a single-ended configuration; or a mono speaker in a bridge-tied-load configuration. The gain can be selected to 20, 26, 32, and 36 dB utilizing the GAIN0 and GAIN1 gain select pins.

A2410 is mainly composed of two pseudo-differential Class-D power amplifiers, gain and mute control and auxiliary circuits. Pseudo-differential Class-D power amplifiers is mainly composed of a two-order integrator filter, PWM comparator and Driver. Gain and mute control use external gain adjustment pins to control gain and mute process. The chip implanted a unique POP suppression circuit which smooth change the gain of Class-D power amplifiers to suppress POP sound in the startup, shutdown and unmute process. The auxiliary circuit containing Bandgap, V_{CM}, V_{DD}, V_{CLAMP} Generator, Digital controller, Oscillator, OTP, OCD, UVP and other sub-modules.

Gain Setting via GAIN0 and GAIN1 Inputs and Selection of C_{IN}

The gain can be selected to 20, 26, 32, and 36 dB utilizing the GAIN0 and GAIN1 gain select pins. The gains listed in the following table are realized by changing the taps on the input resistors and feedback resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance from part-to-part at the same gain may shift by ±20% due to shifts in the actual resistance of the input resistors.

Input capacitor C_I is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. C_I and the input impedance of the amplifier (Z_I) form a high-pass filter. The value of C_I is important, as it directly affects the bass (low-frequency) performance of the circuit. The value of C1 should assure a flat bass response down to 20Hz as following table.

A low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages, and it is important to ensure that boards are cleaned properly.

GAIN1	GAIN0	Gain	Input Impedance	C_{IN}(Min.)
L	L	20dB	60KΩ	0.22μF
L	H	26dB	30KΩ	0.33μF
H	L	32dB	15KΩ	0.68μF
H	H	36dB	9KΩ	1μF

Advised value of C1 is 1μF。

SE and BTL Configuration and the selection of peripheral components

As shown in the following figure, there are two main configurations that may be used. For stereo operation, the A2410 should be configured in a single-ended (SE) half-bridge amplifier. For mono applications, A2410 may be used as a bridge-tied-load (BTL) amplifier. The main difference between the two applications is the external filter is different from the rest of the same peripheral device. The same peripheral components include C_{BYPASS} for hold a common mode voltage, C_S for Power-Supply decoupling, bootstrap capacitors C_{BS}, VCLAMP capacitor C_{VCLAMP}.

The external capacitor CBYP is a critical component and serves several important functions. During start-up or recovery from shutdown mode, CBYP determines the rate at which the amplifier starts. The circuit is designed for a CBYP value of 1μF for best pop performance. A ceramic or tantalum low-ESR capacitor is recommended.

V_{CC} power supply terminal must be added to 0.1μF, 1μF, 10μF and two 470μF C_S to ground (placed as close as possible to the device V_{CC} lead works best.) to reduce the impact of power disturbances on the output.

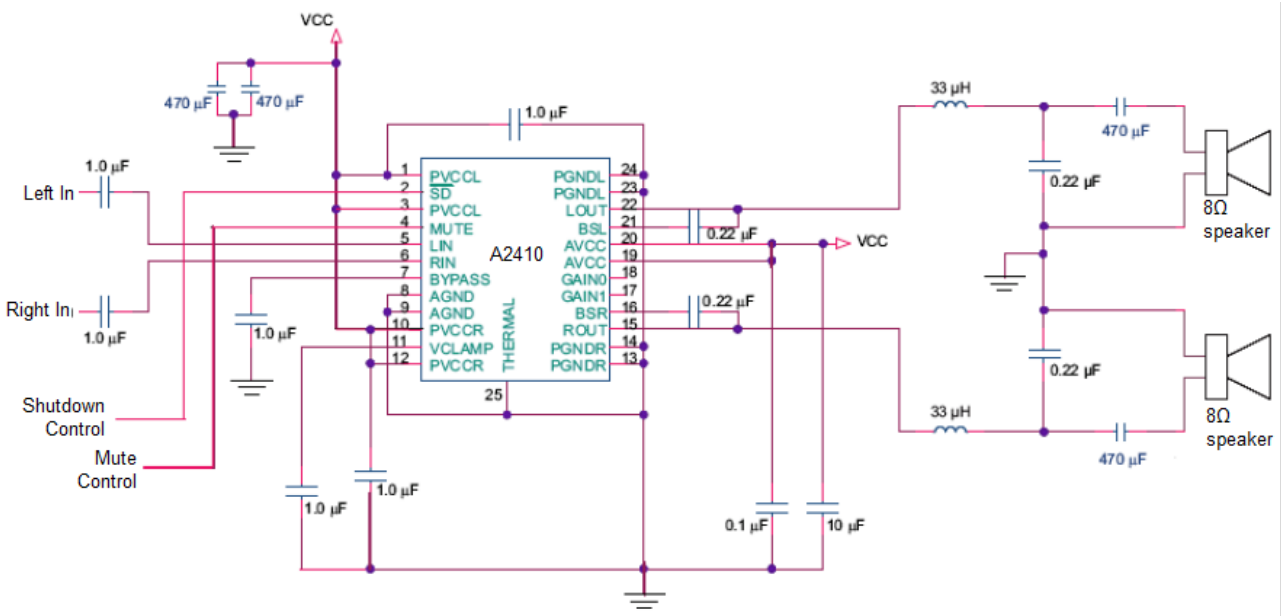
The half H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 220nF ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding bootstrap input. Specifically, one 220nF capacitor must be connected from L_{OUT} to BSL, and one 220nF capacitor must be connected from R_{OUT} to BSR.

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 1μF capacitor must be connected from V_{CLAMP} (pin11) to ground and must be rated for at least 16V.

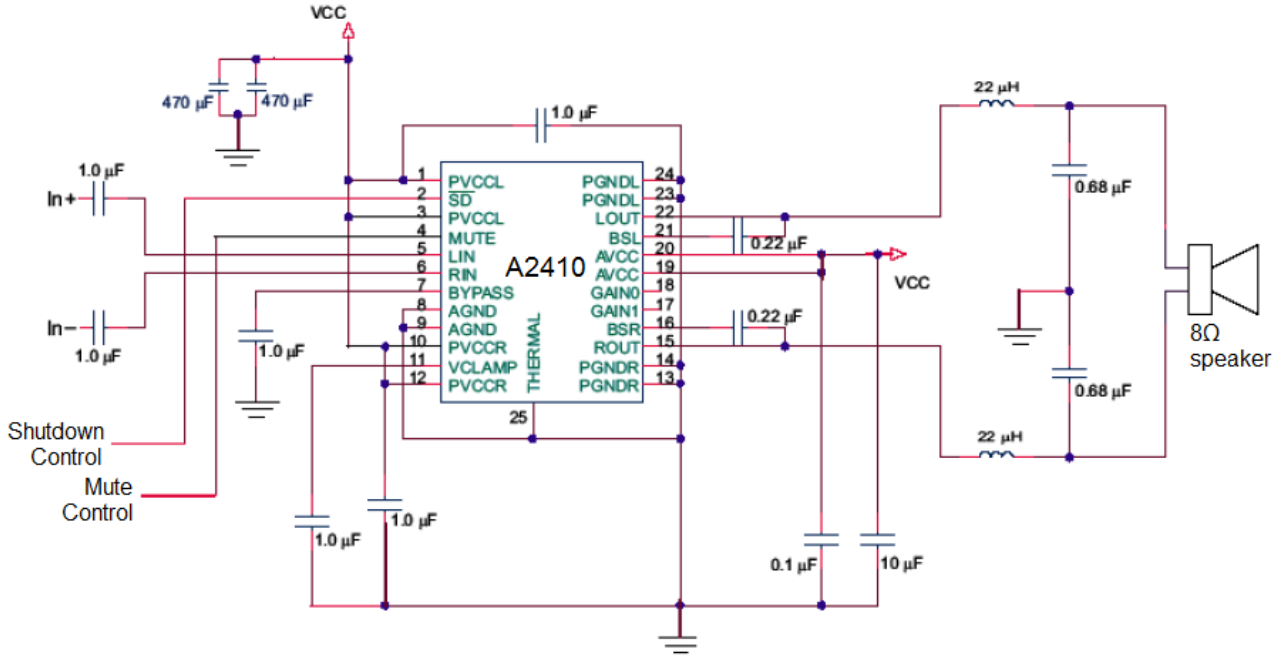
For the best frequency response, a flat-passband output filter (second-order Butterworth) may be used. The output filter components consist of the series inductor and capacitor to ground at the L_{OUT} and R_{OUT} pins. There are several possible configurations, depending on whether the output configuration is single-ended (SE)

or bridge-tied load (BTL). SE single-ended configuration for each channel using a 33μH inductance, a 0.22μF and a 470μF capacitor. The BTL bridge configuration uses two 22μH inductor, two 0.68μF capacitors.

NOTICE: in order to ensure the smaller POP-CLICK noise, it is recommended to start the frontend circuit to establish the DC operating point, and then cancel the SHUTDOWN state of A2410.



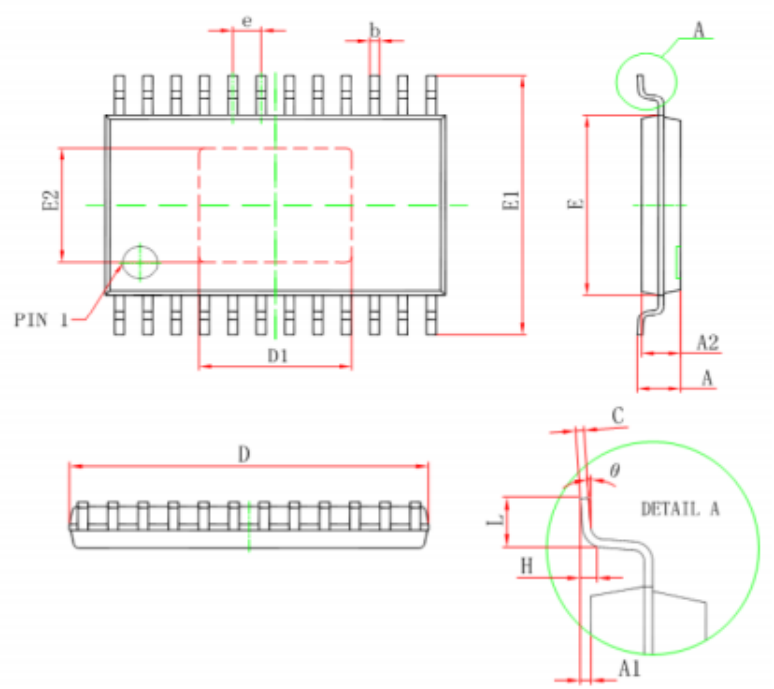
A2410 Single-Ended (SE) Application Schematic



A2410 Bridge-Tie-Load (BTL) Application Schematic

PACKAGE INFORMATION

Dimension in P-TSSOP24 Package (Unit: mm)



Symbol	Min	Max
D	7.700	7.900
D1	3.400	3.600
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A	-	1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65 (BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°

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