DESCRIPTION

A24C02 provides 2048 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 256 words of 8 bits each.
The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.
The A24C02 is accessed via a two-wire serial interface.
The A24C02 is available in TSOT-25, SOP8, DFN8 and TSSOP8 Packages.

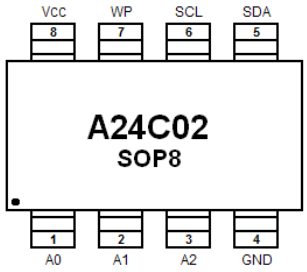
FEATURES

- Two-wire Serial Interface
- V_{CC} = 1.8V to 5.5V
- Bi-directional Data Transfer Protocol
- Internally Organized
  A24C02, 256X8(2Kbits)
- 1 MHz (5V), 400 kHz (1.8V, 2.5V, 2.7V) Compatibility
- 8-byte Page (2K) Write Modes
- Self-timed Write Cycle (5 ms max)
- 1 Million Write Cycles guaranteed
- Data Retention > 100 Years
- Operating Temperature: -40℃ to +85℃
- Available in TSOT-25, SOP8, DFN8 and TSSOP8 Package

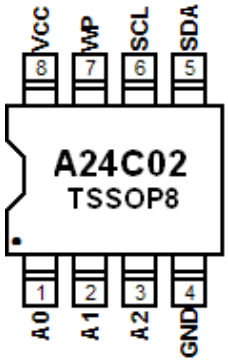
ORDERING INFORMATION

Package Type	Part Number			
TSOT-25	TE5	A24C02TE5R	Tape & Reel	Pb Free
		A24C02TE5VR	Tape & Reel	Green
SOP8	M8	A24C02M8R	Tape & Reel	Pb Free
		A24C02M8U	Tube	Pb Free
		A24C02M8VR	Tape & Reel	Green
		A24C02M8VU	Tube	Green
TSSOP8	TMX8	A24C02TMX8R	Tape & Reel	Pb Free
		A24C02TMX8U	Tube	Pb Free
		A24C02TMX8VR	Tape & Reel	Green
		A24C02TMX8VU	Tube	Green
DFN8	J8	A24C02J8R	Tape & Reel	Pb Free
		A24C02J8VR	Tape & Reel	Green
Note	R: Tape & Reel , T: Tube, V: Green Package			
AiT provides all Pb free products, suffix " V " means Green Package				

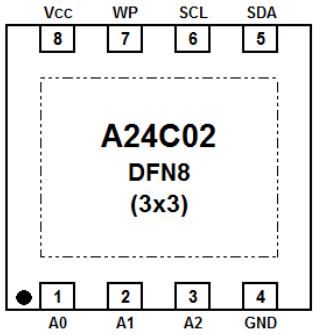
PIN DESCIPTION



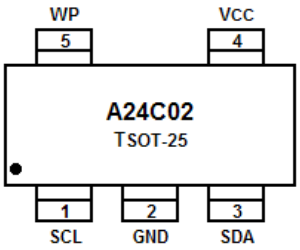
Top View



Top View



Top View



Top View

Pin #				Symbol	Functions
SOP8	TSSOP8	DFN8	TSOT-25		
1	1	1	-	A0	Address Input
2	2	2	-	A1	Address Input
3	3	3	-	A2	Address Input
4	4	4	2	GND	Ground
5	5	5	3	SDA	Serial Data
6	6	6	1	SCL	Serial Clock Input
7	7	7	5	WP	Write Protect
8	8	8	4	V_{CC}	Power Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V to +6.5V
Input / Output Voltage	GND-0.3V to Vcc+0.3V
Operating Ambient Temperature	-40℃ to +85℃
Storage Temperature	-65℃ to +150℃

Stresses above may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Applicable over recommended operating range from: T_A=-40℃ to +85℃, V_{CC} =+1.8V to +5.5V (unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
DC Electrical Characteristics						
Supply Voltage	V_{CC}		1.8	-	5.5	V
Supply Current V_{CC}=5.0V	I_{CC1}	READ at 100kHz	-	0.4	1.0	mA
Supply Current V_{CC}=5.0V	I_{CC2}	WRITE at 100kHz	-	2.0	3.0	mA
Standby Current	I_{SB}	V_{IN}=V_{CC} or GND	-	-	1.0	μA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or GND	-	-	3.0	μA
Output Leakage Current	I_{LO}	V_{OUT}=V_{CC} or GND	-	0.05	3.0	μA
Input Low Level	V_{IL}		-0.6	-	V_{CC}×0.3	V
Input High Level	V_{IH}		V_{CC}×0.7	-	V_{CC}+0.5	V
Output Low Level V_{CC}=5.0V	V_{OL3}	I_{OL}=3.0mA	-	-	0.4	V
Output Low Level V_{CC}=3.0V	V_{OL2}	I_{OL}=2.1mA	-	-	0.4	V
Output Low Level V_{CC}=1.8V	V_{OL1}	I_{OL}=0.15mA	-	-	0.2	V

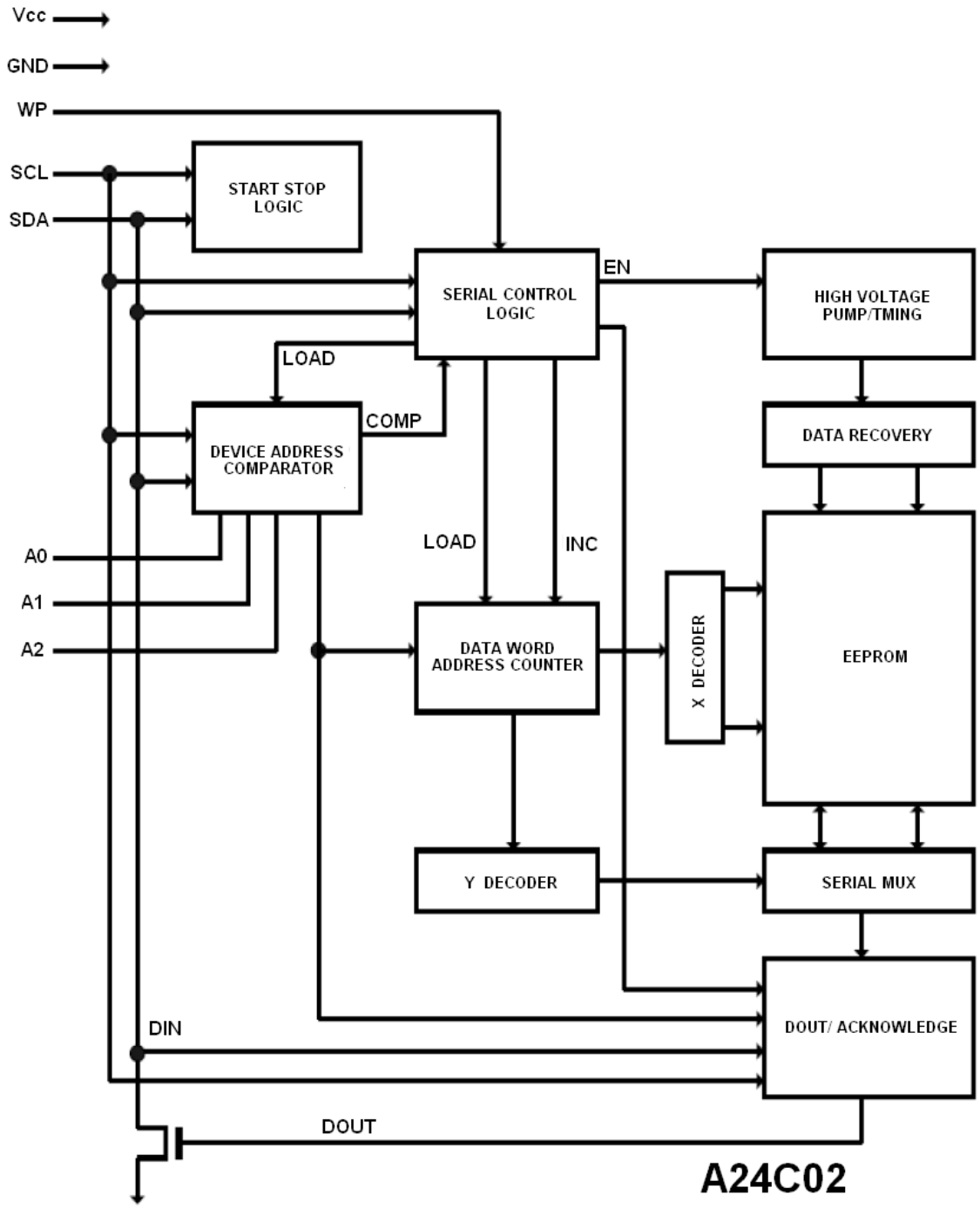
Applicable over recommended operating range from T_A=25℃,f=1.0 MHz, VCC=+1.8V

Parameter	Symbol	Conditions	Min	Typ.	Max	Units
Pin Capacitance						
Input/ Output Capacitance(SDA)	$C_{I/O}$	$V_{I/O}$=0V	-	-	8	pF
Input Capacitance (A0,A1,A2,SCL)	C_{IN}	V_{IN}=0V	-	-	6	pF

Applicable over recommended operating range from T_A=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V, CL=1 TTL Gate and 100 pF (unless otherwise noted)

Parameter	Symbol	1.8-volt			5.0-volt			Units
		Min	Typ.	Max	Min	Typ.	Max	
AC Electrical Characteristics								
Clock Frequency, SCL	f_{SCL}	-	-	400	-	-	1000	kHz
Clock Pulse Width Low	t_{LOW}	1.2	-	-	0.6	-	-	μs
Clock Pulse Width High	t_{HIGH}	0.6	-	-	0.4	-	-	μs
Noise Suppression Time	t_I	-	-	50	-	-	40	μs
Clock Low to Data Out Valid	t_{AA}	0.05	-	0.9	0.05	-	0.55	μs
Time the bus must be free before a new transmission can start	t_{BUF}	1.2	-	-	0.5	-	-	μs
Start Hold Time	$t_{HD.STA}$	0.6	-	-	0.25	-		μs
Start Setup Time	$t_{SU.STA}$	0.6	-	-	0.25	-	-	μs
Data In Hold Time	$t_{HD.DAT}$	0	-	-	0	-	-	μs
Data In Setup Time	$t_{SU.DAT}$	100	-	-	100	-	-	ns
Inputs Rise Time	t_R	-	-	0.3	-	-	0.3	μs
Inputs Fall Time	t_F	-	-	300	-	-	100	ns
Stop Setup Time	$t_{SU.STO}$	0.6	-	-	0.25	-	-	μs
Data Out Hold Time	t_{DH}	50	-	-	50	-	-	ns
Write Cycle Time	t_{WR}	-	-	5	-	-	5	ms
5.0V, 25℃, Byte Mode	Endurance	1M	-	-	-	-	-	Write Cycles

BLOCK DIAGRAM



DETAILED INFORMATION

DEVICE/PAGE ADDRESSES (A2, A1 and A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the A24C02. Eight 2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The A24C02 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following Table.

WP PIN STATUS	PARTS OF THE ARRAY PROTECTED
	A24C02
At V_{CC}	Full (2K) Array
At GND	Normal Read/Write Operations

1. MEMORY ORGANIZATION

   A24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

2. DEVICE OPERATION

   CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see to Figure 1 on page 8). Data changes during SCL high periods will indicate a start or stop condition as defined below.

   START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see to Figure 2 on page 9).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2 on page 9).

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a "0" to acknowledge that it has received each word. This happens during the ninth clock cycle. STANDBY MODE: The A24C02 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

Figure 1: DATA VALIDITY

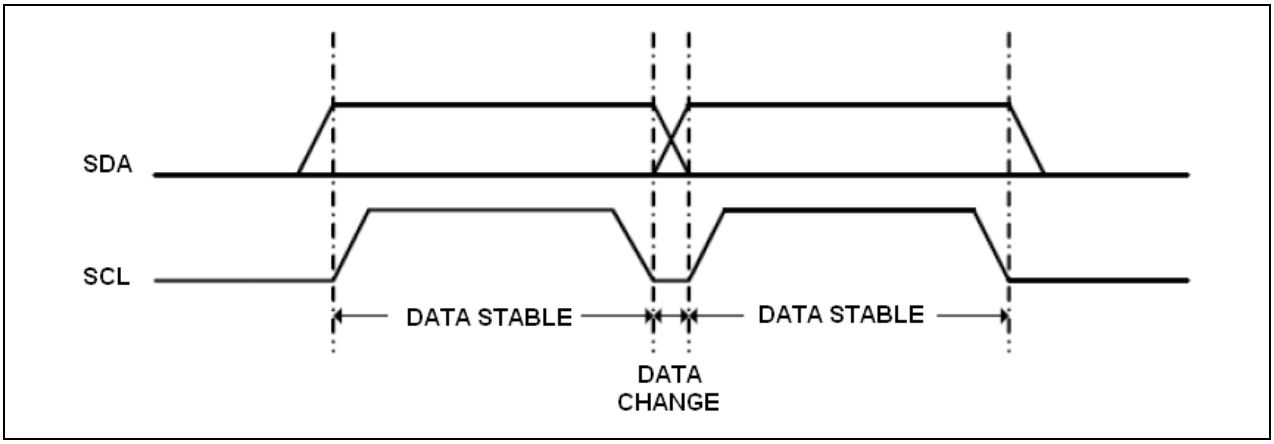


Figure 2: START AND STOP DEFINITION

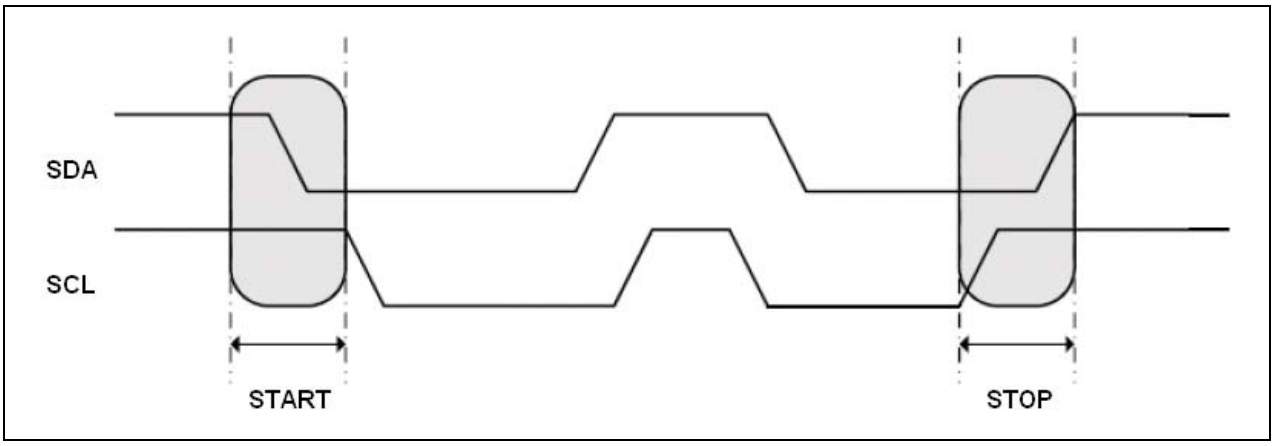
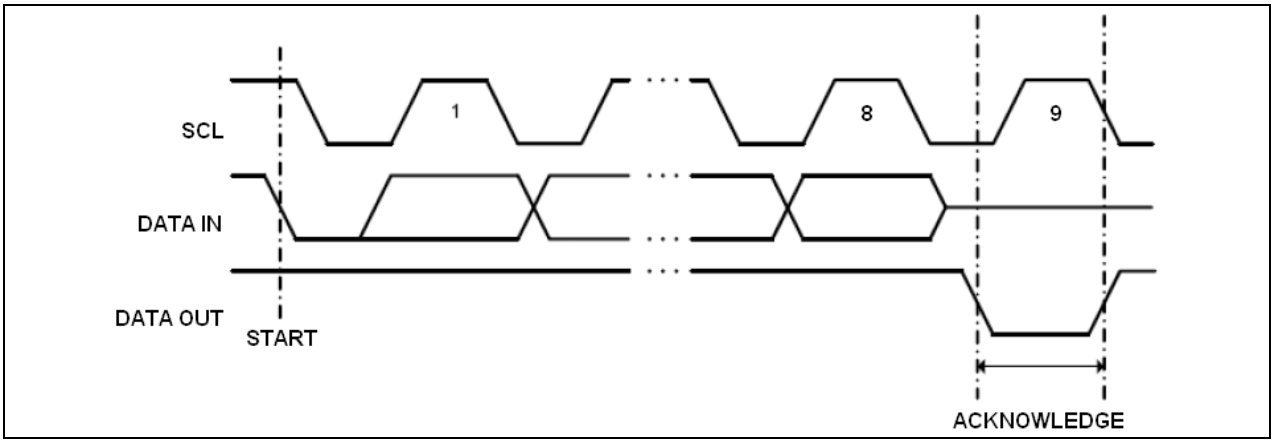


Figure 3: OUTPUT ACKNOWLEDGE



3. DEVICE ADDRESSING

The 2K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see to Figure 4 on page 12).

The device address word consists of a mandatory "1", "0" sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The next 3 bits are the A2, A1 and A0 device address bits for the 2K EEPROM. These 3 bits must compare to their corresponding hardwired input pins.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a "0". If a compare is not made, the chip will return to a standby state.

4. WRITE OPERATIONS

BYTE WRITE: A write operation requires an 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a "0" and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a "0" and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, t_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5 on page 12).

PAGE WRITE: The 2K EEPROM is capable of an 8-byte page write. A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to seven (2K) data words. The EEPROM will respond with a "0" after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6 on page 12).

The data word address lower three (2K) is internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than eight (2K) data words are transmitted to the EEPROM, the data word address will "roll over" and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. READ OPERATIONS

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7 on page 13).

6. Read Operations

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 8 on page 13).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9 on page 14).

Figure 4: DEVICE ADDRESS

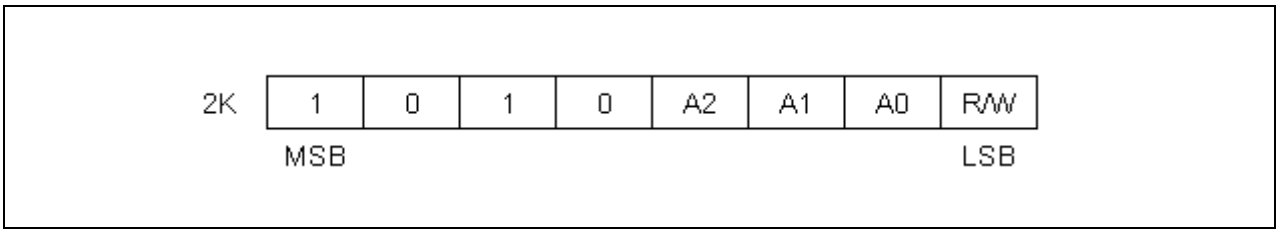


Figure 5: BYTE WRITE

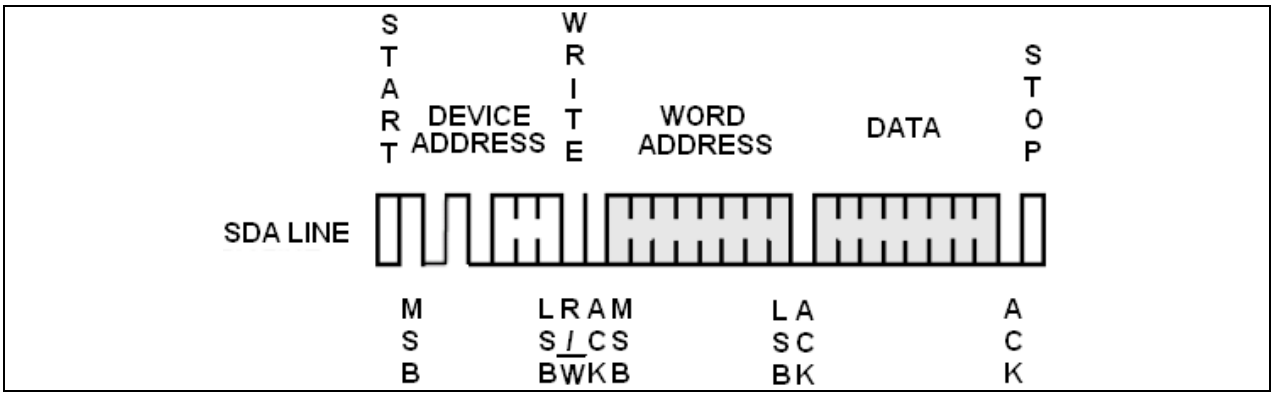


Figure 6: PAGE WRITE

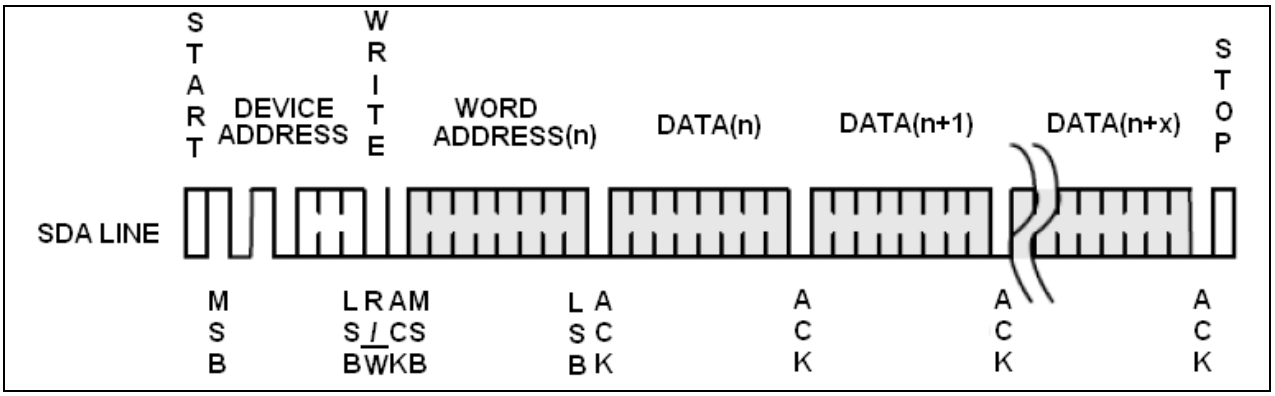


Figure 7: CURRENT ADDRESS READ

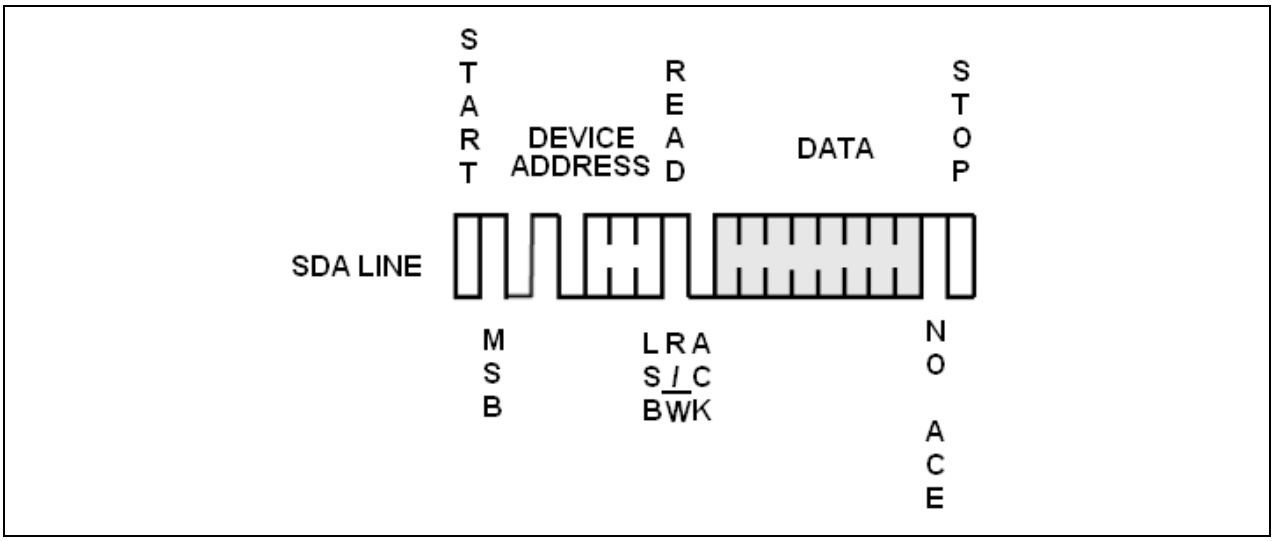


Figure 8: RANDOM READ

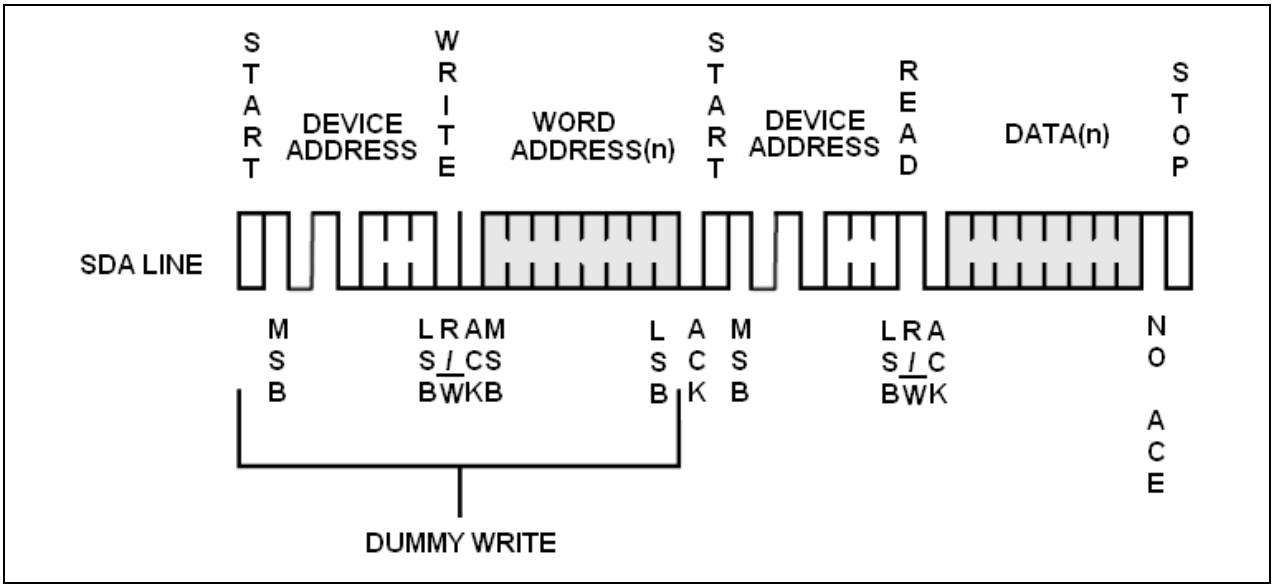
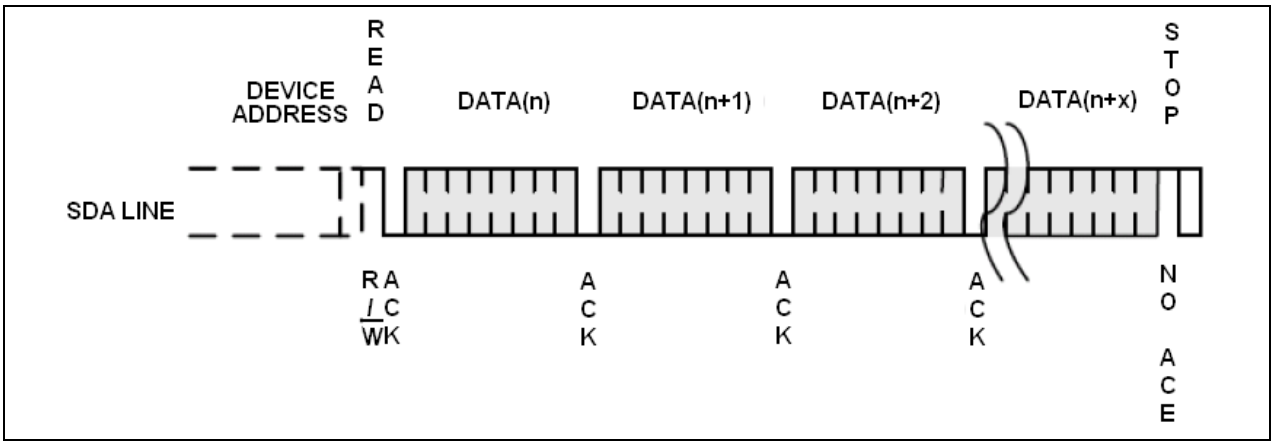
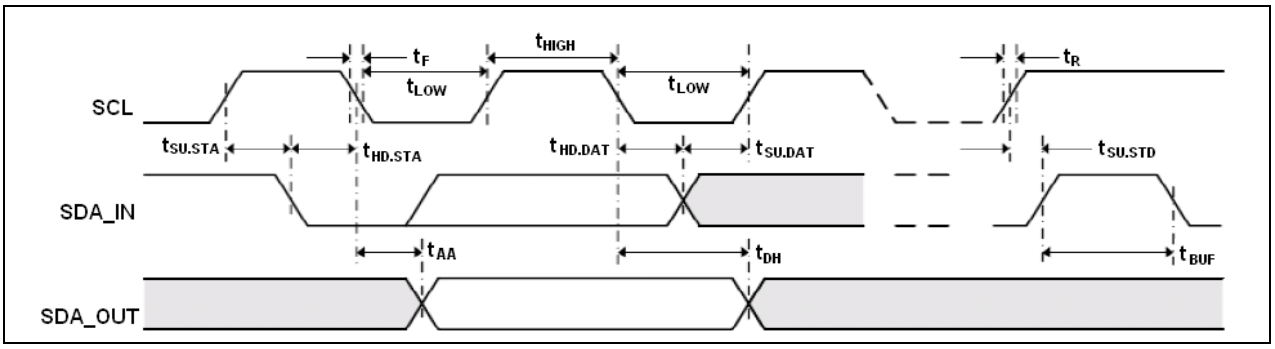


Figure 9: SEQUENTIAL READ



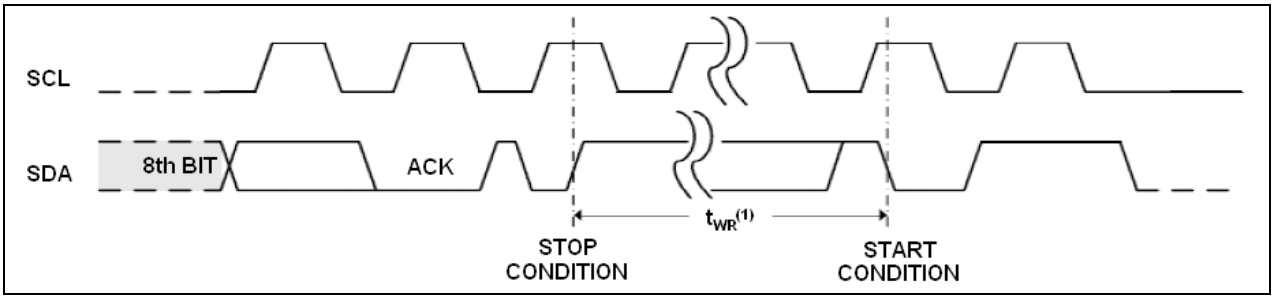
7. BUS TIMING

Figure 10: SCL: SERIAL CLOCK, SDA: SERIAL DATA I/O



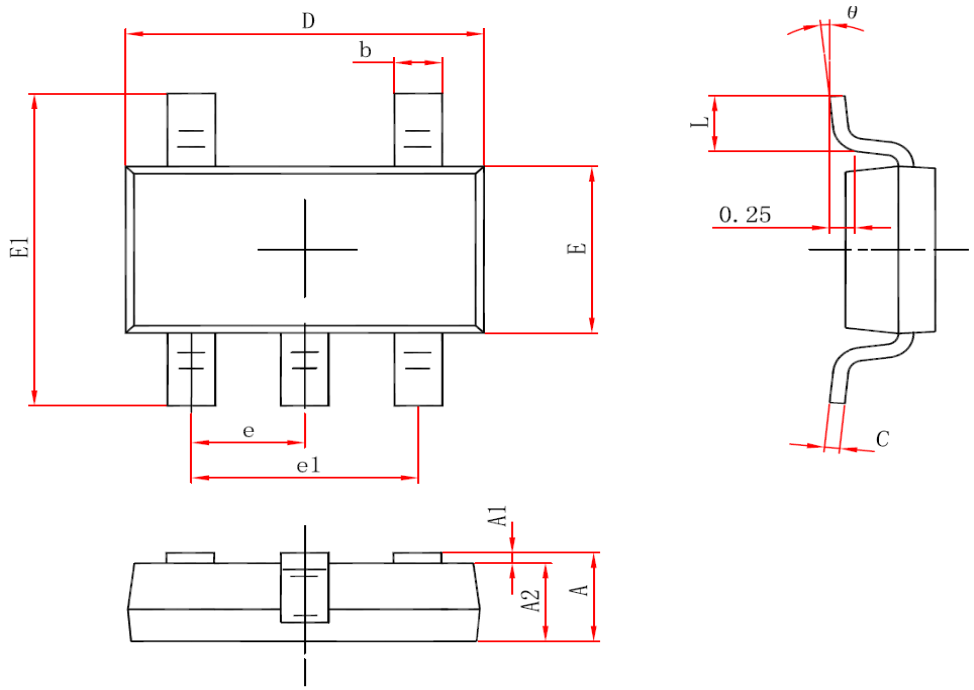
8. WRITE CYCLE TIMING

Figure 11: SCL: SERIAL CLOCK, SDA: SERIAL DATA I/O



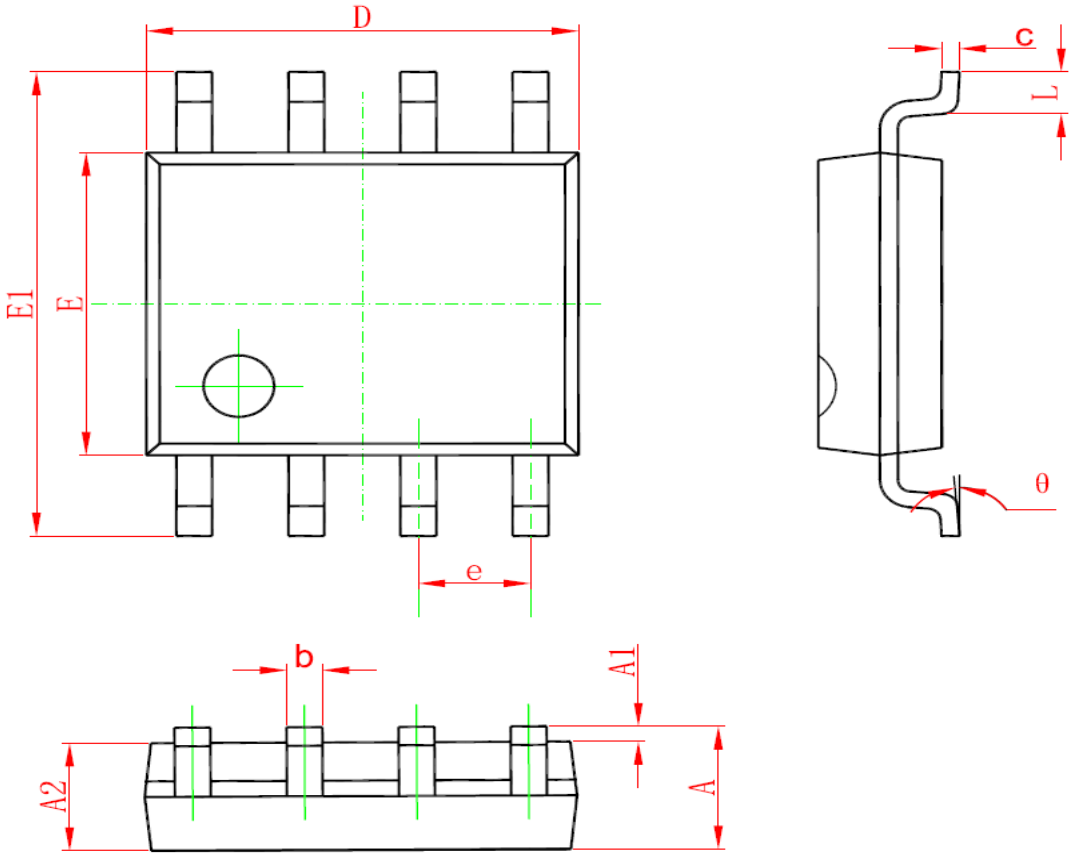
PACKAGE INFORMATION

Dimension in TSOT-25 (Unit: mm)



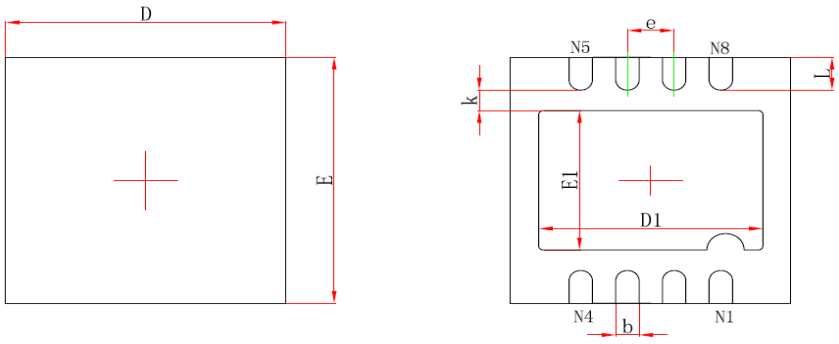
Symbol	Min	Max
A	0.700	0.900
A1	0.000	0.100
A2	0.700	0.800
b	0.350	0.500
c	0.080	0.200
D	2.820	3.020
E	1.600	1.700
E1	2.650	2.950
e	0.95(BSC)	
e1	1.90(BSC)	
L	0.300	0.600
θ	0°	8°

Dimension in SOP8 (Unit: mm)

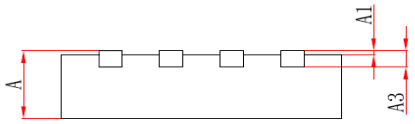


Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.330	0.510
c	0.170	0.250
D	4.700	5.100
E	3.800	4.000
E1	5.800	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

Dimension in DFN8 (Unit: mm)



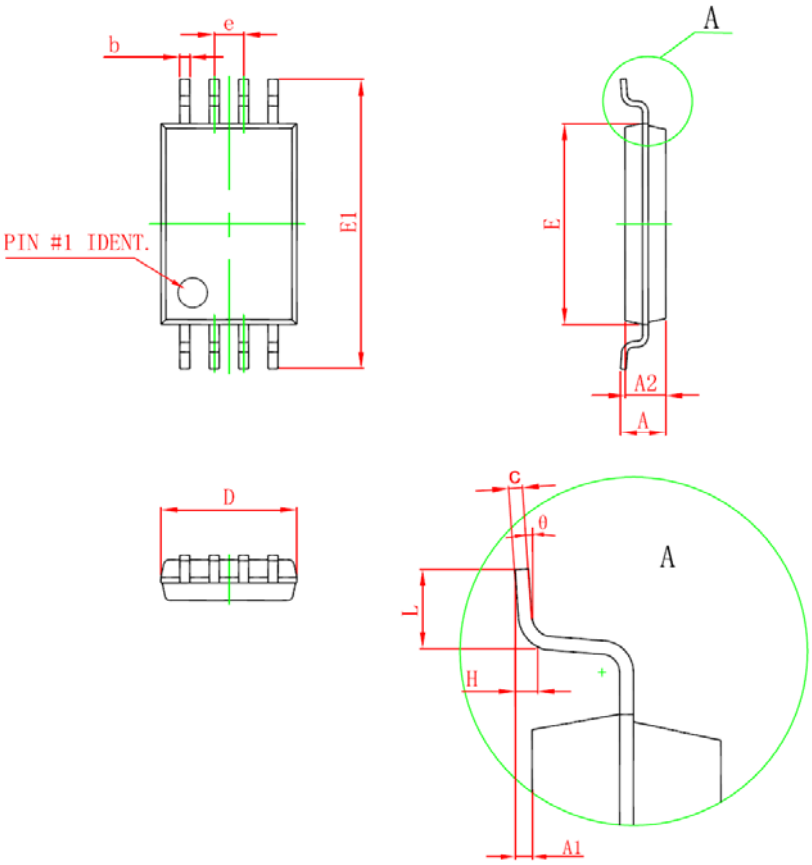
Top View **Bottom View**



Side View

Symbol	Min	Max
A	0.700/0.800	0.800/0.900
A1	0.000	0.050
A3	0.203REF.	
D	2.900	3.100
E	2.900	3.100
D1	2.300	2.500
E1	1.600	1.800
k	0.200MIN.	
b	0.180	0.300
e	0.500TYP.	
L	0.300	0.500

Dimension in TSSOP8 Package (Unit: mm)



Symbol	Min	Max
D	2.900	3.100
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.250	6.550
A	-	1.100
A2	0.800	1.000
A1	0.020	0.150
e	0.65 (BSC)	
L	0.500	0.700
H	0.25(TYP)	
θ	1°	7°

IMPORTANT NOTICE

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