DESCRIPTION

A24C128 provides 131,072 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 16,384 words of 8 bits each.

The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operations are essential.

The A24C128 is available SOP8 and TSSOP8 Package.

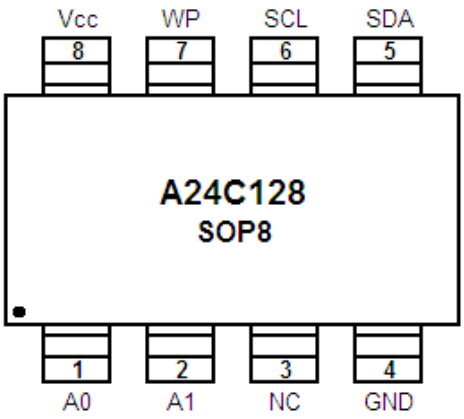
FEATURES

- Two-Wire Serial Interface
- V_{CC}=1.8V To 5.5V
- Bi-Directional Data Transfer Protocol
- Internal Organized
  A24C128, 16,384 X 8 (128K bits)
- 400KHz (1.8V, 2.5V & 2.7V) Compatibility
- 64-byte (128K) Page Write Mode
- Partial Page Writes Allowed
- Self-Timed Write Cycle (5ms Max)
- High-Reliability
- 1 Million Write Cycles guaranteed
- Data Retention > 100 Years
- Operating Temperature: -40°C to +85°C
- Available in SOP8 and TSSOP8 Package

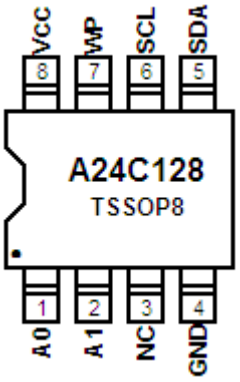
ORDERING INFORMATION

Package Type	Part Number	
SOP8	M8	A24C128M8R
		A24C128M8U
		A24C128M8VR
		A24C128M8VU
TSSOP8	TMX8	A24C128TMX8R
		A24C128TMX8U
		A24C128TMX8VR
		A24C128TMX8VU
Note	R: Tape & Reel U: Tube V: Halogen free Package	
AiT provides all RoHS products suffix " V " means Halogen free Package		

PIN DESCIPTION



Top View



Top View

Pin #		Symbol	Type	Functions
SOP8	TSSOP8			
1	1	A0	I	Address Input
2	2	A1	I	Address Input
3	3	NC	NC	No Connection
4	4	GND	P	Ground
5	5	SDA	I/O & Open-drain	Serial Data
6	6	SCL	I	Serial Clock Input
7	7	WP	I	Write Protect
8	8	V_{CC}	P	Power Supply

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage	-0.3V ~ +6.5V
Input / Output Voltage	GND-0.3V ~ V_{CC} +0.3V
Operating Ambient Temperature	-40℃ ~ +85℃
Storage Temperature	-55℃ ~ +125℃

Stresses above those listed under" Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other condition above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

PIN CAPACITANCE

T_A=25°C, f=1.0MHz, V_{CC}=+1.8V

PARAMETER	SYMBOL	MAX	UNIT	CONDITION
Input / Output Capacitance (SDA)	$C_{I/O}$	8	pF	$V_{I/O}$=0V
Input Capacitance (A0, A1, SCL)	C_{IN}	6	pF	V_{IN}=0V

DC ELECTRICAL CHARACTERISTICS

T_A=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V (Unless otherwise specified.)

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Supply Voltage	V_{CC1}		1.8	-	5.5	V
Supply Voltage	V_{CC2}		2.5	-	5.5	V
Supply Voltage	V_{CC3}		2.7	-	5.5	V
Supply Voltage	V_{CC4}		4.5	-	5.5	V
Supply Current V_{CC}=5.0V	I_{CC1}	Read at 400KHz		0.4	1.0	mA
Supply Current V_{CC}=5.0V	I_{CC2}	Write at 400KHz		2.0	3.0	mA
Supply Current V_{CC}=1.8V	I_{CC1}	V_{IN}=V_{CC} or V_{SS}		0.6	1.0	uA
Supply Current V_{CC}=2.5V	I_{CC2}	V_{IN}=V_{CC} or V_{SS}		1.0	2.0	uA
Supply Current V_{CC}=2.7V	I_{CC3}	V_{IN}=V_{CC} or V_{SS}		1.0	2.0	uA
Supply Current V_{CC}=5.0V	I_{CC4}	V_{IN}=V_{CC} or V_{SS}		1.0	5.0	uA
Input Leakage Current	I_{LI}	V_{IN}=V_{CC} or V_{SS}		0.10	3.0	uA
Output Leakage Current	I_{LO}	V_{OUT}= V_{CC} or V_{SS}		0.05	3.0	uA
Input Low Level	V_{IL}		-0.6	-	V_{CC} x 0.3	V
Input High Level	V_{IH}		V_{CC} x0.7	-	V_{CC}+0.5	V
Output Low Level V_{CC}=5.0V	V_{OL3}	I_{OL}=3.0mA		-	0.4	V
Output Low Level Vcc=3.0V	V_{OL2}	I_{OL}=2.1mA		-	0.4	V
Output Low Level Vcc=1.8V	V_{OL1}	I_{OL}=0.15mA		-	0.2	V

AC ELECTRICAL CHARACTERISTICS

T_A=-40℃ to +85℃, V_{CC}=+1.8V to +5.5V, C_L=1 TTL gate and 100pF, unless otherwise specified.

Parameter	Symbol	1.8-volt			5.0-volt			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
Clock Frequency, SCL	f_{SCL}			400			400	KHz
Clock Pulse Width Low	t_{LOW}	1.2		-	0.6		-	us
Clock Pulse Width High	t_{HIGH}	0.6		-	0.4		-	us
Noise Suppression Time	t_I	-		50			50	ns
Clock Low to Data Out Valid	t_{AA}	0.1		0.9	0.05		0.9	us
Time the bus must be free before a new transmission can start	t_{BUF}	1.2		-	0.5		-	us
Start Hold Time	$t_{HD.STA}$	0.6		-	0.25		-	us
Start Setup Time	$t_{SU.STA}$	0.6		-	0.25		-	us
Data In Hold Time	$t_{HD.DAT}$	0		-	0		-	us
Data In Setup Time	$t_{SU.DAT}$	100		-	100		-	ns
Inputs Rise Time	t_R	-		0.3			0.3	us
Inputs Fall Time	t_F	-		300			300	ns
Stop Setup Time	$t_{SU.STO}$	0.6		-	0.25		-	us
Data Out Hold Time	t_{DH}	50		-	50		-	ns
Write Cycle Time	t_{WR}	-		5			5	ms
5.0V, 25°C, Byte Mode	Endurance	1M		-			-	Write Cycles

NOTE: 1. This parameter is characterized and is not 100% tested.

2. AC measurement conditions: R_L(connects to V_{CC}): 1.3KΩ(2.5V,5V),10KΩ(1.8V)

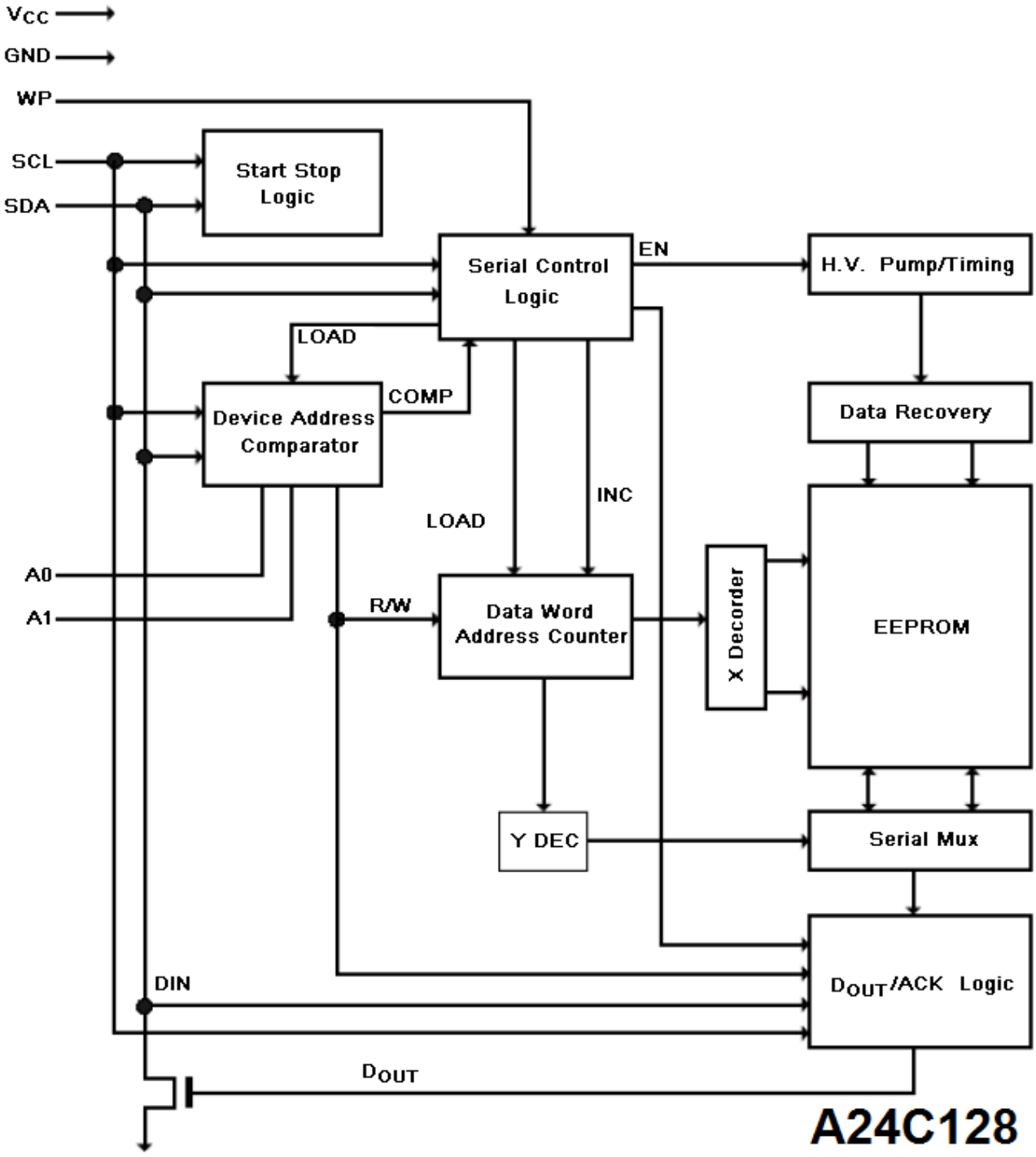
Input pulse voltages: 0.3V_{CC} to 0.7V_{CC}

Input rise and fall time: ≤50ns

Input and output timing reference voltages: 0.5V_{CC}

The value of R_L should be concerned according to the actual loading on the user's system.

BLOCK DIAGRAM



DETAILED INFORMATION

DEVICE/PAGE ADDRESSES (A1 and A0): The A1 and A0 pins are device address inputs that are hard wired for the A24C128. Four 128k devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open- collector devices.

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

WRITE PROTECT (WP): The A24C128 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following Table 1.

Table1: Write Protect

WP PIN STATUS	PARTS OF THE ARRAY PROTECTED
	A24C128
At V_{CC}	Full (128K) Array
At GND	Normal Read/Write Operations

FUNCTIONAL DESCRIPTION

1. Memory Organization

The 128K is internally organized as 256 pages of 64 bytes each. Random word addressing requires a 14-bit data word address.

2. Device Operation

CLOCK and DATA TRANSITIONS: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods (see Figure 1 on page 11). Data changes during SCL high periods will indicate a start or stop condition as defined below.

START CONDITION: A high-to-low transition of SDA with SCL high is a start condition which must precede any other command (see Figure 2 on page 11).

STOP CONDITION: A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (see Figure 2 on page 11)

ACKNOWLEDGE: All addresses and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a “0” to acknowledge that it has received each word. This happens during the ninth clock cycle.

STANDBY MODE: The A24C128 features a low-power standby mode which is enabled: (a) upon power-up and (b) after the receipt of the STOP bit and the completion of any internal operations

MEMORY RESET: After an interruption in protocol, power loss or system reset, any two-wire part can be reset by following these steps:

1. Clock up to 9 cycles.
2. Look for SDA high in each cycle while SCL is high.
3. Create a start condition.

3. Device Addressing

The 128K EEPROM devices all require an 8-bit device address word following a start condition to enable the chip for a read or write operation (see Figure 4 on page 12).

The device address word consists of a mandatory “1”, “0” sequence for the first four most significant bits as shown. This is common to all the Serial EEPROM devices.

The 128K uses the three device address bits A1, A0 to allow as many as four devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A1 and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a “0”. If a compare is not made, the chip will return to a standby state.

DATA SECURITY: The A24C128 has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

4. Write Operations

BYTE WRITE: A write operation requires two 8-bit data word address following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a “0” and then clock in the first 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a “0” and the addressing device, such as a microcontroller, must terminate the write sequence with a stop condition. At this time the EEPROM enters an internally timed write cycle, T_{WR}, to the nonvolatile memory. All inputs are disabled during this write cycle and the EEPROM will not respond until the write is complete (see Figure 5, on page 12).

PAGE WRITE: The 128K devices are capable of 64-byte page writes.

A page write is initiated the same as a byte write, but the microcontroller does not send a stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 63 more data words. The EEPROM will respond with a “0” after each data word received. The microcontroller must terminate the page write sequence with a stop condition (see Figure 6 on page 12).

The data word address lower six (128K) bits are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 64 data words are transmitted to the EEPROM, the data word address will “roll over” and previous data will be overwritten.

ACKNOWLEDGE POLLING: Once the internally timed write cycle has started and the EEPROM inputs are disabled, acknowledge polling can be initiated. This involves sending a start condition followed by the device address word. The read/write bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a "0", allowing the read or write sequence to continue.

5. Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to "1". There are three read operations: current address read, random address read and sequential read.

CURRENT ADDRESS READ: The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address "roll over" during read is from the last byte of the last memory page to the first byte of the first page. The address "roll over" during write is from the last byte of the current page to the first byte of the same page.

Once the device address with the read/write select bit set to "1" is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out. The microcontroller does not respond with an input "0" but does generate a following stop condition (see Figure 7 on page 13).

RANDOM READ: A random read requires a "dummy" byte write sequence to load in the data word address. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 9 on page 13).

SEQUENTIAL READ: Sequential reads are initiated by either a current address read or a random address read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will "roll over" and the sequential read will continue. The sequential read operation is terminated when the microcontroller does not respond with a "0" but does generate a following stop condition (see Figure 10 on page 14)

Figure 1 Data Validity

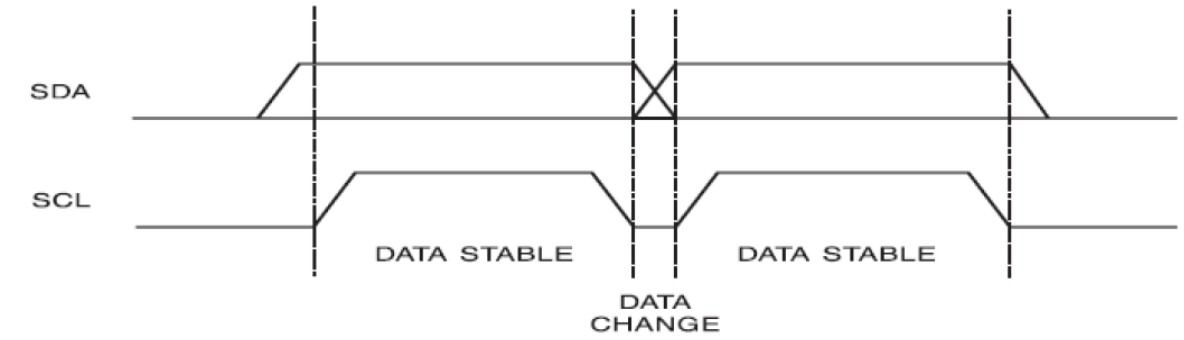


Figure 2 Start and Stop Definition

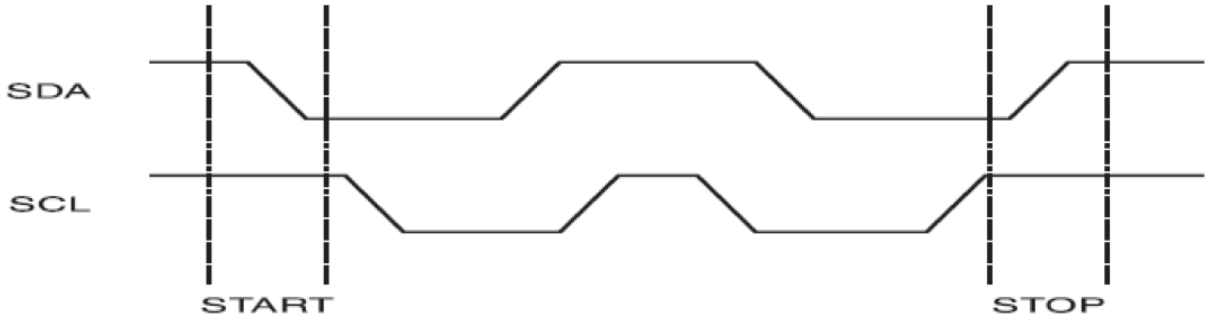


Figure 3 Output Acknowledge

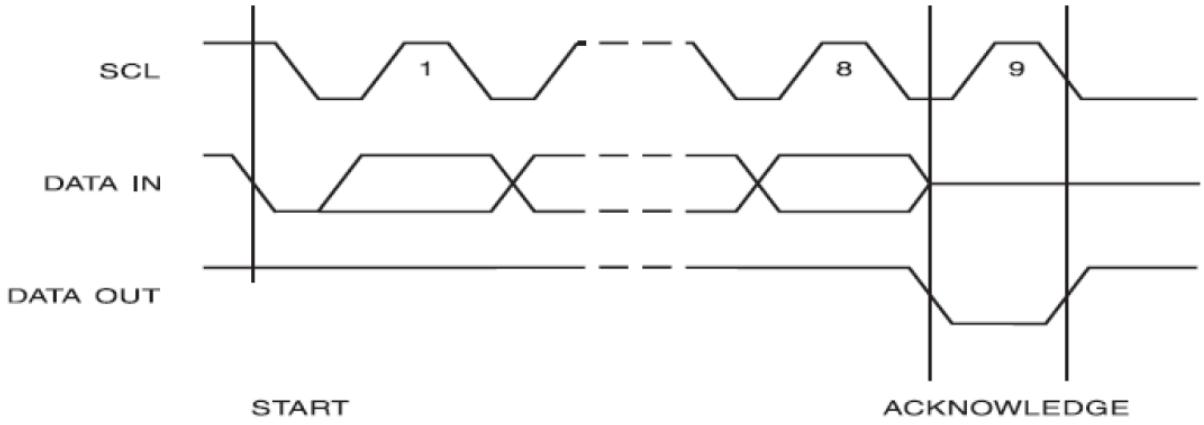


Figure 4 Device Address

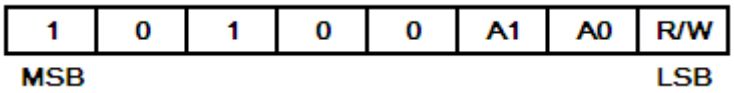


Figure 5 Byte Write

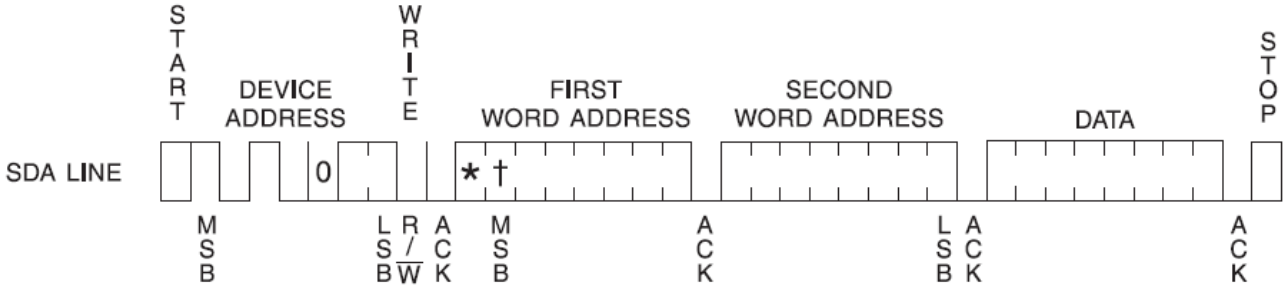


Figure 6 Page Write

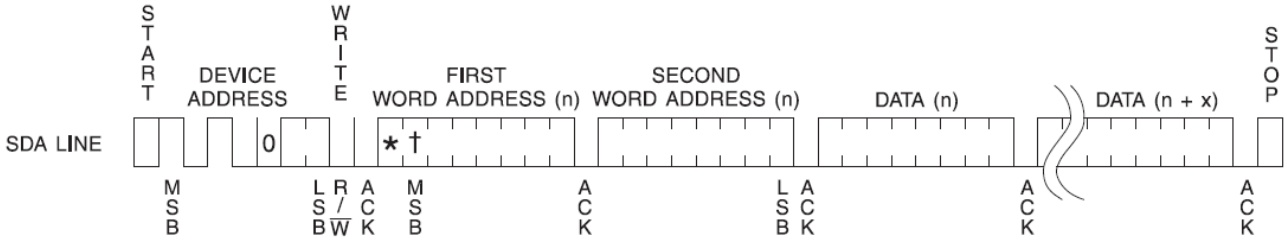


Figure 7 Current Address Read

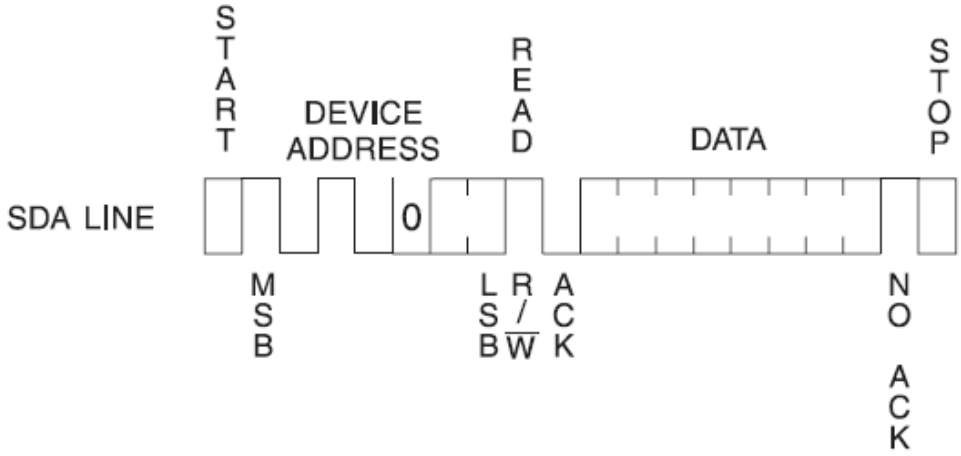
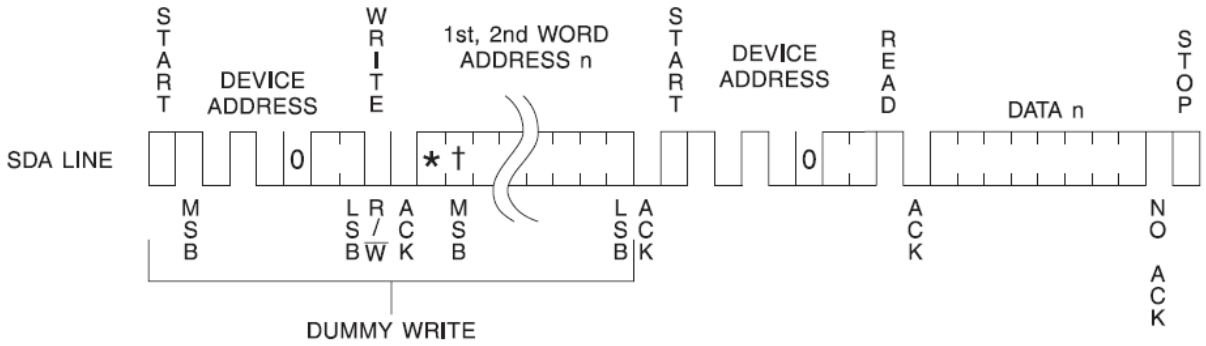
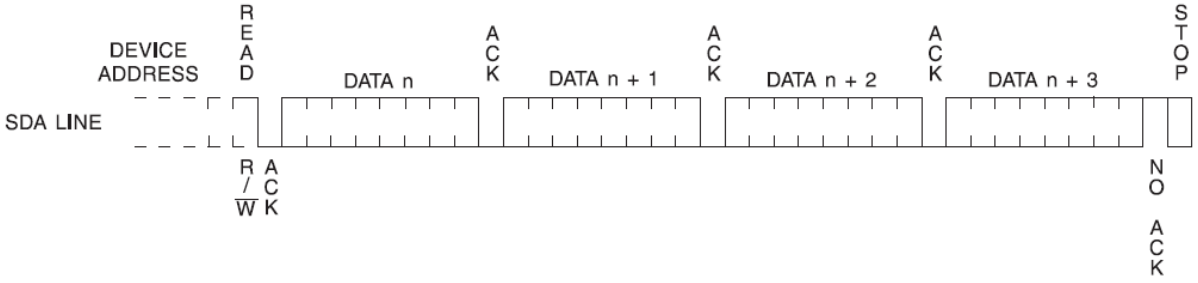


Figure 8 Random Read



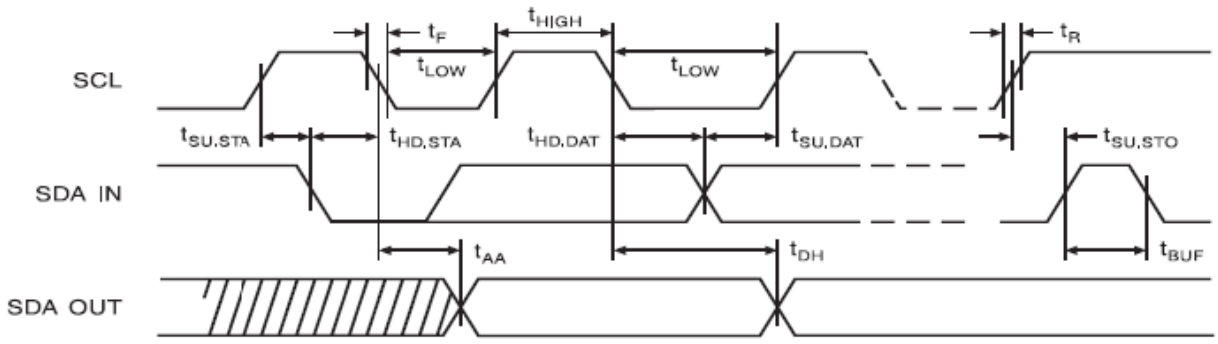
(* = DON'T CARE bit)
(† = DON'T CARE bit for the 128K)

Figure 9 Sequential Read



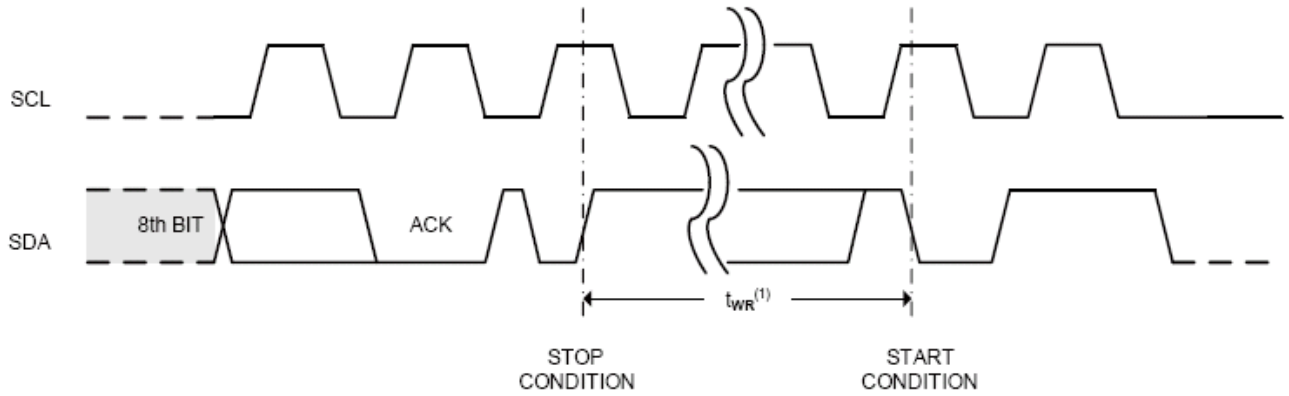
Bus Timing

Figure 10 SCL: Serial Clock, SDA: Serial Data I/O



Write Cycle Timing

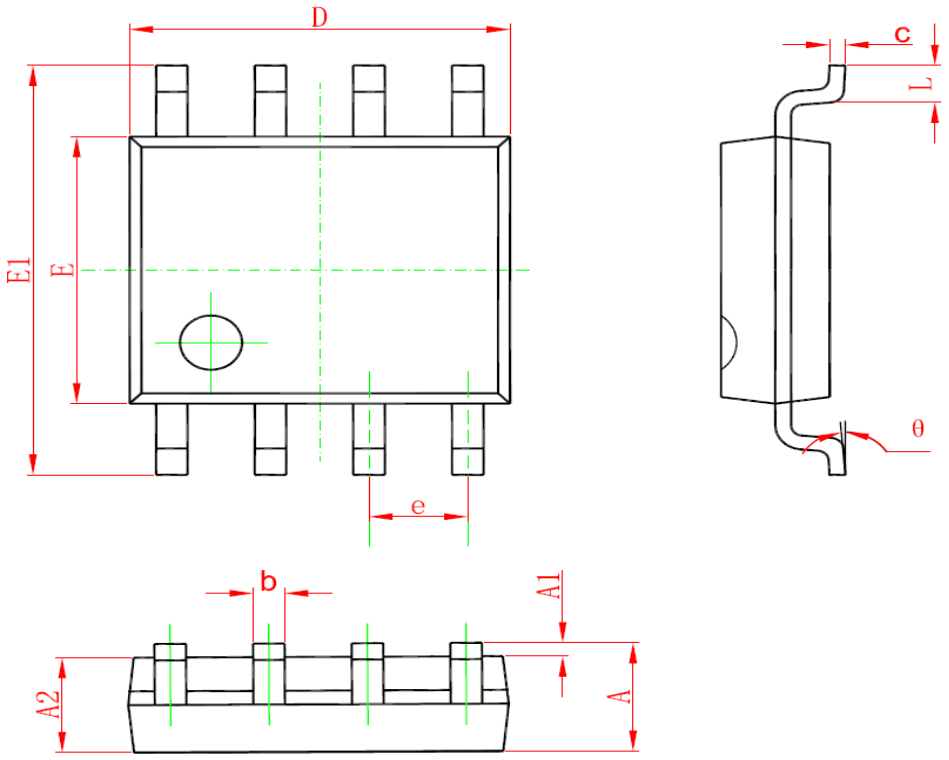
Figure 11 SCL: Serial Clock, SDA: Serial Data I/O



Note: The write cycle time T_{WR} is the time from a valid stop condition of a write sequence to the end of the internal clear/write cycle.

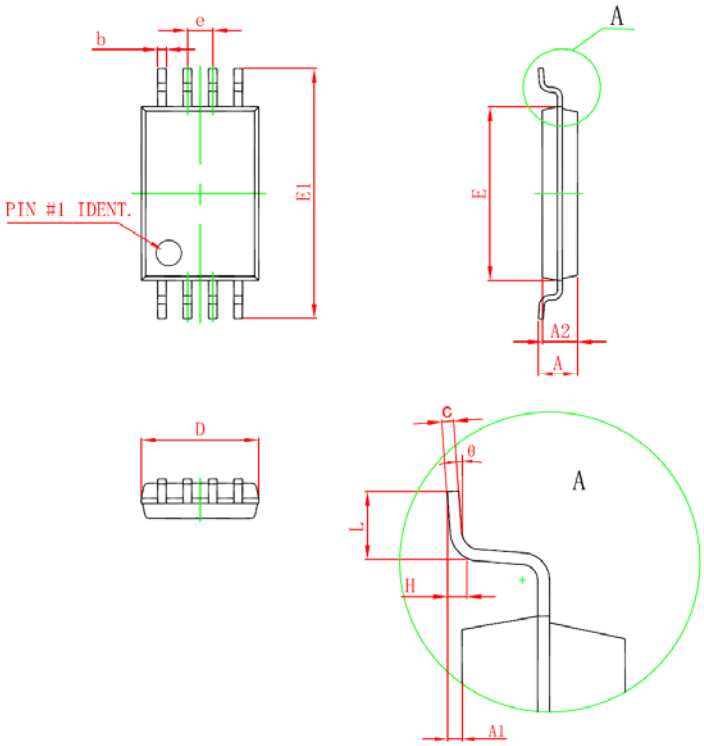
PACKAGE INFORMATION

Dimension in SOP8 (Unit: mm)



Symbol	Min	Max
A	1.350	1.750
A1	0.100	0.250
A2	1.350	1.550
b	0.310	0.510
c	0.170	0.250
D	4.800	5.000
E	3.810	3.99
E1	5.790	6.200
e	1.270(BSC)	
L	0.400	1.270
θ	0°	8°

Dimension in TSSOP8 (Unit: mm)



Symbol	Min	Max
D	2.900	3.100
E	4.300	4.500
b	0.190	0.300
c	0.090	0.200
E1	6.40BSC	
A	-	1.200
A2	0.800	1.050
A1	0.020	0.150
e	0.65 (BSC)	
L	0.450	0.750
H	0.25(TYP)	
θ	0°	8°

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