

# 台康資訊股份有限公司

## 零組件承認書

承認書版本: 1.0

發文編號: AP022031

|   |  |  |                                     |      |           |   |
|---|--|--|-------------------------------------|------|-----------|---|
| 料號  | 6235X571   | 品名規格                                   | SDRAM, 256MB-7, 3.3V, 760pin, MOSEL |      |           |   |
| 承認單位  | CPE2   | 承認人員                                   | 呂銘璋                                 | 承認日期 | 94年10月17日 | <input checked="" type="checkbox"/> 急件 <input type="checkbox"/> 一般件 |
| LOGO  | PSC  | 原廠編號/圖號                                | A2V6U540DTP-7PP                     |      |           |   |
| 廠商  | 奇普仕  | 聯絡人                                    | 陳炳戎                                 | 聯絡電話 | 82263168  |   |
| 送承認原因   | <input type="checkbox"/> 新品 <input checked="" type="checkbox"/> 次來源 <input type="checkbox"/> 其它: _____<br><input type="checkbox"/> 修訂品 <input type="checkbox"/> 代用品, 代用料號: _____ |  |                                     |      | 適用機種      | TMP 48  |
| 電氣項目檢驗重點:   |  |  | 機構項目檢驗重點:                           |      |           |   |
| <input type="checkbox"/> 接觸阻抗   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 尺寸 | <input type="checkbox"/> 表面處理       |      |           |   |
| <input type="checkbox"/> 絕緣阻抗   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 材質 | <input type="checkbox"/> 毛邊         |      |           |   |
| <input type="checkbox"/> 工作電壓   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 外觀 | <input type="checkbox"/> 縮水         |      |           |   |
| <input type="checkbox"/> 工作電流   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 電鍍 | <input type="checkbox"/> 合膠線        |      |           |   |
| <input type="checkbox"/> 逆向電壓   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 印刷 | <input type="checkbox"/> 刮傷         |      |           |   |
| <input type="checkbox"/> 逆向電流   | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 顏色 | <input type="checkbox"/>            |      |           |   |
| <input type="checkbox"/> 耐高壓  | <input type="checkbox"/>   | <input checked="" type="checkbox"/> 包裝 | <input type="checkbox"/>            |      |           |   |
| 注意事項:<br>1. <input type="checkbox"/> 樣品為參考用, 請廠商第一批入料多 1PCS 給 IQC<br>2. 次來源承認已確認 Master Source 承認書 <input checked="" type="checkbox"/> 電氣 <input type="checkbox"/> 機構<br>3. PCB 承認(新品或 Update)須附加電子檔 <input type="checkbox"/> Gerber File <input type="checkbox"/> 機構圖 <input type="checkbox"/> PCB 製作規範 <input type="checkbox"/> JOB 檔<br><input type="checkbox"/> 線路圖<br>4. Update 承認書須註明 庫存: _____ 採購在途: _____ 對策: _____ |  |  |                                     |      |           |   |
| 會簽  | E/E  | 會簽                                     | PM                                  | 林忠平  | 會簽        |   |
|   | M/E  |  | 業務                                  |      |           |   |
| 簽   | SAFETY   | 簽                                      |                                     |      | 簽         |   |
| 審核  | 樣品確認   | 收文單位                                   | 進料                                  | 採購   | 廠商        | 文管 大陸   |
| 林忠平   | 呂銘璋<br>零件工程師   | FILE                                   | ✓                                   | ✓    | ✓         | ✓   |
|   |  | 樣品                                     | ✓                                   |      |           |   |
|   |  | 底片                                     |                                     |      |           |   |
|   |  | 同發文編號: AP                              |                                     | 料號:  |           |   |

料號反向展開(二階)

頁次: 1 / 1  
列印日期: 10-18-2005

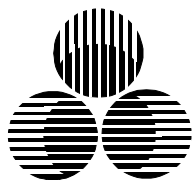
料號 : 02352571 品名規格 : SDRAM, 256MB-7, 3.3V, TSOP II 54, 00  
版次 : 單位 : PCS 最後修改日期 : 07-08-2004

| 料號        | 品名.規格                  | 單位  | 修改日期      | 版次  | 有效碼 |
|-----------|------------------------|-----|-----------|-----|-----|
| 76424002  | PCBA, TWH248-AV        | SET | 07-SEP-04 | .92 | F   |
| √81491200 | RUQX RUR9158, SA, BULK | SET | 07-SEP-04 | .6  | F   |

修改中 BOM

代用品

|          |                |
|----------|----------------|
| 76421004 | PCBA, TWH218   |
| 76424000 | PCBA, TWH248-A |
| 76424001 | PCBA, TWH258   |



奇 普 仕 股 份 有 限 公 司

ULTRA SOURCE TECHNOLOGY CORP. LTD.

台北縣中和市建一路150號17樓 TEL : 886-2-82263168 FAX : 886-2-82263353

17F. NO.150Jian-Yi RD, CHUNG-HO, TAIPEI 235, TAIWAN R.O.C.

積體電路樣品承認書

編號：\_\_\_\_\_

日期： 94 年 1 月 5 日

客戶： \_\_\_\_\_ 台康資訊股份有限公司

品名： \_\_\_\_\_ A2V64S40DTP-7PP

樣品生產廠商： (PSC)

樣品承認簽章處：

業務： \_\_\_\_\_ 陳炳戎 #6608

# ***256Mb SDRAM Specification***

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**A2V56S20BTP**  
**A2V56S30BTP**  
**A2V56S40BTP**

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**PSC** Powerchip Semiconductor Corp.

No.12, Li-Hsin Rd.1, Science-based Industrial Park, Hsin-Chu

Taiwan, R.O.C.

TEL: 886-3-5795000

FAX: 886-3-5792168

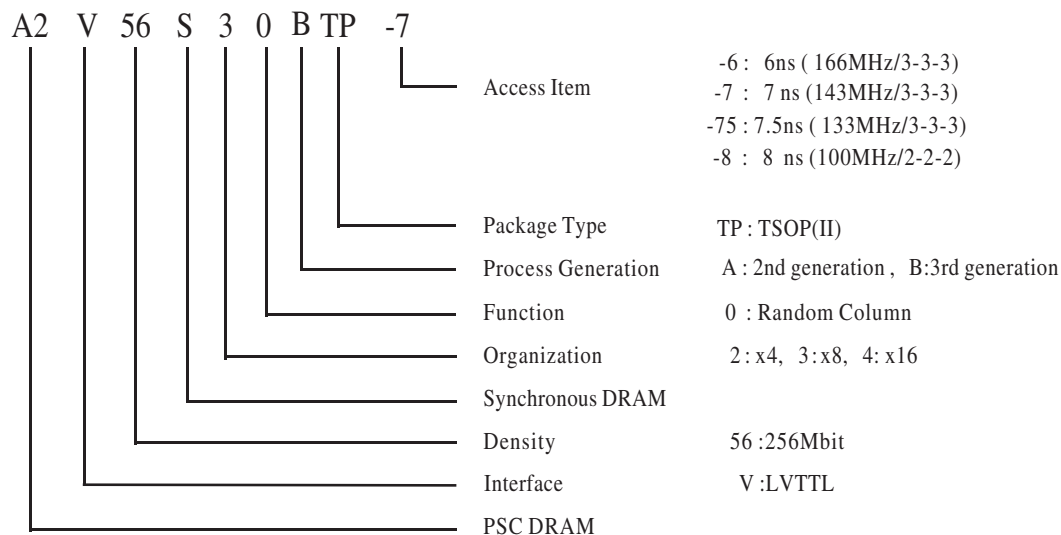
## 256Mb Synchronous DRAM

A2V56S20 BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30 BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40 BTP (4-BANK x 4,194,304-WORD x 16-BIT)

### ORDERING INFORMATION

| Frequency | Speed(ns) | Order Part Number  |          |           |         |                       | Package          |
|-----------|-----------|--------------------|----------|-----------|---------|-----------------------|------------------|
|           |           | Type               | Standard | Low Power | Pb-Free | Low Power and Pb-Free |                  |
| 166MHz    | 6         | A2V56S20/30/40 BTP | -6       | -6L       | -G6     | -G6L                  | 400mil<br>TSOP-2 |
| 143MHz    | 7         | A2V56S20/30/40 BTP | -7       | -7L       | -G7     | -G7L                  | 400mil<br>TSOP-2 |
| 133MHz    | 7.5       | A2V56S20/30/40 BTP | -75      | -75L      | -G75    | -G75L                 | 400mil<br>TSOP-2 |
| 125MHz    | 8         | A2V56S20/30/40 BTP | -8       | -8L       | -G8     | -G8L                  | 400mil<br>TSOP-2 |

### Type Designation Code



**A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)**

**A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)**

**A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)**

## DESCRIPTION

A2V56S20BTP is organized as 4-bank x 16,777,216-word x 4-bit Synchronous DRAM with LVTTTL interface and A2V56S30BTP is organized as 4-bank x 8,388,608-word x 8-bit and A2V56S40BTP is organized as 4-bank x 4,194,304-word x 16-bit. All inputs and outputs are referenced to the rising edge of CLK.

A2V56S20BTP, A2V56S30BTP and A2V56S40BTP achieve very high speed clock rates up to 166MHz, and are suitable for main memories or graphic memories in computer systems.

## FEATURES

| ITEM |   |                  | A2V56S20/30/40BTP |     |     |      |     | Unit |
|------|---|------------------|-------------------|-----|-----|------|-----|------|
|      |   |                  | -6                | -7E | -7  | -75  | -8  |      |
| tCLK | Clock Cycle Time (Min.)                   | CL=2             | -                 | 7   | -   | 10   | 10  | ns   |
|      |   | CL=3             | 6                 | 7   | 7   | 7.5  | 8   | ns   |
| tRAS | Active to Precharge Command Period (Min.) |                  | 42                | 45  | 45  | 45   | 48  | ns   |
| tRCD | Row to Column Delay (Min.)                |                  | 15                | 20  | 20  | 20   | 20  | ns   |
| tAC  | Access Time from CLK (Max.)               | CL=2             | -                 | 5.4 | -   | 6    | 6   | ns   |
|      |   | CL=3             | 5                 | 5.4 | 5.4 | 5.4  | 6   | ns   |
| tRC  | Ref /Active Command Period (Min.)         |                  | 60                | 63  | 63  | 67.5 | 70  | ns   |
| Icc1 | Operation Current (Single Bank) (Max.)    | V56S20           | 100               | 100 | 100 | 100  | 95  | mA   |
|      |   | V56S30           | 110               | 110 | 110 | 110  | 100 | mA   |
|      |   | V56S40           | 130               | 130 | 130 | 130  | 120 | mA   |
| Icc6 | Self Refresh Current (Max.)               | -6,-7E,-7,-75,-8 | 3                 | 3   | 3   | 3    | 3   | mA   |

- Single 3.3V  $\pm$ 0.3V power supply

- Max. Clock frequency:

-6:166MHz<3-3-3>/-7E:143MHz<2-2-2>/-7:143MHz<3-3-3>/-75:133MHz<3-3-3>/-8:100MHz<2-2-2>

- Fully synchronous operation referenced to clock rising edge

- 4-bank operation controlled by BA0,BA1(Bank Address)

- /CAS latency- 2/3 (programmable)

- Burst length- 1/2/4/8/FP (programmable)

- Burst type- Sequential and interleave burst (programmable)

- Byte Control- DQML and DQMU (A2V56S40BTP)

- Random column access

- Auto precharge / All bank precharge controlled by A10

- Auto and self refresh

- 8192 refresh cycles /64ms(4 banks concurrent refresh)

- LVTTTL Interface

- Row address A0-12 /Column address A0-9, 11(x4) / A0-9(x8) / A0-8(x16)

- Package

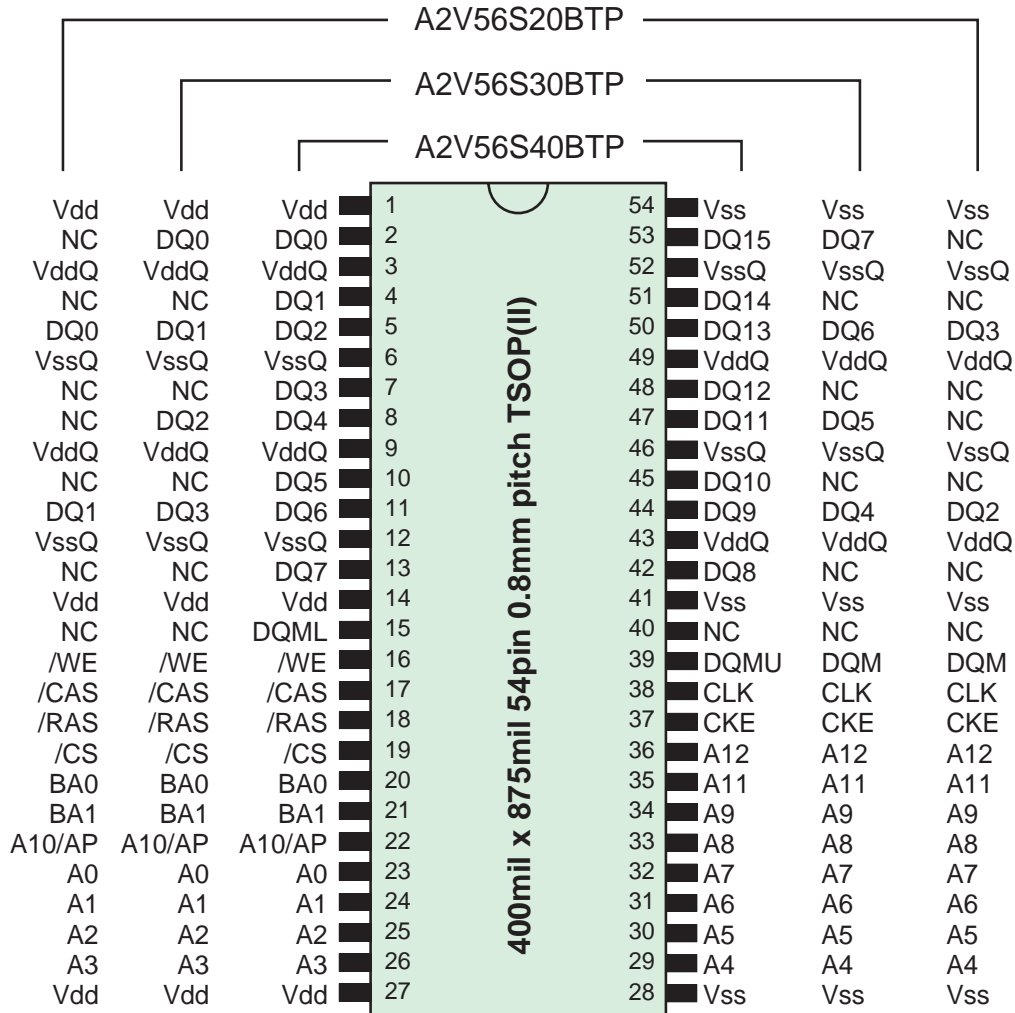
400-mil, 54-pin Thin Small Outline (TSOP II) with 0.8mm lead pitch



# 256Mb Synchronous DRAM

A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## PIN CONFIGURATION (TOP VIEW)



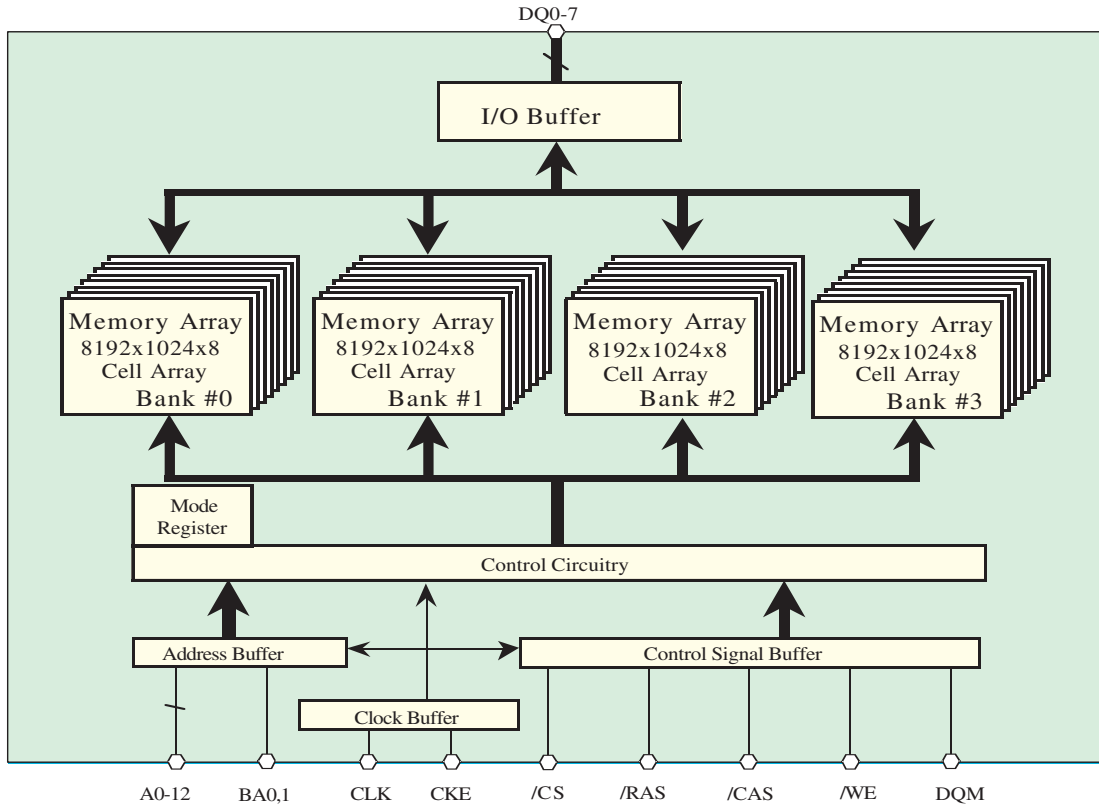
**CLK** : Master Clock  
**CKE** : Clock Enable  
**/CS** : Chip Select  
**/RAS** : Row Address Strobe  
**/CAS** : Column Address Strobe  
**/WE** : Write Enable  
**DQ0-15** : Data I/O

**DQM, DQMU/L** : Output Disable / Write Mask  
**A0-12** : Address Input  
**BA0,1** : Bank Address Input  
**Vdd** : Power Supply  
**VddQ** : Power Supply for Output  
**Vss** : Ground  
**VssQ** : Ground for Output

# 256Mb Synchronous DRAM

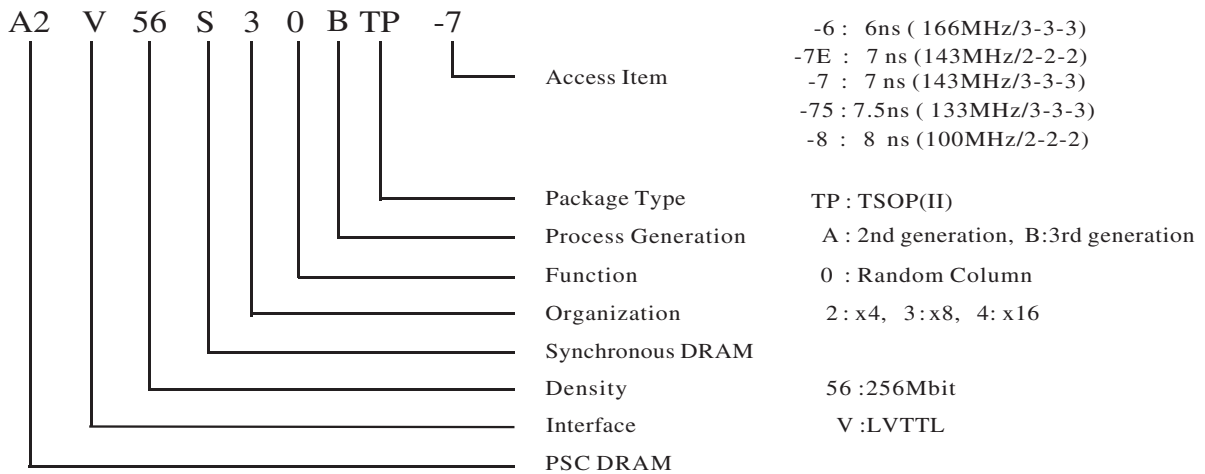
A2V56S20 BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30 BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40 BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## BLOCK DIAGRAM



Note: This figure shows the A2V56S30BTP  
 The A2V56S20BTP configuration is 8192x2048x4 of cell array and DQ0-3  
 The A2V56S40BTP configuration is 8192x512x16 of cell array and DQ0-15

## Type Designation Code







A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## PIN FUNCTION

|   |                |   |
|---|----------------|---|
| CLK                                     | Input          | Master Clock:<br>All other inputs are referenced to the rising edge of CLK  |
| CKE                                     | Input          | Clock Enable:<br>CKE controls internal clock. When CKE is low, internal clock for the following cycle is ceased. CKE is also used to select auto / self-refresh.<br>After self-refresh mode is started, CKE becomes asynchronous input. Self-refresh is maintained as long as CKE is low.   |
| /CS                                     | Input          | Chip Select:<br>When /CS is high, any command means No Operation.   |
| /RAS, /CAS, /WE                         | Input          | Combination of /RAS, /CAS, /WE defines basic commands.  |
| A0-12                                   | Input          | A0-12 specify the Row / Column Address in conjunction with BA0,1. The Row Address is specified by A0-12. The Column Address is specified by A0-9,11(x4)/A0-9(x8)/A0-8(x16). A10 is also used to indicate precharge option. When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, all banks are precharged. |
| BA0,1                                   | Input          | Bank Address:<br>BA0,1 specifies one of four banks to which a command is applied. BA0,1 must be set with ACT, PRE, READ, WRITE commands.  |
| DQ0-3(x4),<br>DQ0-7(x8),<br>DQ0-15(x16) | Input / Output | Data In and Data out are referenced to the rising edge of CLK.  |
| DQM(x4,x8),<br>DQMU/L(x16)              | Input          | Din Mask / Output Disable:<br>When DQM(U/L) is high in burst write, Din for the current cycle is masked. When DQM(U/L) is high in burst read, Dout is disabled at the next but one cycle.   |
| Vdd, Vss                                | Power Supply   | Power Supply for the memory array and peripheral circuitry.   |
| VddQ, VssQ                              | Power Supply   | VddQ and VssQ are supplied to the Output Buffers only.  |

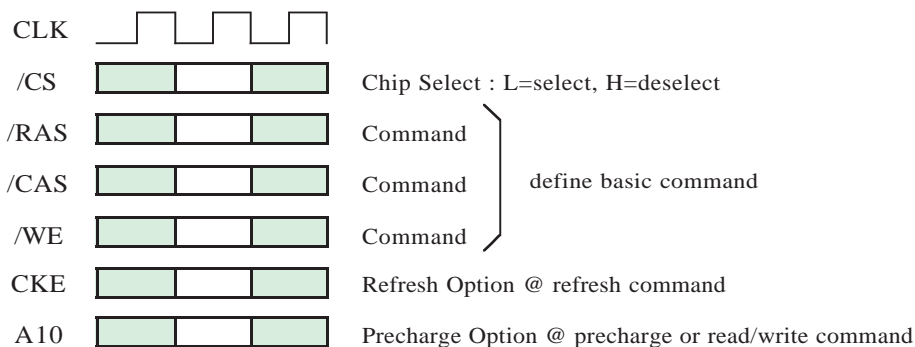
## BASIC FUNCTIONS

The A2V56S20, 30 and 40 BTP provides basic functions, bank (row) activate, burst read / write, bank (row) precharge, and auto / self refresh.

Each command is defined by control signals of /RAS,

/CAS and /WE at CLK rising edge. In addition to 3 signals, /CS, CKE and A10 are used as chip select, refresh option, and precharge option, respectively.

To know the detailed definition of commands, please see the command truth table.



### Activate (ACT) [/RAS =L, /CAS =/WE =H]

ACT command activates a row in an idle bank indicated by BA.

### Read (READ) [/RAS =H, /CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA. First output data appears after /CAS latency. When A10 =H at this command, the bank is deactivated after the burst read (auto-precharge, **READA**).

### Write (WRITE) [/RAS =H, /CAS =/WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write (auto-precharge, **WRITEA**).

### Precharge (PRE) [/RAS =L, /CAS =H, /WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, all banks are deactivated (precharge all, **PREA**).

### Auto-Refresh (REFA) [/RAS =/CAS =L, /WE =CKE =H]

REFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

**COMMAND TRUTH TABLE**

| COMMAND  | MNEMONIC | CKE<br>n-1 | CKE<br>n | /CS | /RAS | /CAS | /WE | BA0,1 | A10<br>/AP | A0-9,<br>11-12 | note |
|--|----------|------------|----------|-----|------|------|-----|-------|------------|----------------|------|
| Deselect   | DESEL    | H          | X        | H   | X    | X    | X   | X     | X          | X              |      |
| No Operation   | NOP      | H          | X        | L   | H    | H    | H   | X     | X          | X              |      |
| Row Address Entry &<br>Bank Activate                   | ACT      | H          | X        | L   | L    | H    | H   | V     | V          | V              |      |
| Single Bank Precharge                                  | PRE      | H          | X        | L   | L    | H    | L   | V     | L          | X              |      |
| Precharge All Banks                                    | PREA     | H          | X        | L   | L    | H    | L   | X     | H          | X              |      |
| Column Address Entry<br>& Write                        | WRITE    | H          | X        | L   | H    | L    | L   | V     | L          | V              |      |
| Column Address Entry<br>& Write with<br>Auto-Precharge | WRITEA   | H          | X        | L   | H    | L    | L   | V     | H          | V              |      |
| Column Address Entry<br>& Read                         | READ     | H          | X        | L   | H    | L    | H   | V     | L          | V              |      |
| Column Address Entry<br>& Read with<br>Auto-Precharge  | READA    | H          | X        | L   | H    | L    | H   | V     | H          | V              |      |
| Auto-Refresh   | REFA     | H          | H        | L   | L    | L    | H   | X     | X          | X              |      |
| Self-Refresh Entry                                     | REFS     | H          | L        | L   | L    | L    | H   | X     | X          | X              |      |
| Self-Refresh Exit                                      | REFSX    | L          | H        | H   | X    | X    | X   | X     | X          | X              |      |
|  |          | L          | H        | L   | H    | H    | H   | X     | X          | X              |      |
| Burst Terminate  | TBST     | H          | X        | L   | H    | H    | L   | X     | X          | X              |      |
| Mode Register Set                                      | MRS      | H          | X        | L   | L    | L    | L   | L     | L          | V              | 1    |

H=High Level, L=Low Level, V=Valid, X=Don't Care, n=CLK cycle number

**NOTE:**

1. A7-9,11-12=L, A0-A6 =Mode Address

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### FUNCTION TRUTH TABLE

| Current State     | /CS | /RAS | /CAS | /WE                  | Address              | Command           | Action  |
|-------------------|-----|------|------|----------------------|----------------------|-------------------|---|
| <b>IDLE</b>       | H   | X    | X    | X                    | X                    | DESEL             | NOP   |
|                   | L   | H    | H    | H                    | X                    | NOP               | NOP   |
|                   | L   | H    | H    | L                    | X                    | TBST              | ILLEGAL*2   |
|                   | L   | H    | L    | X                    | BA, CA, A10          | READ / WRITE      | ILLEGAL*2   |
|                   | L   | L    | H    | H                    | BA, RA               | ACT               | Bank Active, Latch RA   |
|                   | L   | L    | H    | L                    | BA, A10              | PRE / PREA        | NOP*4   |
|                   | L   | L    | L    | H                    | X                    | REFA              | Auto-Refresh*5  |
|                   | L   | L    | L    | L                    | Op-Code,<br>Mode-Add | MRS               | Mode Register Set*5   |
| <b>ROW ACTIVE</b> | H   | X    | X    | X                    | X                    | DESEL             | NOP   |
|                   | L   | H    | H    | H                    | X                    | NOP               | NOP   |
|                   | L   | H    | H    | L                    | X                    | TBST              | NOP   |
|                   | L   | H    | L    | H                    | BA, CA, A10          | READ / READA      | Begin Read, Latch CA,<br>Determine Auto-Precharge                           |
|                   | L   | H    | L    | L                    | BA, CA, A10          | WRITE /<br>WRITEA | Begin Write, Latch CA,<br>Determine Auto-Precharge                          |
|                   | L   | L    | H    | H                    | BA, RA               | ACT               | Bank Active / ILLEGAL*2   |
|                   | L   | L    | H    | L                    | BA, A10              | PRE / PREA        | Precharge / Precharge All   |
|                   | L   | L    | L    | H                    | X                    | REFA              | ILLEGAL   |
| <b>READ</b>       | L   | L    | L    | L                    | Op-Code,<br>Mode-Add | MRS               | ILLEGAL   |
|                   | H   | X    | X    | X                    | X                    | DESEL             | NOP (Continue Burst to END)   |
|                   | L   | H    | H    | H                    | X                    | NOP               | NOP (Continue Burst to END)   |
|                   | L   | H    | H    | L                    | X                    | TBST              | Terminate Burst   |
|                   | L   | H    | L    | H                    | BA, CA, A10          | READ / READA      | Terminate Burst, Latch CA,<br>Begin New Read, Determine<br>Auto-Precharge*3 |
|                   | L   | H    | L    | L                    | BA, CA, A10          | WRITE /<br>WRITEA | Terminate Burst, Latch CA,<br>Begin Write, Determine Auto-<br>Precharge*3   |
|                   | L   | L    | H    | H                    | BA, RA               | ACT               | Bank Active / ILLEGAL*2   |
|                   | L   | L    | H    | L                    | BA, A10              | PRE / PREA        | Terminate Burst, Precharge  |
|                   | L   | L    | L    | H                    | X                    | REFA              | ILLEGAL   |
| L                 | L   | L    | L    | Op-Code,<br>Mode-Add | MRS                  | ILLEGAL           |   |

**FUNCTION TRUTH TABLE (continued)**

| Current State                    | /CS | /RAS | /CAS | /WE | Address           | Command        | Action   |
|----------------------------------|-----|------|------|-----|-------------------|----------------|--|
| <b>WRITE</b>                     | H   | X    | X    | X   | X                 | DESEL          | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | H   | X                 | NOP            | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | L   | X                 | TBST           | Terminate Burst  |
|                                  | L   | H    | L    | H   | BA, CA, A10       | READ / READA   | Terminate Burst, Latch CA, Begin Read, Determine Auto-Precharge*3  |
|                                  | L   | H    | L    | L   | BA, CA, A10       | WRITE / WRITEA | Terminate Burst, Latch CA, Begin Write, Determine Auto-Precharge*3 |
|                                  | L   | L    | H    | H   | BA, RA            | ACT            | Bank Active / ILLEGAL*2  |
|                                  | L   | L    | H    | L   | BA, A10           | PRE / PREA     | Terminate Burst, Precharge   |
|                                  | L   | L    | L    | H   | X                 | REFA           | ILLEGAL  |
|                                  | L   | L    | L    | L   | Op-Code, Mode-Add | MRS            | ILLEGAL  |
| <b>READ with AUTO PRECHARGE</b>  | H   | X    | X    | X   | X                 | DESEL          | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | H   | X                 | NOP            | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | L   | X                 | TBST           | ILLEGAL  |
|                                  | L   | H    | L    | H   | BA, CA, A10       | READ / READA   | ILLEGAL  |
|                                  | L   | H    | L    | L   | BA, CA, A10       | WRITE / WRITEA | ILLEGAL  |
|                                  | L   | L    | H    | H   | BA, RA            | ACT            | Bank Active / ILLEGAL*2  |
|                                  | L   | L    | H    | L   | BA, A10           | PRE / PREA     | ILLEGAL*2  |
|                                  | L   | L    | L    | H   | X                 | REFA           | ILLEGAL  |
|                                  | L   | L    | L    | L   | Op-Code, Mode-Add | MRS            | ILLEGAL  |
| <b>WRITE with AUTO PRECHARGE</b> | H   | X    | X    | X   | X                 | DESEL          | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | H   | X                 | NOP            | NOP (Continue Burst to END)  |
|                                  | L   | H    | H    | L   | X                 | TBST           | ILLEGAL  |
|                                  | L   | H    | L    | H   | BA, CA, A10       | READ / READA   | ILLEGAL  |
|                                  | L   | H    | L    | L   | BA, CA, A10       | WRITE / WRITEA | ILLEGAL  |
|                                  | L   | L    | H    | H   | BA, RA            | ACT            | Bank Active / ILLEGAL*2  |
|                                  | L   | L    | H    | L   | BA, A10           | PRE / PREA     | ILLEGAL*2  |
|                                  | L   | L    | L    | H   | X                 | REFA           | ILLEGAL  |
|                                  | L   | L    | L    | L   | Op-Code, Mode-Add | MRS            | ILLEGAL  |

## FUNCTION TRUTH TABLE (continued)

| Current State         | /CS | /RAS | /CAS | /WE | Address              | Command      | Action                      |
|-----------------------|-----|------|------|-----|----------------------|--------------|-----------------------------|
| PRE -<br>CHARGING     | H   | X    | X    | X   | X                    | DESEL        | NOP (Idle after tRP)        |
|                       | L   | H    | H    | H   | X                    | NOP          | NOP (Idle after tRP)        |
|                       | L   | H    | H    | L   | X                    | TBST         | ILLEGAL*2                   |
|                       | L   | H    | L    | X   | BA, CA, A10          | READ / WRITE | ILLEGAL*2                   |
|                       | L   | L    | H    | H   | BA, RA               | ACT          | ILLEGAL*2                   |
|                       | L   | L    | H    | L   | BA, A10              | PRE / PREA   | NOP*4 (Idle after tRP)      |
|                       | L   | L    | L    | H   | X                    | REFA         | ILLEGAL                     |
|                       | L   | L    | L    | L   | Op-Code,<br>Mode-Add | MRS          | ILLEGAL                     |
| ROW<br>ACTIVATING     | H   | X    | X    | X   | X                    | DESEL        | NOP (Row Active after tRCD) |
|                       | L   | H    | H    | H   | X                    | NOP          | NOP (Row Active after tRCD) |
|                       | L   | H    | H    | L   | X                    | TBST         | ILLEGAL*2                   |
|                       | L   | H    | L    | X   | BA, CA, A10          | READ / WRITE | ILLEGAL*2                   |
|                       | L   | L    | H    | H   | BA, RA               | ACT          | ILLEGAL*2                   |
|                       | L   | L    | H    | L   | BA, A10              | PRE / PREA   | ILLEGAL*2                   |
|                       | L   | L    | L    | H   | X                    | REFA         | ILLEGAL                     |
|                       | L   | L    | L    | L   | Op-Code,<br>Mode-Add | MRS          | ILLEGAL                     |
| WRITE RE-<br>COVERING | H   | X    | X    | X   | X                    | DESEL        | NOP                         |
|                       | L   | H    | H    | H   | X                    | NOP          | NOP                         |
|                       | L   | H    | H    | L   | X                    | TBST         | ILLEGAL*2                   |
|                       | L   | H    | L    | X   | BA, CA, A10          | READ / WRITE | ILLEGAL*2                   |
|                       | L   | L    | H    | H   | BA, RA               | ACT          | ILLEGAL*2                   |
|                       | L   | L    | H    | L   | BA, A10              | PRE / PREA   | ILLEGAL*2                   |
|                       | L   | L    | L    | H   | X                    | REFA         | ILLEGAL                     |
|                       | L   | L    | L    | L   | Op-Code,<br>Mode-Add | MRS          | ILLEGAL                     |

## FUNCTION TRUTH TABLE (continued)

| Current State                | /CS | /RAS | /CAS | /WE               | Address           | Command      | Action                |
|------------------------------|-----|------|------|-------------------|-------------------|--------------|-----------------------|
| <b>RE-FRESHING</b>           | H   | X    | X    | X                 | X                 | DESEL        | NOP (Idle after tRC)  |
|                              | L   | H    | H    | H                 | X                 | NOP          | NOP (Idle after tRC)  |
|                              | L   | H    | H    | L                 | X                 | TBST         | ILLEGAL               |
|                              | L   | H    | L    | X                 | BA, CA, A10       | READ / WRITE | ILLEGAL               |
|                              | L   | L    | H    | H                 | BA, RA            | ACT          | ILLEGAL               |
|                              | L   | L    | H    | L                 | BA, A10           | PRE / PREA   | ILLEGAL               |
|                              | L   | L    | L    | H                 | X                 | REFA         | ILLEGAL               |
| <b>MODE REGISTER SETTING</b> | L   | L    | L    | L                 | Op-Code, Mode-Add | MRS          | ILLEGAL               |
|                              | H   | X    | X    | X                 | X                 | DESEL        | NOP (Idle after tRSC) |
|                              | L   | H    | H    | H                 | X                 | NOP          | NOP (Idle after tRSC) |
|                              | L   | H    | H    | L                 | X                 | TBST         | ILLEGAL               |
|                              | L   | H    | L    | X                 | BA, CA, A10       | READ / WRITE | ILLEGAL               |
|                              | L   | L    | H    | H                 | BA, RA            | ACT          | ILLEGAL               |
|                              | L   | L    | H    | L                 | BA, A10           | PRE / PREA   | ILLEGAL               |
| L                            | L   | L    | H    | X                 | REFA              | ILLEGAL      |                       |
| L                            | L   | L    | L    | Op-Code, Mode-Add | MRS               | ILLEGAL      |                       |

### ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

BA=Bank Address, RA=Row Address, CA=Column Address, NOP=No Operation

### NOTES:

1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state. May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and/or data-integrity are not guaranteed.

## FUNCTION TRUTH TABLE (continued)

| Current State                     | CKE <sub>n-1</sub> | CKE <sub>n</sub> | /CS | /RAS | /CAS | /WE | Add | Action                             |
|-----------------------------------|--------------------|------------------|-----|------|------|-----|-----|------------------------------------|
| SELF-REFRESH*1                    | H                  | X                | X   | X    | X    | X   | X   | INVALID                            |
|                                   | L                  | H                | H   | X    | X    | X   | X   | Exit Self-Refresh (Idle after tRC) |
|                                   | L                  | H                | L   | H    | H    | H   | X   | Exit Self-Refresh (Idle after tRC) |
|                                   | L                  | H                | L   | H    | H    | L   | X   | ILLEGAL                            |
|                                   | L                  | H                | L   | H    | L    | X   | X   | ILLEGAL                            |
|                                   | L                  | H                | L   | L    | X    | X   | X   | ILLEGAL                            |
|                                   | L                  | L                | X   | X    | X    | X   | X   | NOP (Maintain Self-Refresh)        |
| POWER DOWN                        | H                  | X                | X   | X    | X    | X   | X   | INVALID                            |
|                                   | L                  | H                | X   | X    | X    | X   | X   | Exit Power Down to Idle            |
|                                   | L                  | L                | X   | X    | X    | X   | X   | NOP (Maintain Power Down)          |
| ALL BANKS IDLE*2                  | H                  | H                | X   | X    | X    | X   | X   | Refer to Function Truth Table      |
|                                   | H                  | L                | L   | L    | L    | H   | X   | Enter Self-Refresh                 |
|                                   | H                  | L                | H   | X    | X    | X   | X   | Enter Power Down                   |
|                                   | H                  | L                | L   | H    | H    | H   | X   | Enter Power Down                   |
|                                   | H                  | L                | L   | H    | H    | L   | X   | ILLEGAL                            |
|                                   | H                  | L                | L   | H    | L    | X   | X   | ILLEGAL                            |
|                                   | H                  | L                | L   | L    | X    | X   | X   | ILLEGAL                            |
|                                   | L                  | X                | X   | X    | X    | X   | X   | Refer to Current State =Power Down |
| ANY STATE other than listed above | H                  | H                | X   | X    | X    | X   | X   | Refer to Function Truth Table      |
|                                   | H                  | L                | X   | X    | X    | X   | X   | Begin CLK Suspend at Next Cycle*3  |
|                                   | L                  | H                | X   | X    | X    | X   | X   | Exit CLK Suspend at Next Cycle*3   |
|                                   | L                  | L                | X   | X    | X    | X   | X   | Maintain CLK Suspend               |

### ABBREVIATIONS:

H=High Level, L=Low Level, X=Don't Care

### NOTES:

1. CKE Low to High transition will re-enable CLK and other inputs **asynchronously**. A minimum setup time must be satisfied before any command other than EXIT.
2. Self-Refresh can be entered only from the All Banks Idle State.
3. Must be legal command.







# 256Mb Synchronous DRAM

A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## POWER ON SEQUENCE

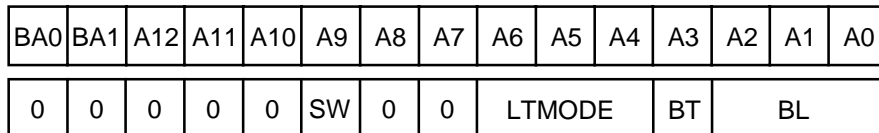
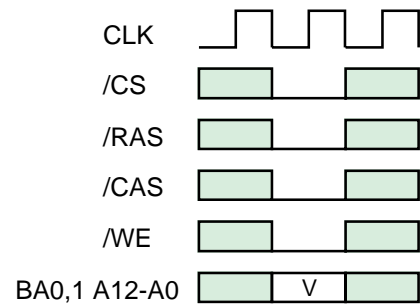
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Apply power and start clock. Attempt to maintain CKE high, DQM high and NOP condition at the inputs.
2. Maintain stable power, stable clock, and NOP input conditions for a minimum of 200µs.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

## MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register (MRS). The mode register stores these data until the next MRS command, which may be issued when all banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



|    |   |              |
|----|---|--------------|
| SW | 0 | Burst Write  |
|    | 1 | Single Write |

|              |       |              |
|--------------|-------|--------------|
| LATENCY MODE | CL    | /CAS LATENCY |
|              | 0 0 0 | R            |
|              | 0 0 1 | R            |
|              | 0 1 0 | 2            |
|              | 0 1 1 | 3            |
|              | 1 0 0 | R            |
|              | 1 0 1 | R            |
|              | 1 1 0 | R            |
| 1 1 1        | R     |              |

|              |           |      |      |
|--------------|-----------|------|------|
| BURST LENGTH | BL        | BT=0 | BT=1 |
|              | 0 0 0     | 1    | 1    |
|              | 0 0 1     | 2    | 2    |
|              | 0 1 0     | 4    | 4    |
|              | 0 1 1     | 8    | 8    |
|              | 1 0 0     | R    | R    |
|              | 1 0 1     | R    | R    |
|              | 1 1 0     | R    | R    |
| 1 1 1        | Full Page | R    |      |

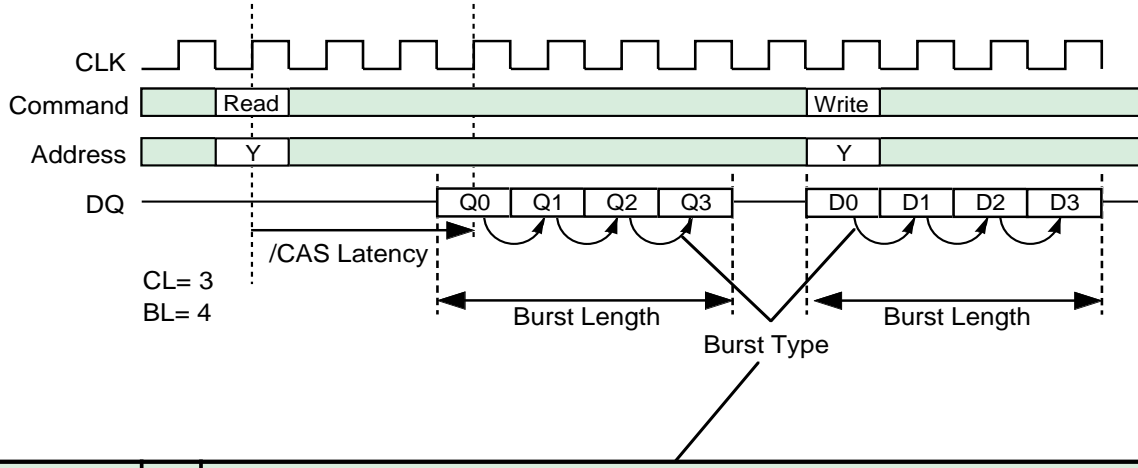
|            |   |             |
|------------|---|-------------|
| BURST TYPE | 0 | SEQUENTIAL  |
|            | 1 | INTERLEAVED |

R: Reserved for Future Use

# 256Mb Synchronous DRAM



A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)



| Initial Address |    |    | BL | Column Addressing |   |   |   |   |   |   |   |             |   |   |   |   |   |   |   |
|-----------------|----|----|----|-------------------|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|
| A2              | A1 | A0 |    | Sequential        |   |   |   |   |   |   |   | Interleaved |   |   |   |   |   |   |   |
| 0               | 0  | 0  | 8  | 0                 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 0           | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| 0               | 0  | 1  |    | 1                 | 2 | 3 | 4 | 5 | 6 | 7 | 0 | 1           | 0 | 3 | 2 | 5 | 4 | 7 | 6 |
| 0               | 1  | 0  |    | 2                 | 3 | 4 | 5 | 6 | 7 | 0 | 1 | 2           | 3 | 0 | 1 | 6 | 7 | 4 | 5 |
| 0               | 1  | 1  |    | 3                 | 4 | 5 | 6 | 7 | 0 | 1 | 2 | 3           | 2 | 1 | 0 | 7 | 6 | 5 | 4 |
| 1               | 0  | 0  |    | 4                 | 5 | 6 | 7 | 0 | 1 | 2 | 3 | 4           | 5 | 6 | 7 | 0 | 1 | 2 | 3 |
| 1               | 0  | 1  |    | 5                 | 6 | 7 | 0 | 1 | 2 | 3 | 4 | 5           | 4 | 7 | 6 | 1 | 0 | 3 | 2 |
| 1               | 1  | 0  |    | 6                 | 7 | 0 | 1 | 2 | 3 | 4 | 5 | 6           | 7 | 4 | 5 | 2 | 3 | 0 | 1 |
| 1               | 1  | 1  |    | 7                 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7           | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| -               | 0  | 0  | 4  | 0                 | 1 | 2 | 3 |   |   |   |   | 0           | 1 | 2 | 3 |   |   |   |   |
| -               | 0  | 1  |    | 1                 | 2 | 3 | 0 |   |   |   |   | 1           | 0 | 3 | 2 |   |   |   |   |
| -               | 1  | 0  |    | 2                 | 3 | 0 | 1 |   |   |   |   | 2           | 3 | 0 | 1 |   |   |   |   |
| -               | 1  | 1  |    | 3                 | 0 | 1 | 2 |   |   |   |   | 3           | 2 | 1 | 0 |   |   |   |   |
| -               | -  | 0  | 2  | 0                 | 1 |   |   |   |   |   |   | 0           | 1 |   |   |   |   |   |   |
| -               | -  | 1  |    | 1                 | 0 |   |   |   |   |   |   | 1           | 0 |   |   |   |   |   |   |

## OPERATIONAL DESCRIPTION

### BANK ACTIVATE

The SDRAM has four independent banks. Each bank is activated by the ACT command with the bank addresses (BA0,1). A row is indicated by the row addresses (A0,1). A row is indicated by the row addresses A0-12. The minimum activation interval between one bank and the other bank is tRRD. Multiple banks can be active state concurrently by issuing multiple ACT commands.

### PRECHARGE

The PRE command deactivates the bank indicated by BA0,1. When multiple banks are active, the precharge all command (PREA, PRE + A10=H) is available to deactivate them at the same time.

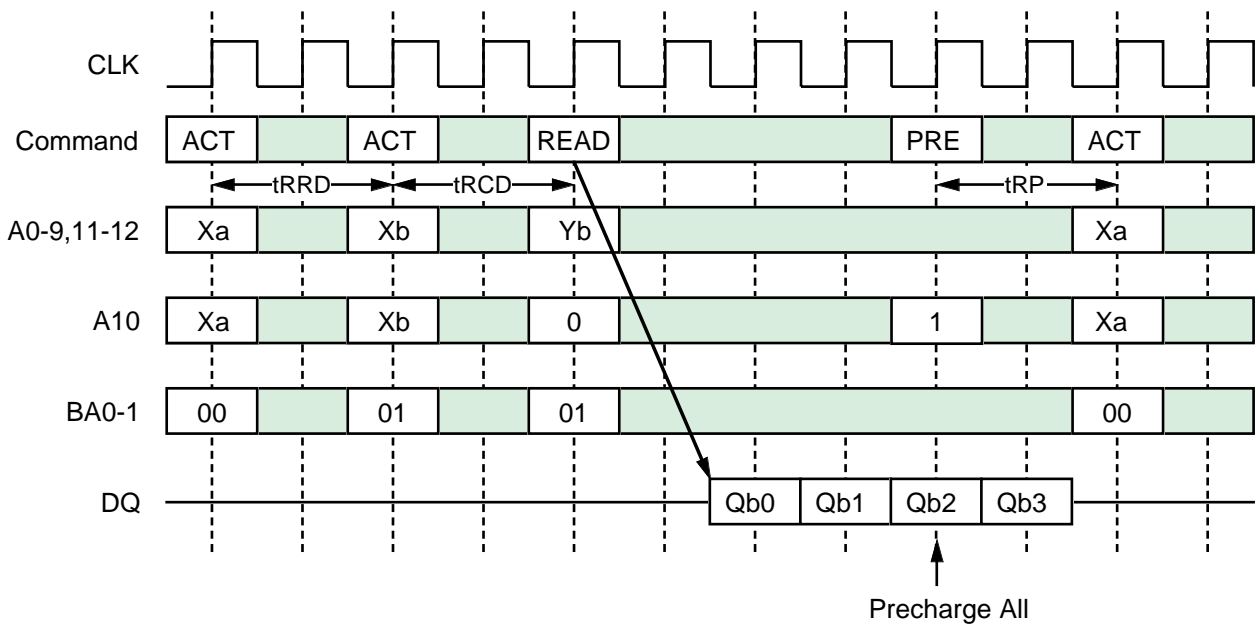
After tRP from the precharge, an ACT command to the same bank can be issued. BA0-1 are **“DON’T CARE”** in this case.

### READ

After tRCD from the bank activation, a READ command can be issued. 1st output data is available after the /CAS Latency from the READ, followed by (BL -1) consecutive data when the Burst Length is BL. The start address is specified by A0-A9,A11(x4), A0-9(X8), A0-8(X16) , and the address sequence of burst data is defined by the Burst Type. A READ command may be applied to any active bank, so the row precharge time (tRP) can be hidden behind continuous output data by interleaving the multiple banks. When A10 is high at a READ command, the auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, TBST, ACT) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA.

In any case,  $tRCD+BL \geq tRAS_{min}$  must be met.

**Bank Activation and Precharge All (BL=4, CL=3)**

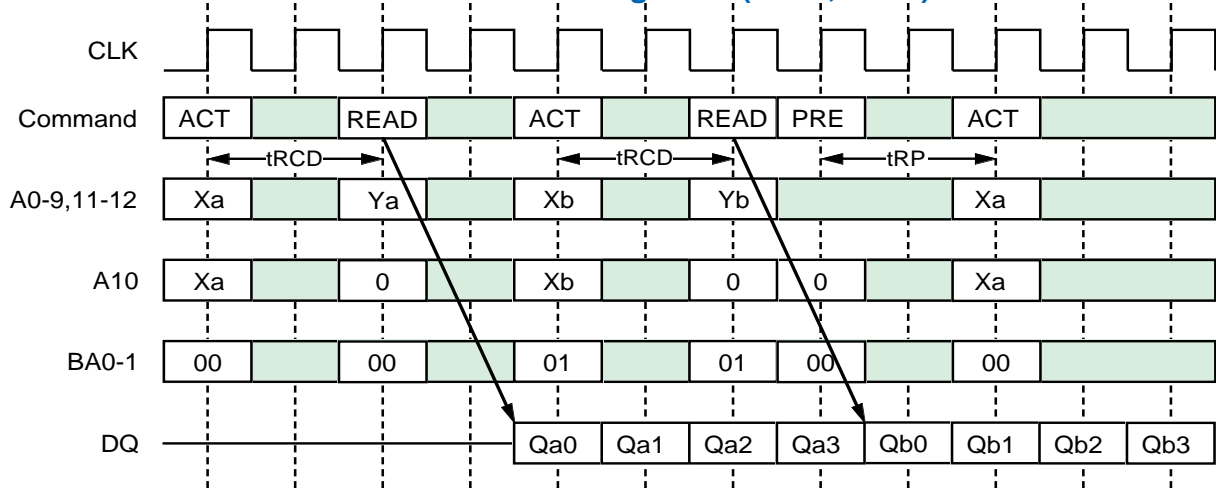


# 256Mb Synchronous DRAM

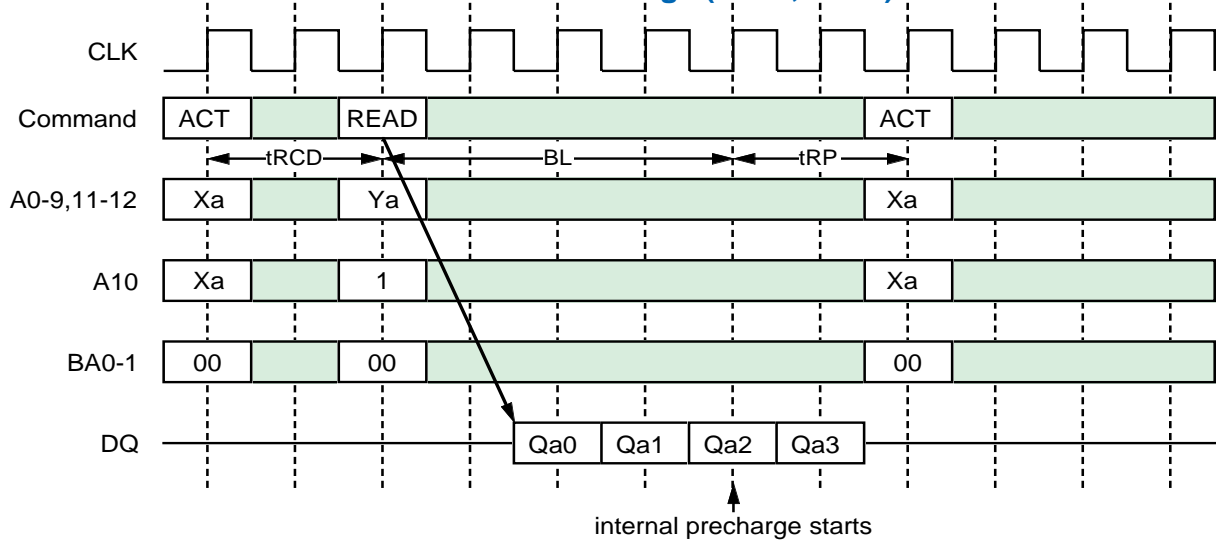


A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

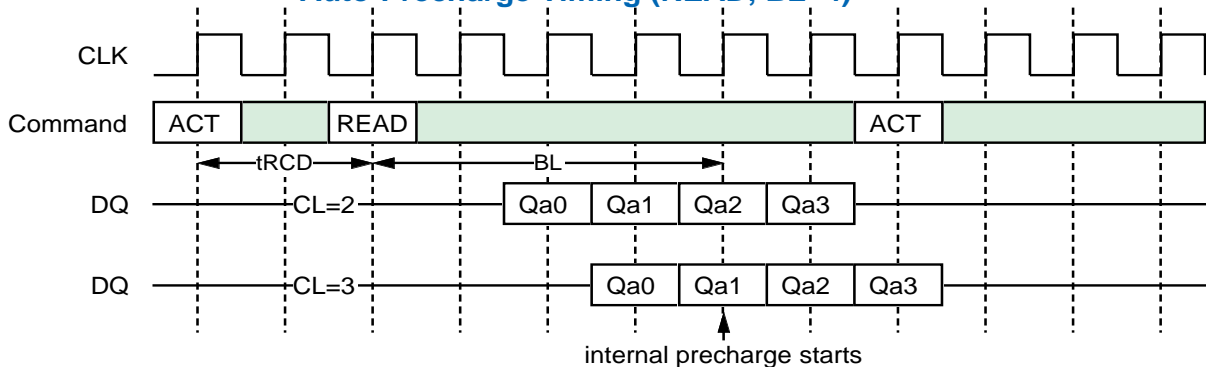
## Multi Bank Interleaving Read (CL=2, BL=4)



## Read with Auto-Precharge (CL=2, BL=4)



## Auto-Precharge Timing (READ, BL=4)





# 256Mb Synchronous DRAM

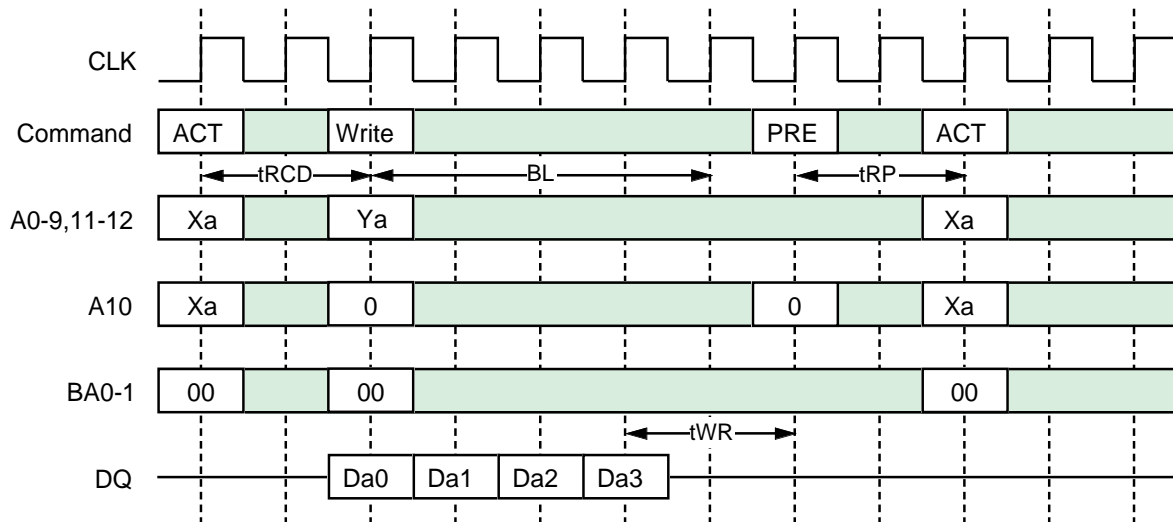
A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## WRITE

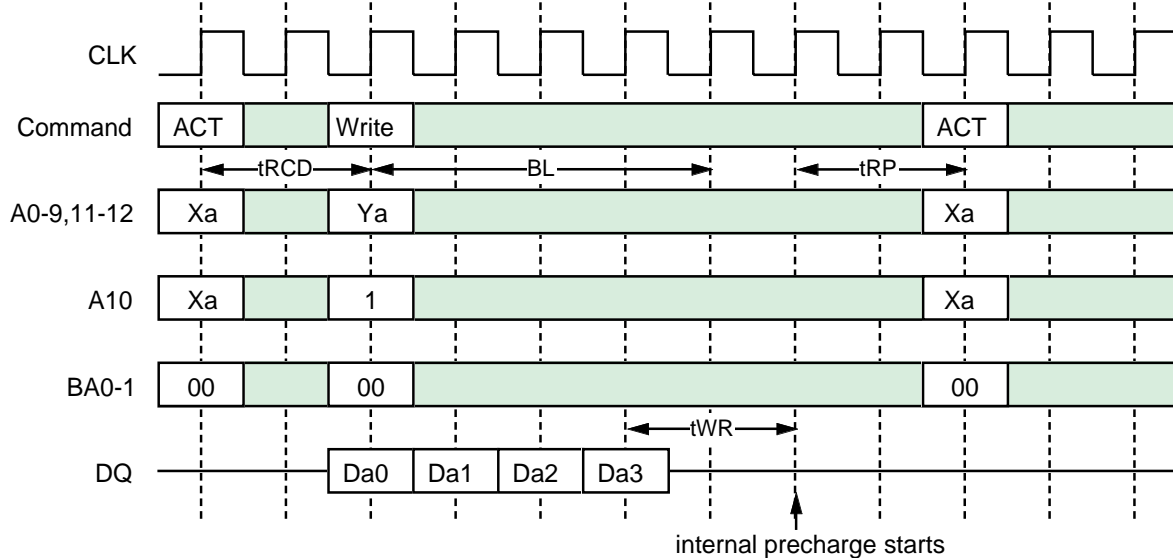
A WRITE command can be issued to any active bank. The start address is specified by A0-9,11(x4),A0-9(x8), A0-8(x16). 1st input data is set at the same cycle as the WRITE. The consecutive data length to be write is defined by the Burst Length. The address sequence of burst data is defined by Burst Type. Minmum delay time of a WRITE command after an ACT command to the same bank is tRCD. From the last input data to the PRE command , the write recovery time (tWR) is

required. When A10 is high at a WRITE command , auto-precharge (WRITEEA) is performed. Any command (READ,WRITE,PRE,ACT,TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at tWR after the last input data cycle . The next ACT command can be issued after (BL+tWR-1+tRP) from the previous WRITEEA. In any case, tRCD+BL+tWR-1 ≥ tRASmin must be met.

Write (BL=4)



Write with Auto-Precharge (BL=4)



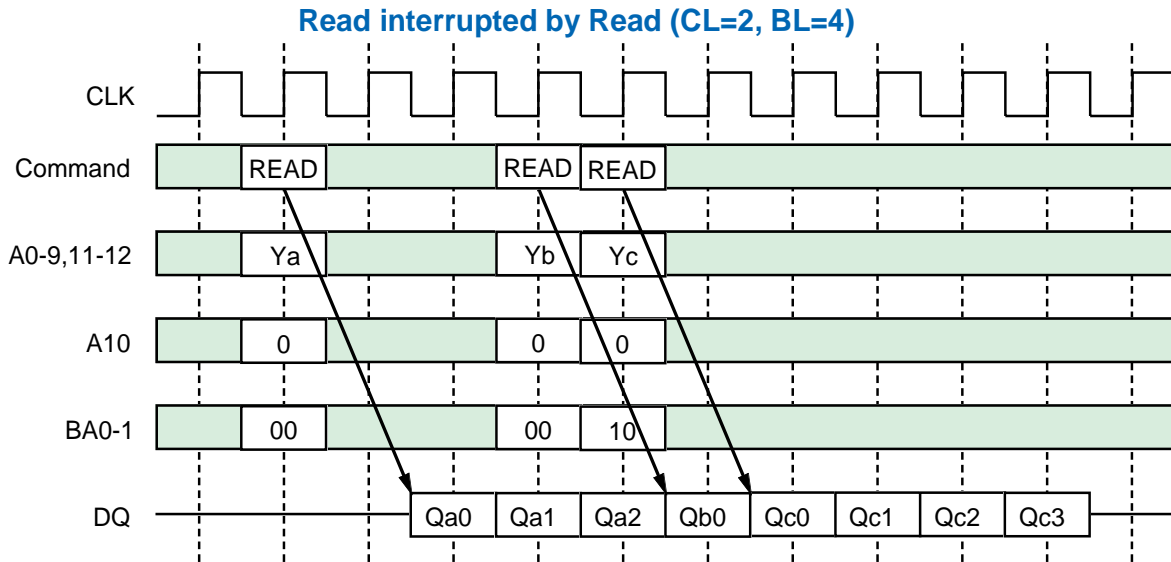


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## BURST INTERRUPTION

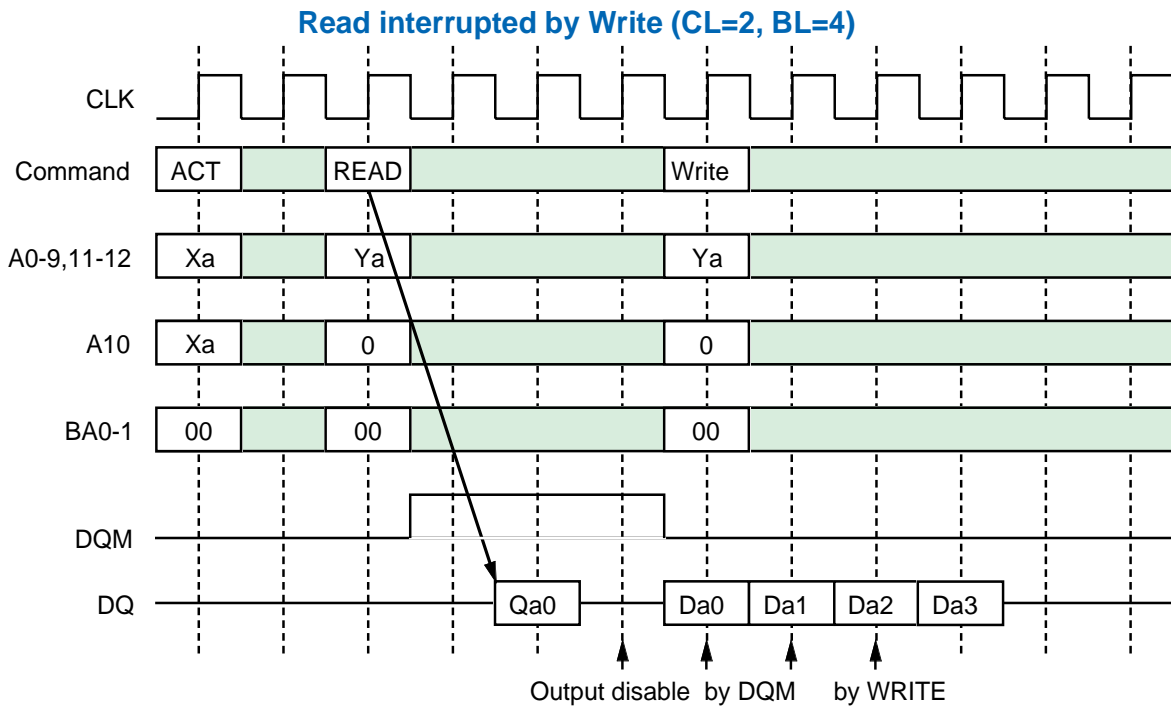
### [ Read Interrupted by Read ]

Burst read operation can be interrupted by new read of any bank. Random column access is allowed. READ to READ interval is minimum 1 CLK..



### [ Read Interrupted by Write ]

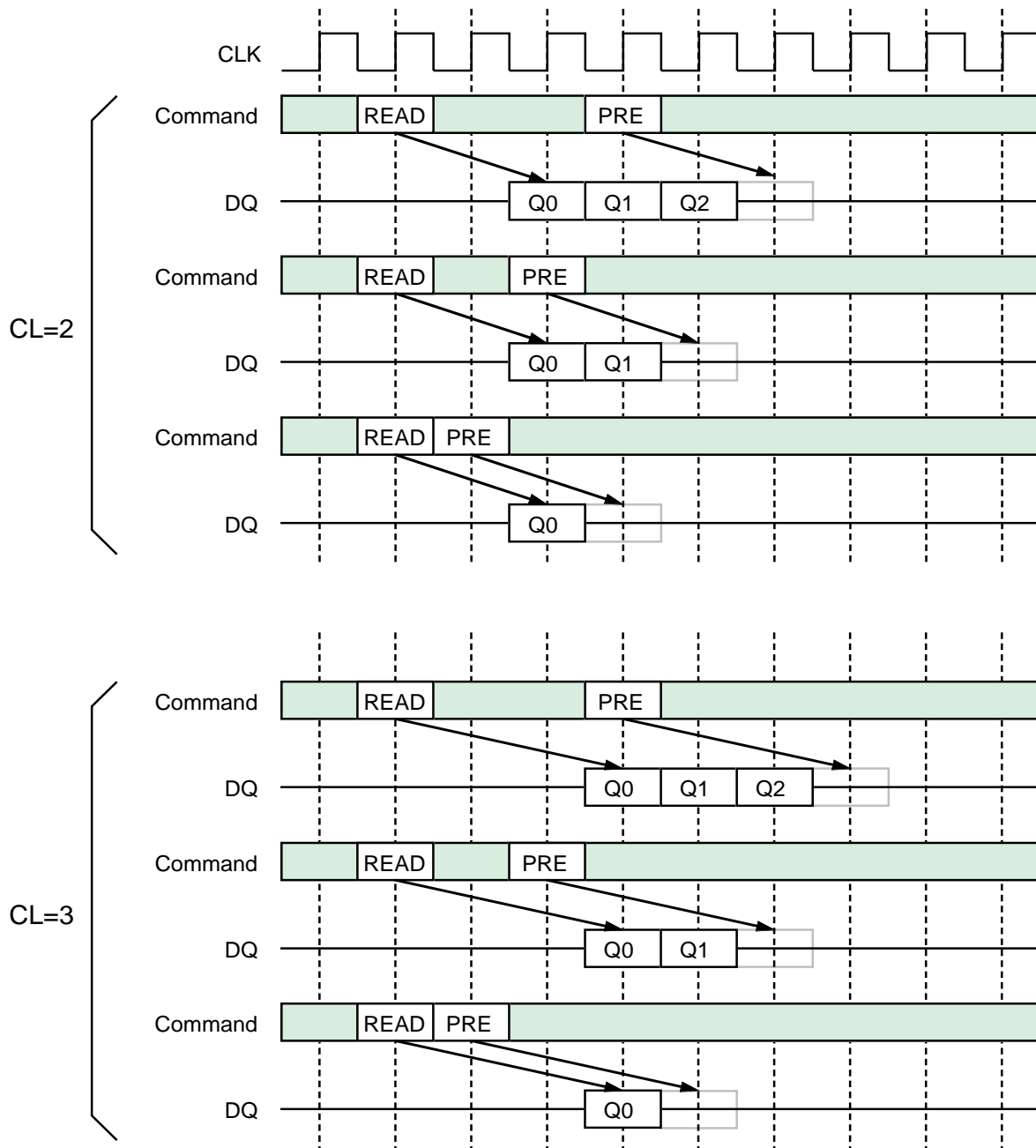
Burst read operation can be interrupted by write of any bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQM to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.



## [ Read Interrupted by Precharge ]

Burst read operation can be interrupted by precharge of the same bank. READ to PRE interval is minimum 1 CLK. A PRE command to output disable latency is equivalent to the /CAS Latency. As a result, READ to PRE interval determines valid data length to be output. The figure below shows examples of BL=4.

Read interrupted by Precharge (BL=4)







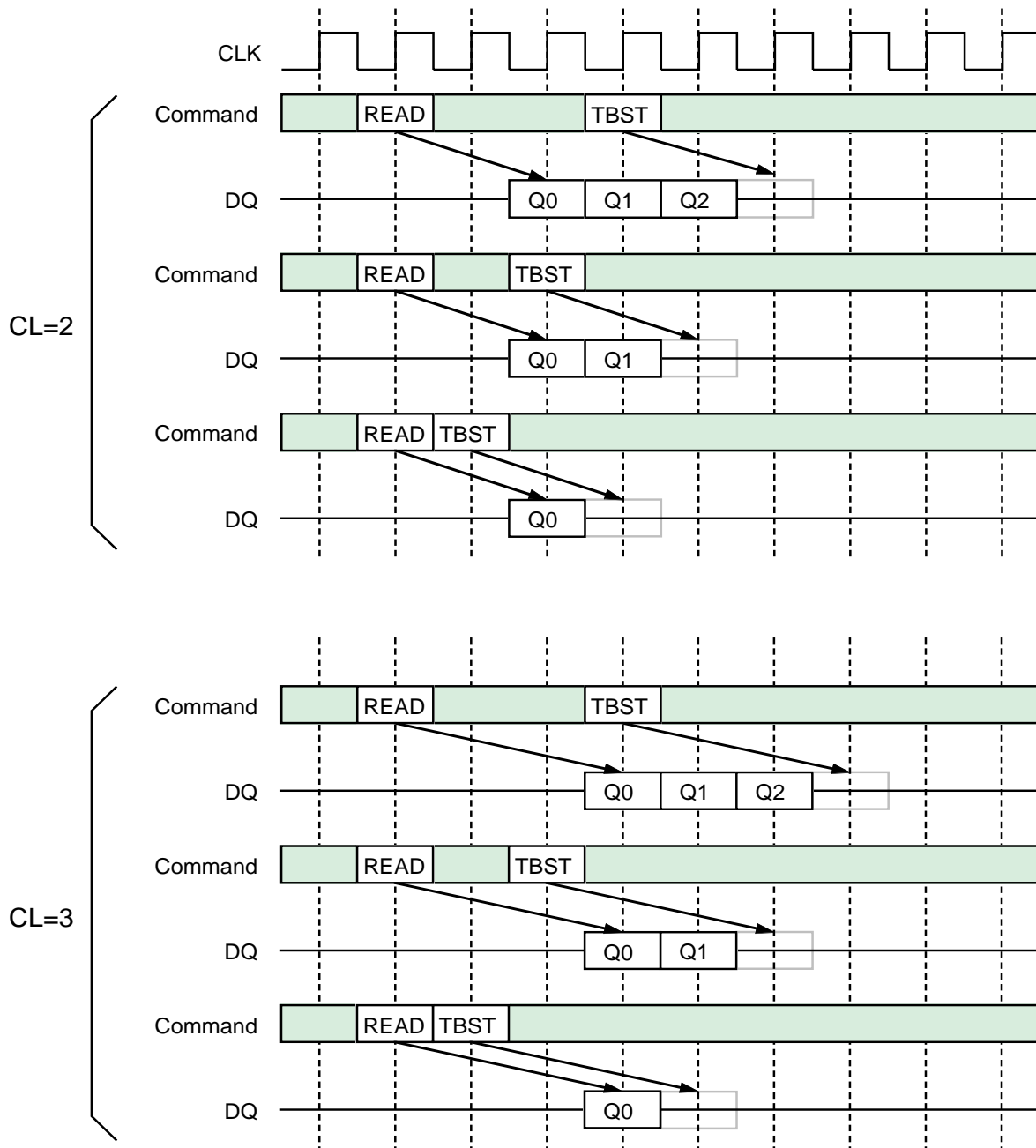
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## [Read Interrupted by Burst Terminate]

Similarly to the precharge, a burst terminate command can interrupt the burst read operation and disable the data output. The terminated bank remains active.

READ to TBST interval is minimum 1 CLK. A TBST command to output disable latency is equivalent to the /CAS Latency.

### Read interrupted by Terminate (BL=4)



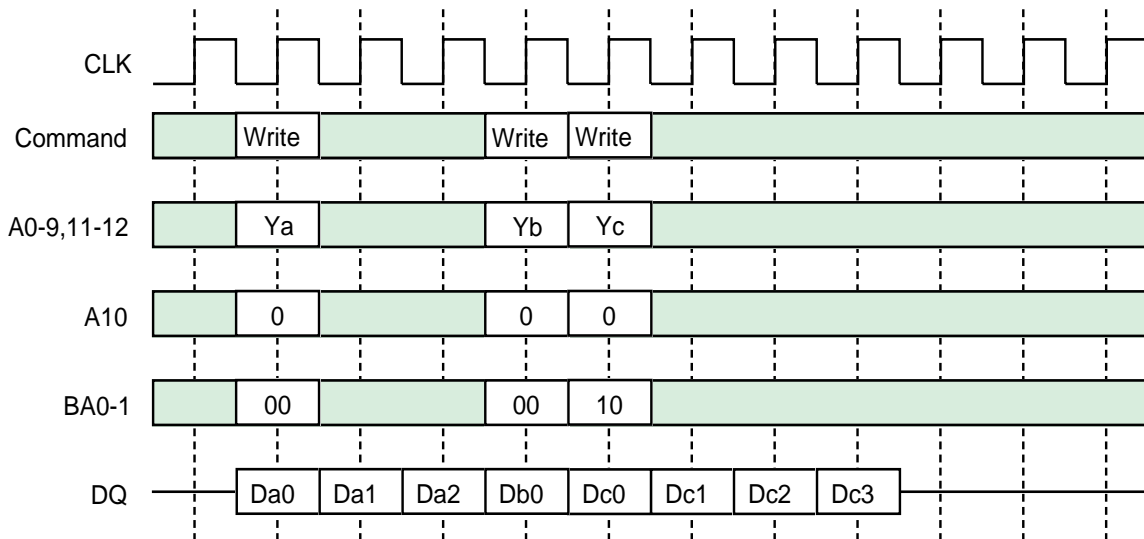


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## [ Write Interrupted by Write ]

Burst write operation can be interrupted by new write of any bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CLK.

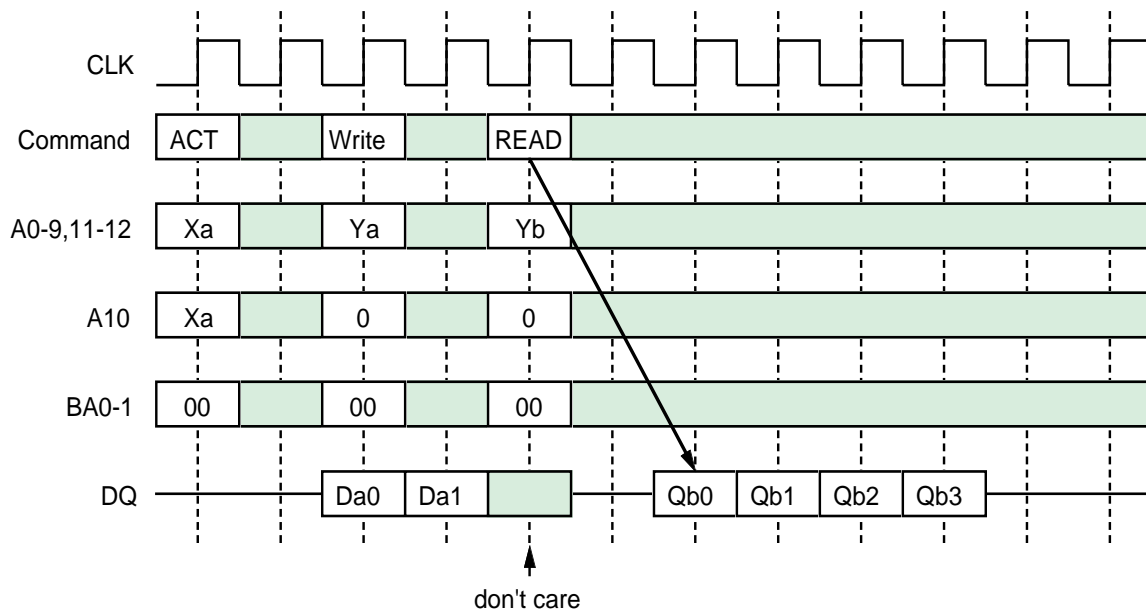
Write interrupted by Write (BL=4)



## [ Write Interrupted by Read ]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CLK. The input data on DQ at the interrupting READ cycle is "don't care".

Write interrupted by Read (CL=2, BL=4)



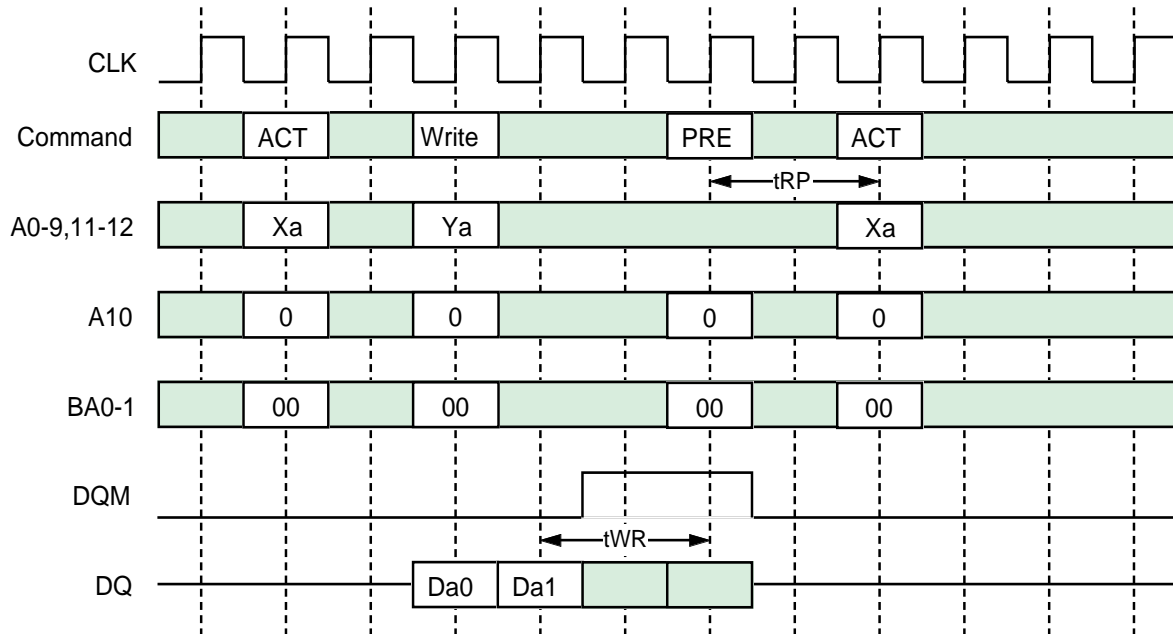


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## [ Write Interrupted by Precharge ]

Burst write operation can be interrupted by precharge of the same bank. Write recovery time ( $t_{WR}$ ) is required from the last data to PRE command. During write recovery, data inputs must be masked by DQM.

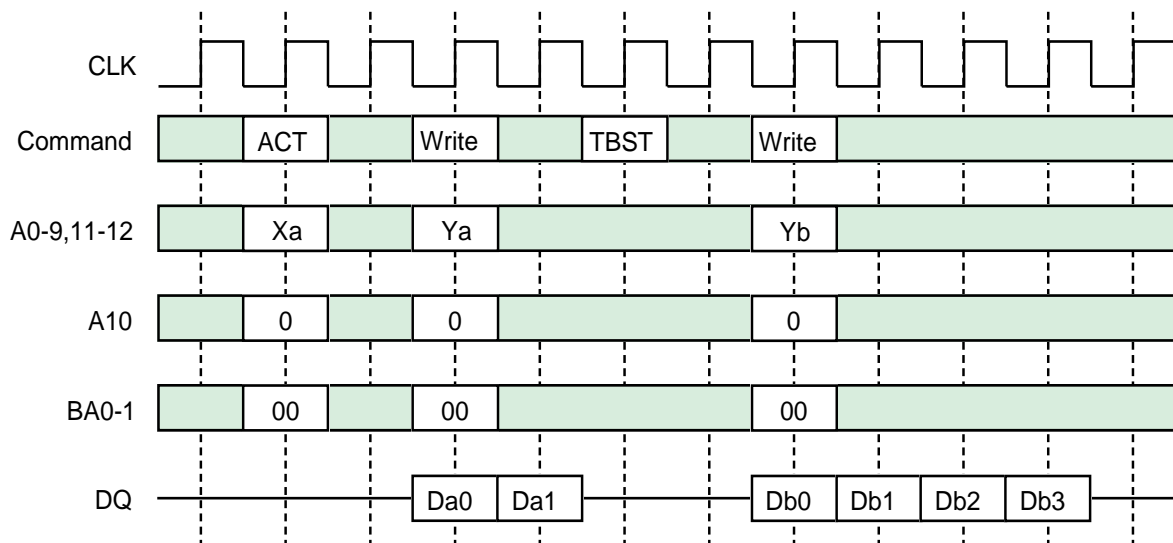
Write interrupted by Precharge (BL=4)



## [Write Interrupted by Burst Terminate]

Burst terminate command can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active. WRITE to TBST interval is minimum 1 CLK.

Write interrupted by Terminate (BL=4)



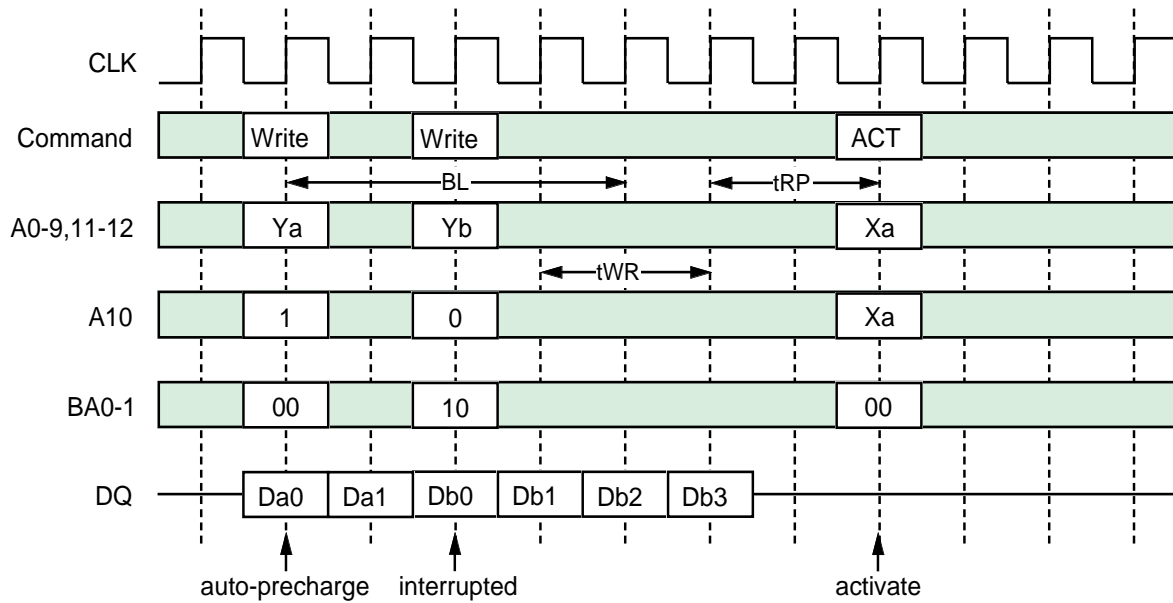


A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

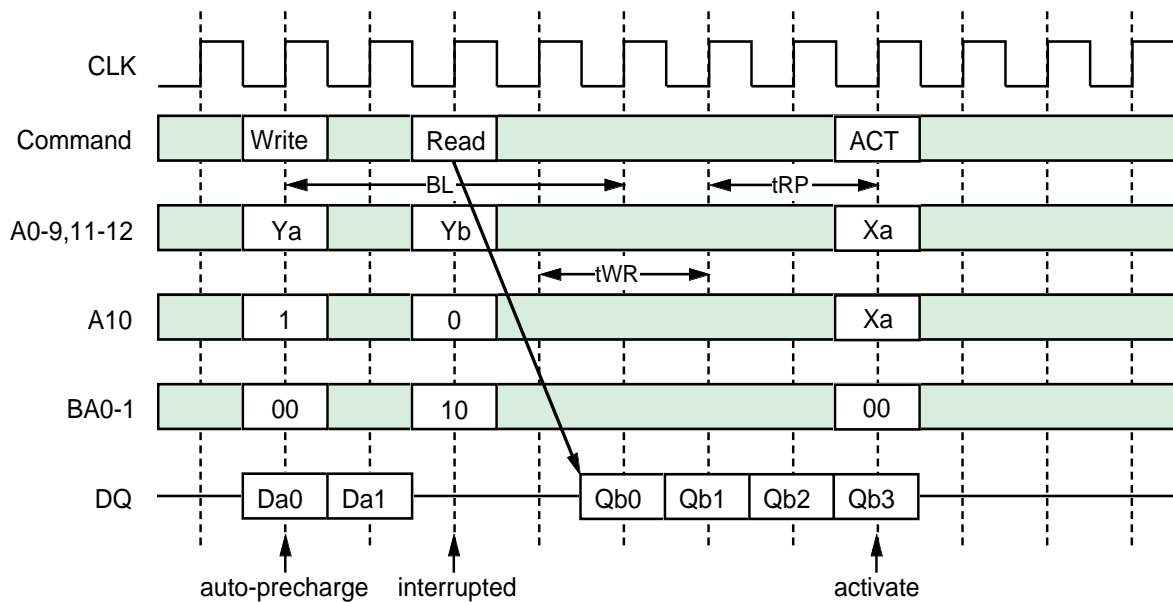
## [Write with Auto-Precharge Interrupted by Write or Read to another Bank]

Burst write with auto-precharge can be interrupted by write or read to another bank. Next ACT command can be issued after  $(BL+tWR-1+tRP)$  from the WRITEA. Auto-precharge interruption by a command to the same bank is inhibited.

### WRITEA interrupted by WRITE to another bank (BL=4)



### WRITEA interrupted by READ to another bank (CL=2, BL=4)



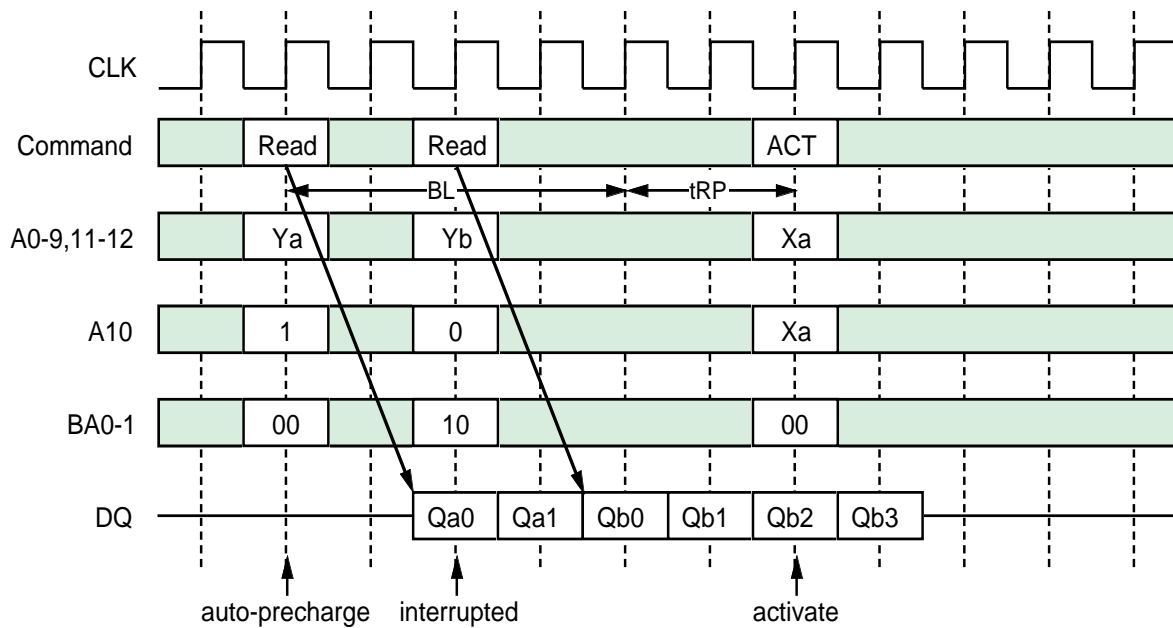


A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
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 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

### [Read with Auto-Precharge Interrupted by Read to another Bank]

Burst write with auto-precharge can be interrupted by write or read to another bank. Next ACT command can be issued after (BL+tRP) from the READA. Auto-precharge interruption by a command to the same bank is inhibited.

#### READA interrupted by READ to another bank (CL=2, BL=4)



### [Full Page Burst]

Full page burst length is available for only the sequential burst type. Full page burst read or write is repeated until a Precharge or a Burst Terminate command is issued. In case of the full page burst, a read or write with auto-precharge command is illegal.

### [Single Write]

When single write mode is set, burst length for write is always one, independently of Burst Length defined by (A2-0).



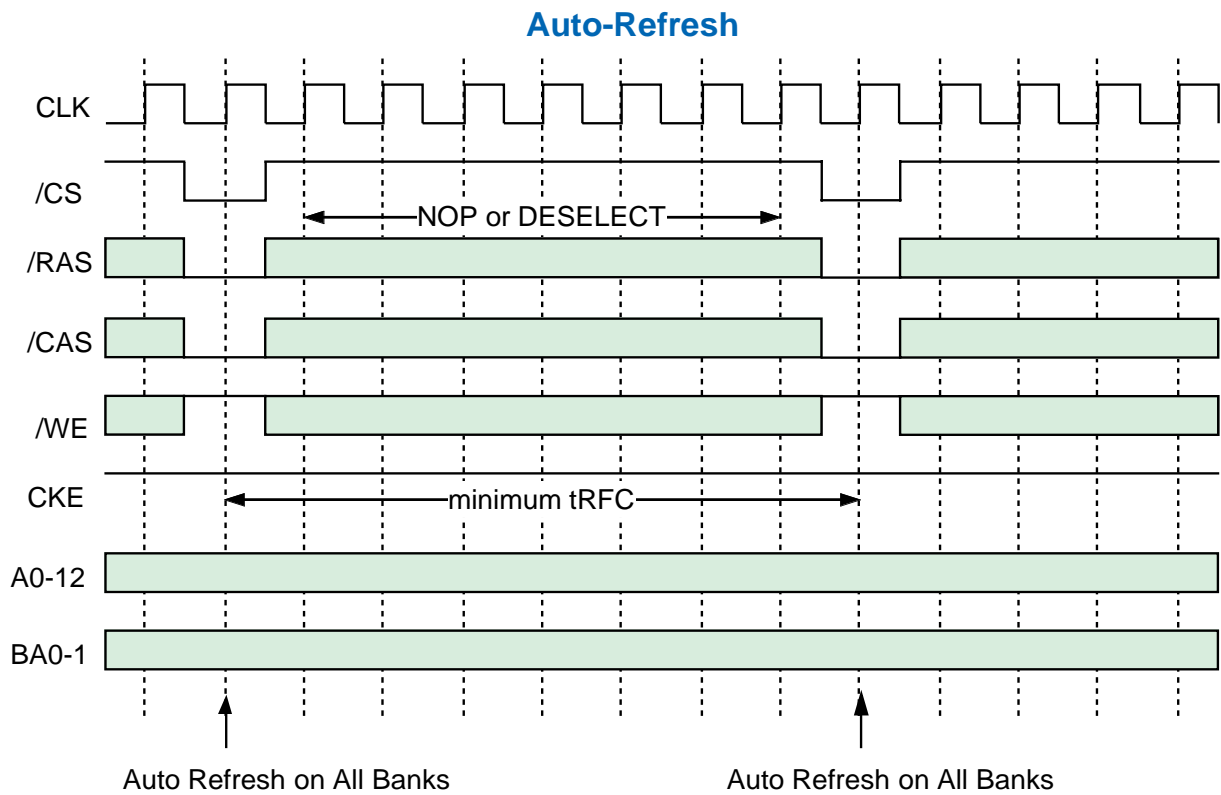
# 256Mb Synchronous DRAM

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## AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA (/CS= /RAS= /CAS= L, /WE= /CKE= H) command. The refresh address is generated internally. 8192 REFA cycles within 64ms refresh 256M bit memory cells. The auto-refresh is performed on 4 banks

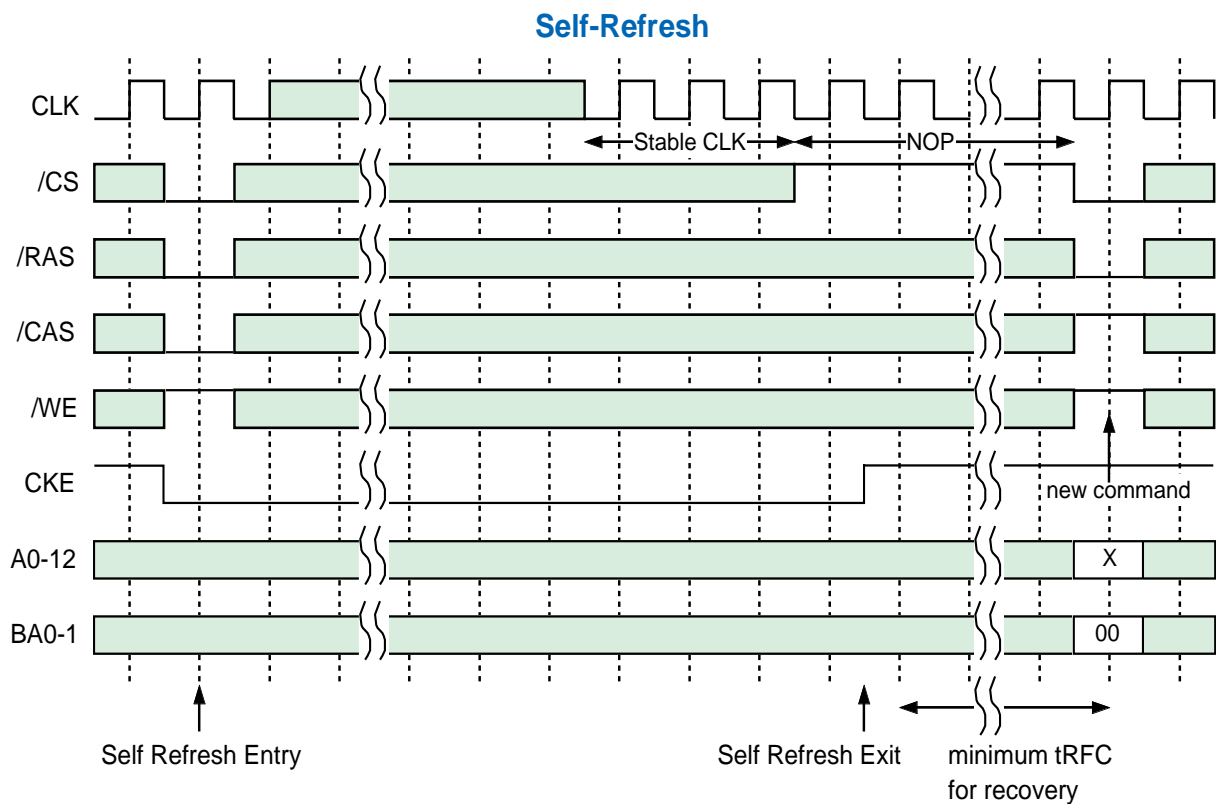
concurrently. Before performing an auto-refresh, all banks must be in the idle state. Auto-refresh to auto-refresh interval is minimum tRFC. Any command must not be supplied to the device before tRFC from the REFA command.



### SELF REFRESH

Self-refresh mode is entered by issuing a REFS command ( $/CS= /RAS= /CAS= L, /WE= H, CKE= L$ ). Once the self-refresh is initiated, it is maintained as long as CKE is kept low. During the self-refresh mode, CKE is asynchronous and the only enabled input. All other inputs including CLK are disabled and ignored, so that power consumption due to synchro-

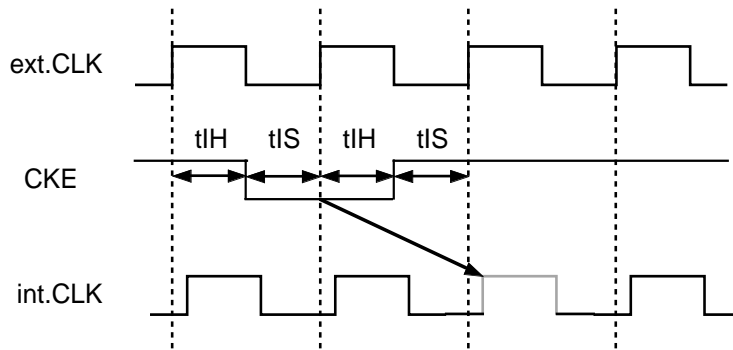
nous inputs is saved. To exit the self-refresh, supplying stable CLK inputs, asserting DESEL or NOP command and then asserting CKE=H. After tRFC from the 1st CLK edge following CKE=H, all banks are in the idle state and a new command can be issued, but DESEL or NOP commands must be asserted till then.



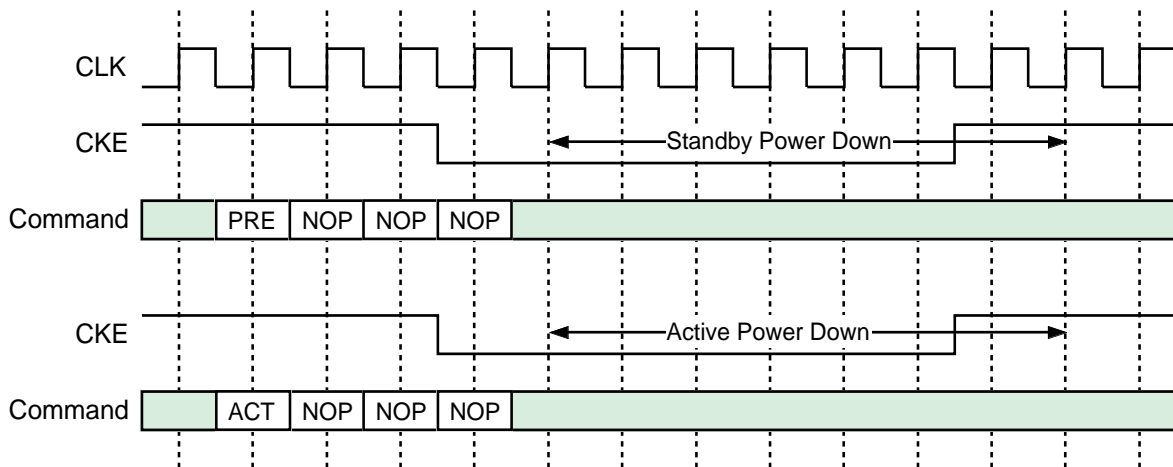
## CLK SUSPEND

CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input

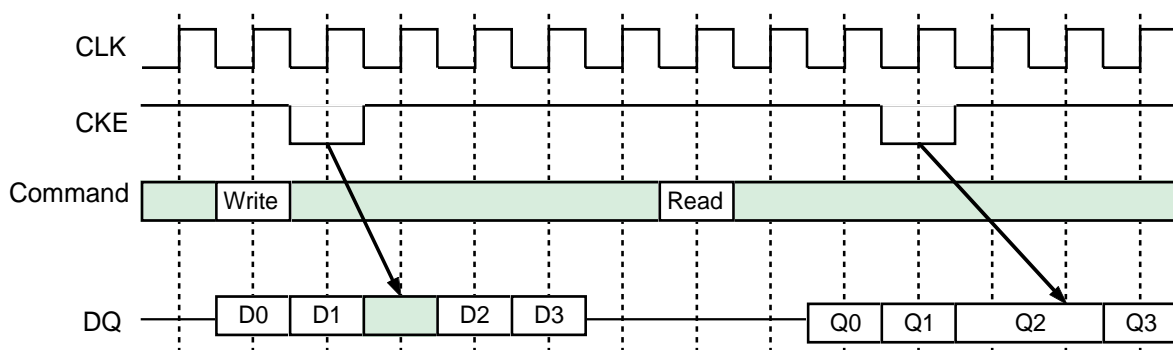
suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle. A command at the suspended cycle is ignored.



### Power Down by CKE



### DQ Suspend by CKE

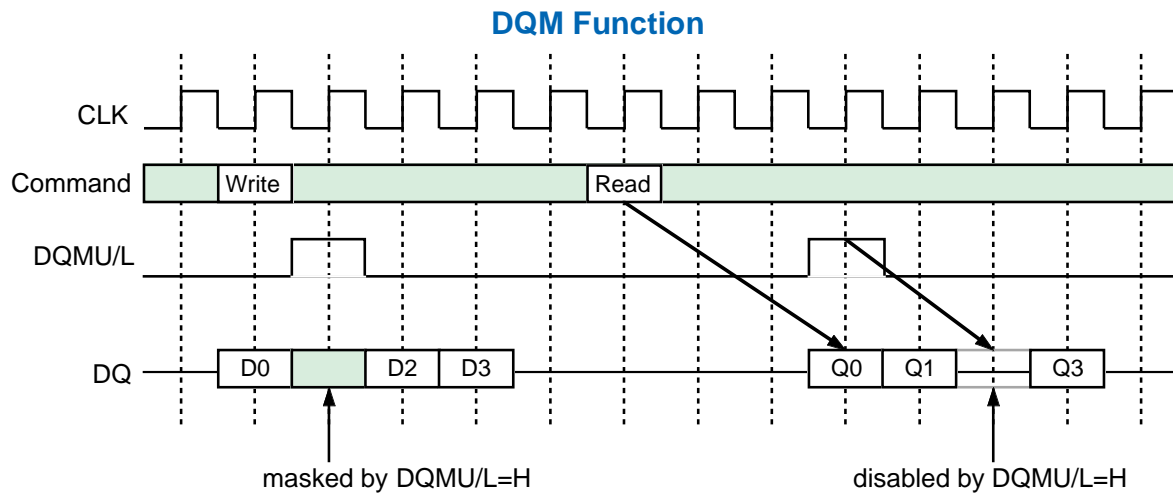




## DQM CONTROL

DQM is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQM(U,L) masks input data word by word. DQM(U,L)

to write mask latency is 0. During reads, DQM(U,L) forces output to Hi-Z word by word. DQM(U,L) to output Hi-Z latency is 2.



## 256Mb Synchronous DRAM

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A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

### ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter                 | Conditions           | Ratings    | Unit |
|--------|---------------------------|----------------------|------------|------|
| Vdd    | Supply Voltage            | with respect to Vss  | -0.5 - 4.6 | V    |
| VddQ   | Supply Voltage for Output | with respect to VssQ | -0.5 - 4.6 | V    |
| VI     | Input Voltage             | with respect to Vss  | -0.5 - 4.6 | V    |
| VO     | Output Voltage            | with respect to VssQ | -0.5 - 4.6 | V    |
| IO     | Output Current            |                      | 50         | mA   |
| Pd     | Power Dissipation         | Ta = 25°C            | 1000       | mW   |
| Topr   | Operating Temperature     |                      | 0 - 70     | °C   |
| Tstg   | Storage Temperature       |                      | -65 - 150  | °C   |

### RECOMMENDED OPERATING CONDITIONS

(Ta=0 - 70 °C ,unless otherwise noted)

| Symbol | Parameter                           | Limits |      |           | Unit |
|--------|-------------------------------------|--------|------|-----------|------|
|        |                                     | Min.   | Typ. | Max.      |      |
| Vdd    | Supply Voltage                      | 3.0    | 3.3  | 3.6       | V    |
| Vss    | Supply Voltage                      | 0      | 0    |           | V    |
| VddQ   | Supply Voltage for output           | 3.0    | 3.3  | 3.6       | V    |
| VssQ   | Supply Voltage for output           | 0      | 0    | 0         | V    |
| VIH*1  | High-Level Input Voltage all inputs | 2.0    |      | VddQ +0.3 | V    |
| VIL*2  | Low-level Input Voltage all inputs  | -0.3   |      | 0.8       | V    |

### CAPACITANCE

(Ta=0 -70°C,Vdd=VddQ=3.3±0.3V,Vss=VssQ=0V,unless otherwise noted)

| Symbol | Parameter                      | Test Condition                                 | Limits (min.) | Limits (max.) |        | Unit |
|--------|--------------------------------|--|---------------|---------------|--------|------|
|        |                                |  |               | -6/-7E/-7     | -75/-8 |      |
| CI(A)  | Input Capacitance, address pin | @ 1MHz<br>1.4V bias<br>200mV swing<br>Vcc=3.3V | 2.5           | 3.8           | 5.0    | pF   |
| CI(C)  | Input Capacitance, control pin |  | 2.5           | 3.8           | 5.0    | pF   |
| CI(K)  | Input Capacitance, CLK pin     |  | 2.5           | 3.5           | 4.0    | pF   |
| CI/O   | Input Capacitance, I/O pin     |  | 4.0           | 6.5           | 6.5    | pF   |

## AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 - 70°C, Vdd=VddQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

| ITEM   | Symbol |  | Organi-<br>zation | Limits (max.)    |     |     |     |     | Unit | Note |
|--|--------|--|-------------------|------------------|-----|-----|-----|-----|------|------|
|  |        |  |                   | -6               | -7E | -7  | -75 | -8  |      |      |
| Operating current                                | Icc1   | tRC=min, tCLK=min<br>BL=1, IOL=0mA                   | x4                | 100              | 100 | 100 | 100 | 95  | mA   | 1    |
|  |        |  | x8                | 110              | 110 | 110 | 110 | 100 |      |      |
|  |        |  | x16               | 130              | 130 | 130 | 130 | 120 |      |      |
| Precharge Standby current in Non-Power down mode | Icc2N  | CKE=VILmax<br>tCLK=15ns                              | x4/x8/x16         | 20               | 20  | 20  | 20  | 20  | mA   | 2,3  |
|  | Icc2NS | CKE=VIHmin<br>CLK=VILmax(fixed)                      | x4/x8/x16         | 15               | 15  | 15  | 15  | 15  |      |      |
| Precharge Standby current in Power down mode     | Icc2P  | CKE=VIHmin<br>tCLK=15ns(Note)                        | x4/x8/x16         | 2                | 2   | 2   | 2   | 2   | mA   | 2    |
|  | Icc2PS | CKE=VIHmin<br>tCLK=VILmax(fixed)                     | x4/x8/x16         | 1                | 1   | 1   | 1   | 1   |      |      |
| Active Standby current                           | Icc3N  | CKE=/CS=VIHmin<br>tCLK=15ns(Note)                    | x4/x8/x16         | 30               | 30  | 30  | 30  | 30  | mA   | 3,5  |
|  | Icc3NS | CKE=VIHmin<br>tCLK=VILmax(fixed)                     | x4/x8/x16         | 20               | 20  | 20  | 20  | 20  |      |      |
| Burst current                                    | Icc4   | All Bank Active<br>tCLK = min<br>BL=4, CL=3, IOL=0mA | x4                | 140              | 140 | 140 | 140 | 110 | mA   | 5    |
|  |        |  | x8                | 150              | 150 | 150 | 150 | 120 |      |      |
|  |        |  | x16               | 160              | 160 | 160 | 160 | 130 |      |      |
| Auto-refresh current                             | Icc5   | tRC=min, tCLK=min                                    | x4/x8/x16         | 160              | 160 | 160 | 160 | 160 | mA   |      |
| Self-refresh current                             | Icc6   | CKE < 0.2V   | x4/x8/x16         | -6,-7E,-7,-75,-8 | 3   | 3   | 3   | 3   |      |      |

### NOTE:

- 1.address are changed 3 times during tRC , only 1 bank is active & all other banks are idle
- 2.all banks are idle
- 3.input signals are changed one time during 3x tCLK
- 4.input signals are stable
- 5.all banks are active

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0 - 70°C, Vdd=VddQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

| Symbol   | Parameter                      | Test Conditions         | Limits |      | unit |
|----------|--------------------------------|-------------------------|--------|------|------|
|          |                                |                         | Min.   | Max. |      |
| VOH (DC) | High-Level Output Voltage (DC) | IOH=-2mA                | 2.4    |      | V    |
| VOL (DC) | Low-level Output Voltage (DC)  | IOL= 2mA                |        | 0.4  | V    |
| IOZ      | Off-state Output Current       | Q floating VO=0 -- VddQ | -10    | 10   | µA   |
| Ii       | Input Current                  | VIH = 0 -- VddQ +0.3V   | -10    | 10   | µA   |

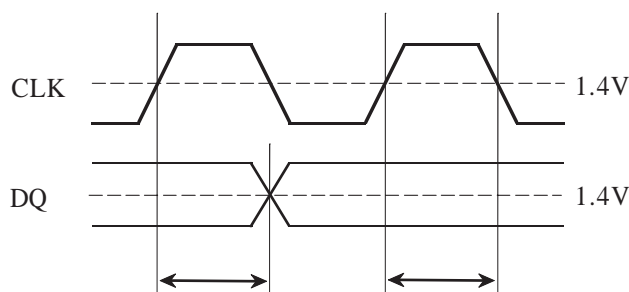
## AC TIMING REQUIREMENTS

(Ta=0 - 70°C, Vdd=VddQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

Input Pulse Levels:0.8V-2.0V

Input Timing Measurement Level:1.4V

| Symbol | Parameter                     | Limits |      |      |      |      |      |      |      |      |      | Unit |    |
|--------|-------------------------------|--------|------|------|------|------|------|------|------|------|------|------|----|
|        |                               | -6     |      | -7E  |      | -7   |      | -75  |      | -8   |      |      |    |
|        |                               | Min.   | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |    |
| tCLK   | CLK cycle time                | CL=2   | -    |      | 7    |      | -    |      | 10   |      | 10   |      | ns |
|        |                               | CL=3   | 6    |      | 7    |      | 7    |      | 7.5  |      | 8    |      | ns |
| tCH    | CLK High pulse width          | 2      |      | 2.5  |      | 2.5  |      | 2.5  |      | 3    |      | ns   |    |
| tCL    | CLK Low pulse width           | 2      |      | 2.5  |      | 2.5  |      | 2.5  |      | 3    |      | ns   |    |
| tT     | Transition time of CLK        | 1      | 10   | 1    | 10   | 1    | 10   | 1    | 10   | 1    | 10   | ns   |    |
| tIS    | Input Setup time (all inputs) | 1.8    |      | 1.8  |      | 1.8  |      | 1.8  |      | 2    |      | ns   |    |
| tIH    | Input Hold time (all inputs)  | 1      |      | 1    |      | 1    |      | 1    |      | 1    |      | ns   |    |
| tRC    | Row Cycle time                | 60     |      | 63   |      | 63   |      | 67.5 |      | 70   |      | ns   |    |
| tRFC   | Refresh Cycle Time            | 60     |      | 70   |      | 70   |      | 75   |      | 80   |      | ns   |    |
| tRCD   | Row to Column Delay           | 15     |      | 20   |      | 20   |      | 20   |      | 20   |      | ns   |    |
| tRAS   | Row Active time               | 42     | 120K | 45   | 120K | 45   | 120K | 45   | 120K | 48   | 120K | ns   |    |
| tRP    | Row Precharge time            | 15     |      | 20   |      | 20   |      | 20   |      | 20   |      | ns   |    |
| tWR    | Write Recovery time           | 12     |      | 14   |      | 14   |      | 15   |      | 20   |      | ns   |    |
| tRRD   | Act to Act Delay time         | 12     |      | 14   |      | 14   |      | 15   |      | 20   |      | ns   |    |
| tRSC   | Mode Register Set Cycle time  | 12     |      | 14   |      | 14   |      | 15   |      | 20   |      | ns   |    |
| tREF   | Refresh Interval time         |        | 7.8  |      | 7.8  |      | 7.8  |      | 7.8  |      | 7.8  | us   |    |



Any AC timing is referenced to the input signal passing through 1.4V.



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## SWITCHING CHARACTERISTICS

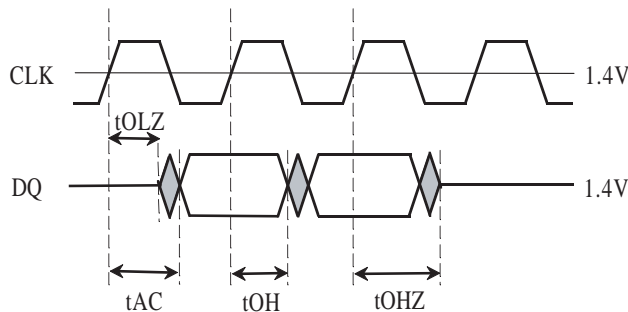
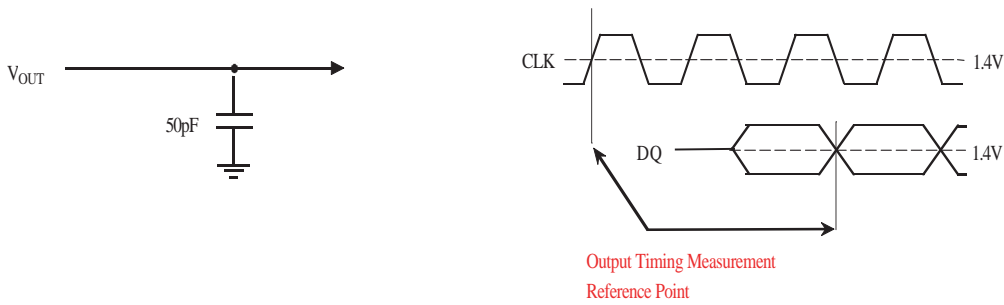
(Ta=0 - 70°C, Vdd=VddQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

| Symbol | Parameter                                  | Limits |      |      |      |      |      |      |      |      |      | Unit | Note |
|--------|--|--------|------|------|------|------|------|------|------|------|------|------|------|
|        |  | -6     |      | -7E  |      | -7   |      | -75  |      | -8   |      |      |      |
|        |  | Min.   | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |      |
| tAC    | Access time from CLK                       | CL=2   |      |      | 5.4  |      |      |      | 6    |      | 6    | ns   | *1   |
|        |  | CL=3   |      | 5    | 5.4  |      | 5.4  |      | 5.4  |      | 6    | ns   |      |
| tOH    | Output Hold time from CLK                  | CL=2   |      |      | 2.7  |      |      | 3    |      | 3    |      | ns   |      |
|        |  | CL=3   | 2.5  |      | 2.7  |      | 2.7  |      | 3    |      | 3    | ns   |      |
| tOLZ   | Delay time, output low-impedance from CLK  | 0      |      | 0    |      | 0    |      | 0    |      | 0    |      | ns   |      |
| tOHZ   | Delay time, output high-impedance from CLK | 2.5    | 5    | 2.7  | 5.4  | 2.7  | 5.4  | 3    | 5.4  | 3    | 6    | ns   |      |

NOTE:

1. If clock rising time is longer than 1ns, (tr/2-0.5ns) should be added to the parameter.

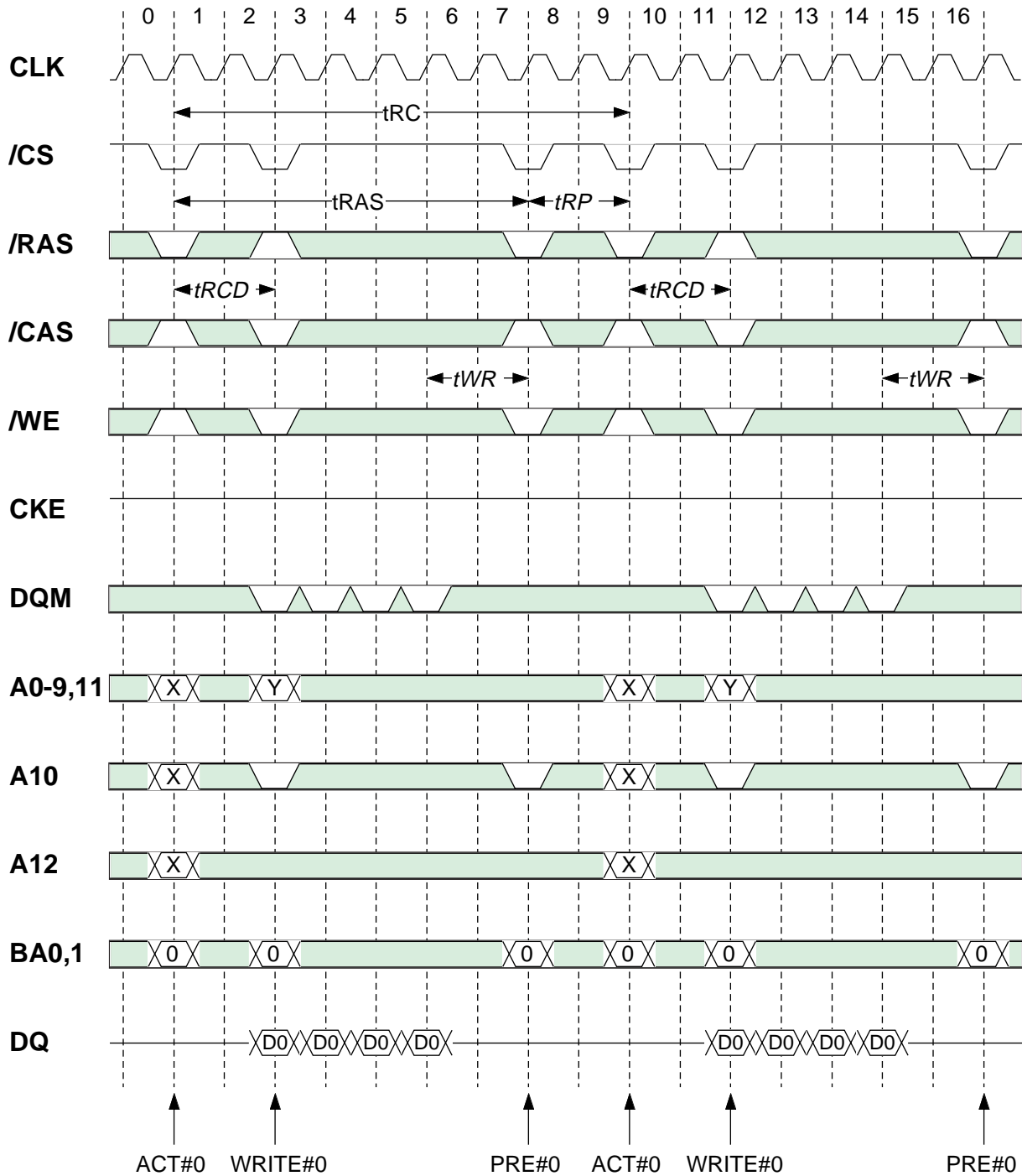
## Output Load Condition



# 256Mb Synchronous DRAM

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## Burst Write (Single Bank) [BL=4]

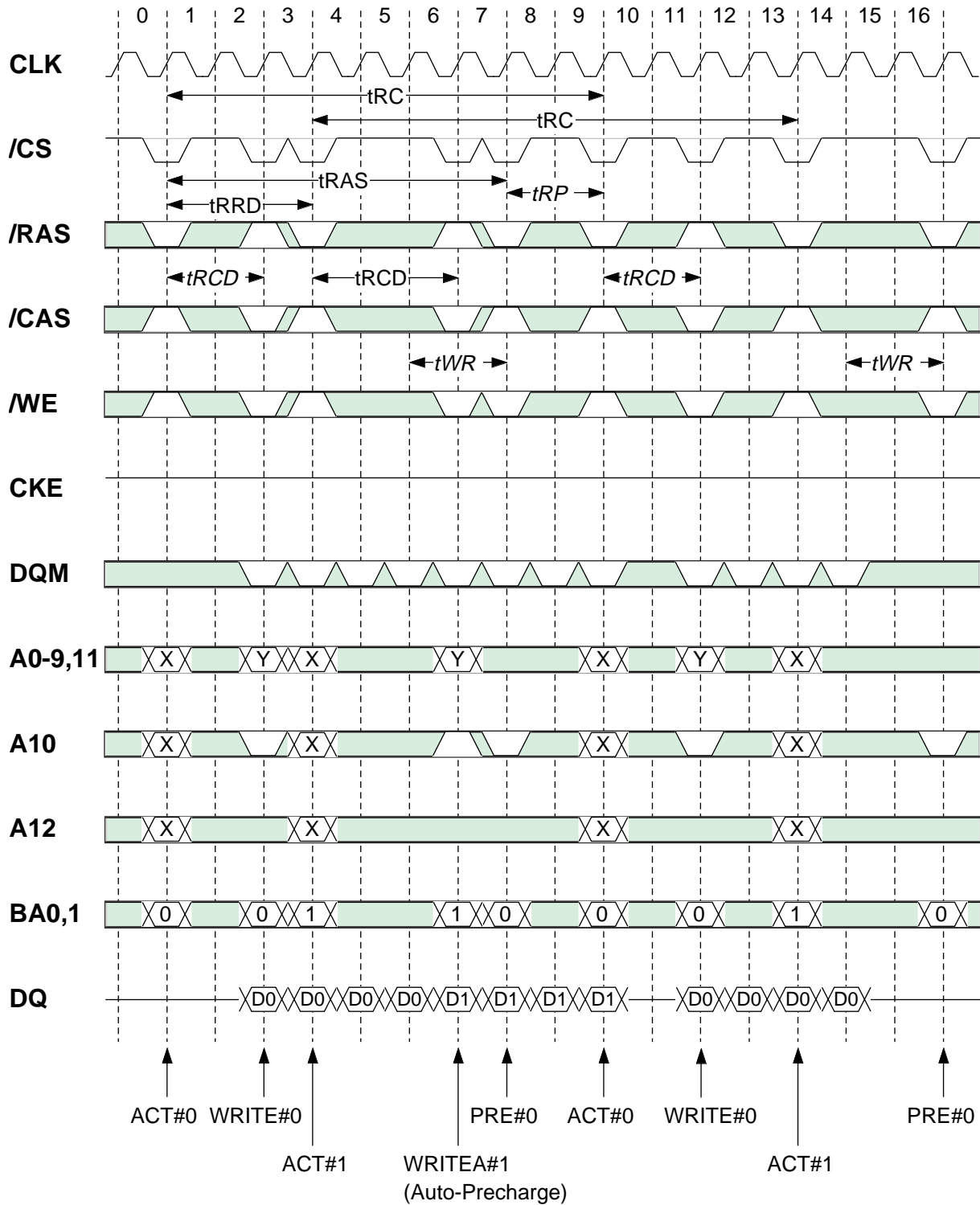


*Italic parameter* shows minimum case



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## Burst Write (Multi Bank) [BL=4]



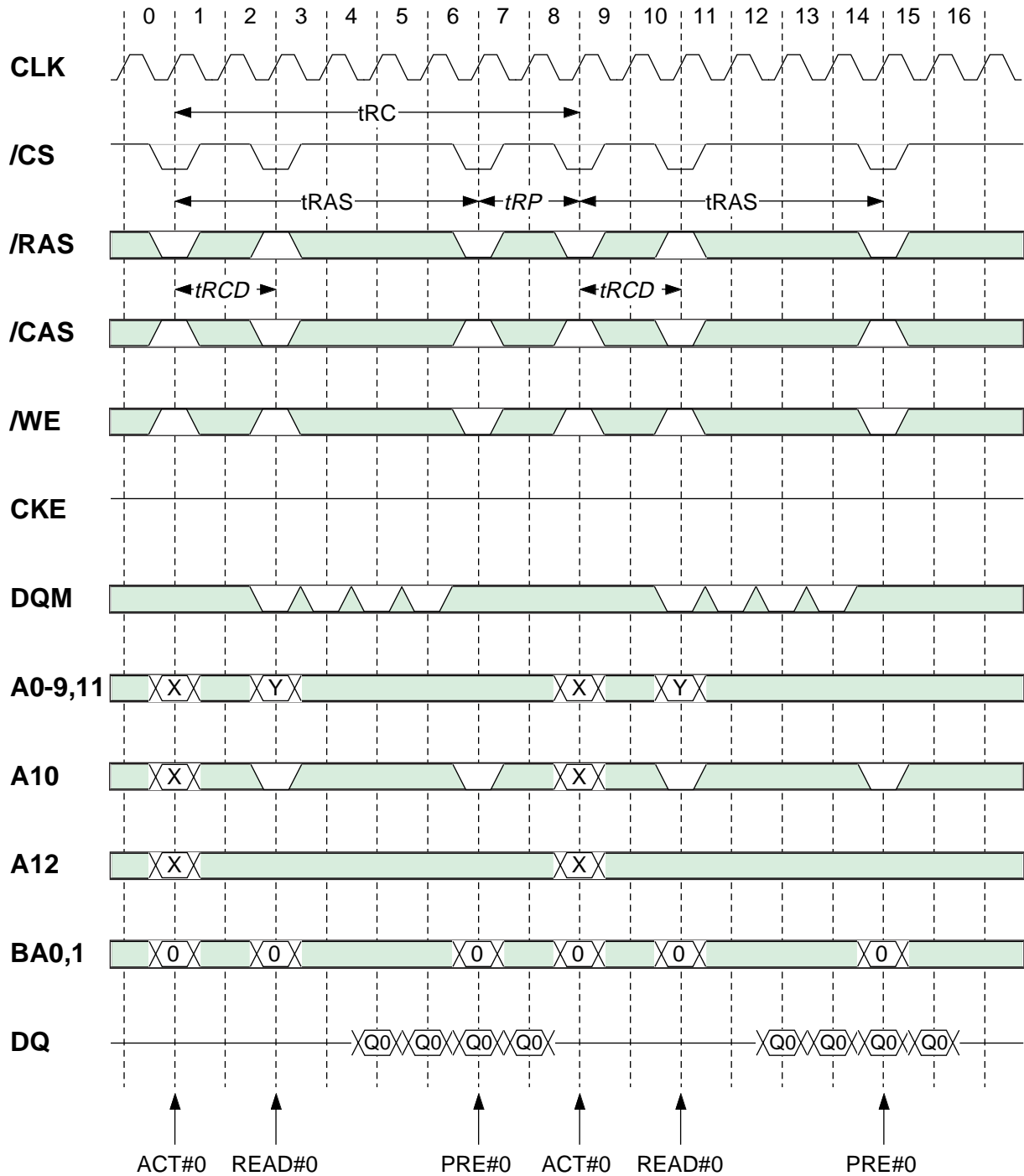
*Italic parameter* shows minimum case

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## Burst Read (Single Bank) [CL=2, BL=4]



*Italic parameter* shows minimum case

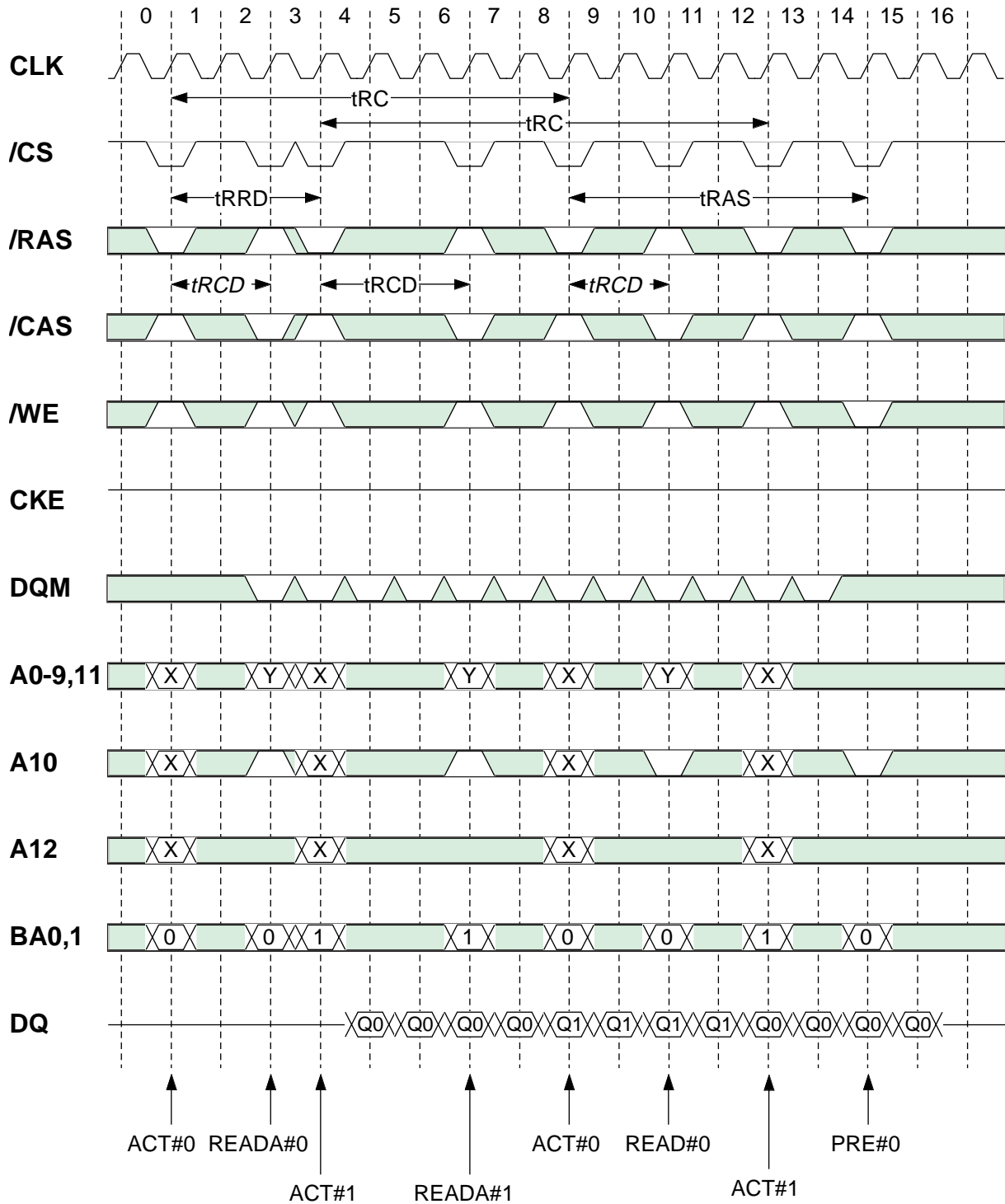


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## Burst Read (Multi Bank) [CL=2, BL=4]



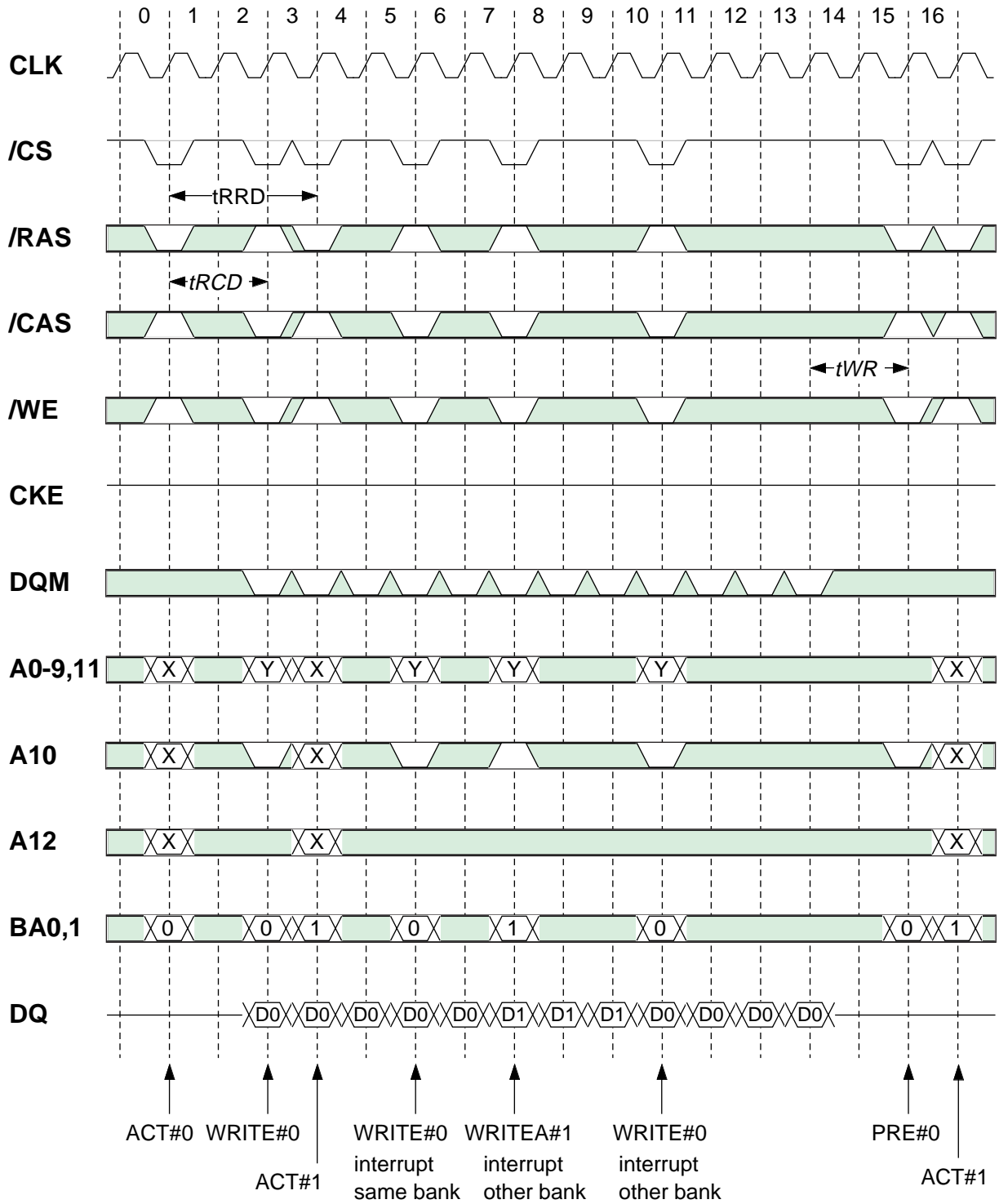
*Italic parameter* shows minimum case

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## Write Interrupted by Write [BL=4]

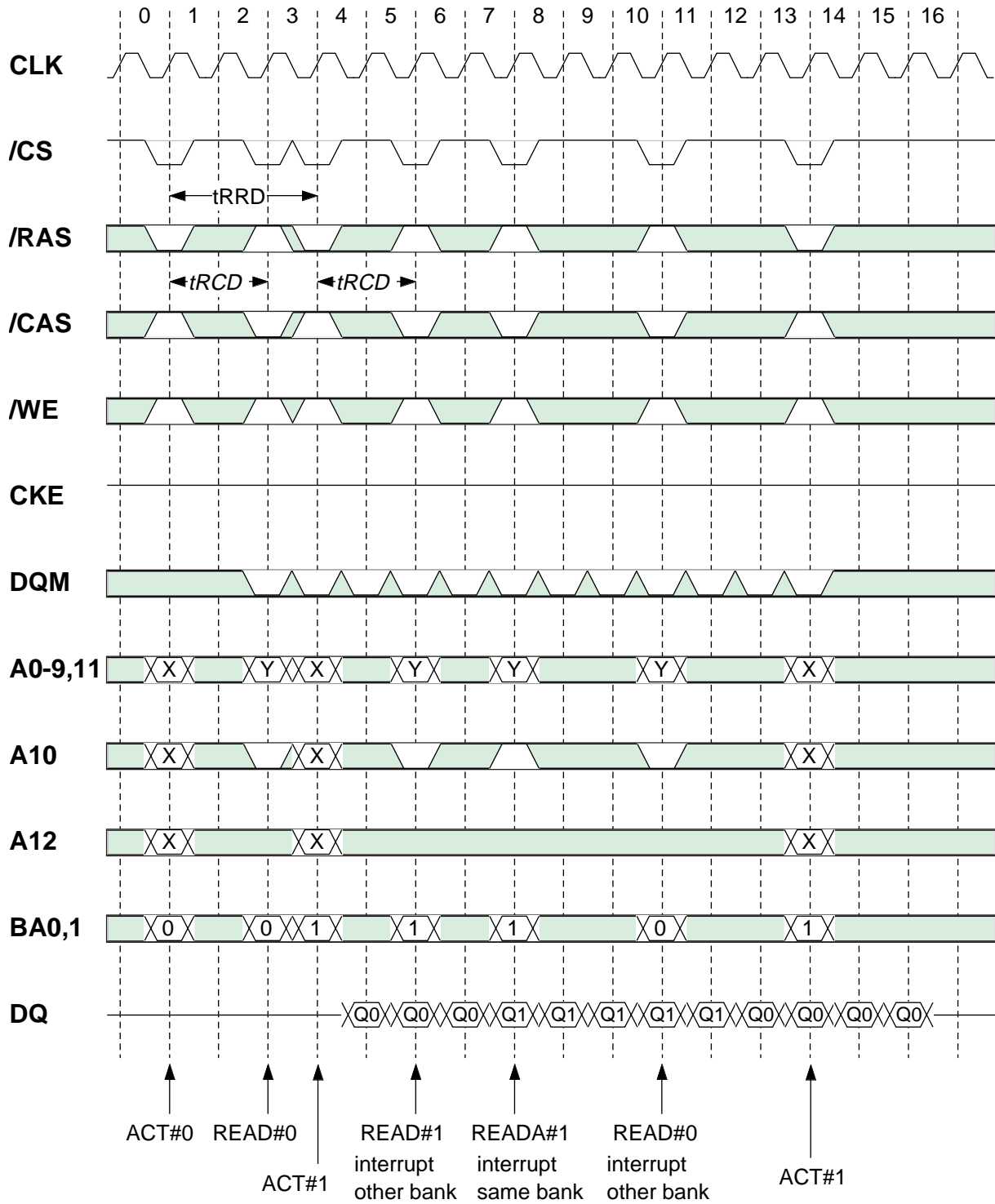


*Italic parameter* shows minimum case



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## Read Interrupted by Read [CL=2, BL=4]

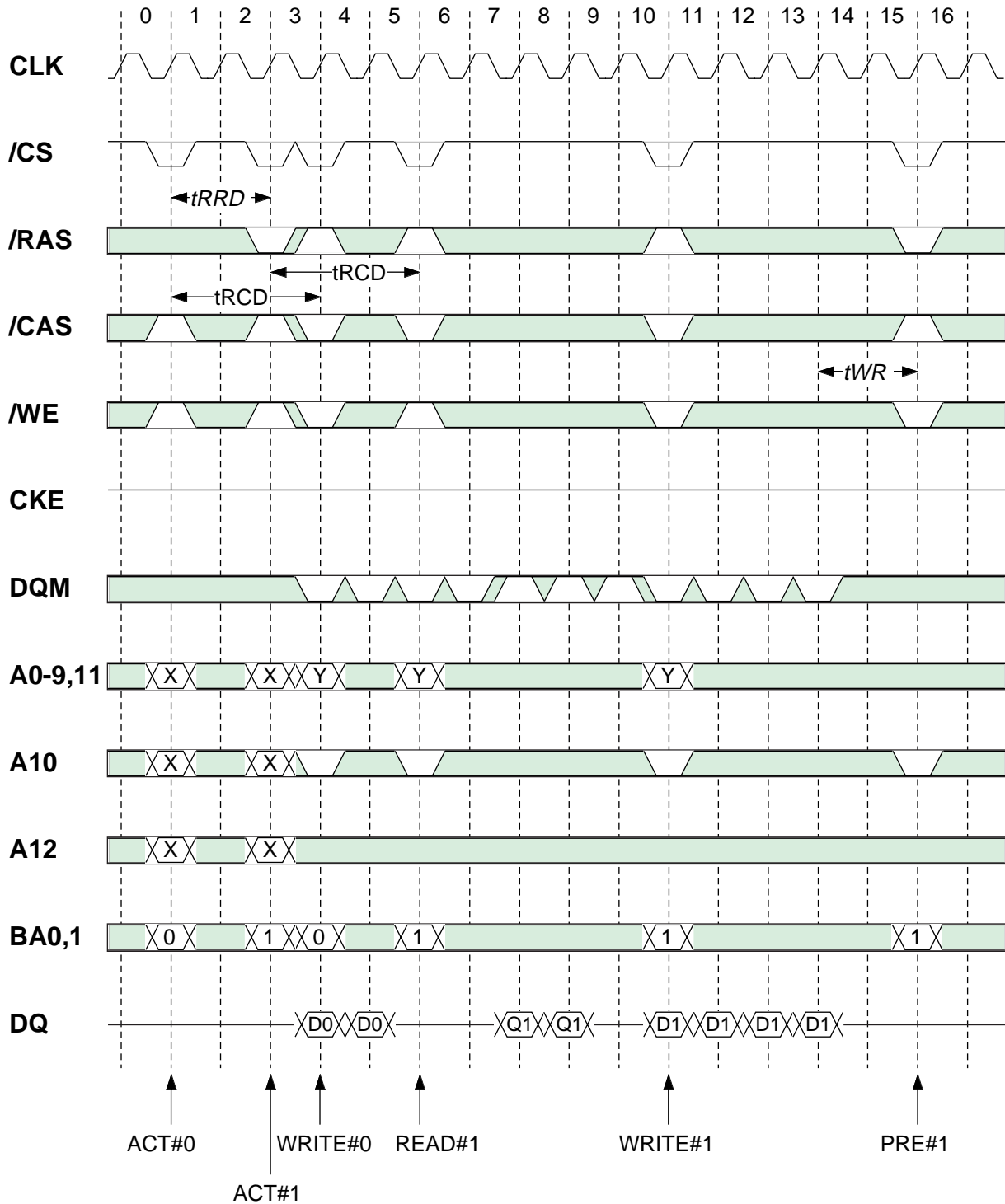


*Italic parameter* shows minimum case

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## Write Interrupted by Read, Read Interrupted by Write [CL=2, BL=4]



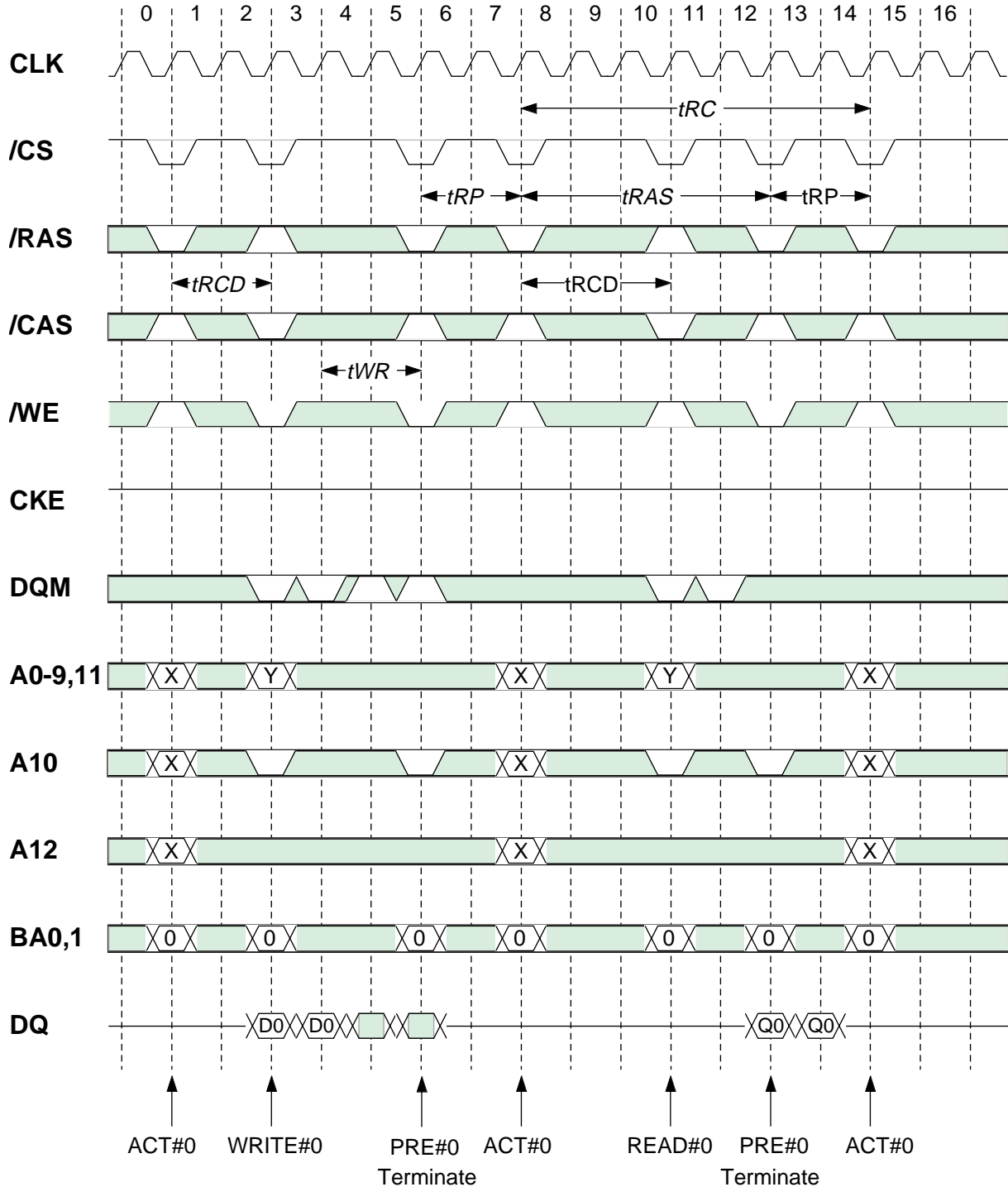
*Italic parameter* shows minimum case



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## Write / Read Terminated by Precharge [CL=2, BL=4]



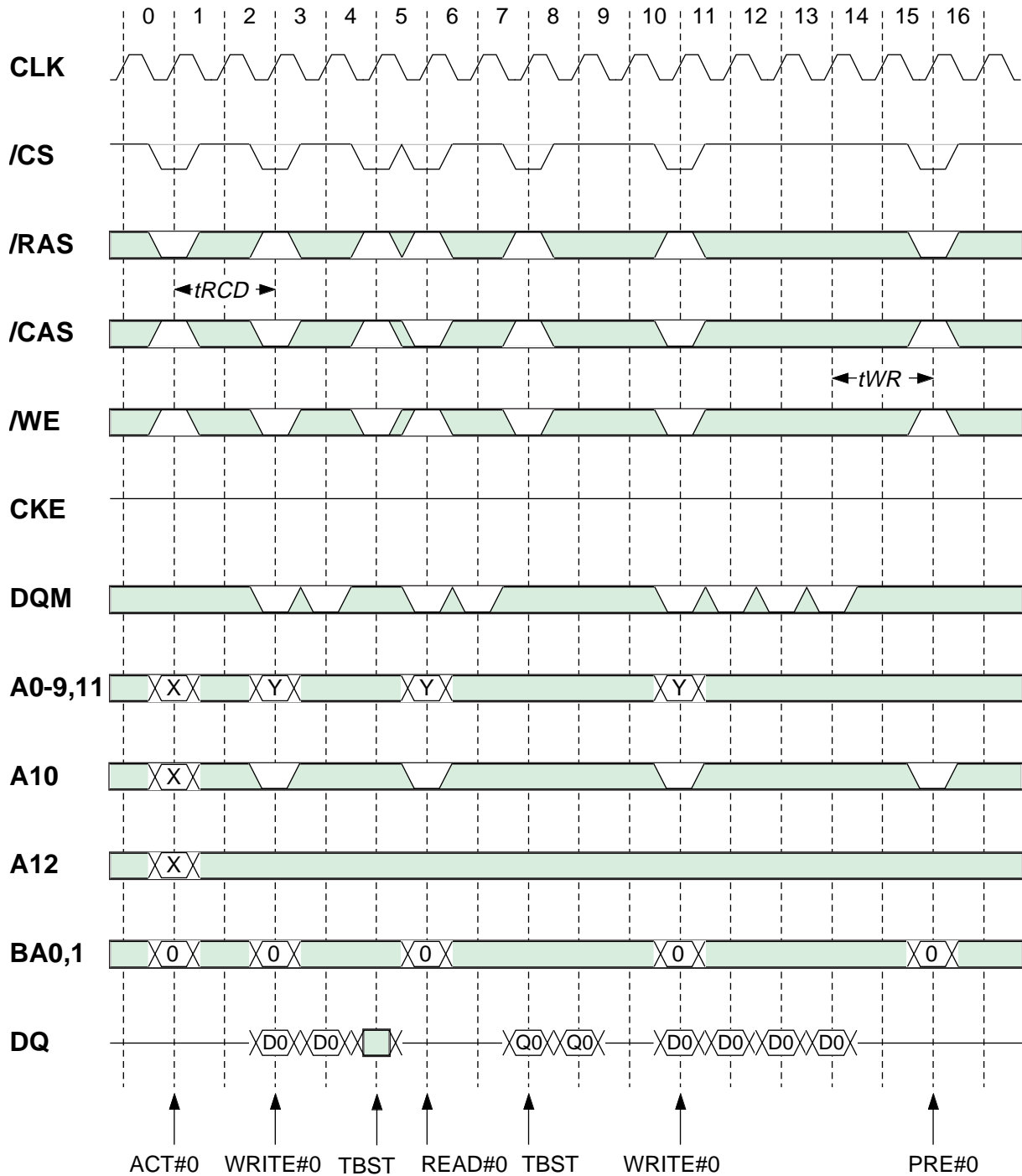
*Italic parameter* shows minimum case



# 256Mb Synchronous DRAM

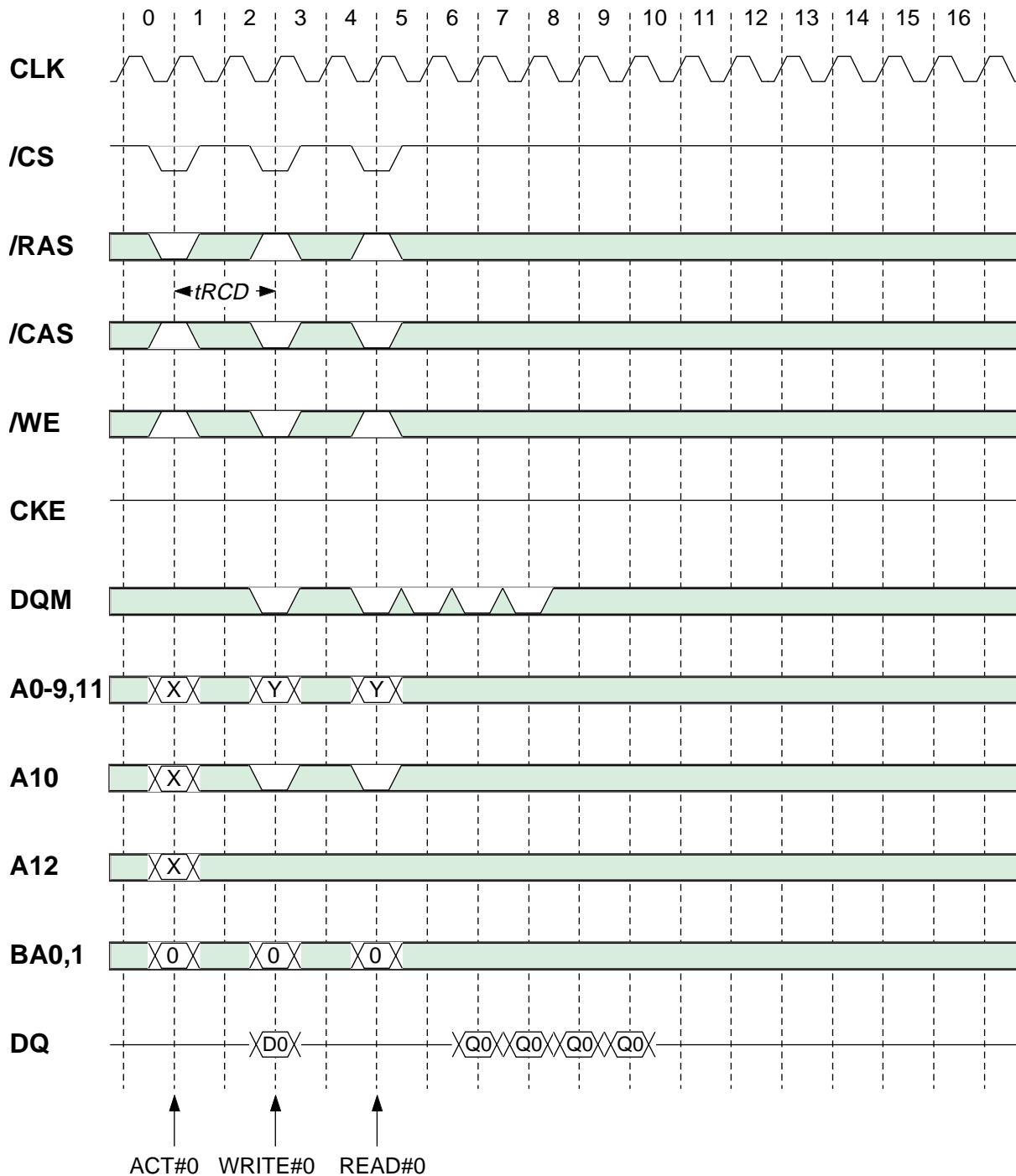
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## Write / Read Terminated by Burst Terminate [CL=2, BL=4]



*Italic parameter* shows minimum case

## Single Write Burst Read [CL=2, BL=4]



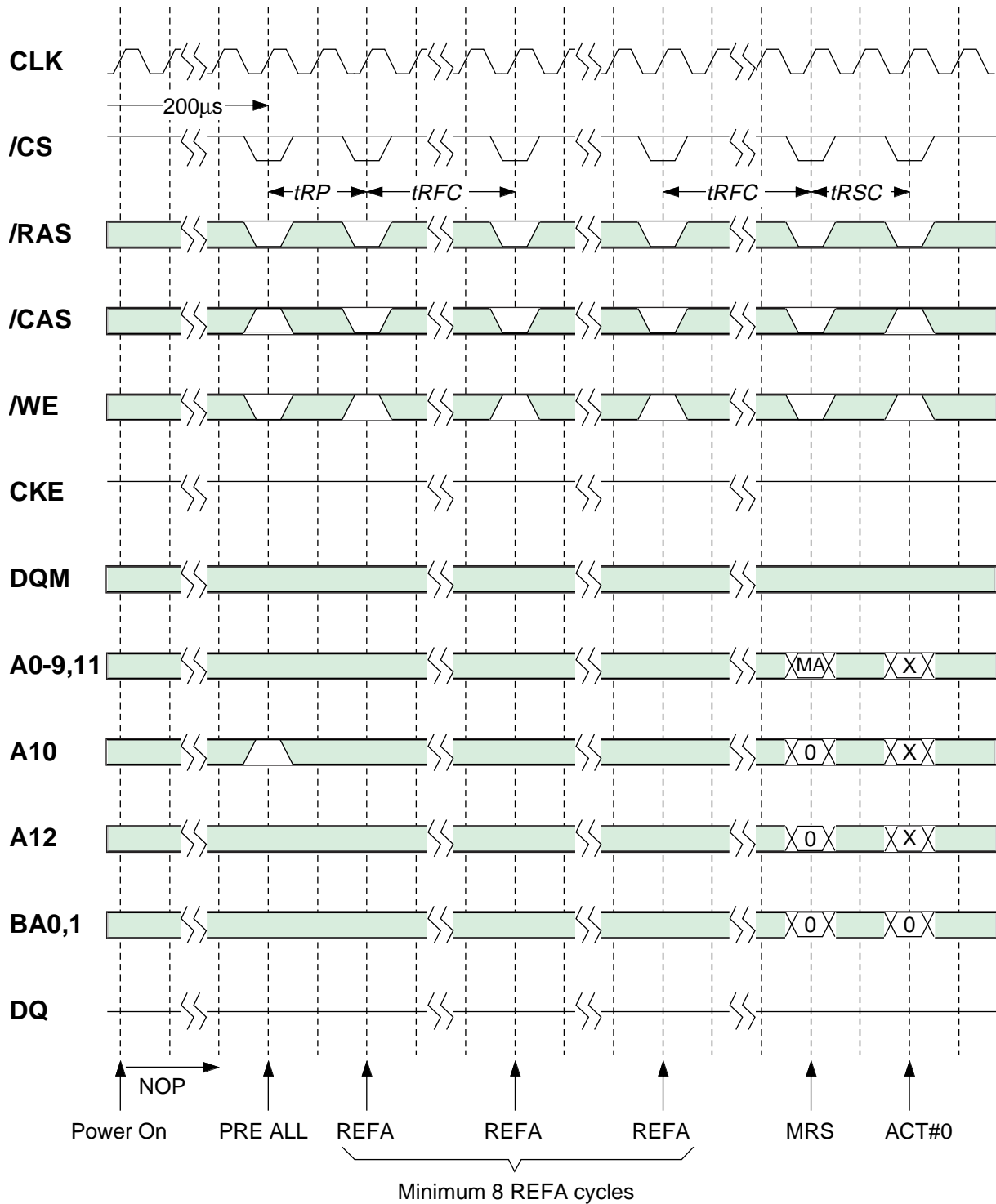
*Italic parameter* shows minimum case



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## Power-Up Sequence and Intialize



*Italic paramater* shows minimum case

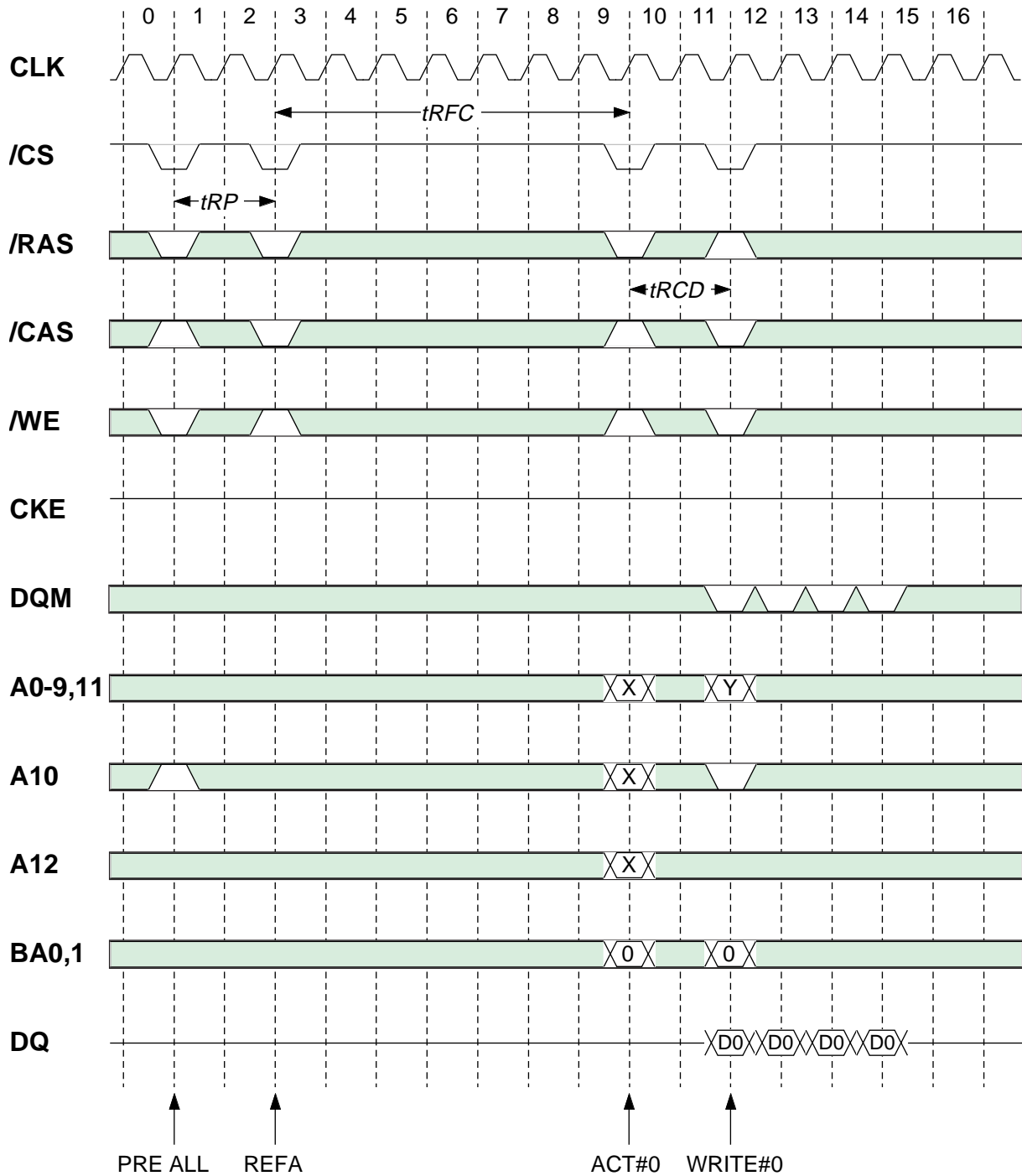


# 256Mb Synchronous DRAM



A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## Auto Refresh



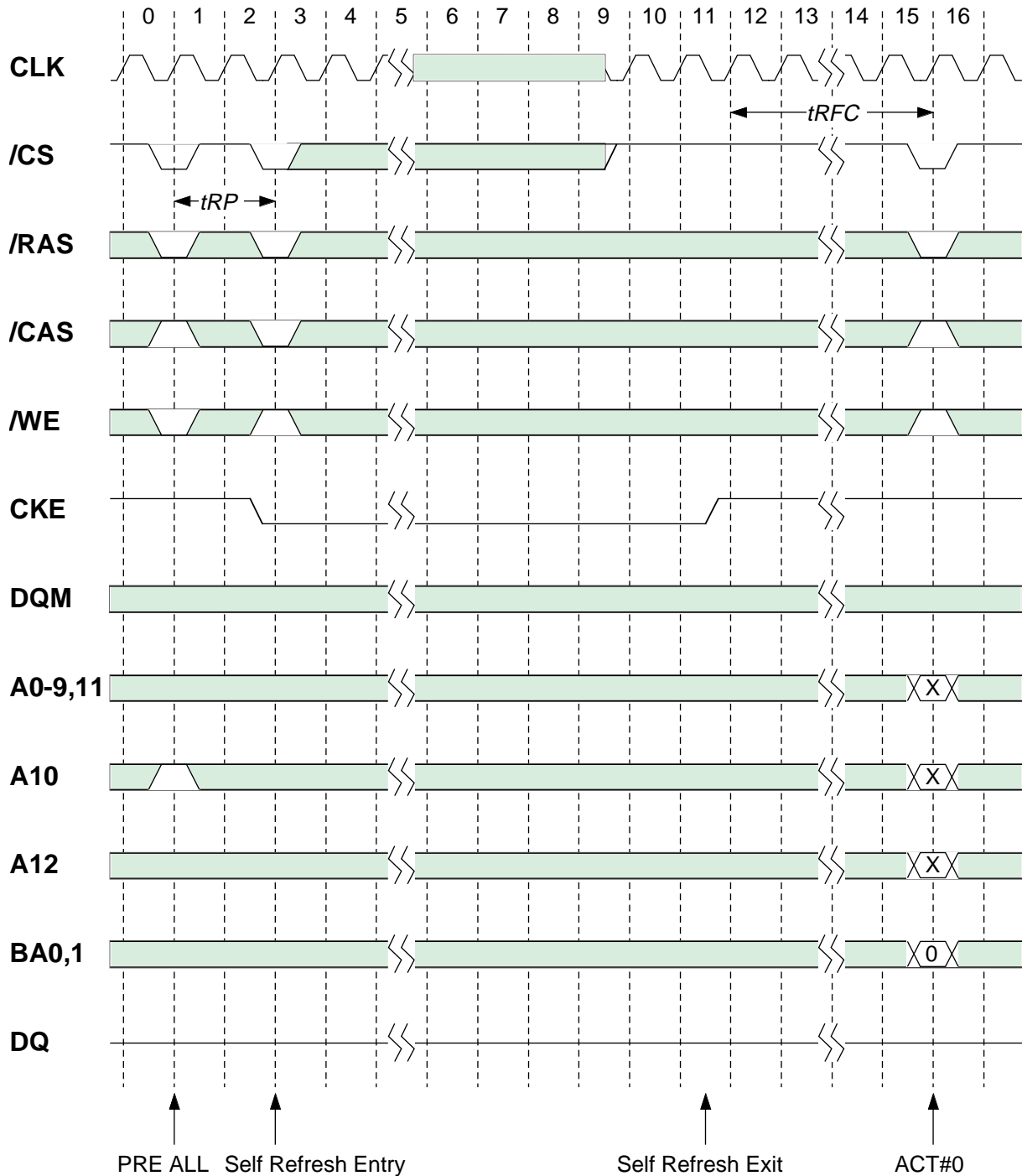
All banks must be idle before REFA is issued.

*Italic parameter* shows minimum case

# 256Mb Synchronous DRAM

A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## Self Refresh



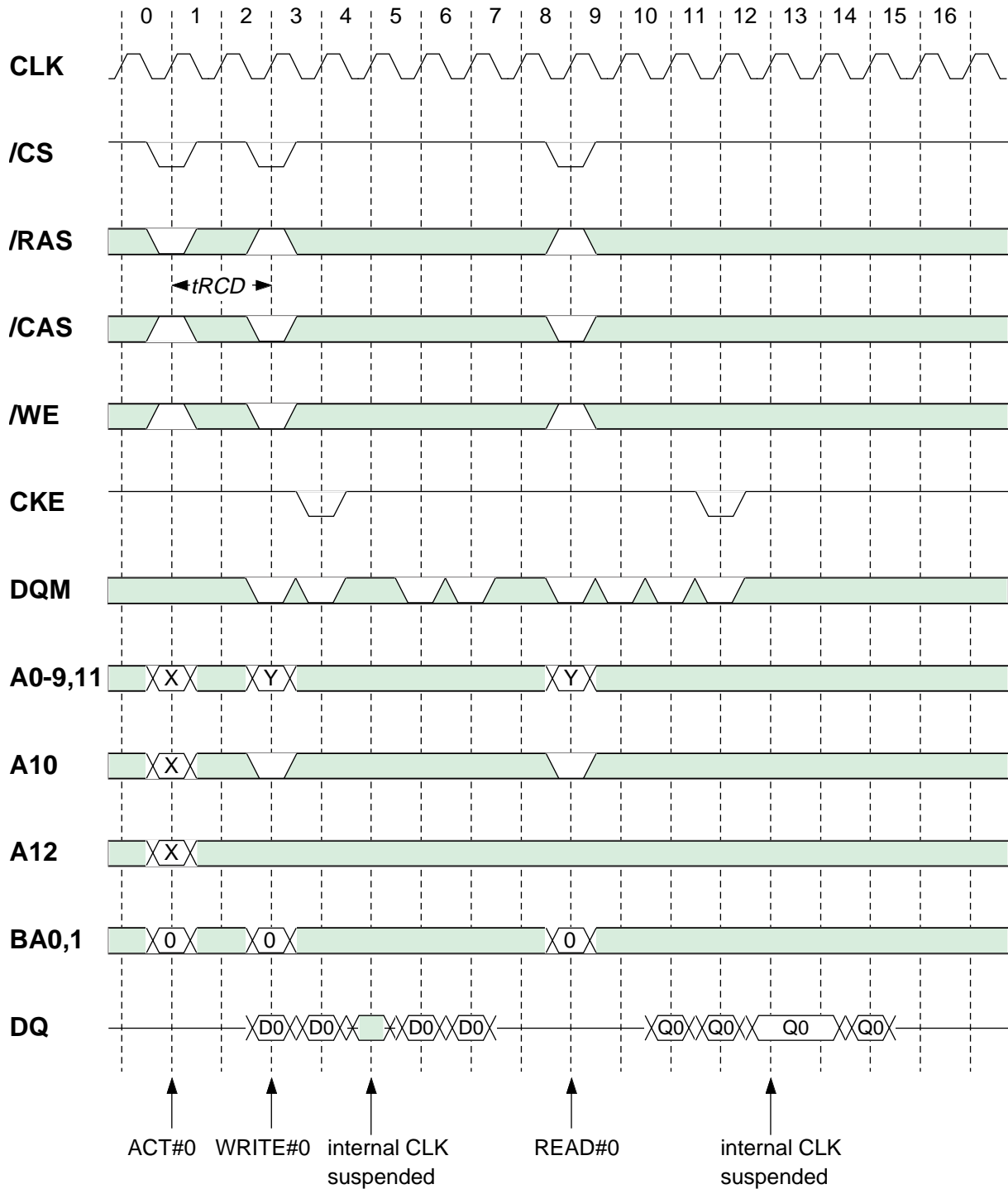
All banks must be idle before REFS is issued.

*Italic parameter* shows minimum case



A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)  
 A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)  
 A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## CLK Suspension [CL=2, BL=4]



*Italic parameter* shows minimum case



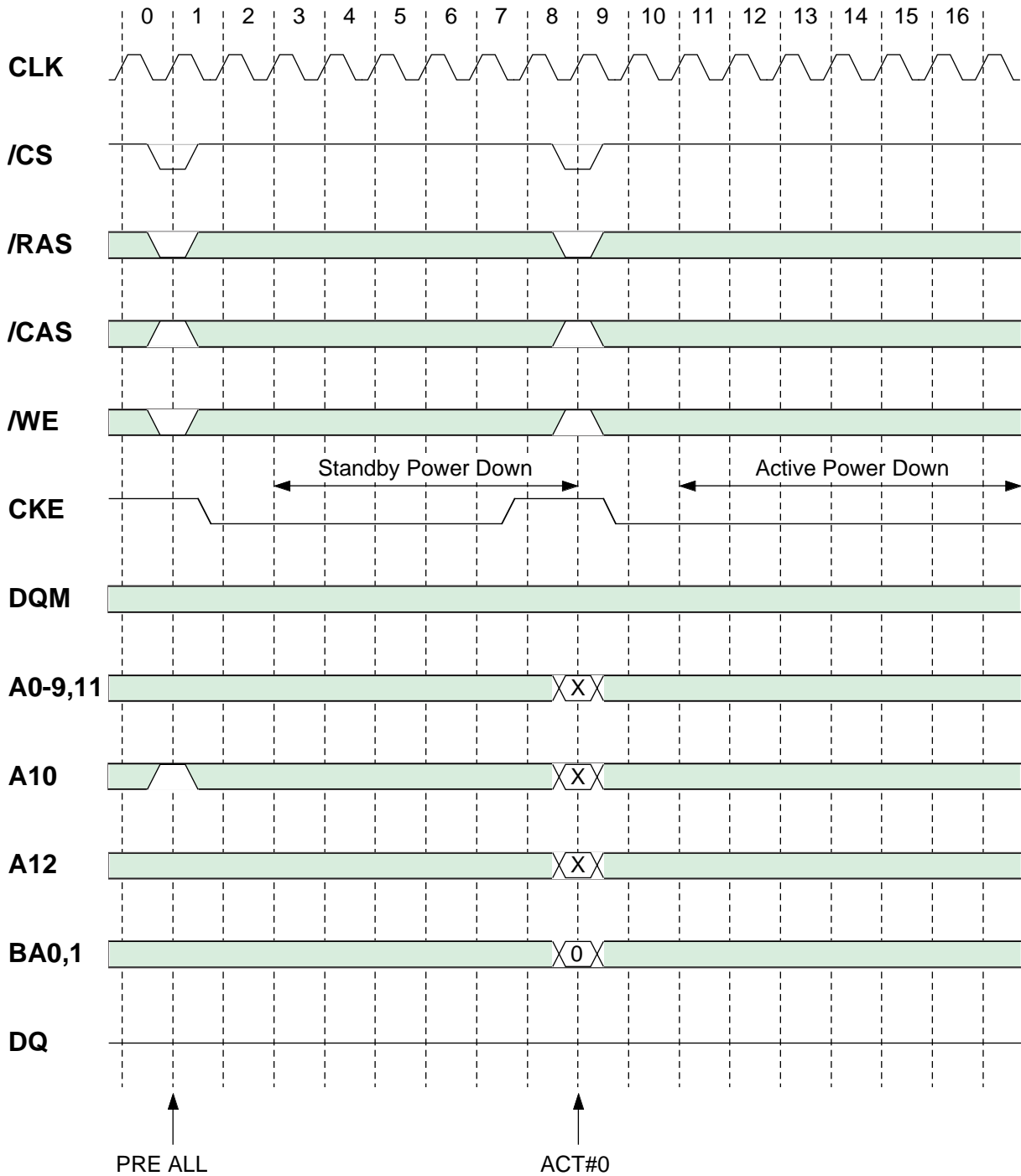
# 256Mb Synchronous DRAM

A2V56S20BTP (4-BANK x 16,777,216-WORD x 4-BIT)

A2V56S30BTP (4-BANK x 8,388,608-WORD x 8-BIT)

A2V56S40BTP (4-BANK x 4,194,304-WORD x 16-BIT)

## Power Down



*Italic parameter* shows minimum case