台康資訊股份有限公司

零組件承認書

承認書版本: 1.0　　發文編號: AP02>>009

料號	02350861	品名規格	GP. SDRAM. 64MB-6ns. 3.3V. TSOP II -54		
承認單位	oper	承認人員	李銘豫	承認日期	94年9月6日 ☑急件 ☐一般件
LOGO	PSC	原廠編號/圖號	A2V64S40CTP-G6PP		
廠商	奇菱	聯絡人	陳為孫	聯絡電話	8226 3168
送承認原因	☑新品 ☐次來源 ☐其它:_____ ☐修訂品 ☐代用品, 代用料號:_____			適用機種	TM4141

電氣項目檢驗重點 :		機構項目檢驗重點 :	
☐接觸阻抗	☐	☑尺　寸	☐表面處理
☐絕緣阻抗	☐	☑材　質	☐毛　邊
☐工作電壓	☐	☑外　觀	☐縮　水
☐工作電流	☐	☑電　鍍	☐合膠線
☐逆向電壓	☐	☑印　刷	☐刮　傷
☐逆向電流	☐	☑顏　色	☐
☐耐高壓	☐	☑包　裝	☐

注意事項:

1. ☐樣品為參考用, 請廠商第一批入料多 1PCS 給 IQC
2. 次來源承認已確認 Master Source 承認書 ☐電氣 ☐機構
3. PCB 承認(新品或 Update)須附加電子檔☐Gerber File ☐機構圖☐ PCB 製作規範 ☐ JOB 檔 ☐線路圖
4. Update 承認書須註明 庫存:_____ 採購在途:_____ 對策:_____

保證書後補

會簽			會簽			會簽		
	E/E			PM				
	M/E			業務				
	SAFETY							

審核	樣品確認	收文單位	進料	採購	廠商	文管	大陸	
原理	李銘豫	FILE	✓	✓	✓	✓		
		樣　品	✓					
	零件工程師	底　片						
		同發文編號: AP		料號:				

表單編號: 09-007-G

奇 普 仕 股 份 有 限 公 司
ULTRA SOURCE TECHNOLOGY CORP. LTD.
台北縣中和市建一路150號17樓 TEL：886-2-82263168 FAX：886-2-82263353
17F. NO.150Jian-Yi RD, CHUNG-HO, TAIPEI 235, TAIWAN R.O.C.

積體電路樣品承認書

編號：_____
日期：94 年 7 月21 日

客戶：台康資訊股份有限公司

品名：A2V64S40CTP-G6PP

樣品生產廠商 ： *(PSC)*

樣品承認簽章處：

業務：陳志強

64Mb SDRAM Specification

A2V64S40CTP

PSC Powerchip Semiconductor Corp.

No.12, Li-Hsin Rd.1, Science-based Industrial Park, Hsin-Chu
Taiwan, R.O.C.
TEL: 886-3-5795000
FAX: 886-3-5792168

General Description

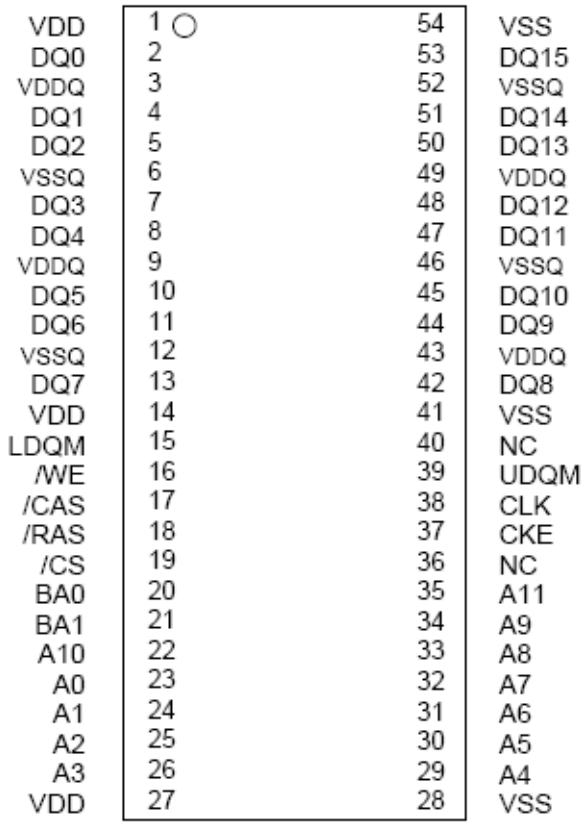
The A2V64S40CTP is 67,108,864 bits synchronous high data rate Dynamic RAM organized as 4 x 1,048,576 words by 16 bits. Synchronous design allows precise cycle controls with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

- 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - CAS latency (2 & 3)
  - Burst length (1, 2, 4, 8 & Full page)
  - Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock
- Auto & self refresh
- 64ms refresh period (4K cycle)
- Burst read single write operation
- LDQM & UDQM for masking

Pin Configurations

54-pin Plastic TSOP (II)



(Top view)

Ordering Information:

Frequency	Speed(ns)	Order Part Number			Package
		Type	Standard	Pb-Free	
200MHZ	5	A2V64S40CTP	-5	-G5	400mil TSOP-2
166MHZ	6	A2V64S40CTP	-6	-G6	400mil TSOP-2
143MHZ	7	A2V64S40CTP	-7	-G7	400mil TSOP-2
133MHZ	7.5	A2V64S40CTP	-75	-G75	400mil TSOP-2

Pin Descriptions

SYMBOL	TYPE	DESCRIPTION
CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.
CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), ACTIVE POWER-DOWN (row active in any bank), DEEP POWER DOWN (all banks idle), or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.
/CS	Input	Chip Select: /CS enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when /CS is registered HIGH. /CS provides for external bank selection on systems with multiple banks. /CS is considered part of the command code.
/CAS, /RAS, /WE	Input	Command Inputs: /CAS, /RAS, and /WE (along with /CS) define the command being entered.
LDQM, UDQM,	Input	Input/Output Mask: DQM is sampled HIGH and is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when during a READ cycle. LDQM corresponds to DQ0–DQ7, UDQM corresponds to DQ8–DQ15. LDQM and UDQM are considered same state when referenced as DQM.
BA0, BA1	Input	Bank Address Input(s): BA0 and BA1 define to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. These pins also select between the mode register and the extended mode register.
A0–A11	Input	Address Inputs: A0–A11 are sampled during the ACTIVE command (row address A0–A11) and READ/WRITE command (column-address A0–A7; with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
DQ0–DQ15	I/O	Data Input/Output: Data bus.
NC	–	Internally Not Connected: These could be left unconnected, but it is recommended they be connected or V_{SS}.
$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
V_{DD}	Supply	Core Power Supply.
V_{SS}	Supply	Ground.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_{IN},V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	° C
Power dissipation	P_D	1.0	W
Short circuit current	I_{OS}	50	mA

NOTES:
Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85° C for Extended, 0 to 70° C for Commercial)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
	V_{DDQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0		V_{DDQ} + 0.3	V	1
Input logic low voltage	V_{IL}	-0.3	0	0.8	V	2
Output logic high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -0.1mA
Output logic low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 0.1mA
Input leakage current	I_{LI}	-5	-	5	uA	3
Output leakage current	I_{oL}	-5	-	5	uA	3

Note:
1. VIH(max) = 4.6V AC for pulse width ≤ 10ns acceptable.
2. VIL(min) = -1.5V AC for pulse width ≤ 10ns acceptable.
3. Any input 0V ≤ VIN ≤ VDD + 0.3V, all other pins are not under test = 0V.
4. Dout is disabled , 0V ≤ VOUT ≤ VDD.

CAPACITANCE (Vdd =3.3V, T_A = 23°C, f = 1MHz, Vref = 0.9V ± 50mV)

Parameter	Symbol	Min	Max	Unit	Note
Clock	Cclk	2.0	4.0	pF	
/CAS,/RAS,/WE,/CS,CKE,L/UDQM	Cin	2.0	4.0	pF	
Address	C_{ADD}	2.0	4.0	pF	
DQ0~DQ15	C_{OUT}	3.0	6.0	pF	

DC CHARACTERISTICS

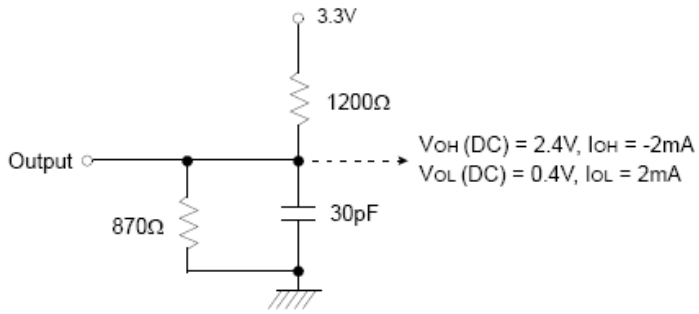
Recommended operating conditions (Voltage referenced to V_{SS} = 0V, T_A = -25 to 85° C for Extended, 0 to 70° C for Commercial)

Parameter	Symbol	Test Condition	Version				Unit	Note
			-5	-6	-7	-75		
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 t_{RC} ≥ t_{RC}(min) I_O = 0 mA	120	110	100	95	mA	1
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	2	2	2	2	mA	
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	1	1	1	1		
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	20	20	20	20	mA	
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	15	15	15	15		
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC} = 10ns	10	10	10	10	mA	
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	10	10	10	10		
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), CS ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	30	30	30	30	mA	
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	25	25	25	25		
Operating Current (Burst Mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs	160	150	140	130	mA	1
Refresh Current	I_{CC5}	t_{ARFC} ≥ t_{ARFC}(min)	180	180	180	180	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	1	1	1	1	mA	

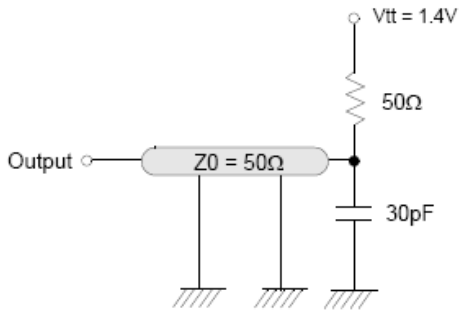
NOTES:
1. Measured with outputs open.
2. Refresh period is 64ms.
3. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ).

AC OPERATING TEST CONDITIONS (V_{DD} = 3.3V, T_A = -25 to 85° C for Extended, 0 to 70° C for Commercial)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4 / 0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Figure 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter	Symbol	Version				Unit	Note
		-5	-6	-7	-75		
Row active to row active delay	t_{RRD}(min)	10	12	14	15	ns	1
RAS to CAS delay	t_{RCD}(min)	15	18	21	21	ns	1
Row precharge time	t_{RP}(min)	15	18	21	21	ns	1
Row active time	t_{RAS}(min)		40	42	45	ns	1
	t_{RAS}(max)	100	100	100	100	us	
Row cycle time	t_{RC}(min)		58	63	67.5	ns	1
Last data in to row precharge	t_{RDL}(min)	2	2	2	2	CLK	2
Last data in to Active delay	t_{DAL}(min)					-	
Last data in to new col. address delay	t_{CDL}(min)	1	1	1	1	CLK	2
Last data in to burst stop	t_{BDL}(min)	1	1	1	1	CLK	2
Auto refresh cycle time	t_{ARFC}(min)		60	70	75	ns	

NOTES:
1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.

AC CHARACTERISTICS(AC operating conditions unless otherwise noted)

Parameter		Symbol	-5		-6		-7		-75		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency=3	t_{CC} (3)	5		6		7		7.5		ns	1
	CAS latency=2	t_{CC} (2)	10		10		10		10			
CLK to valid output delay	CAS latency=3	t_{SAC} (3)			5		6		6		ns	1,2
	CAS latency=2	t_{SAC} (2)			6		6		6			
Output data hold time	CAS latency=3	t_{OH} (3)			2.5		3		3		ns	2
	CAS latency=2	t_{OH} (2)			3		3		3			
CLK high pulse width		t_{CH}			2.5		3		3		ns	3
CLK low pulse width		t_{CL}			2.5		3		3		ns	3
Input setup time		t_{SS}			1.5		2		2		ns	3
Input hold time		t_{SH}			1		1		1		ns	3
CLK to output in Low-Z		t_{SLZ}			1		1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	t_{SHZ}			5		6		6		ns	
	CAS latency=2				6		6		6			

NOTES :
1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
   If tr & tf is longer than 1ns, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]ns should be added to the parameter.

TRUTH TABLE

Command Truth Table

COMMAND	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	BA1	BA0	A10/AP	A11, A9 ~ A0
Device deselect	DSL	H	X	H	X	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X	X
Burst stop	BST	H	H	L	H	H	L	X	X	X	X
Read	RD	H	X	L	H	L	H	V	V	L	V
Read with auto precharge	RDA	H	X	L	H	L	H	V	V	H	V
Write	WR	H	X	L	H	L	L	V	V	L	V
Write with auto precharge	WRA	H	X	L	H	L	L	V	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V	V
Precharge select bank	PRE	H	X	L	L	H	L	V	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	L	X
Extended mode register set	EMRS	H	X	L	L	L	L	H	L	L	V

(V=Valid, X=Don´t Care, H=Logic High, L=Logic Low)

CKE Truth Table

Current state	Function	Symbol	CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	/Address
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend mode		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	Auto refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SREF	H	L	L	L	L	H	X
Idle	Power down entry	PD	H	L	L	H	H	H	X
			H	L	H	X	X	X	X
Idle	Deep power down entry	DPD	H	L	L	H	H	L	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Power down	Power down exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Deep power down	Deep power down exit		L	H	X	X	X	X	X

(V=Valid, X=Don´t Care, H=Logic High, L=Logic Low)

Function Truth Table

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	Row activating	
	L	L	H	L	BA,A10	PRE/PALL	NOP	
	L	L	L	H	X	REF	Auto refresh	
	L	L	L	L	OC,BA1=L	MRS	Mode register set	
	L	L	L	L	OC,BA1=H	EMRS	Extended mode register set	
Row active	H	X	X	X	X	DESL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	BST	NOP	
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read	2
	L	H	L	L	BA,CA,A10	WR/WRA	Begin write	2
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Precharge / Precharge all banks	3
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS / EMRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst,begin new read	4
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst,begin write	4,5
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst → Precharging	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → Write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	RD/RDA	Terminate burst, start read : Determine AP	4,5
	L	H	L	L	BA,CA,A10	WR/WRA	Terminate burst,new write : Determine AP	4
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Terminate burst → Precharging	6
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	

Current state	/CS	/RAS	/CAS	/WE	/Address	Command	Action	Notes
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after tRP	
	L	H	H	H	X	NOP	Nop → Enter idle after tRP	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	Nop → Enter idle after tRP	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS/EMRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter bank active after tRCD	
	L	H	H	H	X	NOP	Nop → Enter bank active after tRCD	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	1
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1
	L	L	H	H	BA,RA	ACT	ILLEGAL	1,7
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA	MRS / EMRS	ILLEGAL	
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after tDPL	
	L	H	H	H	X	NOP	Nop → Enter row active after tDPL	
	L	H	H	L	X	BST	Nop → Enter row active after tDPL	
	L	H	L	H	BA,CA,A10	RD/RDA	Begin read	5
	L	H	L	L	BA,CA,A10	WR/WRA	Begin new write	
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after tDPL	
	L	H	H	H	X	NOP	Nop → Enter precharge after tDPL	
	L	H	H	L	X	BST	Nop → Enter precharge after tDPL	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	1,5
	L	L	H	H	BA,RA	ACT	ILLEGAL	1
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	1
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Refresh	H	X	X	X	X	DESL	Nop → Enter idle after tRC1	
	L	H	H	H	X	NOP	Nop → Enter idle after tRC1	
	L	H	H	L	X	BST	Nop → Enter idle after tRC1	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	OC,BA1=L	MRS / EMRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DESL	Nop → Enter idle after tRSC	
	L	H	H	H	X	NOP	Nop → Enter idle after tRSC	
	L	H	H	L	X	BST	Nop → Enter idle after tRSC	
	L	H	L	H	BA,CA,A10	RD/RDA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WR/WRA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	
	L	L	L	H	X	REF	ILLEGAL	
	L	L	L	L	MODE	MRS	ILLEGAL	

Notes: 1. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending

on the state of that bank.
2. Illegal if tRCD is not satisfied.
3. Illegal if tRAS is not satisfied.
4. Must satisfy burst interrupt condition.
5. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
6. Must mask preceding data which don't satisfy tDPL.
7. Illegal if tRRD is not satisfied

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with Normal MRS

Address	BA0 ~ BA1	A11 ~ A10/AP	A9*2	A8	A7	A6	A5	A4	A3	A2	A1	A0
Function	"0" Setting for Normal MRS	RFU*1	W.B.L	Test Mode		CAS Latency			BT	Burst Length		

Normal MRS Mode

Test Mode			CAS Latency				Burst Type			Burst Length				
A8	A7	Type	A6	A5	A4	Latency	A3	Type		A2	A1	A0	BT=0	BT=1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential		0	0	0	1	1
0	1	Reserved	0	0	1	1	1	Interleave		0	0	1	2	2
1	0	Reserved	0	1	0	2	Mode Select			0	1	0	4	4
1	1	Reserved	0	1	1	3	BA1	BA0	Mode	0	1	1	8	8
Write Burst Length			1	0	0	Reserved	0	0	Setting for Normal MRS	1	0	0	Reserved	Reserved
A9	Length		1	0	1	Reserved				1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved				1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved				1	1	1	Full Page	Reserved

B. POWER UP SEQUENCE

1. Apply power and attempt to maintain CKE at a high state and all other inputs may be undefined.
- Apply VDD before or at the same time as VDDQ.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200us.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

C. BURST SEQUENCE

BURST LENGTH	STARTING COLUMN ADDRESS	ORDER OF ACCESSES WITHIN A BURST	
		TYPE=SEQUENTIAL	TYPE=INTERLEAVED
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	N=A0 – A8 (location 0 – y)	Cn, Cn+1, Cn+2, Cn+3, Cn+4..., …Cn-1, Cn…	Not Supported

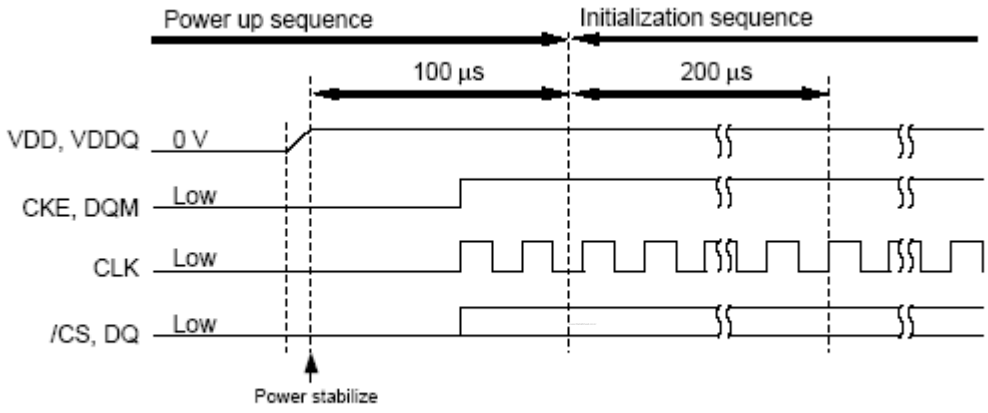
NOTE:
1. For full-page accesses: y = 512.
2. For a burst length of two, A1–A8 select the block-of-two burst; A0 selects the starting column within the block.
3. For a burst length of four, A2–A8 select the block-of-four burst; A0–A1 select the starting column within the block.
4. For a burst length of eight, A3–A8 select the block-of-eight burst; A0–A2 select the starting column within the block.
5. For a full-page burst, the full row is selected and A0–A8 select the starting column.
6. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.

7. For a burst length of one, A0–A8 select the unique column to be accessed, and mode register bit M3 is ignored.

Power-up sequence

Power-up sequence
The SDRAM should be goes on the following sequence with power up.
The CLK, CKE, /CS, DQM and DQ pins keep low till power stabilizes.
The CLK pin is stabilized within 100 µs after power stabilizes before the following initialization sequence.
The CKE and DQM is driven to high between power stabilizes and the initialization sequence.
This SDRAM has VDD clamp diodes for CLK, CKE, address, /RAS, /CAS, /WE, /CS, DQM and DQ pins. If the sepins go high before power up, the large current flows from these pins to VDD through the diodes.

Initialization sequence
When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After tRP delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQM and CKE to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.



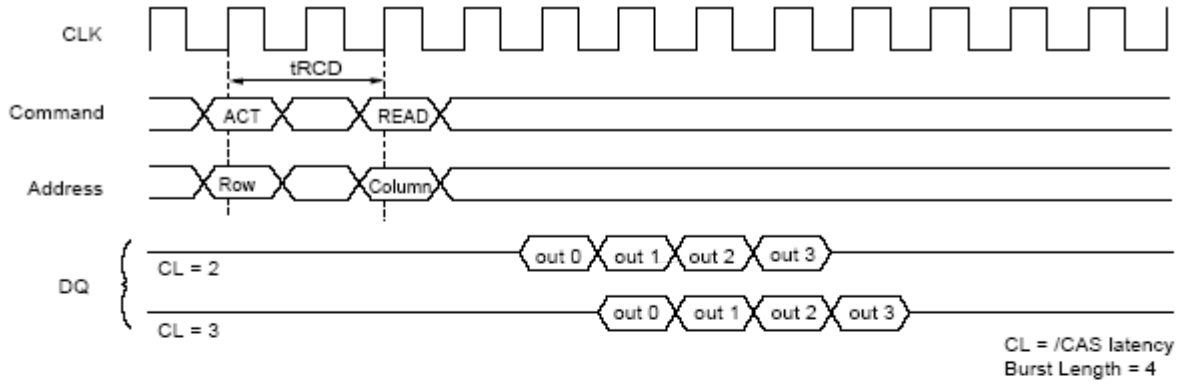
Power-up sequence and Initialization sequence

Operation of the SDRAM

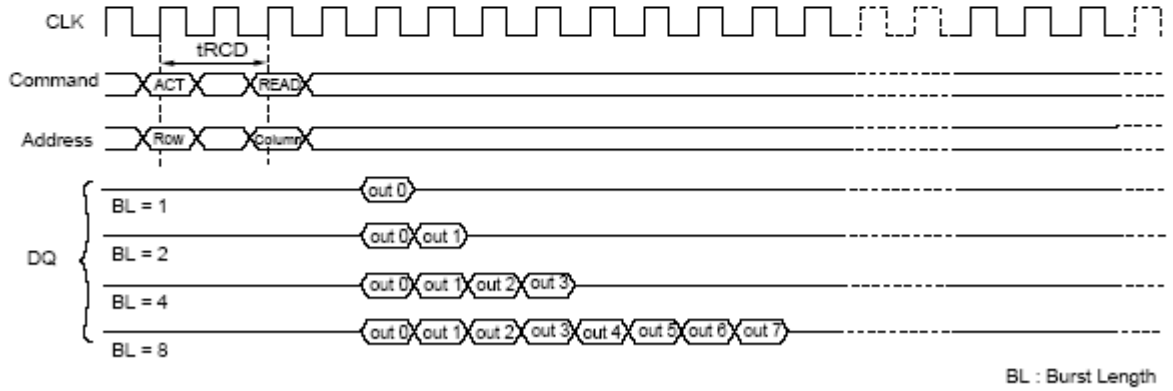
Read/Write Operations

Bank active
Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACT) command. An interval of tRCD is required between the bank active command input and the following read/write command input.

Read operation
A read operation starts when a read command is input. Output buffer becomes Low-Z in the (/CAS Latency - 1) cycle after read command set. The SDRAM can perform a burst read operation.
The burst length can be set to 1, 2, 4 and 8. The start address for a burst read is specified by the column address and the bank select address at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the /CAS Latency. The /CAS Latency can be set to 2 or 3.
When the burst length is 1, 2, 4 and 8 the DOUT buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.
The /CAS latency and burst length must be specified at the mode register.



/CAS Latency



Burst Length

Write operation

Burst write or single write mode is selected

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the same clock as a write command set. (The latency of data input is 0 clock.) The burst length can be set to 1, 2, 4 and 8, like burst read operations. The write start address is specified by the column address and the bank select address at the write command set cycle.

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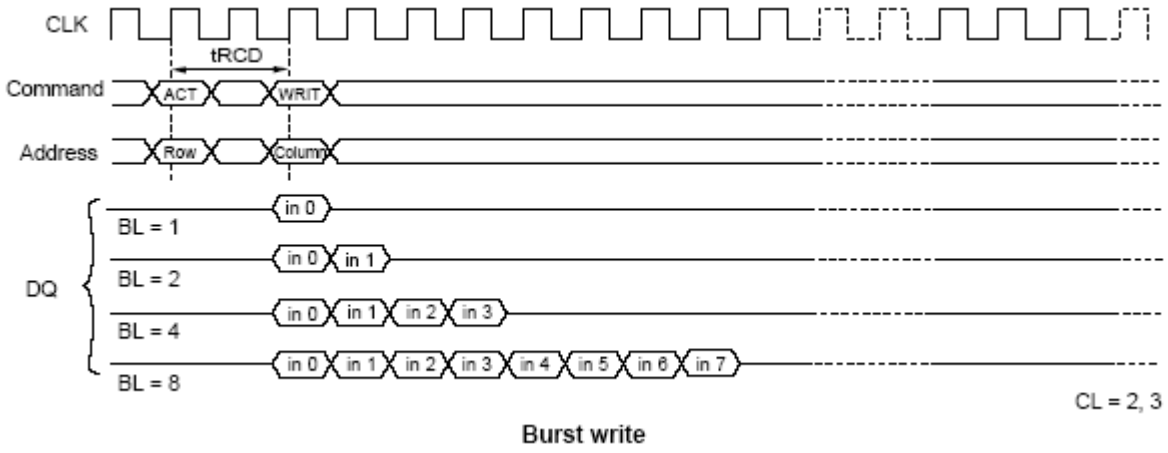
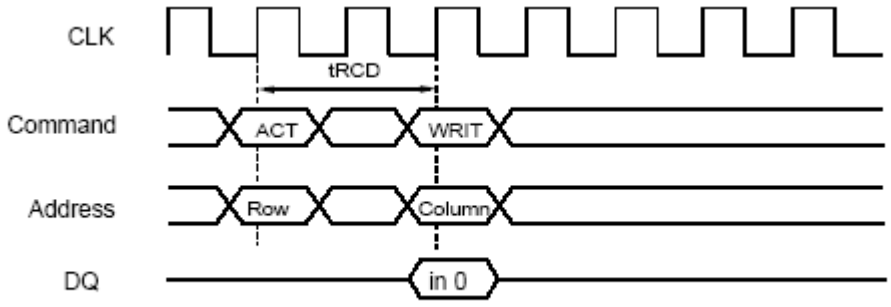


Burst write

2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 0 clock).



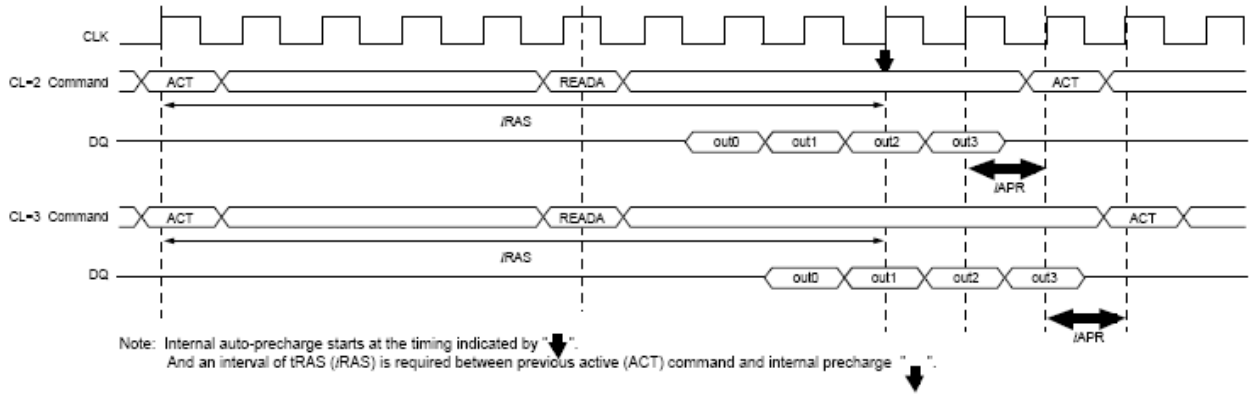
Single write

Auto Precharge

Read with auto-precharge
In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval defined by /APR is required before execution of the next command.

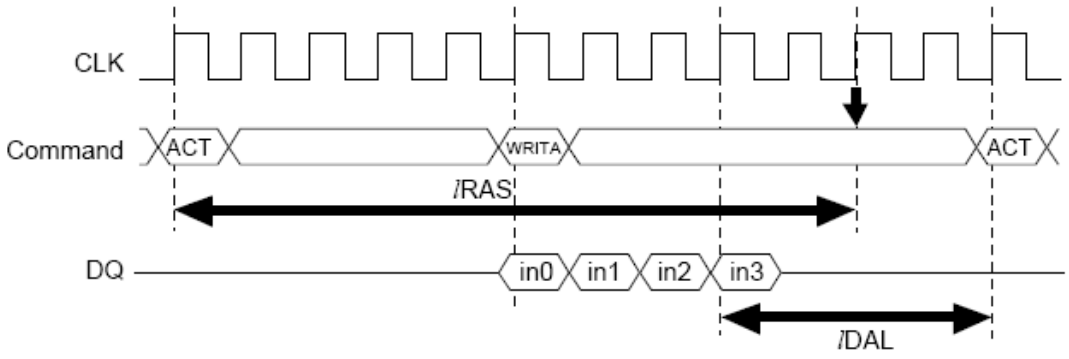
[Clock cycle time]

/CAS latency	Precharge start cycle
3	2 cycle before the final data is output
2	1 cycle before the final data is output



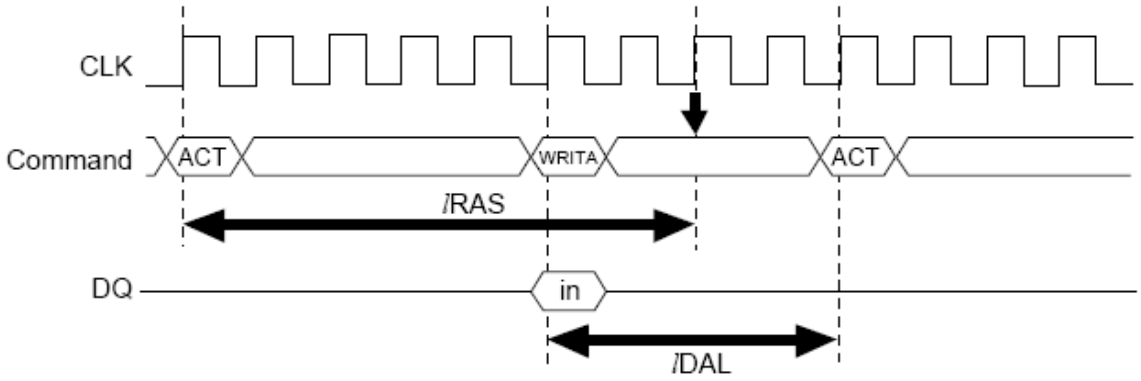
Burst Read (BL = 4)

Write with auto-precharge
In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACT) command. In addition, an interval of /DAL is required between the final valid data input and input of next command.



Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (/RAS) is required between previous active (ACT) command and internal precharge "↓".

Burst Write (BL = 4)

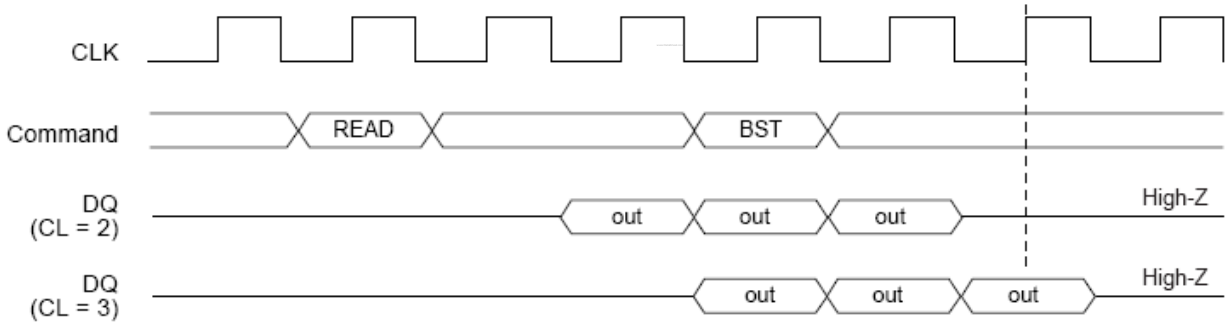


Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of tRAS (tRAS) is required between previous active (ACT) command
and internal precharge "↓".

Single Write

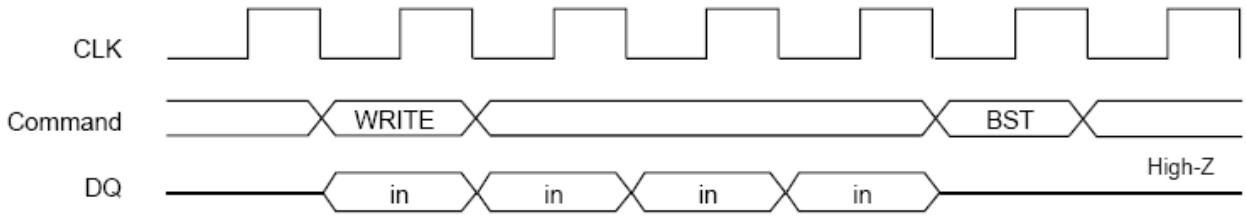
Burst Stop Command

During a read cycle, when the burst stop command is issued, the burst read data are terminated and the data bus goes to High-Z after the /CAS latency from the burst stop command.



Burst Stop at Read

During a write cycle, when the burst stop command is issued, the burst write data are terminated and data bus goes to High-Z at the same clock with the burst stop command.

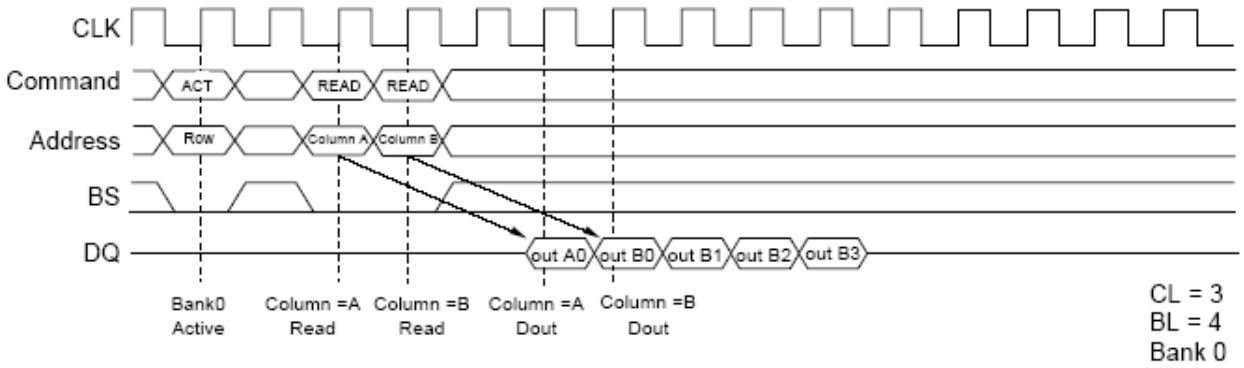


Burst Stop at Write

Command Intervals

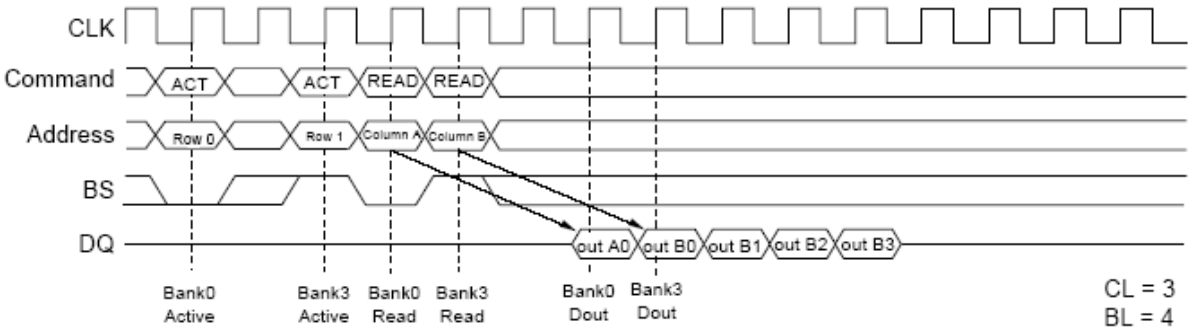
Read command to Read command interval

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (same ROW address in same bank)

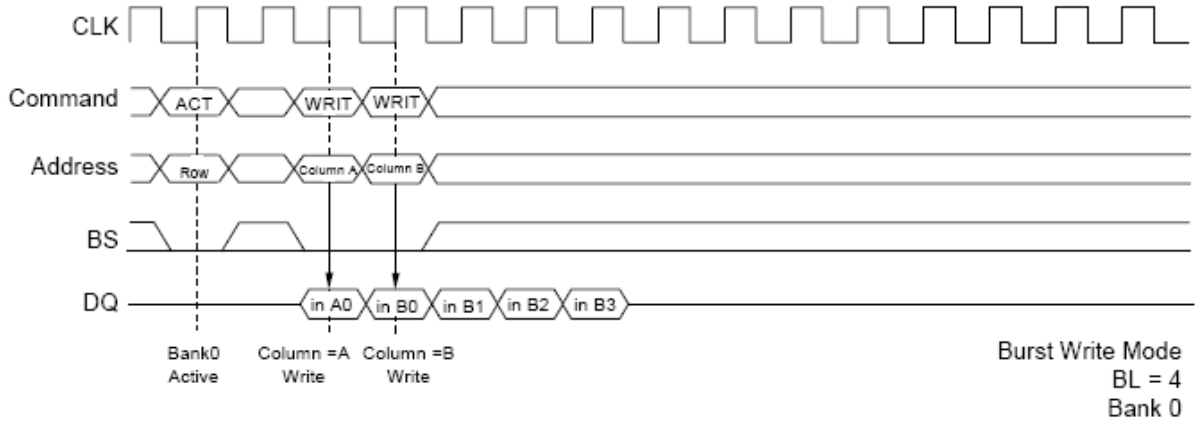
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.



READ to READ Command Interval (different bank)

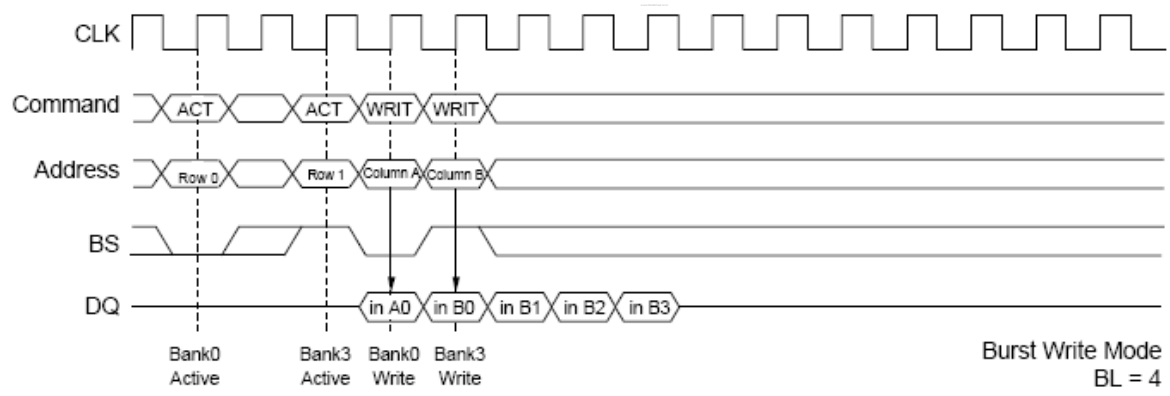
Write command to Write command interval

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.



WRITE to WRITE Command Interval (same ROW address in same bank)

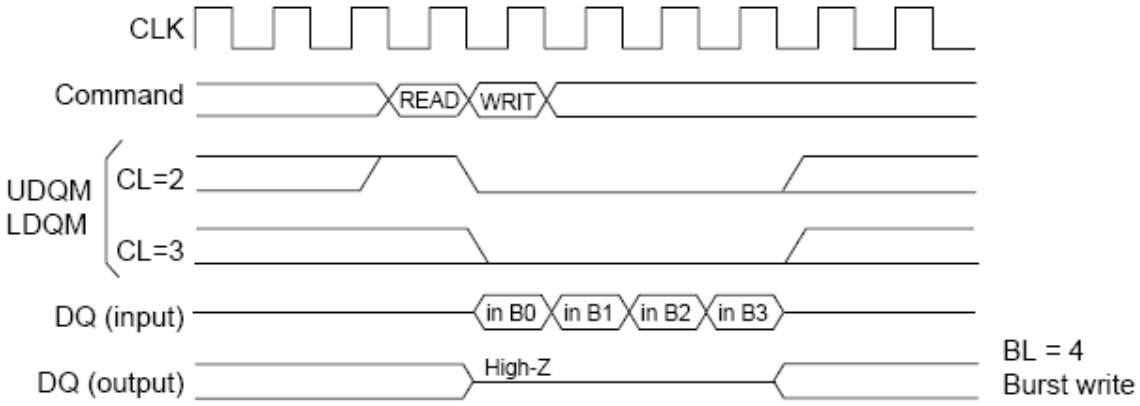
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. In the case of burst write, the second write command has priority.



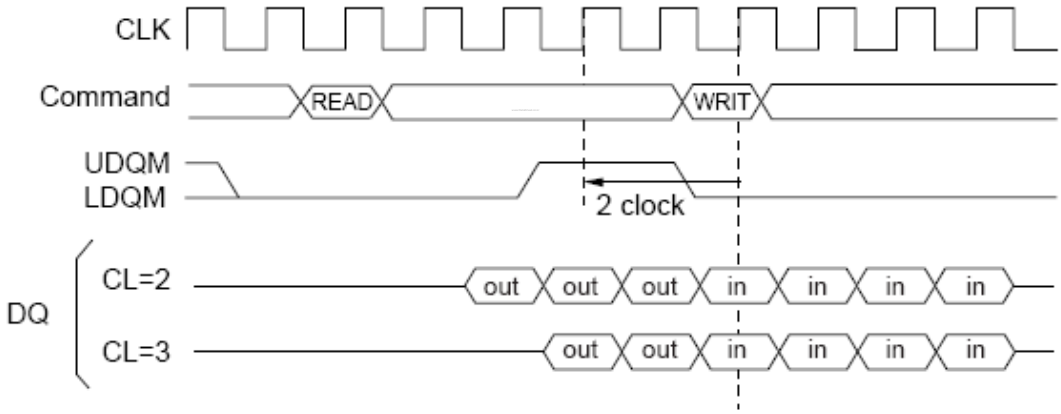
WRITE to WRITE Command Interval (different bank)

Read command to Write command interval

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.



READ to WRITE Command Interval (1)

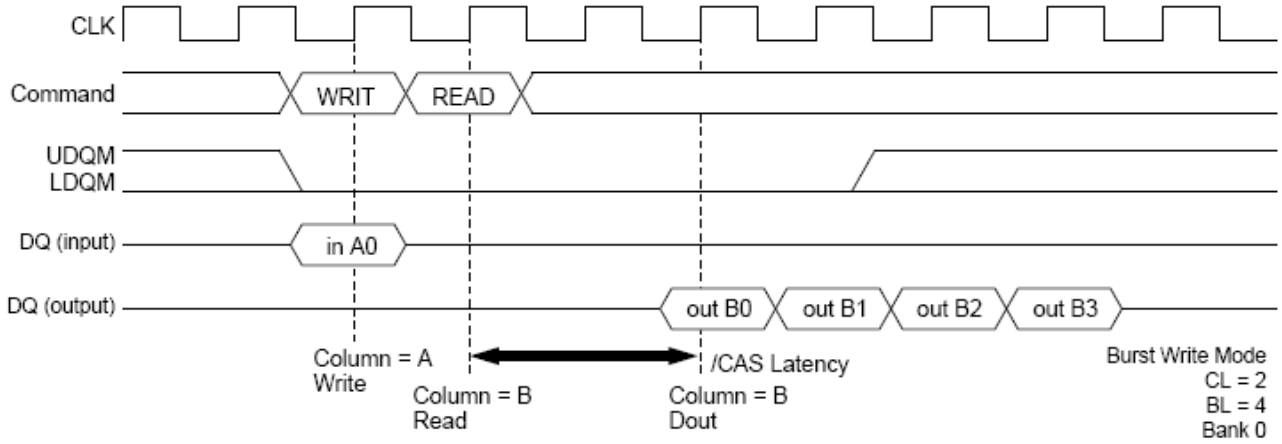


READ to WRITE Command Interval (2)

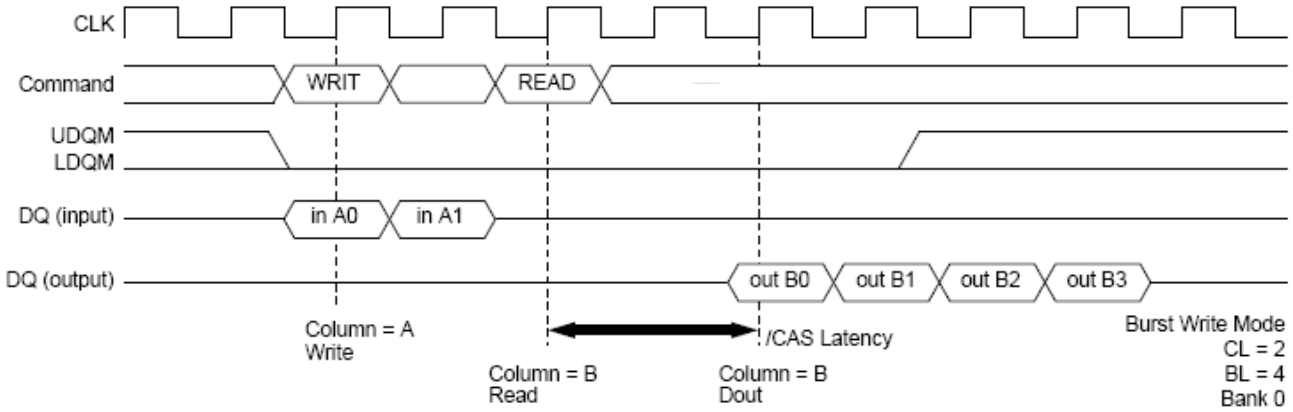
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 cycle, provided that the other bank is in the bank active state. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input.

Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed.



WRITE to READ Command Interval (1)

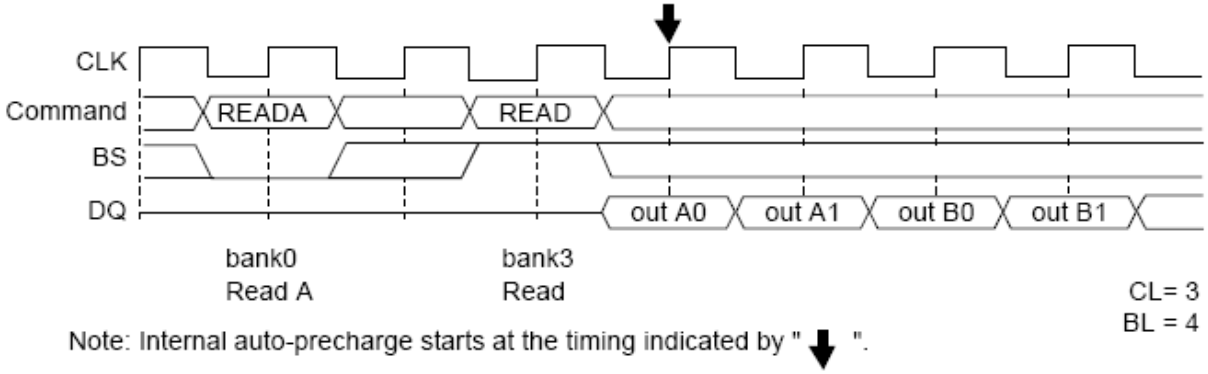


WRITE to READ Command Interval (2)

2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank active command.
3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

Read with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.

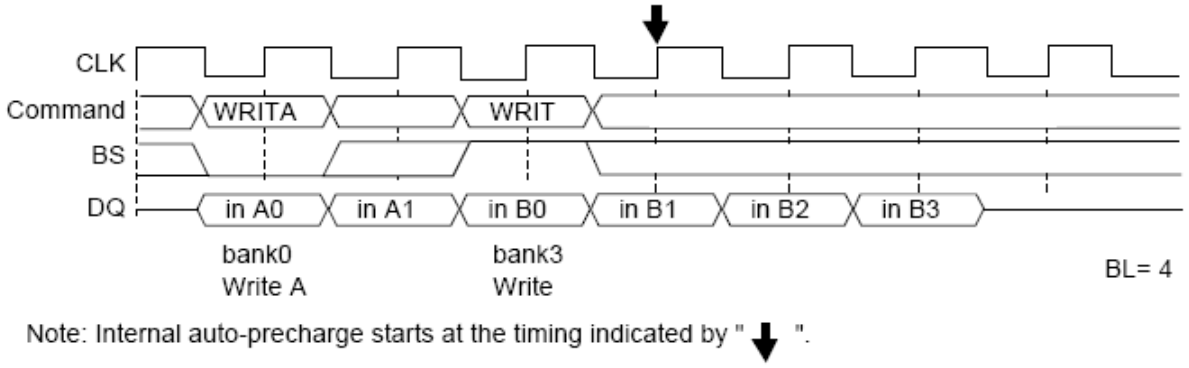


Read with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts 2 clocks later from the second command.

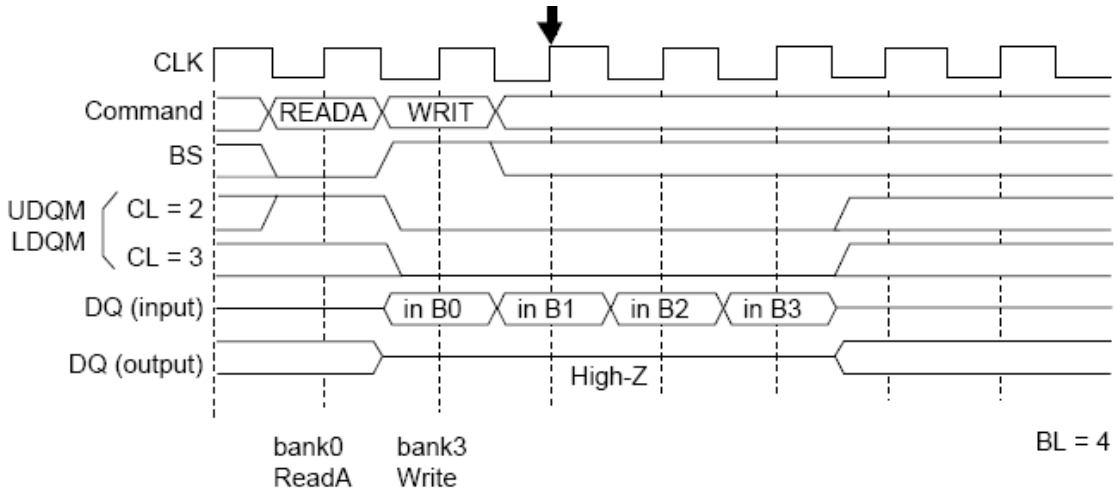


Write with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command (the same bank) is illegal.

Read with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, UDQM and LDQM must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.



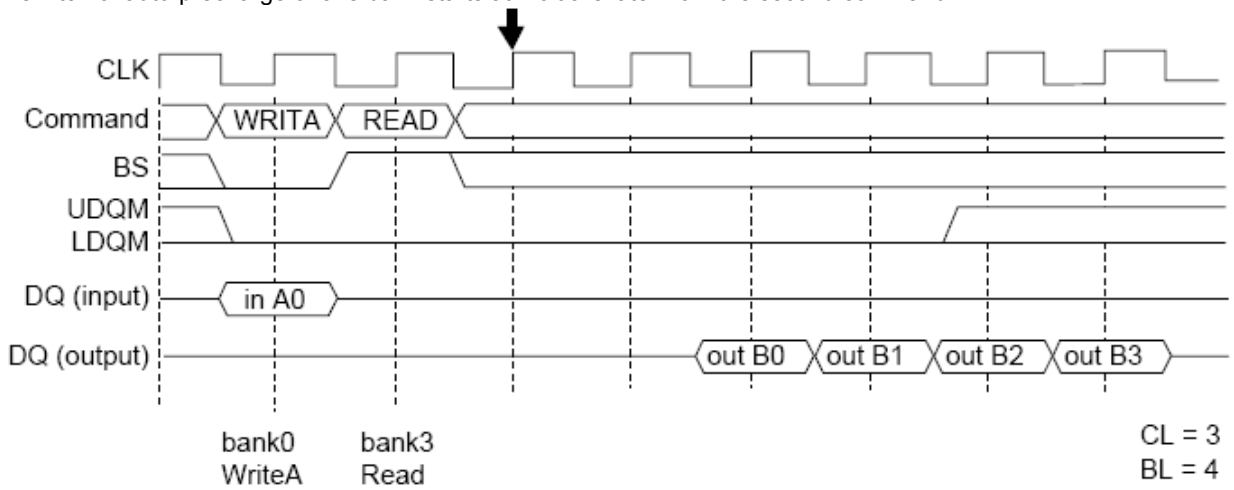
Note: Internal auto-precharge starts at the timing indicated by " ".

Read with Auto Precharge to Write Command Interval (Different bank)

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

Write with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at 2 clocks later from the second command.

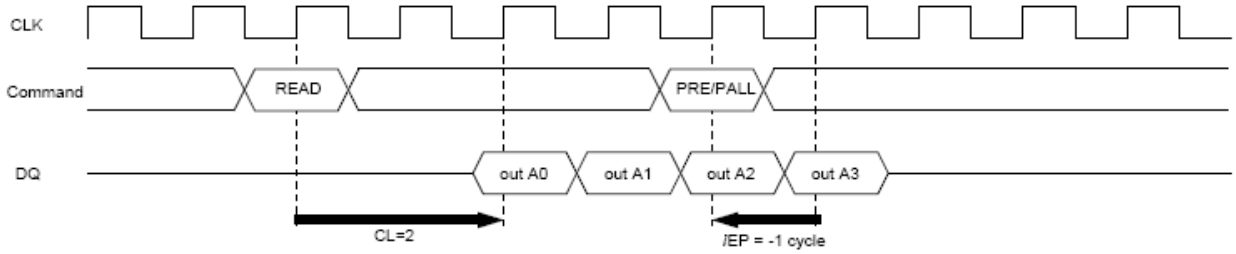


Note: Internal auto-precharge starts at the timing indicated by " ".

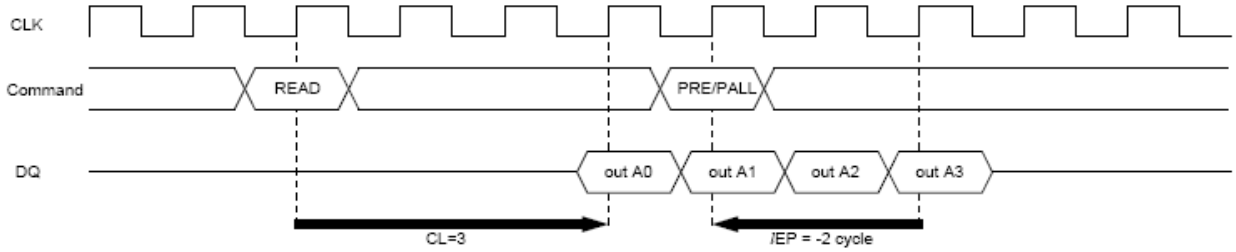
Write with Auto Precharge to Read Command Interval (Different bank)

2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

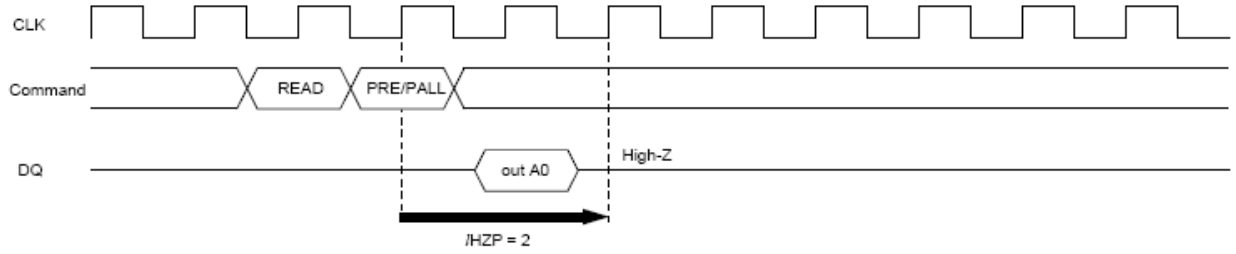
Read command to Precharge command interval (same bank)
When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by /HZP, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by /EP must be assured as an interval from the final data output to precharge command execution.



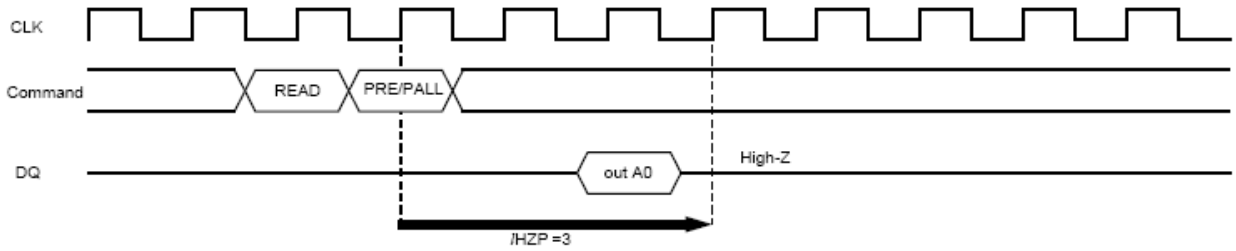
READ to PRECHARGE Command Interval (same bank): To output all data (CL = 2, BL = 4)



READ to PRECHARGE Command Interval (same bank): To output all data (CL = 3, BL = 4)

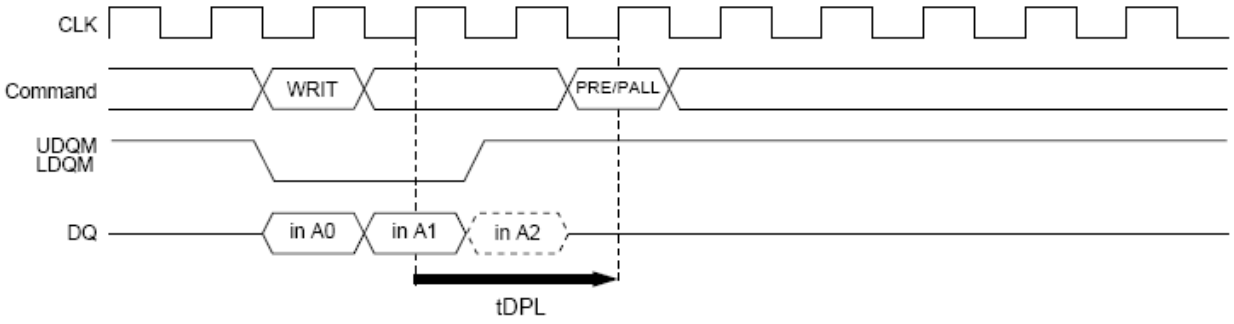


READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 2, BL = 1, 2, 4, 8)

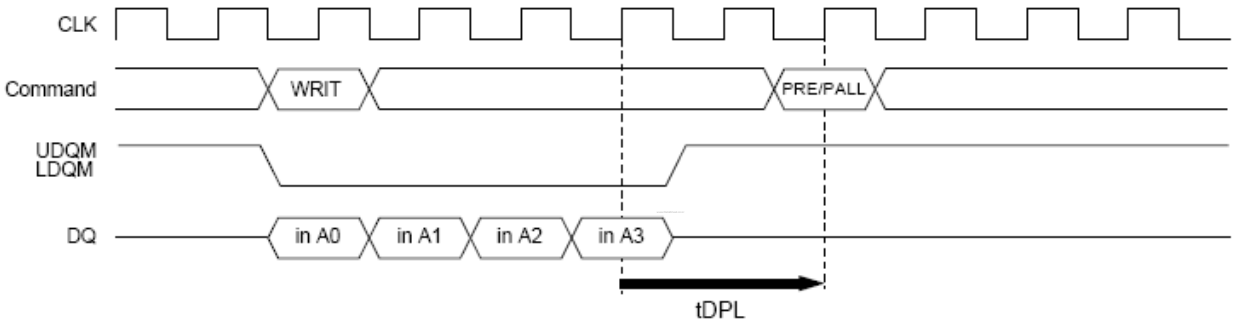


READ to PRECHARGE Command Interval (same bank): To stop output data (CL = 3, BL = 1, 2, 4, 8)

Write command to Precharge command interval (same bank)
When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of UDQM and LDQM for assurance of the clock defined by tDPL.



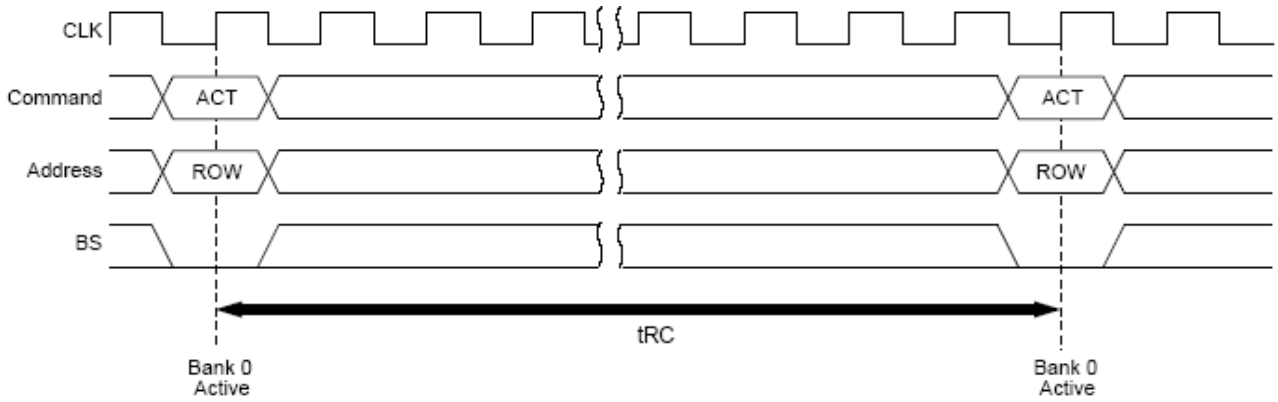
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To stop write operation))



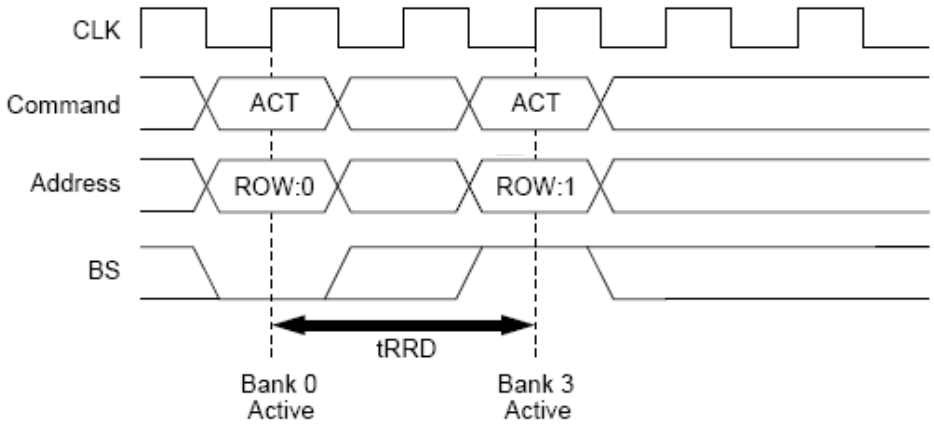
WRITE to PRECHARGE Command Interval (same bank) (BL = 4 (To write all data))

Bank active command interval

1. Same bank: The interval between the two bank active commands must be no less than tRC.
2. In the case of different bank active commands: The interval between the two bank active commands must be no less than tRRD.



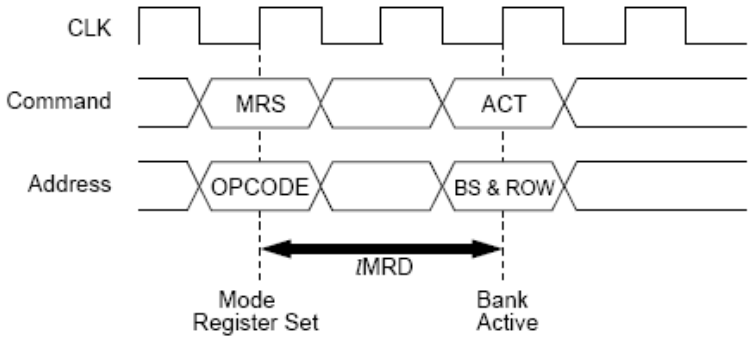
Bank Active to Bank Active for Same Bank



Bank Active to Bank Active for Different Bank

Mode register set to Bank active command interval

The interval between setting the mode register and executing a bank active command must be no less than /MRD.

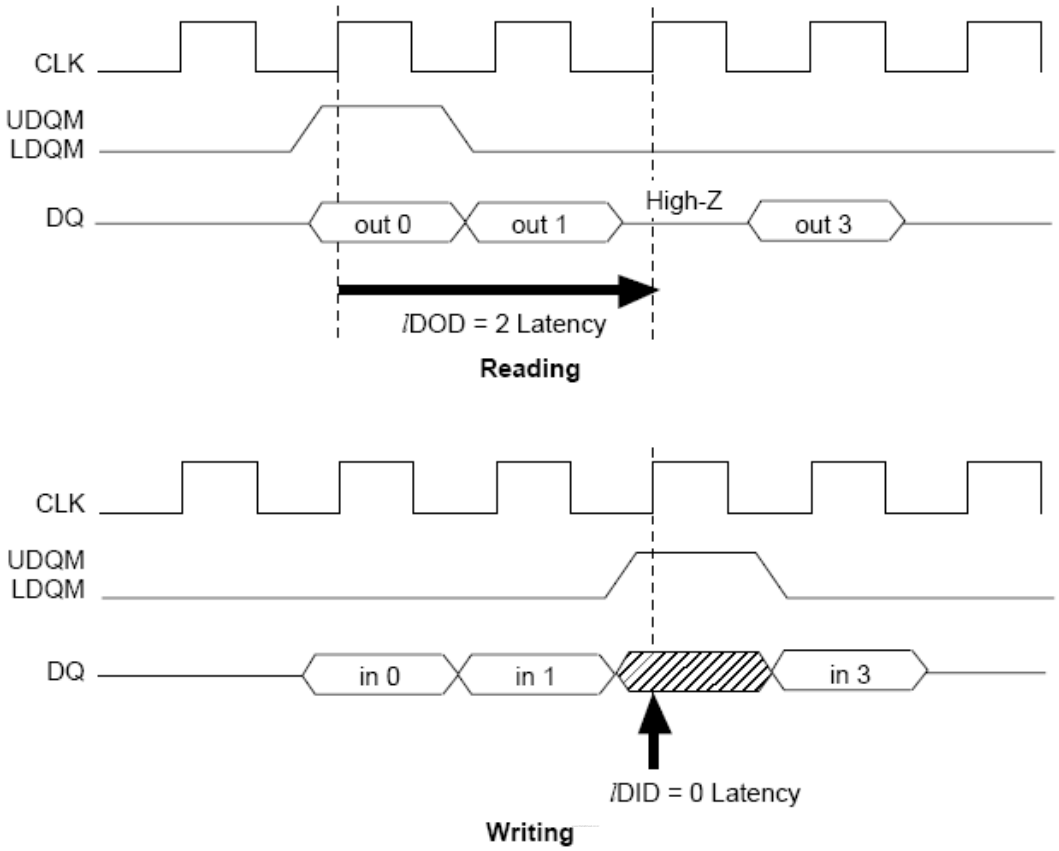


Mode register set to Bank active command interval

DQM Control
The UDQM and LDQM mask the upper and lower bytes of the DQ data, respectively. The timing of UDQM and LDQM is different during reading and writing.

Reading
When data is read, the output buffer can be controlled by UDQM and LDQM. By setting UDQM and LDQM to Low, the output buffer becomes Low-Z, enabling data output. By setting UDQM and LDQM to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of UDQM and LDQM during reading is 2 clocks.

Writing
Input data can be masked by UDQM and LDQM. By setting DQM to Low, data can be written. In addition, when UDQM and LDQM are set to High, the corresponding data is not written, and the previous data is held. The latency of UDQM and LDQM during writing is 0 clock.


CLK
UDQM
LDQM
DQ
out 0
out 1
High-Z
out 3
tDOD = 2 Latency
Reading
CLK
UDQM
LDQM
DQ
in 0
in 1
in 3
tDID = 0 Latency
Writing

Refresh

Auto-refresh
All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycles are required to refresh all the ROW addresses within tREF (max.). The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh
After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During selfrefresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within tREF (max.) period on the condition 1 and 2 below.
1. Enter self-refresh mode within time as below* after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
2. Start burst refresh or distributed refresh at equal interval to all refresh addresses within time as below*after exiting from self-refresh mode.

Note: tREF (max.) / refresh cycles.

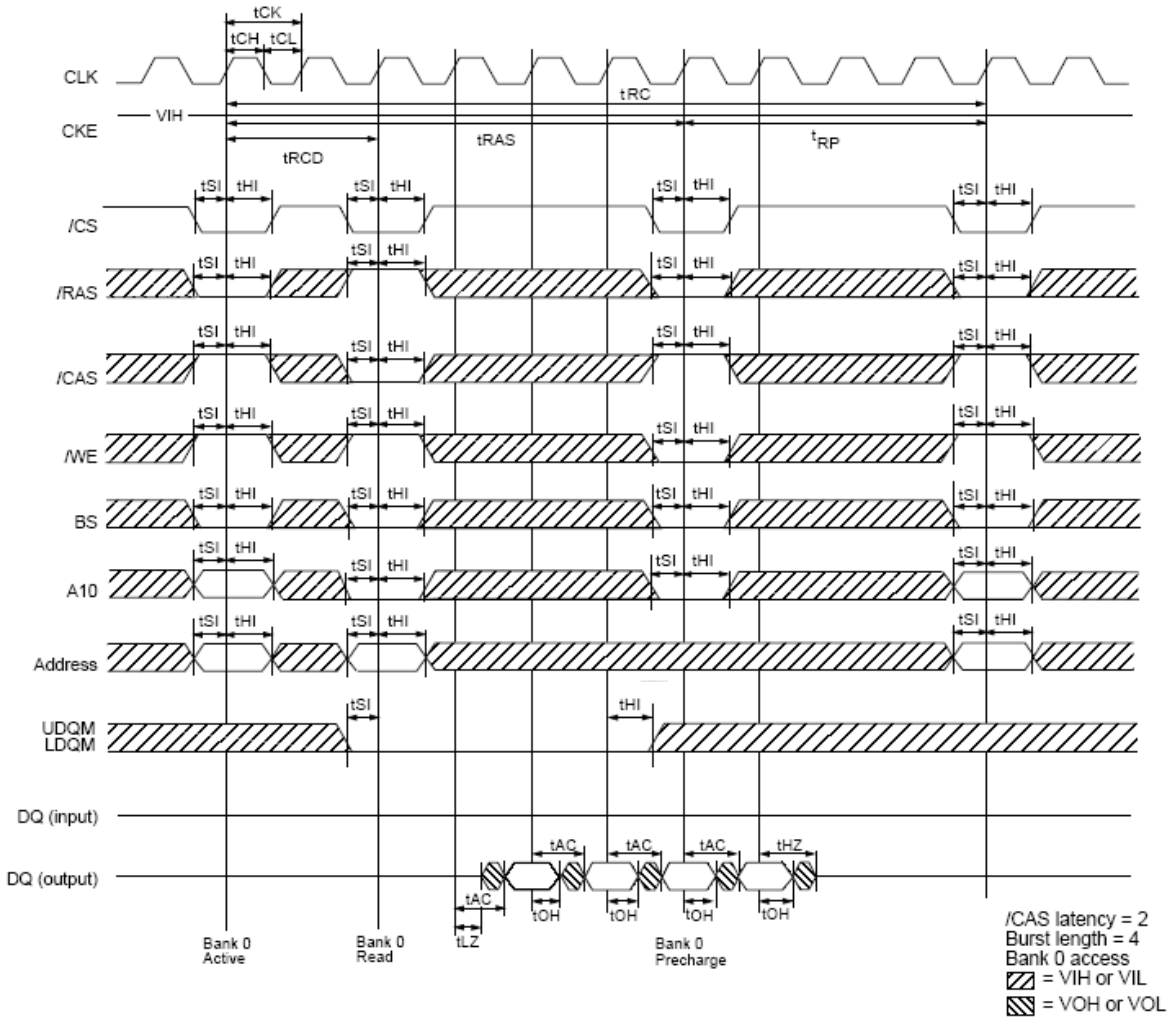
Others

Power-down mode
The SDRAM enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

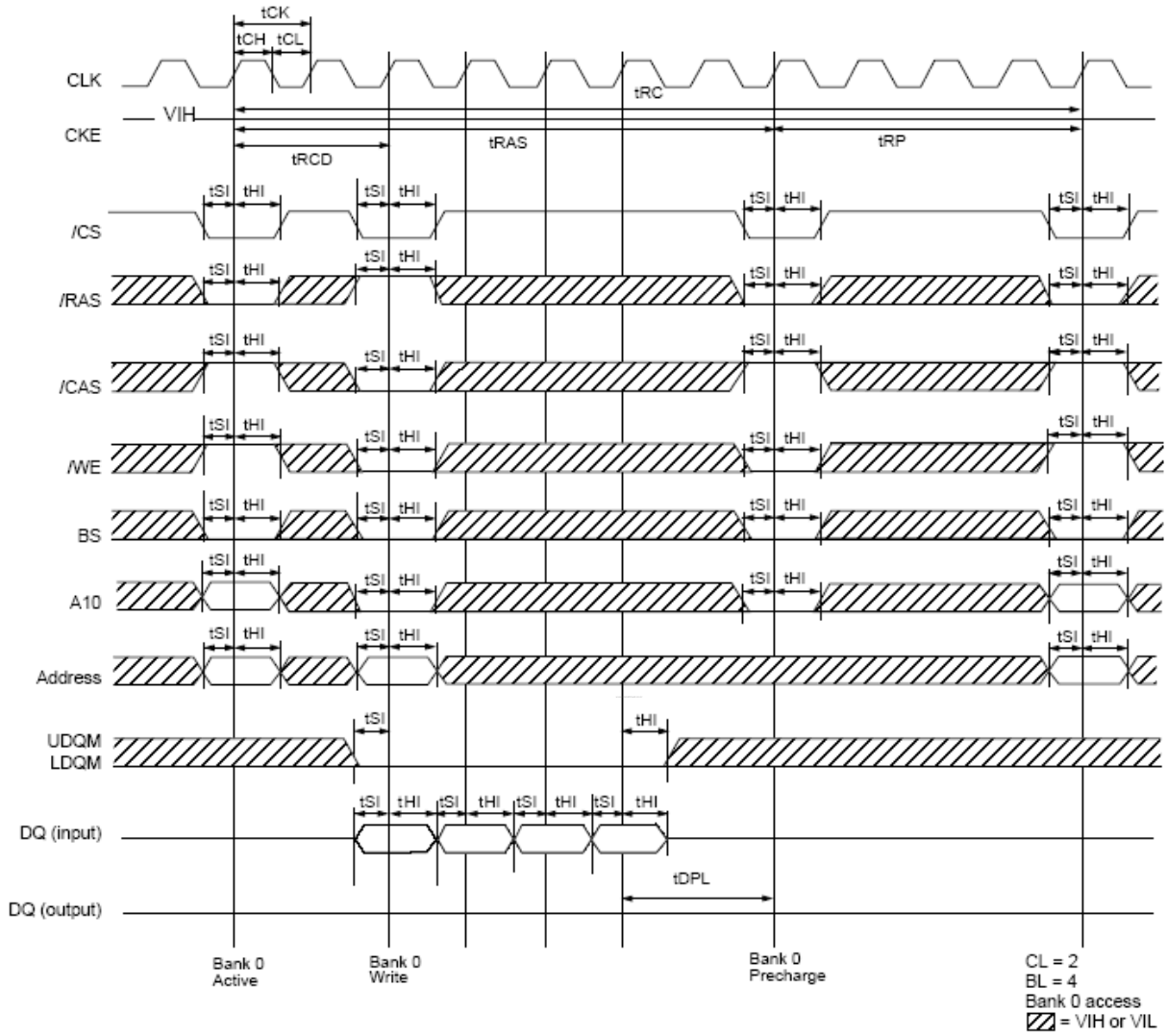
Clock suspend mode
By driving CKE to Low during a bank active or read/write operation, the SDRAM enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

Timing Waveforms

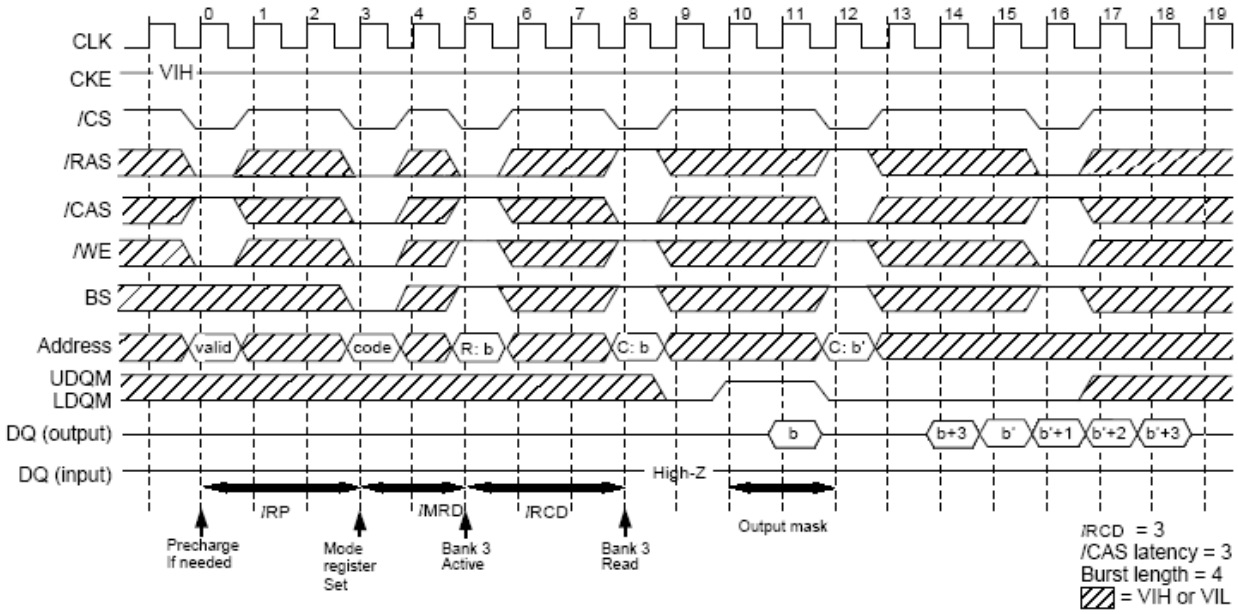
Read Cycle



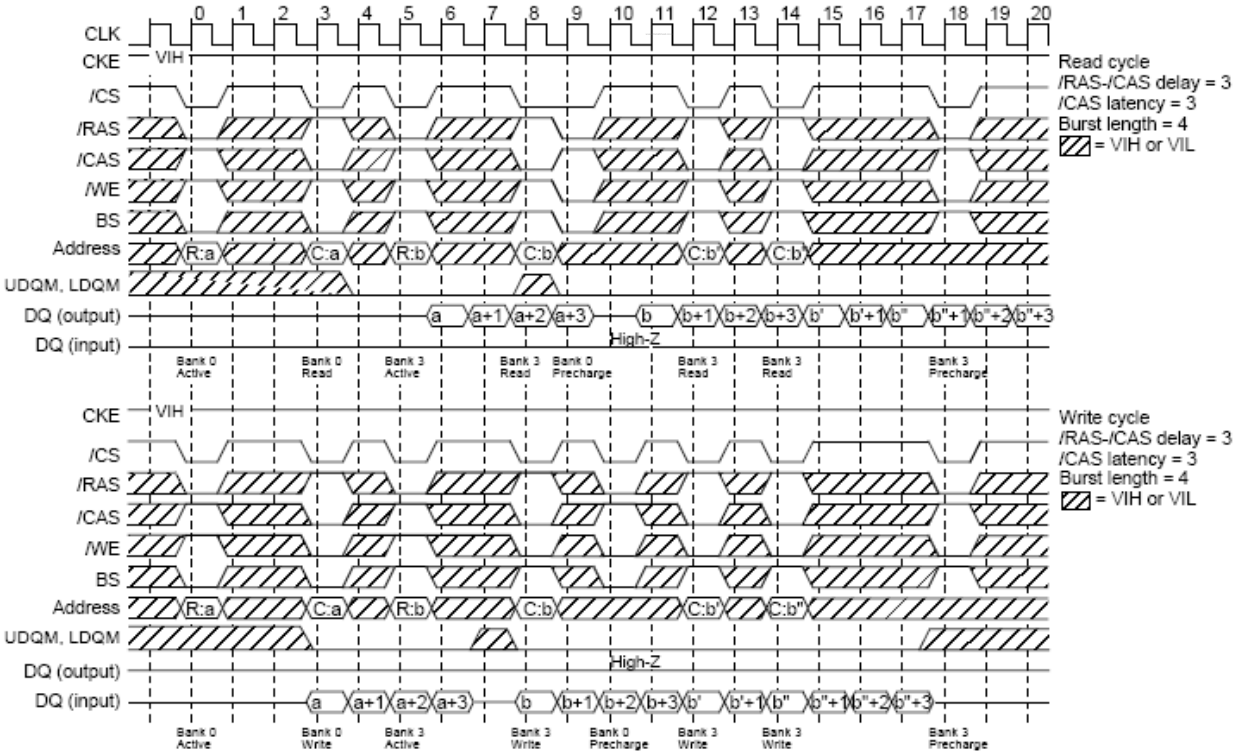
Write Cycle


tCK
tCH
tCL
CLK
VIH
CKE
tRC
tRAS
tRP
tRCD
/CS
/RAS
/CAS
/WE
BS
A10
Address
UDQM
LDQM
tSI
tHI
DQ (input)
DQ (output)
tDPL
Bank 0
Active
Bank 0
Write
Bank 0
Precharge
CL = 2
BL = 4
Bank 0 access
= VIH or VIL

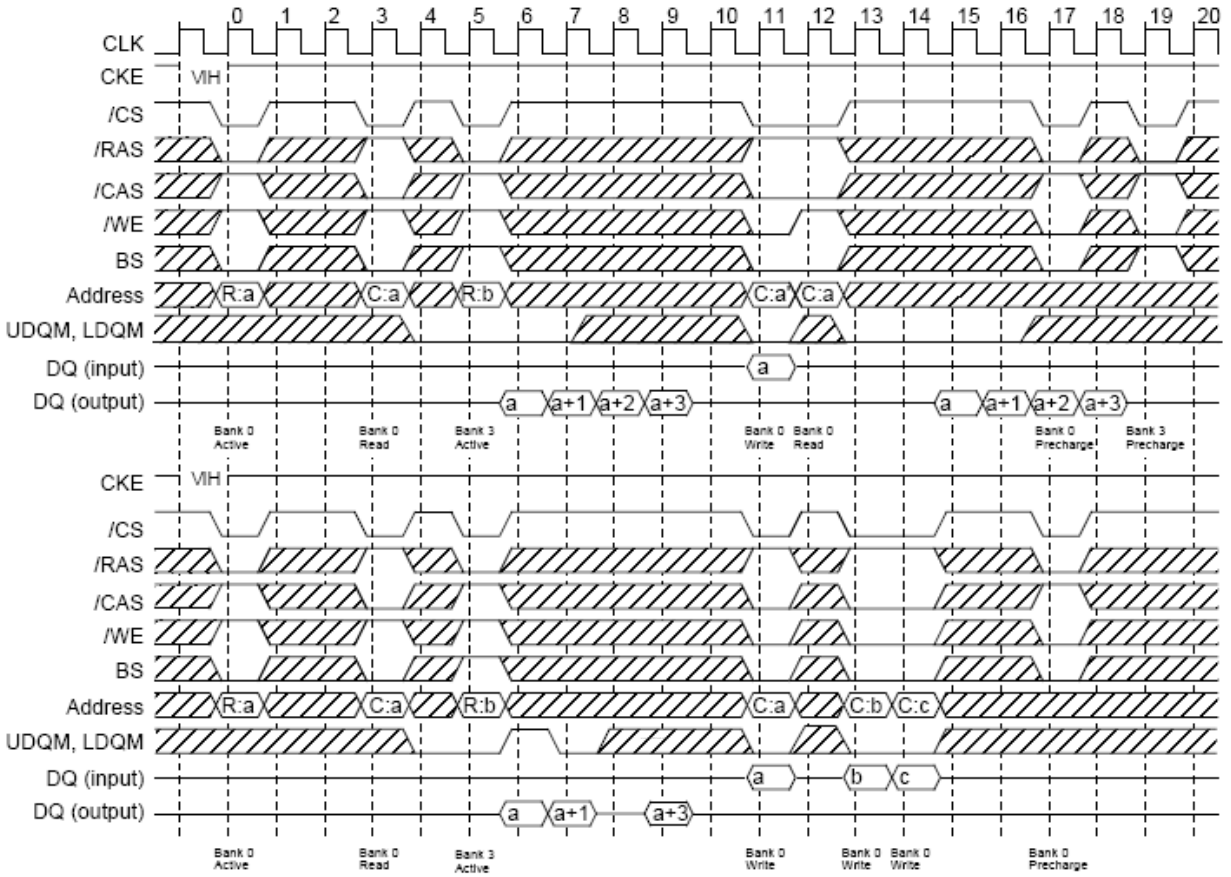
Mode Register Set Cycle



Read Cycle/Write Cycle

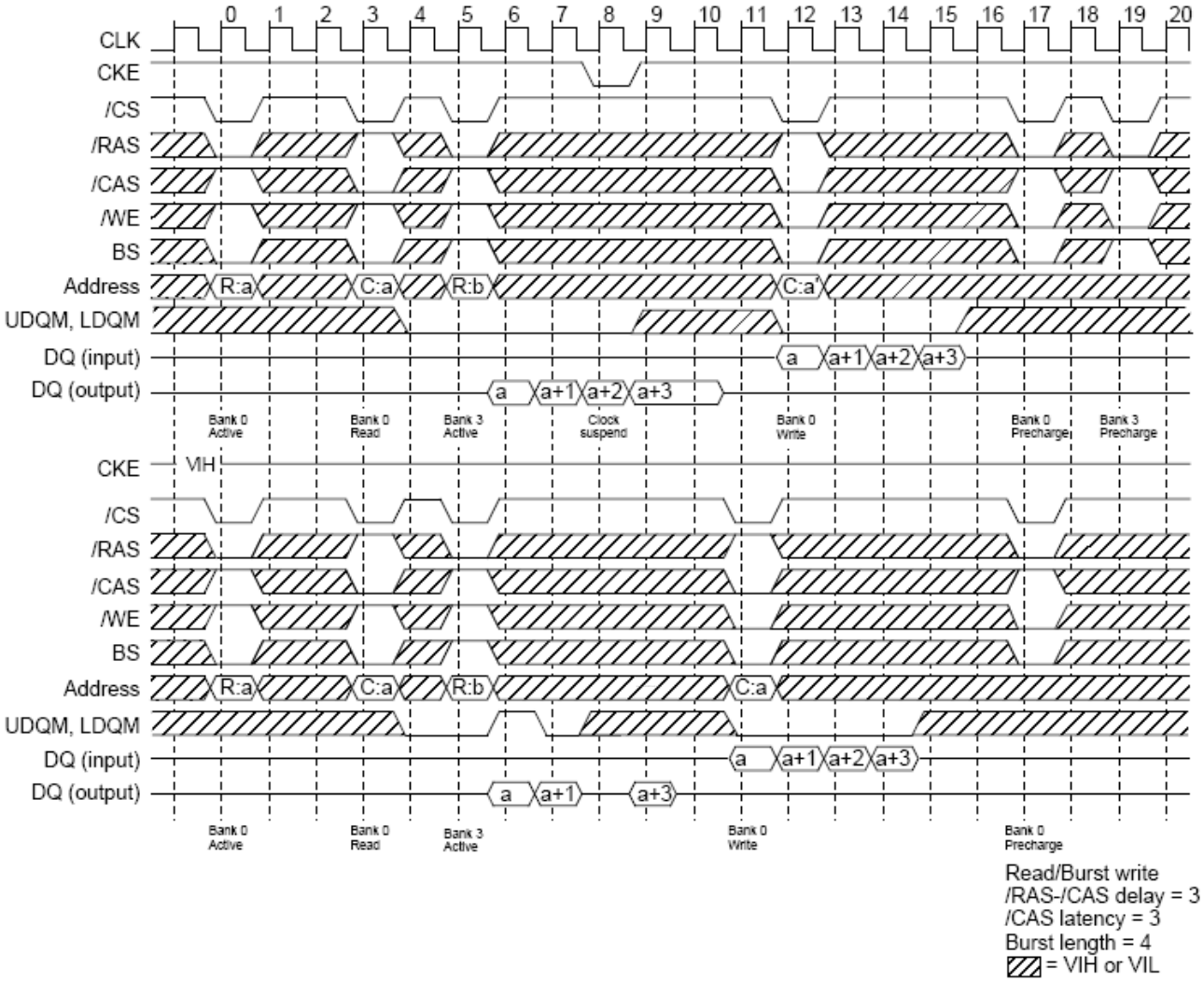


Read/Single Write Cycle



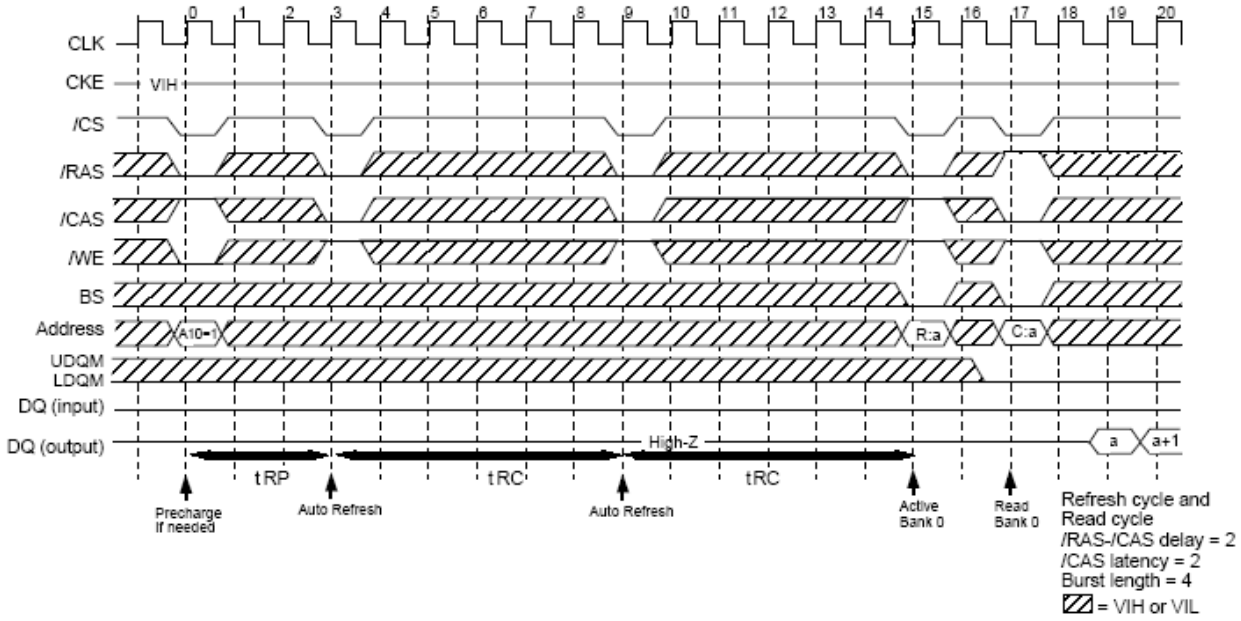
Read/Single write
/RAS-/CAS delay = 3
/CAS latency = 3
Burst length = 4
▨ = VIH or VIL

Read/Burst Write Cycle

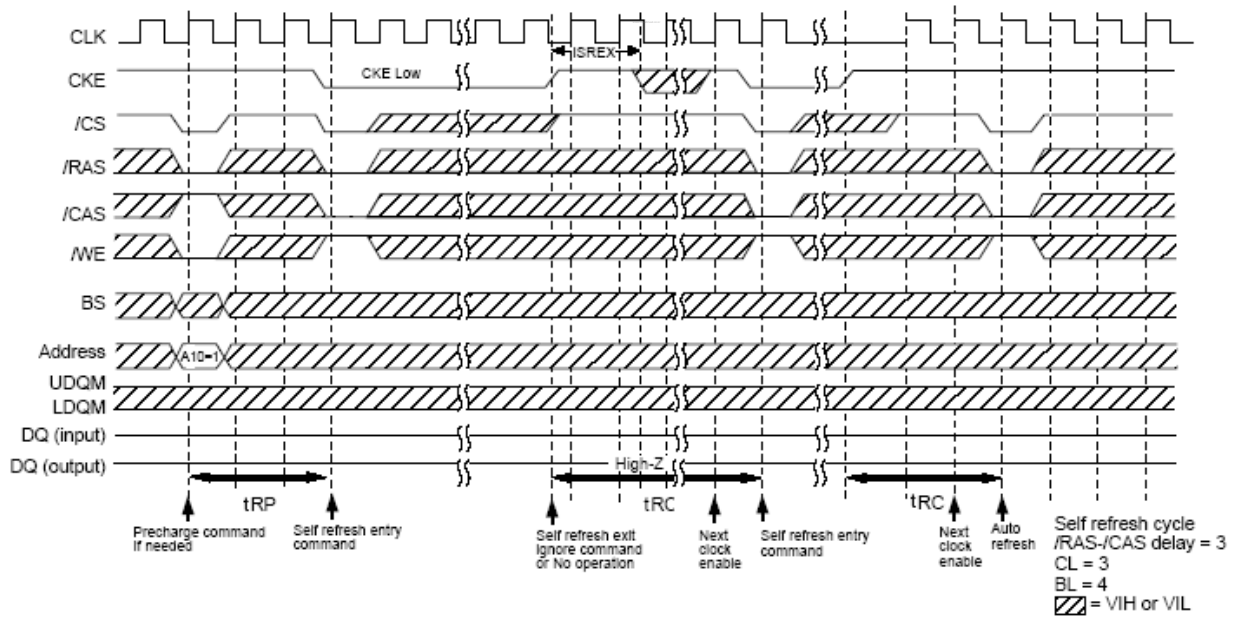


Read/Burst write
/RAS-/CAS delay = 3
/CAS latency = 3
Burst length = 4
▨ = VIH or VIL

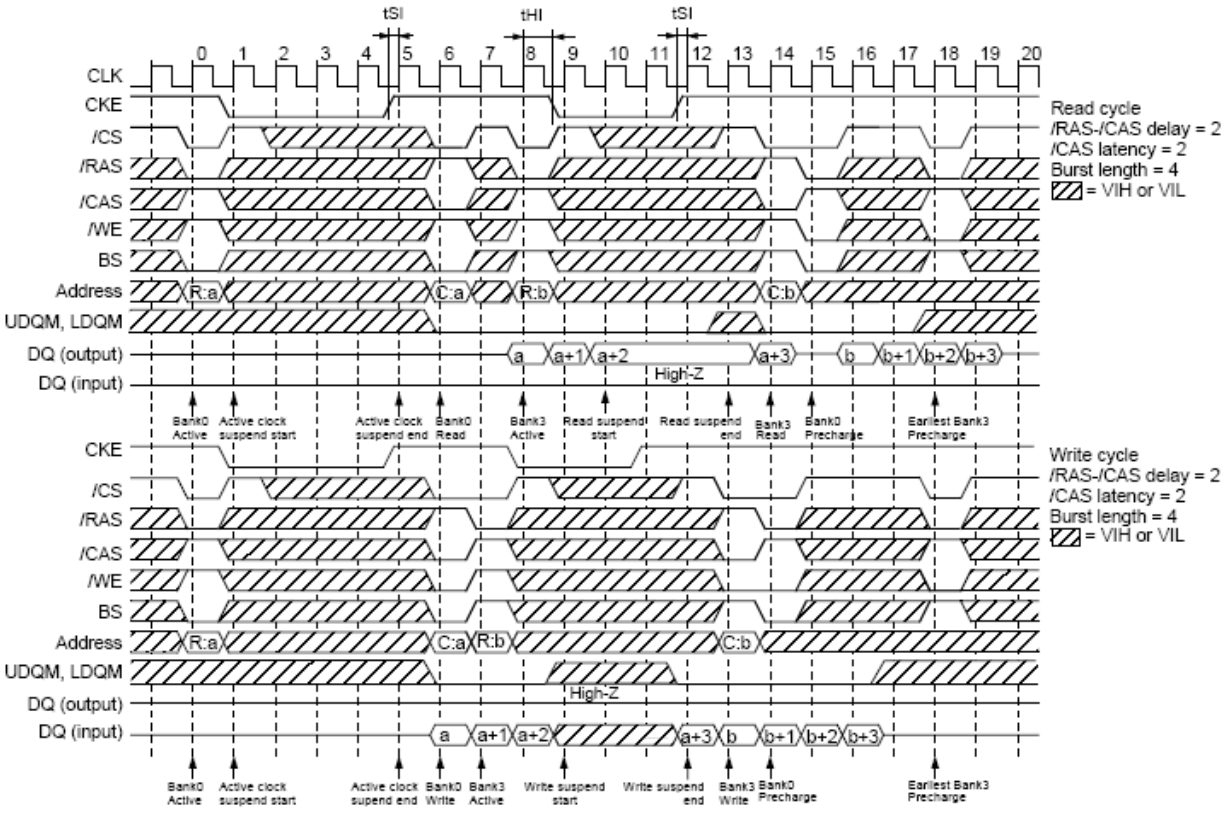
Auto Refresh Cycle



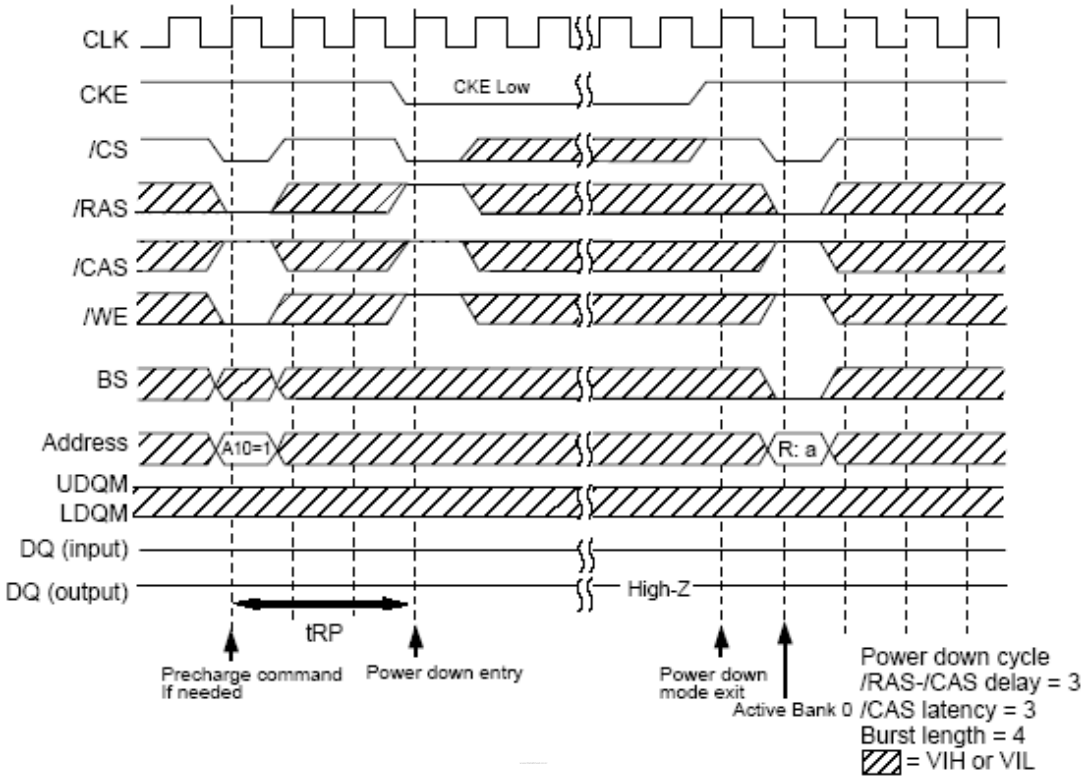
Self Refresh Cycle



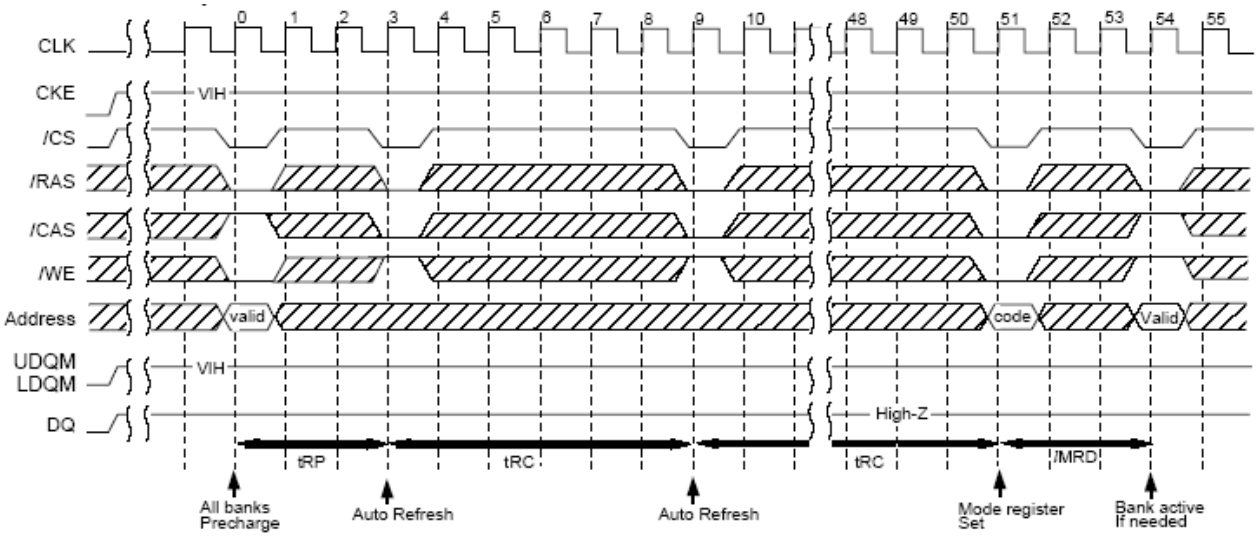
Clock Suspend Mode



Power Down Mode



Initialization Sequence



ELECTRONICS TESTING CENTER, TAIWAN

Address : No. 8, Lane 29, Wen-Ming Rd., Lo-Shan Tsun Kui-Shan Hsiang, Taoyuan Hsien 333 Taiwan, R.O.C
TEL : 886-3-328-0026 ext 291,292,
FAX : 886-3-327-6176

Testing Report

Company : Siliconware Precision Industries Co.,Ltd
Address: NO.123, SEC 3, DA FONG RD,TANTZU TAICHUNG TAIWAN R.O.C
Receive Date : 26th Jul., 2004
Date Issued : 2th Aug., 2004

For Office Use
Application No. : ET93O-07-016
Reviewed by :
Total Pages : 2 This Page : 1

Notes :
1. This report relates only to the items tested, and the content of this report is for references, but not for advertising publicity or other commercial purpose.
2. The testing report shall not be reproduced except in full, without the written approval of ETC.

Electronics Testing Center, Taiwan

Peter Huang
Manager

Y.H. Tseng
Lab. Leader

Testing Item & Experimental:

Submitted Substance	Instruments	Modified Method
Lead and its compounds(Pb)	ICP-OES	US EPA 3050B
Cadmium and its compounds(Cd)	ICP-OES	US EPA 3050B
Mercury and its compounds(Hg)	ICP-OES	US EPA 3051A
Hexavalent-Chromium (VI), Cr^{6+}	UV-VIS	US EPA 3060A & 7196A
Polybrominated Biphenyls(PBBs)	GC-MS	US EPA 8082A/8081A/8270C
Polybrominated Diphenylethers (PBDEs)	GC-MS	US EPA 8082A/8081A/8270C

Results:

ET93O-07-016

Sample Description **54LOC-TSOP II Lead free**

Style/Item No. ----

ETC **ELECTRONICS TESTING CENTER, TAIWAN**

Address : No. 8, Lane 29, Wen-Ming Rd., Lo-Shan Tsun Kui-Shan Hsiang, Taoyuan Hsien 333 Taiwan, R.O.C
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2. The testing report shall not be reproduced except in full, without the written approval of ETC.

Analytical Substance	Testing Result (ppm, mg/ kg-each of sample)		
	ET93O-07-016	Note	MDL
Lead (Pb)	15.51	----	0.0360
Cadmium (Cd)	2.23	----	0.0018
Mercury (Hg)	N.D.	----	0.0216
Chromium (VI), Cr^{6+}	N.D.	<0.05	0.0033
PBBs	N.D.	----	0.1000
PBDEs	N.D.	----	0.1000

Notice For Customer:
1. MDL means Method Detection Limitation.
2. IDL means Instrument Detection Limitation.
3. N.D. means non-detected.
4. Each of samples was made for twice and calculated by mean value.
5. ppm means 10^{-6} of part per million; ppb means 10^{-9} of part per billion.

Test Report

REPORT NO. : **LPCI/08316/07**
CTS REF. : **CTS/07/2054/Hitachi Chemical**
DATE REPORTED : JUNE 01, 2007
PAGE : 1 of 4

HITACHI CHEMICAL CO LTD.

The following merchandise was (were) submitted and identified by the client as:

Sample Name	:	CEL – 9200HF10
Sample Received	:	2007/05/07
Testing Date	:	2007/05/07 to 2007/05/15
Date Reported	:	2007/06/01

Test Result : Please see the next page

Analysts: Lim Meng Hoe, Jocelyn Christmas

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

REPORT NO. : **LPCI/08316/07**
CTS REF. : **CTS/07/2054/Hitachi Chemical**
DATE REPORTED : JUNE 01, 2007
PAGE : 2 of 4

Company : **HITACHI CHEMICAL CO LTD.**

Test Result

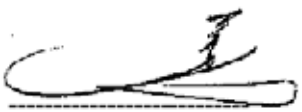
Sample Name : CEL – 9200HF10

Test Item (s) :	Unit	Method	MDL	Result
Chromium VI (Cr6+)	ppm	UV-Vis as per EPA 3060 A / 7196 A	2	N.D.
Cadmium (Cd)	ppm	ICP-OES as per EN 1122, method B:2001 (acid digestion method)	2	N.D.
Lead (Pb)	ppm	ICP-OES as per US EPA 3050B (acid digestion method)	2	N.D.
Mercury (Hg)	ppm	ICP-OES as per US EPA 3052 (acid digestion method)	2	N.D.

NOTE: (a) N.D. = Not detected (<MDL)
(b) ppm = mg/kg
(c) MDL= Method Detection Limit

Analyst: Lim Meng Hoe

SGS LABORATORY SERVICES (M) SDN. BHD.



CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

REPORT NO. : **LPCI/08316/07**
CTS REF. : **CTS/07/2054/Hitachi Chemical**
DATE REPORTED : JUNE 01, 2007
PAGE : 3 of 4

Company : **HITACHI CHEMICAL CO LTD.**

Test Result

Sample Name : CEL – 9200HF10

Test Item (s) :	Unit	Method	MDL	Result
PBBs (Polybrominated Biphenyls)				
Monobromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Dibromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Tribromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Tetrabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Pentabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Hexabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Heptabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Octabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Nonabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Decabromo Biphenyl	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
PBDEs (Polybrominated Diphenyl ethers)				
Monobromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Dibromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Tribromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Tetrabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Pentabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Hexabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Heptabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Octabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Nonabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.
Decabromo Diphenyl Ether	ppm	GCMS as per EPA 3540C/3550B	5	N.D.

NOTE: (a) N.D. = Not detected (<MDL)
(b) ppm = mg/kg
(c) MDL= Method Detection Limit

Analyst: Jocelyn Christmas

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

Company : HITACHI CHEMICAL CO LTD.

Test Result

Sample Name : CEL – 9200HF10

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

REPORT NO: LPCI/08316/07
SGS LABORATORY SERVICES (M) SDN BHD

1. DETERMINATION OF HEXAVALENT CHROMIUM BY METHOD US EPA 3060A/7196A

Sample Preparation
↓
Add colour-developing reagent
↓
Acidify with H_2SO_4
↓
Let stand for 5-10 min
↓
Analyses by UV- Spectrophotometer (540 nm)

2. DETERMINATION OF LEAD CONTENT BY US EPA 3050B

Cut sample in small pieces
↓
Weight sample (1.0g) into digestion vessel
↓
Acid digestion (HCl and HNO_3)
↓
"Totally Dissolved"
↓
Analyses by ICP (220.353 nm)

3. MICROWAVE ASSISTED ACID DIGESTION OF SILICEOUS AND ORGANICALLY BASED METRICES (US EPA 3052)

Cut sample in small pieces
↓
Weight sample (0.2-0.5g) into digestion vessel
↓
Acid digestion (HF and HNO_3) – Microwave
↓
"Totally Dissolved"
↓
Analyses by ICP

4. PLASTIC – DETERMINATION OF CADMIUM – WET DECOMPOSITION METHOD (EN 1122) – METHOD B

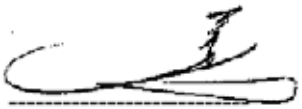
Cut sample in small pieces
↓
Weight sample (1.0g) into Kjeldahl flask
↓
Acid digestion (H_2SO_4)
↓
"Totally Dissolved"
↓
Analyses by ICP (228.802 nm)

5. DETERMINATION OF PBB/PBDE WITH GC-MS

Cut sample in small pieces
↓
Weight sample (2g) into extraction thimble
↓
Soxhlet Extraction with Toluene
↓
Filter through 0.45 um membrane filter
↓
Analyses by GC-MS (with appropriate dilution)

**** End of Report ****

SGS LABORATORY SERVICES (M) SDN. BHD.



CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Test Report

Application No	07-05-QAC-117
Date of Receipt	2007/05/21
Date of Performance	2007/05/22
Date of Issue	2007/05/28
Manufacturer	LS Cable
Address	No.12-9, Bo-ai 3rd Rd., Zuoying District, Kaohsiung City 813, Taiwan (R.O.C.)
Sample Description	LEAD FRAME
Report Content	A. Sample Information & Results B. Sample Photo C. Flow Chart

1. Any sample(s) and its information listed in this document are provided and identified by clients.
2. This report only refers to the specimen(s); it does not imply the result of production to tested sample(s).
3. This Test Report cannot be reproduced, except in full, without prior written permission of the laboratory.

Tested by:_____
Engineer

Checked by:_____
Laboratory Representative

Approved by:_____
Department Manager

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

A. Sample Information

	NO.1
Sample No.	07-05-QAC-117
Sample Description	LEAD FRAME
Model No.	---

Test Results

Analytical Substance	Method & Instruments		Unit (ppm)	
			NO.1	MDL
Cr^{+6} (CAS NO.1333-82-0)	UV-VIS	US EPA 3060A & 7196A	N.D.	2.0
Cd (CAS NO.7440-43-9)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Hg (CAS NO.7439-97-6)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Pb (CAS NO.7439-92-1)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Sb	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
As	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Be	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Bi	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Se	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

tributyly tin & Tributyl Tin Oxide	GC-FPD	NIEA T504.30B	N.D.	1.0
Bis(2-ethylhexyl) phthalate (CAS NO.117-81-7)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
Bis(2-methoxyethyl) phthalate (CAS NO.117-82-8)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
Dibutyphahthalate (CAS NO.84-74-2)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
PBBs (CAS NO.059536-65-1)				
Monobromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Dibromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tribromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tetrabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Pentabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Hexabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Heptabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Octabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Nonabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Decabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
PBDEs **(CAS NO.1163-19-5)**				
Monobromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Dibromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tribromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tetrabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Pentabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Hexabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Heptabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Octabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Nonabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Decabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0

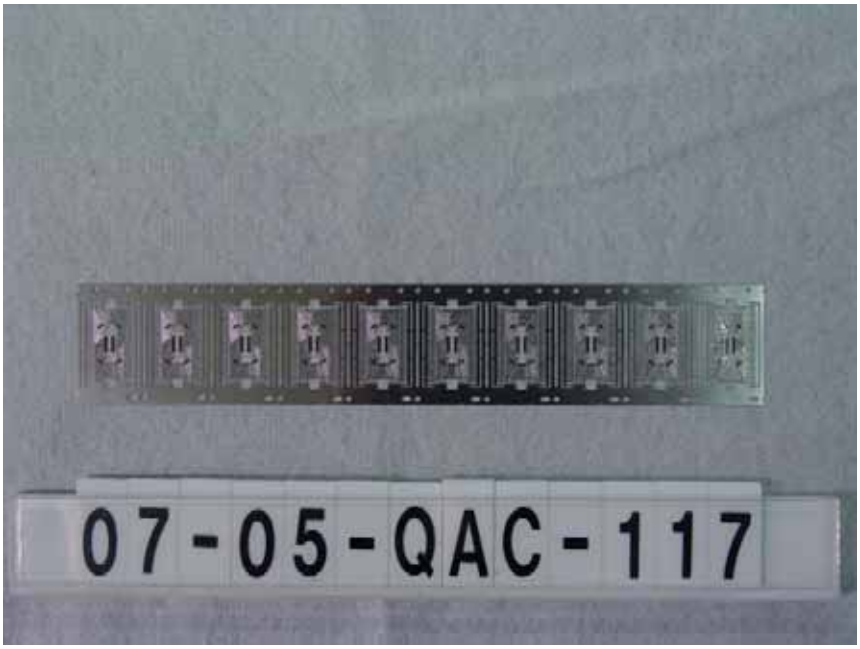
No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Note:

1. MDL : Method Detection Limitation.
2. N.D. : Not Detected.
3. ppm : = mg/kg (0.1% = 1000 ppm)
4. --- : Not Applicable

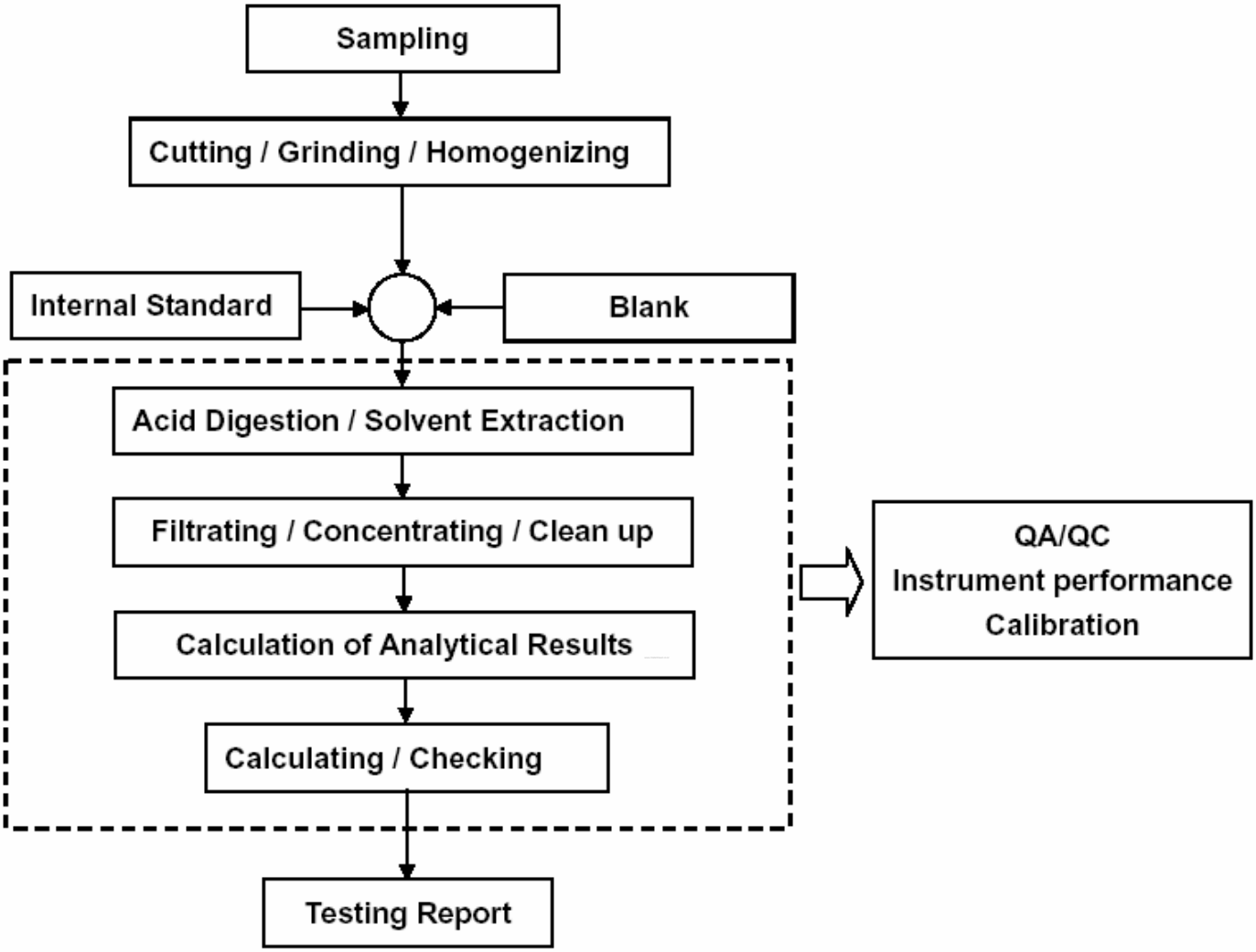
No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

B. Sample Photo



No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

C. Flow Chart



---End of Report---

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Test Report

Application No	07-05-QAC-138
Date of Receipt	2007/05/23
Date of Performance	2007/05/24
Date of Issue	2007/05/30
Manufacturer	Hitachi Chemical Co., Ltd.Goi Works
Address	14,Goi Minami Kaigan,Ichihara-shi,Chiba,290-8567,Japan
Sample Description	Die Pad Tape
Report Content	A. Sample Information & Results B. Sample Photo C. Flow Chart

1. Any sample(s) and its information listed in this document are provided and identified by clients.
2. This report only refers to the specimen(s); it does not imply the result of production to tested sample(s).
3. This Test Report cannot be reproduced, except in full, without prior written permission of the laboratory.

Tested by:_____
Engineer

Checked by:_____
Laboratory Representative

Approved by:_____
Department Manager

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

A. Sample Information

	NO.1
Sample No.	07-05-QAC-138
Sample Description	Die Pad Tape
Model No.	HM-122U-FE100

Test Results

Analytical Substance	Method & Instruments		Unit (ppm)	
			NO.1	MDL
Cr^{+6} (CAS NO.1333-82-0)	UV-VIS	US EPA 3060A & 7196A	N.D.	2.0
Cd (CAS NO.7440-43-9)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Hg (CAS NO.7439-97-6)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Pb (CAS NO.7439-92-1)	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Sb	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
As	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Be	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Bi	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0
Se	ICP-OES	US EPA 3051A & 6010B	N.D.	2.0

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Organic tin compounds				
triphenyl tin (CAS NO.000668-34-8)	GC-FPD	NIEA T504.30B	N.D.	1.0
tributyly tin & Tributyl Tin Oxide	GC-FPD	NIEA T504.30B	N.D.	1.0
Certain phthalates				
Bis(2-ethylhexyl) phthalate (CAS NO.117-81-7)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
Bis(2-methoxyethyl) phthalate (CAS NO.117-82-8)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
Dibutyphahthalate (CAS NO.84-74-2)	GC-MS	US EPA 3540C & 8270C	N.D.	1.0
PBBs (CAS NO.059536-65-1)				
Monobromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Dibromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tribromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tetrabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Pentabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0

No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Hexabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Heptabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Octabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Nonabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Decabromobiphenyl	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
PBDEs **(CAS NO.1163-19-5)**				
Monobromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Dibromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tribromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Tetrabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Pentabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Hexabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Heptabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0

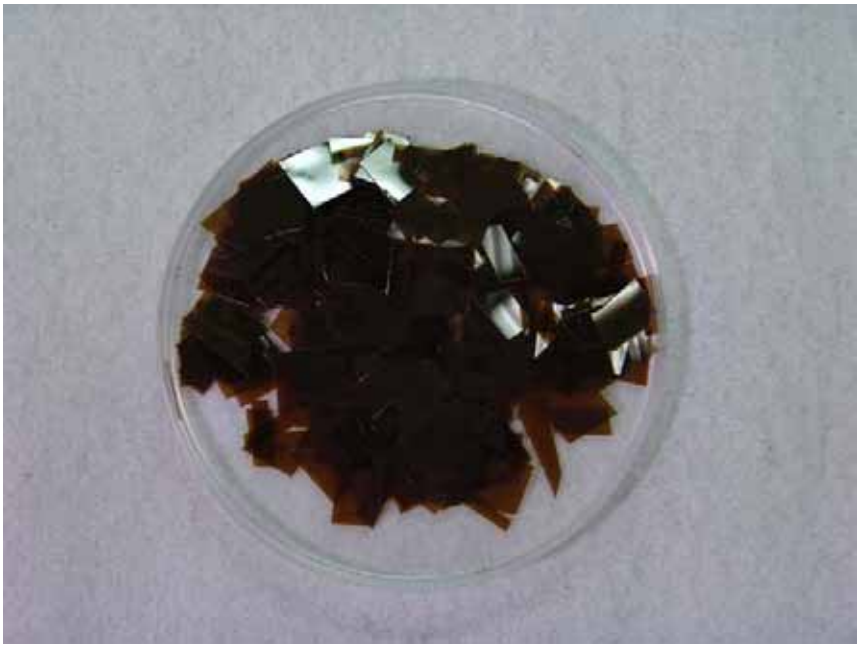
No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

Octabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Nonabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0
Decabromobiphenyl ether	GC-MS	US EPA 3540C & 8270C	N.D.	5.0

Note:
1. MDL : Method Detection Limitation.
2. N.D. : Not Detected.
3. ppm : = mg/kg (0.1% = 1000 ppm)
4. --- : Not Applicable

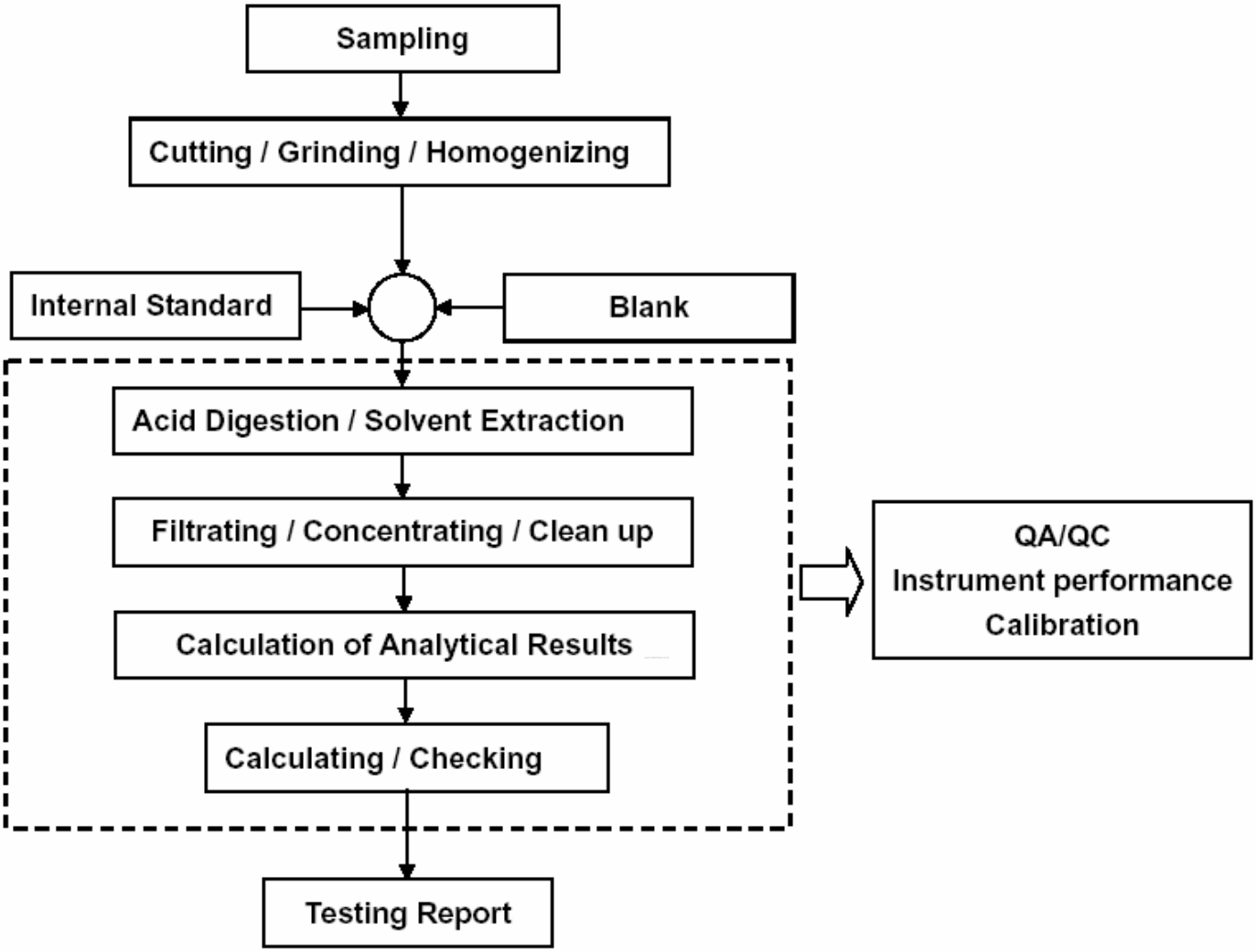
No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

B. Sample Photo



No. 8, Lane 29, Wen-Ming Rd., Kui-Shan, Taoyuan County, Taiwan 33383 ● 03-328-0026 ● www.etc.org.tw

C. Flow Chart



---End of Report---

Test Report

No. LPCI/00631/07 Date : 2007/01/18 Page: 1 of 4
CTS Ref. CTS/07/0151/Malaysian

MALAYSIAN ELECTRONICS MATERIALS SDN. BHD.
LOT 5, JALAN RAGUM 15/17, 40200 SHAH ALAM,
SELANGOR DARUL EHSAN.

The following merchandise was (were) submitted and identified by the client as:

Sample Description	:	WIRE SGA4
Sample Receiving Date	:	2007/01/12
Testing Period	:	2007/01/12 to 2007/01/18

Test Requested	:	In accordance with the RoHS Directive 2002/95/EC, and its amendment directives.
Test Method	:	(1) With reference to BS EN 1122:2001, Method B for Cadmium Content. Analysis was performed by ICP (2) With reference to EPA Method 3050B for Lead Content. Analysis was performed by ICP (3) With reference to EPA Method 3052 for Mercury Content. Analysis was performed by ICP (4) With reference to EPA Method 3060A & 7196A for Hexavalent Chromium. Analysis was performed by UV/Vis Spectrophotometry. (5) With reference to EPA Method 3540C/3550B for PBB / PBDE Content. Analysis was performed by GC/MS.
Test Results	:	Please refer to next page.
Analysts	:	Hasimah & Jocelyn

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

No. LPCI/00631/07 Date : 2007/01/18
CTS Ref. CTS/07/0151/Malaysian

Test results by chemical method (Unit: mg/kg)

Test Item(s):	Method (refer to)	Result	MDL
Cadmium(Cd)	(1)	N.D.	2
Lead (Pb)	(2)	N.D.	2
Mercury (Hg)	(3)	N.D.	2
Hexavalent Chromium (CrVI) by alkaline extraction	(4)	N.D.	2
Sum of Polybrominated Biphenyl (PBBs)	(5)	N.D.	-
Monobromobiphenyl		N.D.	5
Dibromobiphenyl		N.D.	5
Tribromobiphenyl		N.D.	5
Tetrabromobiphenyl		N.D.	5
Pentabromobiphenyl		N.D.	5
Hexabromobiphenyl		N.D.	5
Heptabromobiphenyl		N.D.	5
Octabromobiphenyl		N.D.	5
Nonabromobiphenyl		N.D.	5
Decabromobiphenyl		N.D.	5
Sum of Polybrominated Diphenylethers (PBDEs)		N.D.	-
Monobromodiphenyl ether		N.D.	5
Dibromodiphenyl ether		N.D.	5
Tribromodiphenyl ether		N.D.	5
Tetrabromodiphenyl ether		N.D.	5
Pentabromodiphenyl ether		N.D.	5
Hexabromodiphenyl ether		N.D.	5
Heptabromodiphenyl ether		N.D.	5
Octabromodiphenyl ether		N.D.	5
Nonabromodiphenyl ether		N.D.	5
Decabromodiphenyl ether		N.D.	5

Test Part Description :
As per page 3

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

Test Part Description :

Sample Description : WIRE SGA4

Note : (1) mg/kg = ppm
(2) N.D. = Not Detected
(3) MDL = Method Detection Limit

SGS LABORATORY SERVICES (M) SDN. BHD.

CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

1. DETERMINATION OF HEXAVALENT CHROMIUM BY METHOD US EPA 3060A/7196A

Sample Preparation
↓
Add colour-developing reagent
↓
Acidify with H_2SO_4
↓
Let stand for 5-10 min
↓
Analyses by UV- Spectrophotometer (540 nm)

2. DETERMINATION OF LEAD CONTENT BY US EPA 3050B

Cut sample in small pieces
↓
Weight sample (1.0g) into digestion vessel
↓
Acid digestion (HCl and HNO_3)
↓
"Totally Dissolved"
↓
Analyses by ICP

3. MICROWAVE ASSISTED ACID DIGESTION OF SILICEOUS AND ORGANICALLY BASED METRICES (US EPA 3052)

Cut sample in small pieces
↓
Weight sample (0.2-0.5g) into digestion vessel
↓
Acid digestion (HF and HNO_3) – Microwave
↓
"Totally Dissolved"
↓
Analyses by ICP

4. PLASTIC – DETERMINATION OF CADMIUM – WET DECOMPOSITION METHOD (EN 1122) – METHOD B

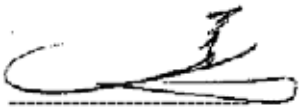
Cut sample in small pieces
↓
Weight sample (1.0) into Kjeldahl flask
↓
Acid digestion (H_2SO_4)
↓
"Totally Dissolved"
↓
Analyses by ICP

5. DETERMINATION OF PBB/PBDE WITH GC-MS

Cut sample in small pieces
↓
Weight sample (2g) into extraction thimble
↓
Soxhlet Extraction with Toluene
↓
Filter through 0.45 um membrane filter
↓
Analyses by GC-MS (with appropriate dilution)

**** End of Report ****

SGS LABORATORY SERVICES (M) SDN. BHD.



CHONG KIEN LEN
B.Sc.(HONS) AMIC
LAB MANAGER

Test Report

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.

NO.329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Report No. : KA/2007/50399
Date : 2007/05/14
Page : 1 of 4

The following sample(s) was/were submitted and identified by/on behalf of the client as :

Sample Description	:	錫鉍電鍍製程
Style/Item No.	:	Sn-Bi 電鍍製程
Sample Receiving Date	:	2007/05/07
Testing Period	:	2007/05/07 TO 2007/05/14

==========

Test Result(s) : - Please see the next page(s) -

Katherine Ho / Supervisor
Signed for and on behalf of
SGS Taiwan Limited

TW 4919711

Test Report

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.

NO.329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Report No. : KA/2007/50399
Date : 2007/05/14

Test Result(s)

PART NAME NO.1 : SILVER COLORED METAL

Test Item (s)	Unit	Method	MDL	Result No. 1
Cadmium (Cd)	mg/kg	With reference to IEC 62321, ED.1 (111/54/CDV). Determination of Cadmium by ICP-AES.	2	n.d.
Halogen-Chlorine (Cl) (CAS No:007782-50-5)	mg/kg	With reference to prEN14582 method B. Analysis was performed by IC method.	50	n.d.
Hexavalent Chromium Cr(VI) by Spot test / boiling water extraction	**	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of Hexavalent Chromium for metallic samples by Spot test / Colorimetric Method.	See Note 5	Negative
Mercury (Hg)	mg/kg	With reference to IEC 62321, ED.1 (111/54/CDV). Determination of Mercury by ICP-AES.	2	n.d.
Lead (Pb)	mg/kg	With reference to IEC 62321, ED.1 (111/54/CDV). Determination of Lead by ICP-AES.	2	n.d.
Sum of PBBs	mg/kg	With reference to IEC 62321, ED.1 (111/54/CDV). Determination of PBBs and PBDEs by GC/MS.	-	n.d.
Monobromobiphenyl			5	n.d.
Dibromobiphenyl			5	n.d.
Tribromobiphenyl			5	n.d.
Tetrabromobiphenyl			5	n.d.
Pentabromobiphenyl			5	n.d.
Hexabromobiphenyl			5	n.d.
Heptabromobiphenyl			5	n.d.
Octabromobiphenyl			5	n.d.
Nonabromobiphenyl			5	n.d.
Decabromobiphenyl			5	n.d.

TW 4919710

Test Report

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.

NO.329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Report No. : KA/2007/50399
Date : 2007/05/14

Test Item (s)	Unit	Method	MDL	Result No. 1
Sum of PBDEs (Mono to Nona)(Note 4)	mg/kg	With reference to IEC 62321, ED.1 (111/54/CDV). Determination of PBBs and PBDEs by GC/MS.	-	n.d.
Monobromobiphenyl ether			5	n.d.
Dibromobiphenyl ether			5	n.d.
Tribromobiphenyl ether			5	n.d.
Tetrabromobiphenyl ether			5	n.d.
Pentabromobiphenyl ether			5	n.d.
Hexabromobiphenyl ether			5	n.d.
Heptabromobiphenyl ether			5	n.d.
Octabromobiphenyl ether			5	n.d.
Nonabromobiphenyl ether			5	n.d.
Decabromobiphenyl ether			5	n.d.
Sum of PBDEs (Mono to Deca)			-	n.d.

Note :
1. mg/kg = ppm
2. n.d. = Not Detected
3. MDL = Method Detection Limit
4. According to 2005/717/EC DecaBDE is exempt.
5. Spot-test:
   Negative = Absence of Cr(VI) coating / surface layer, Positive = Presence of Cr(VI) coating / surface layer; (The tested sample should be further verified by boiling-water-extraction method if the spot test result cannot be confirmed.)
   Boiling-water-extraction:
   Negative = Absence of Cr(VI) coating / surface layer,
   Positive = Presence of Cr(VI) coating / surface layer the detected concentration in boiling-water-extraction solution is equal or greater than 0.02 mg/kg with 50 cm^2 sample surface area.
6. " - " = Not Regulated
7. " --- " = Not Conducted
8. ** = Qualitative analysis (No Unit)

TW4919709

SGS Taiwan Ltd. 台灣檢驗科技股份有限公司 | No. 208, Chung Hwa 2nd Road San Min District Kaohsiung, Taiwan. /高雄市三民區中華二路208號
t (886-7) 323-0920 f (886-7) 315-7484 www.tw.sgs.com
Member of SGS Group

Test Report

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.

NO.329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Report No. : KA/2007/50399
Date : 2007/05/14

** End of Report **

TW 4919708

SGS Taiwan Ltd. 台灣檢驗科技股份有限公司
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Test Report

No. : CE/2007/63291A Date : 2007/07/11 Page : 1 of 6

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.
NO. 329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

The following sample(s) was/were submitted and identified by/on behalf of the client as :

Sample Description	:	TSOPII-54 PACKAGE
Style/Item No.	:	P2V64SxxCTP-XXX (64M SDR 0.11)
Sample Receiving Date	:	2007/06/14
Testing Period	:	2007/06/14 TO 2007/06/23

==========

Test Result(s) : Please refer to next page(s).

Daniel Yeh, M.R. / Operation Manager
Signed for and on behalf of
SGS TAIWAN LTD.
Chemical Laboratory - Taipei

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.
NO. 329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Test Result(s)

PART NAME NO.1 : MIXED ALL PARTS

Test Item (s):	Unit	Method	MDL	Result No.1
Cadmium (Cd)	mg/kg	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of Cadmium by ICP-AES.	2	n.d.
Lead (Pb)	mg/kg	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of Lead by ICP-AES.	2	n.d.
Mercury (Hg)	mg/kg	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of Mercury by ICP-AES.	2	n.d.
Hexavalent Chromium Cr(VI) by alkaline extraction	mg/kg	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of Hexavalent Chromium for non-metallic samples by UV/Vis Spectrometry.	2	n.d.
Antimony (Sb)	mg/kg	With reference to US EPA Method 3050B for Antimony Content. Analysis was performed by ICP-AES.	2	n.d.
Halogen	---	With reference to prEN14582 method B. Analysis was performed by IC method for F, Cl, Br, I content.	---	---
Halogen-Chlorine (Cl) (CAS No.: 007782-50-5)	mg/kg	With reference to prEN14582 method B. Analysis was performed by IC method for Chlorine content.	50	n.d.
Halogen-Fluorine (F) (CAS No.: 007782-41-4)	mg/kg	With reference to prEN14582 method B. Analysis was performed by IC method for Fluorine content.	50	n.d.
Halogen-Bromine (Br) (CAS No.: 007726-95-6)	mg/kg	With reference to prEN14582 method B. Analysis was performed by IC method for Bromine content.	50	n.d.
Halogen-Iodine (I) (CAS No.: 007553-56-2)	mg/kg	With reference to prEN14582 method B. Analysis was performed by IC method for Iodine content.	50	n.d.

FORMOSA ADVANCED TECHNOLOGIES CO., LTD.
NO. 329, HO-NAN ST., TOULIU 640 YUNLIN, TAIWAN, R.O.C.

Test Item (s):	Unit	Method	MDL	Result No.1
Sum of PBBs	mg/kg	With reference to IEC 62321, Ed.1 111/54/CDV. Determination of PBB and PBDE by GC/MS.	-	n.d.
Monobromobiphenyl			5	n.d.
Dibromobiphenyl			5	n.d.
Tribromobiphenyl			5	n.d.
Tetrabromobiphenyl			5	n.d.
Pentabromobiphenyl			5	n.d.
Hexabromobiphenyl			5	n.d.
Heptabromobiphenyl			5	n.d.
Octabromobiphenyl			5	n.d.
Nonabromobiphenyl			5	n.d.
Decabromobiphenyl			5	n.d.
Sum of PBDEs (Mono to Nona) (Note 4)			-	n.d.
Monobromobiphenyl ether			5	n.d.
Dibromobiphenyl ether			5	n.d.
Tribromobiphenyl ether			5	n.d.
Tetrabromobiphenyl ether			5	n.d.
Pentabromobiphenyl ether			5	n.d.
Hexabromobiphenyl ether			5	n.d.
Heptabromobiphenyl ether			5	n.d.
Octabromobiphenyl ether			5	n.d.
Nonabromobiphenyl ether			5	n.d.
Decabromobiphenyl ether			5	n.d.
Sum of PBDEs (Mono to Deca)			-	n.d.

Note : 1. mg/kg = ppm
2. n.d. = Not Detected
3. MDL = Method Detection Limit
4. According to 2005/717/EC DecaBDE is exempt.
5. "---" = Not Conducted
6. " - " = Not Regulated
7. The sample(s) was/were analyzed on behalf of the applicant as mixing sample in one testing. The above result(s) was/were only given as the informality value.

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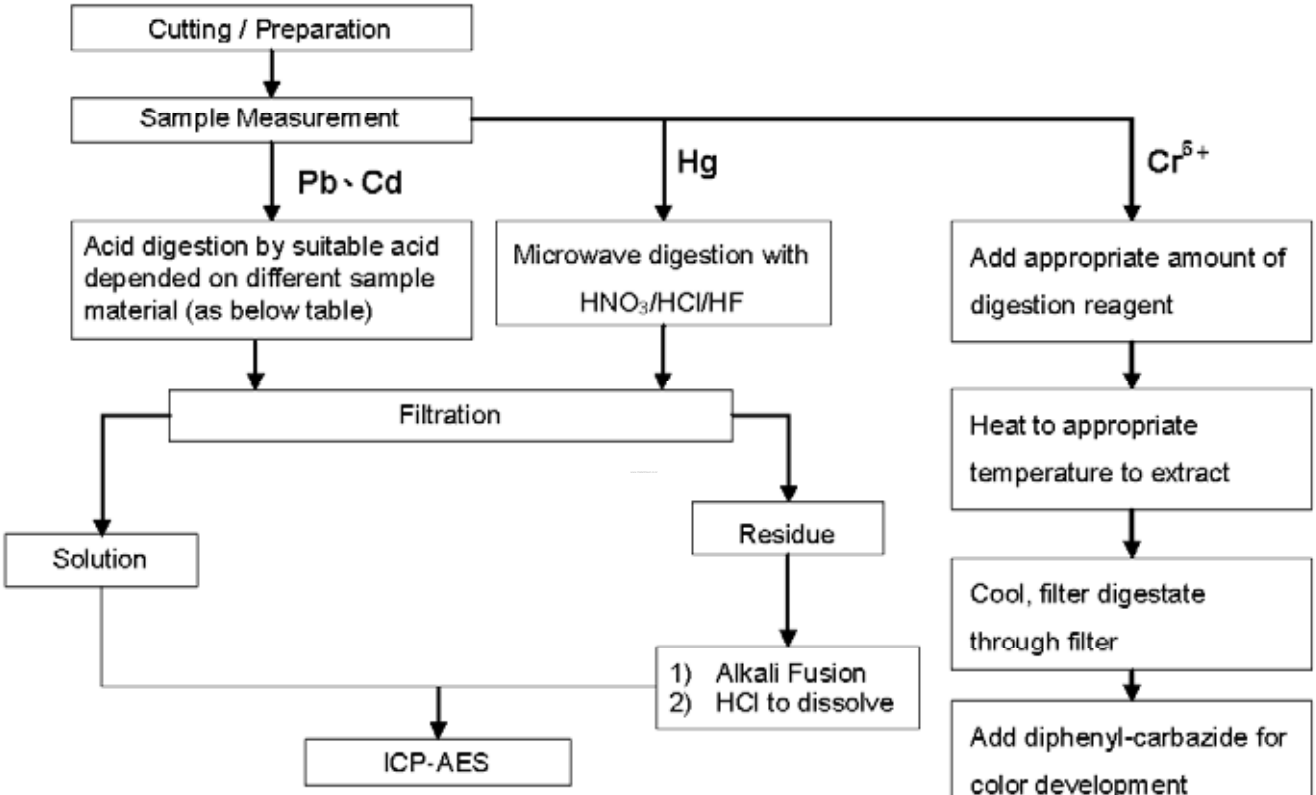
1) These samples were dissolved totally by pre-conditioning method according to below flow chart. (Cr6+ test method excluded)
2) Name of the person who made measurement: Troy Chang
3) Name of the person in charge of measurement: Daniel Yeh



Sample Material	Digestion Acid
Steel, copper, aluminum, solder	Aqua regia, HNO_3, HCl, HF, H_2O_2
Glass	HNO_3/HF
Gold, platinum, palladium, ceramic	Aqua regia
Silver	HNO_3
Plastic	H_2SO_4, H_2O_2, HNO_3, HCl
Others	Any acid to total digestion

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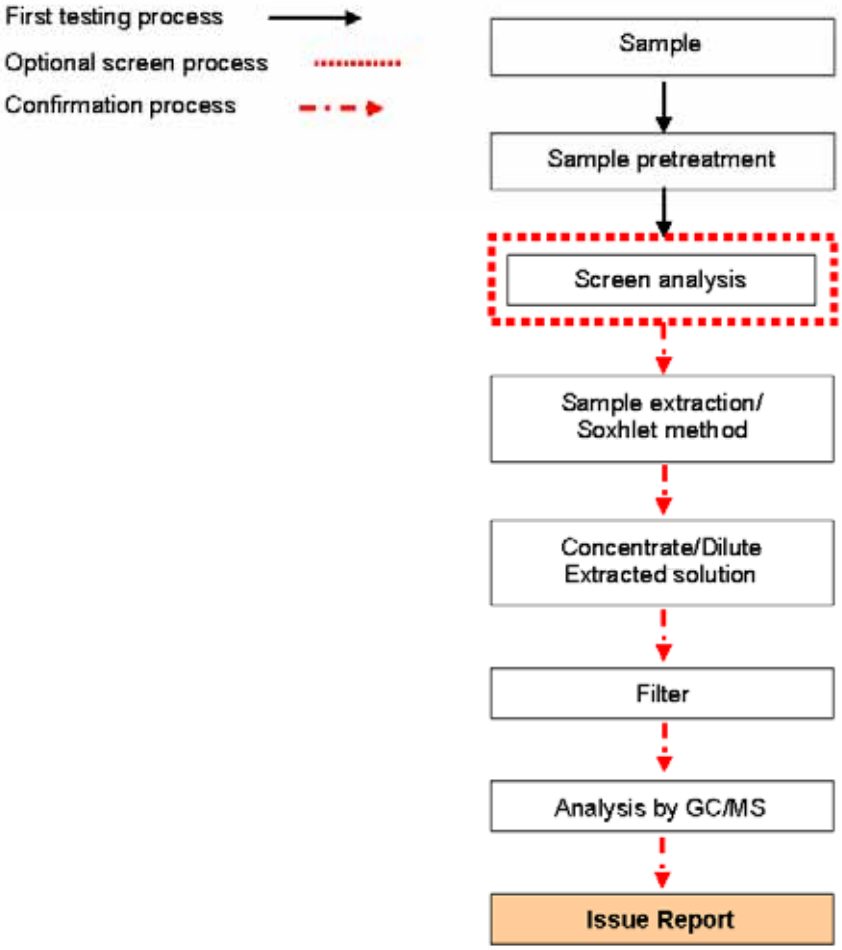
PBB/PBDE analytical FLOW CHART



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** End of Report **

禁用危害物質不含有保證書

Non-Contain of Restricted Hazardous Substance Guarantee Letter

本公司特在此保證：

本公司交付給台康資訊公司所有的產品(產品、零組件、材料、模組、包裝材料、製程用料等均屬之)，決不含有台康資訊公司所規範的禁用危害物質(如附表一：GP、GP2保證物質類別管制表)。而且當所交付之產品含有之禁用物質如有任何變更時，本公司亦負有主動修改相關資料及通知台康資訊公司知悉之責任。

以上針對禁用物質的保證內容如有不實，因而造成台康資訊公司任何之信譽損害或相關之費用產生，本公司願意承擔所有應負之責任。

We hereby guarantee：

Our company provides TAICOM DATA SYSTEM Company of all products(product, component, raw material, module, packaging material, production used related materials) such that it doesn't include restricted hazardous substance as stipulated in the document (Chart I: GP, GP2 Substance Management Form). And if there is any modification to the products or components. We will modify the document and will notify TAICOM DATA SYSTEM Company.

If the above statements has any falsification, which damages TAICOM image or bear any expenses. We will shoulder all the responsibility.

廠商名稱 (Vendor Name)：Zentel Electronics Corp.

產品名稱 (Product Name)：PLC：A2V64S40CTP-G6

A2V28S40CTP-G6

A3V56S40FTP-G6

保證物質類別 (Level of Guarantee Substance)：GP Level☑ GP2 Level☐ (勾選)

簽署 (Signature by)：堀明朝

職稱/職務 (Title/Position)：董事長

日期 (Date)：96. 8. 10

公司章 (Company Stamp)：

表單編號：21-014-A

GP、GP2 保證物質類別管制表

說明：GP Level 只需符合"必要的項目"，GP2 Level 則需符合"必要的項目"及"宣告項目"

一、必要的項目 **Essential items：GP,GP2 Level**

分類 Kinds	項目 Item	物質名稱 Substances Name	最大含有量 ppm (mg/kg) Maximum Concentration Valuc
重金屬 Heavy Metals	1	鉛及其化合物 Lead and its compounds	< 700
	2	汞及其化合物 Mercury and its compounds	< 700
	3	鎘及其化合物 Cadmium and its compounds	< 70
	4	六價鉻及其化合物 Hexavalent Chromium and its compounds	< 700
	5	包材中的重金屬的總合 (鎘+鉛+汞+六價鉻) Sum of heavy metals in packing material (Cd+Pb+Cd+Cr(VI))	Cd+Pb+Hg+Cr(VI)< 100
有機溴化合物 Brominated organic compounds	6	聚溴聯苯 PBBs	< 700
	7	溴聯苯醚 PBDEs	< 700

二、宣告項目 **Declaration items：GP2 Level**

分類 Kinds	項目 Item	物質名稱 Substances Name	最大含有量 ppm (mg/kg) Maximum Concentration Value
有機氯化合物 Chlorinated organic compounds	8	多氯聯苯及多氯對聯三苯 PCBs and PCTs	50
	9	氯化石蠟(C10~C13) ChlorinatedParaffins(10-13 carbon)	10000
	10	聚氯乙烯 PVC	Banned
	11	石棉 Asbestos	banned
	12	偶氮染料 Azo colorant	30
	13	破壞臭氧層物質 Ozone Depleting Substance	banned
其他金屬 Other metal	14	鎳及其化合物 Nickel & its compounds	0.5μg/cm²/week

簽署（**Signature by**）：_____ 日期（**Date**）：96. 8. 10

表單編號：21-014-A

供 應 商 危 害 物 質 一 覽 表 (Supplier Hazardous Substance Summary List)

供應商(Supplier)：奇普仕

表單編號:21-011-C

項 Item	產品類型(規格品名) Type of Product (Part Name)	台康料號 Taicom Part No.	細項 NO.	分離之均勻材質 (Homogeneous Material) Sub-parts	含有物質(Material/Substance) mg/kg=ppm						不含有物質保證書 (Non-contain Material Guarantee)	分析報告 Test Report	分析報告號碼(實驗室名稱) Test Report No.(Lab. Name)	備註/材料狀態 Remark /Component Status	GP類別 GP Level
					鉛 (Pb)	鎘 (Cd)	汞 (Hg)	六價鉻 (Cr+6)	PBB	PBDE					
1	A2V64S40CTP-G6PP	02350861	1-1	EMC	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	V	V	LPCI/08316/07		GP
			1-2	Lead Frame	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.		V	07-05-QAC-117		
			1-3	Die Attach	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.		V	07-05-QAC-138		
			1-4	Gold Wire	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.		V	LPCI/00631/07		
			1-5	Lead Finish	N.D.	N.D.	N.D.	Negative	N.D.	N.D.		V	KA/2007/50399		
			1-6	MIXED ALL PARTS	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.		V	CE/2007/63291A		

1.表單填寫參閱範例
2.產品類型可依個別產品或系列產品填寫
3.項次依實際狀況增減
4.不含有物質成份依分離成均質材料系列填寫,若爲單體整個測試,則註明"整個混測"
5.若測試項目含有排除條款之物質,可在材料狀態欄位中備註