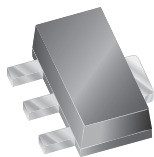


Chopper-Stabilized, Precision Hall-Effect Switch

Features and Benefits

- Resistant to Physical Stress
- Superior Temperature Stability
- Output Short-Circuit Protection
- Operation From Unregulated Supply
- Reverse Battery Protection
- Solid-State Reliability
- Small Size

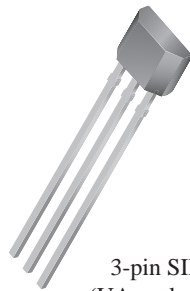
Packages:



3-pin SOT89
(LT package)



3-pin SOT23W
(LH package)



3-pin SIP
(UA package)

Not to scale

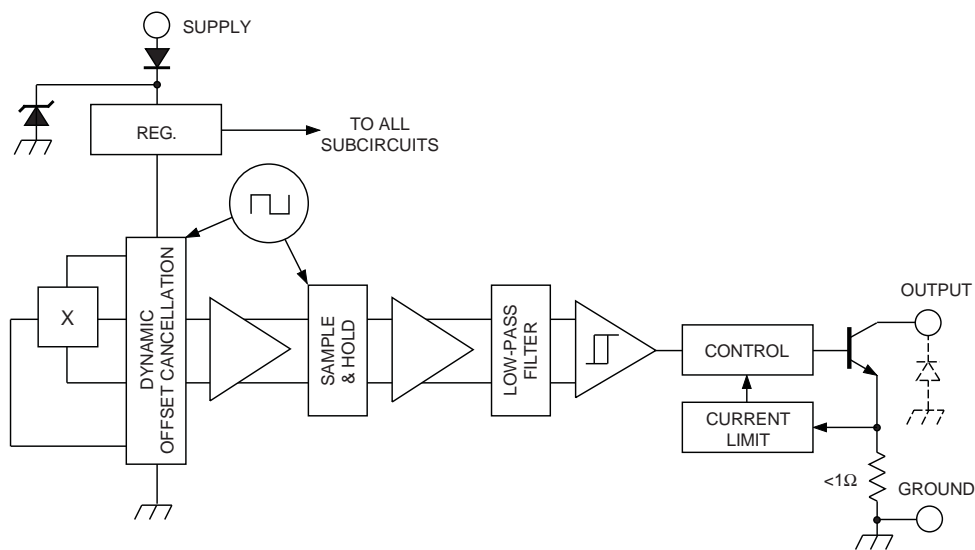
Description

The A3240 Hall-effect switch is an extremely temperature-stable and stress-resistant sensor IC especially suited for operation over extended temperature ranges to +150°C. Superior high-temperature performance is made possible through dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

The device includes on a single silicon chip a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit protected open-collector output to sink up to 25 mA. A south pole of sufficient strength will turn the output on. An on-board regulator permits operation with supply voltages of 4.2 to 24 volts.

Three package styles provide a magnetically optimized package for most applications. Package type LH is a modified SOT23W surface-mount package, LT is a miniature SOT89/TO-243AA transistor package for surface-mount applications; while UA is a three-lead ultra-mini-SIP for through-hole mounting. The LH and UA packages are also available in a lead (Pb) free version (suffix, -T), with a 100% matte tin plated leadframe.

Functional Block Diagram



Dwg. FH-020-1

Selection Guide

Part Number	Packing*	Mounting	Ambient, T_A (°C)	$B_{RP(MIN)}$ (G)	$B_{OP(MAX)}$ (G)
A3240ELHLT-T	7-in. reel, 3000 pieces/reel	Surface Mount	-40 to 85	5.0	50
A3240ELTTR-T	7-in. reel, 1000 pieces/reel	Surface Mount			
A3240EUA-T	Bulk, 500 pieces/bag	SIP through hole			
A3240LLHLT-T	7-in. reel, 3000 pieces/reel	Surface Mount	-40 to 150		
A3240LLTTR-T	7-in. reel, 1000 pieces/reel	Surface Mount			
A3240LUA-T	Bulk, 500 pieces/bag	SIP through hole			

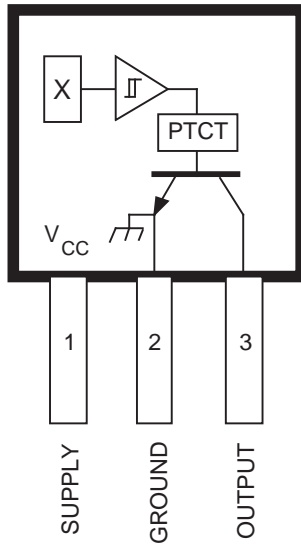


*Contact Allegro for additional packing options.

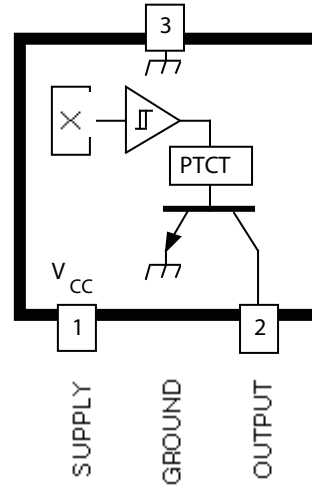
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		26.5	V
Reverse Battery Voltage	V_{RCC}		-30	V
Output Off Voltage	V_{OUT}		26	V
Continuous Output Current	I_{OUT}	Internal current limiting is intended to protect the device from output short circuits.	25	mA
Reverse Output Current	I_{ROUT}		-50	mA
Package Power Dissipation	P_D		See graph	W
Magnetic Flux Density	B	1 G = 0.1 mT (millitesla)	Unlimited	G
Operating Ambient Temperature	T_A	Range E	-40 to 85	°C
		Range L	-40 to 150	°C
Maximum Junction Temperature	$T_J(max)$		165	°C
Storage Temperature	T_{stg}		-65 to 170	°C

Suffix '-LT' & '-UA' Pinning
(SOT89/TO-243AA & ultra-min SIP)



Suffix '-LH' Pinning
(SOT23W)

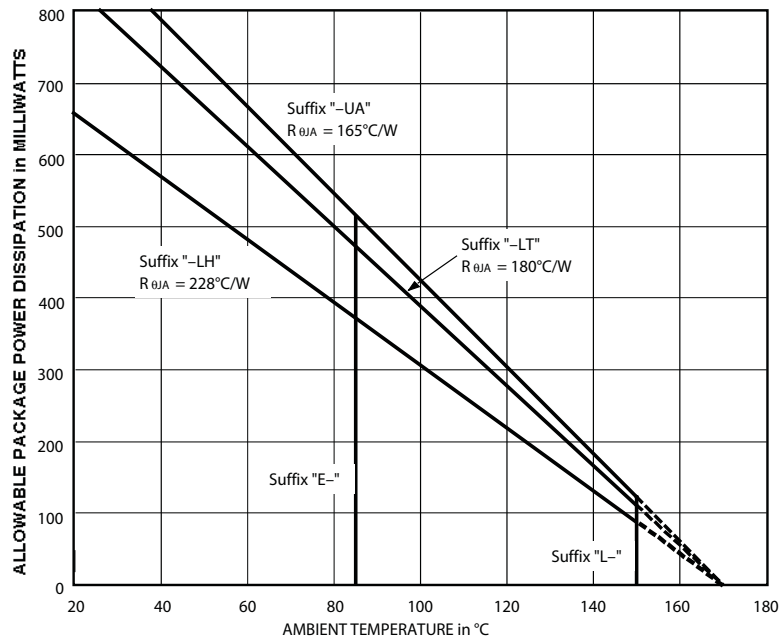


Dwg. PH-003-2

Dwg. PH-003-4

Pinning is shown viewed from branded side.

Package Power Dissipation



Dwg. GH-046-2D

ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	V_{CC}	Operating, $T_J < 170^\circ\text{C}^1$	4.2	–	24	V
Output Leakage Current	I_{OFF}	$V_{OUT} = 24\text{ V}$, $B < B_{RP}$	–	–	10	μA
Output Saturation Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$, $B > B_{OP}$	–	185	500	mV
Output Current Limit	I_{OM}	$B > B_{OP}$	30	–	60	mA
Power-On Time	t_{po}	$V_{CC} > 4.2\text{ V}$	–	–	50	μs
Chopping Frequency	f_C		–	340	–	kHz
Output Rise Time	t_r	$R_L = 820\ \Omega$, $C_L = 20\text{ pF}$	–	0.2	2.0	μs
Output Fall Time	t_f	$R_L = 820\ \Omega$, $C_L = 20\text{ pF}$	–	0.1	2.0	μs
Supply Current	I_{CC}	$B < B_{RP}$, $V_{CC} = 12\text{ V}$	–	3.0	6.0	mA
		$B > B_{OP}$, $V_{CC} = 12\text{ V}$	–	4.0	6.0	mA
Reverse Battery Current	I_{CC}	$V_{RCC} = -30\text{ V}$	–	–	-5.0	mA
Zener Voltage	$V_Z + V_D$	$I_{CC} = 15\text{ mA}$, $T_A = 25^\circ\text{C}$	28	32	37	V
Zener Impedance	$z_z + z_D$	$I_{CC} = 15\text{ mA}$, $T_A = 25^\circ\text{C}$	–	50	–	Ω

NOTES: 1. Maximum voltage must be adjusted for power dissipation and junction temperature.
 2. B_{OP} = operate point (output turns on); B_{RP} = release point (output turns off).
 3. Typical Data is at $T_A = +25^\circ\text{C}$ and $V_{CC} = 12\text{ V}$ and is for design information only.

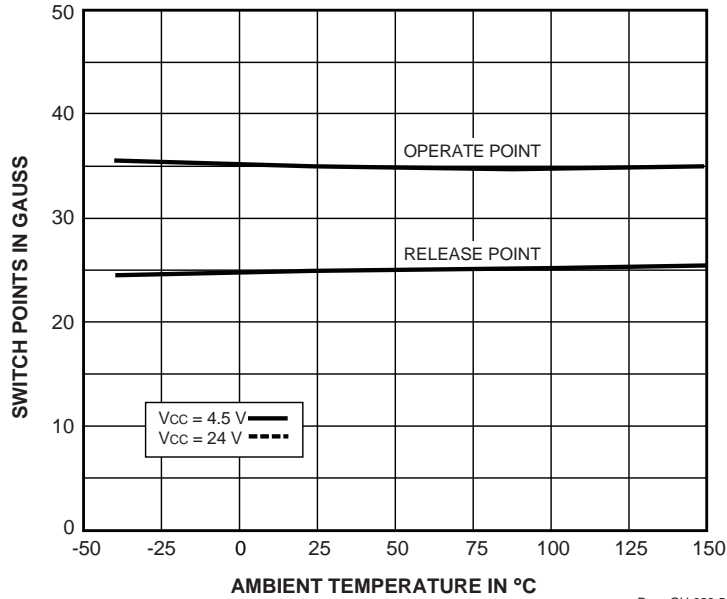
MAGNETIC CHARACTERISTICS over operating supply voltage and temperature ranges.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B_{OP}		–	35	50	G
Release Point	B_{RP}		5.0	25	–	G
Hysteresis	B_{hys}	$B_{OP} - B_{RP}$	–	10	–	G

NOTES: 1. Typical Data is at $T_A = +25^\circ\text{C}$ and $V_{CC} = 12\text{ V}$ and is for design information only.
 2. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

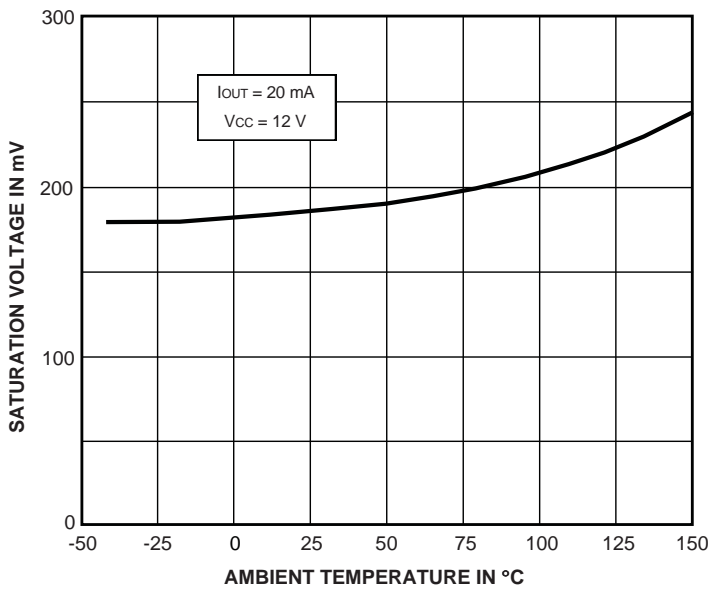
TYPICAL OPERATING CHARACTERISTICS
as a function of temperature

SWITCH POINTS



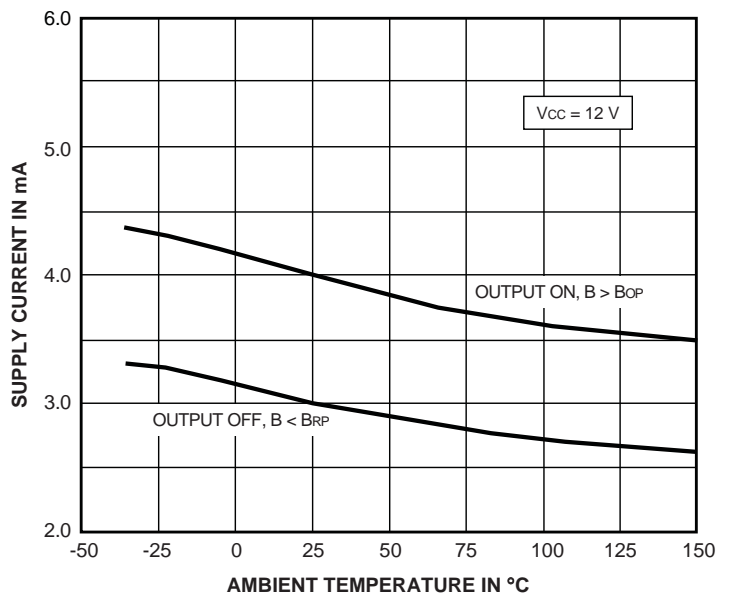
Dwg. GH-026-5

OUTPUT SATURATION VOLTAGE



Dwg. GH-029-4

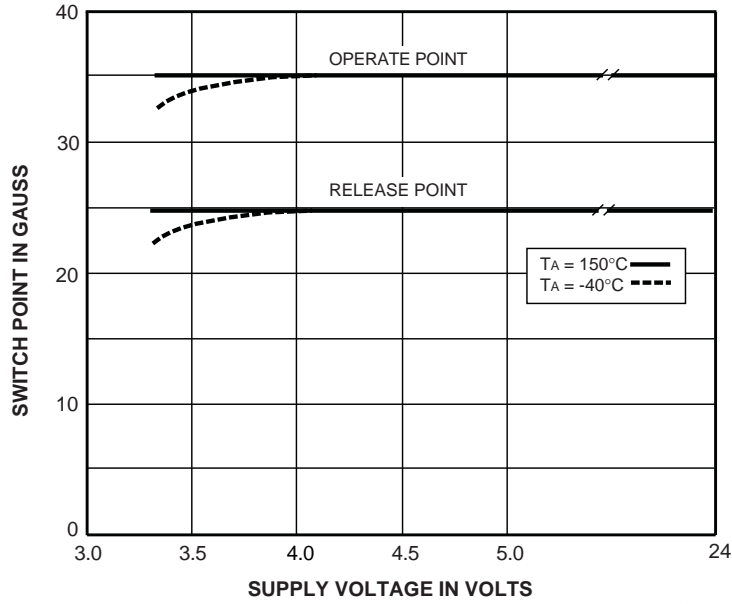
SUPPLY CURRENT



Dwg. GH-028-5

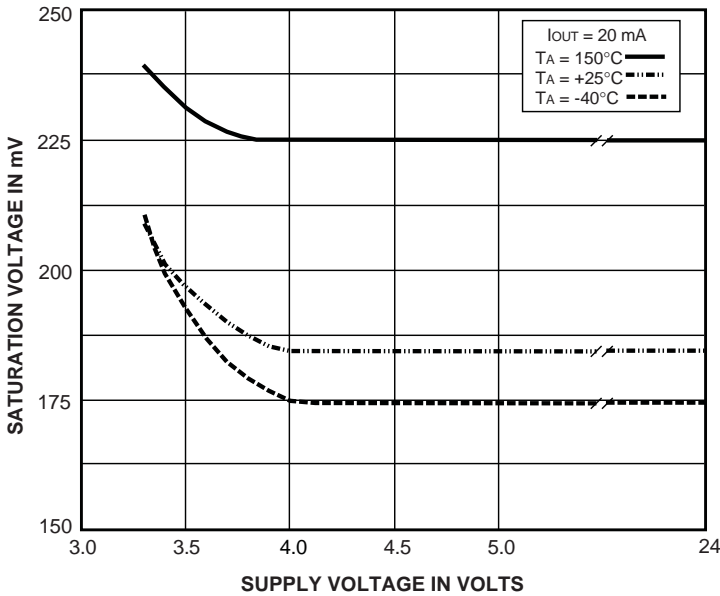
TYPICAL OPERATING CHARACTERISTICS
as a function of supply voltage

SWITCH POINTS



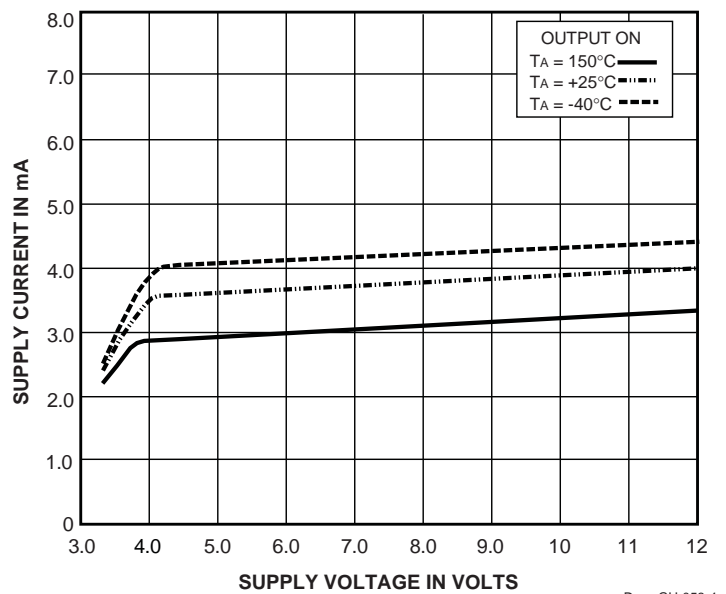
Dwg. GH-021-2

OUTPUT SATURATION VOLTAGE



Dwg. GH-055-1

SUPPLY CURRENT



Dwg. GH-058-4

FUNCTIONAL DESCRIPTION

Chopper-Stabilized Technique. The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaining the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability. A relatively high sampling frequency is used in order that faster signals can be processed.

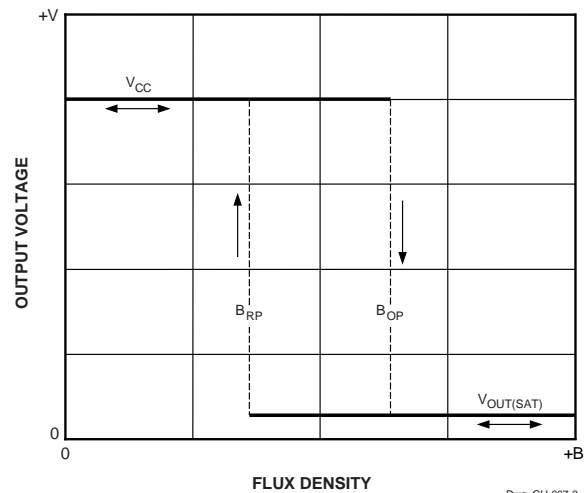
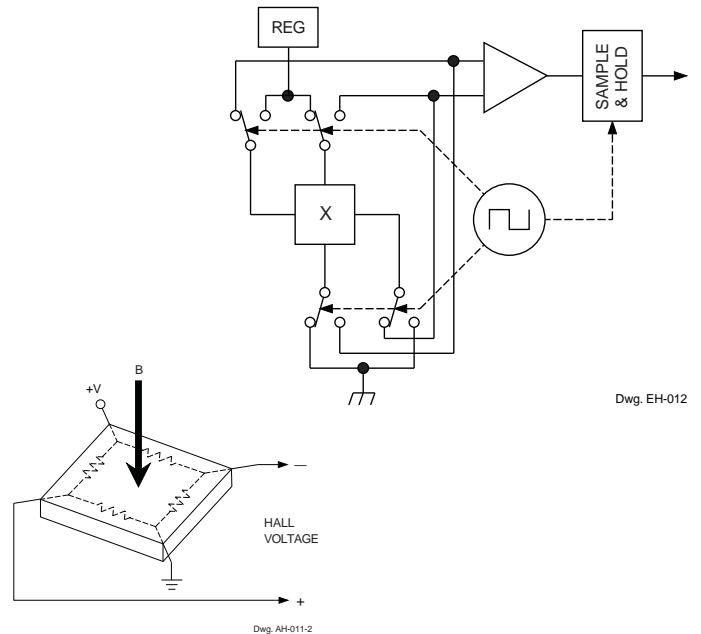
More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.

Operation. The output of these devices switches low (turns on) when a magnetic field (south pole) perpendicular to the Hall element exceeds the operate point threshold (B_{OP}). After turn-on, the output is capable of sinking 25 mA and the output voltage is $V_{OUT(SAT)}$. When the magnetic field is reduced below the release point (B_{RP}), the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis (B_{HYS}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

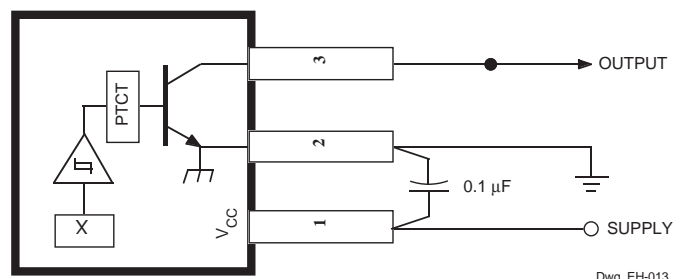
Applications. It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique.

The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation, such as linear magnets, are possible. Extensive applications information on magnets and Hall-effect devices is also available in *Application Note 27701*, or at

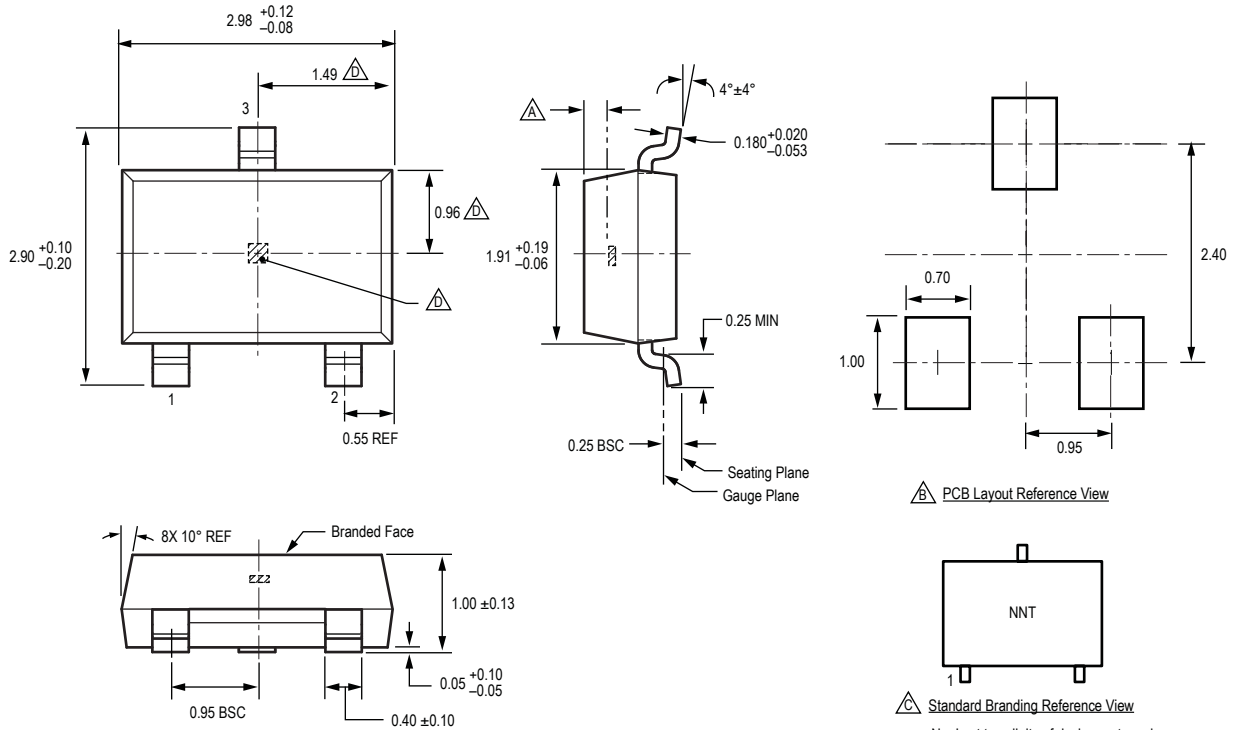
www.allegromicro.com



○ SUPPLY



Package LH, 3-Pin (SOT-23W)

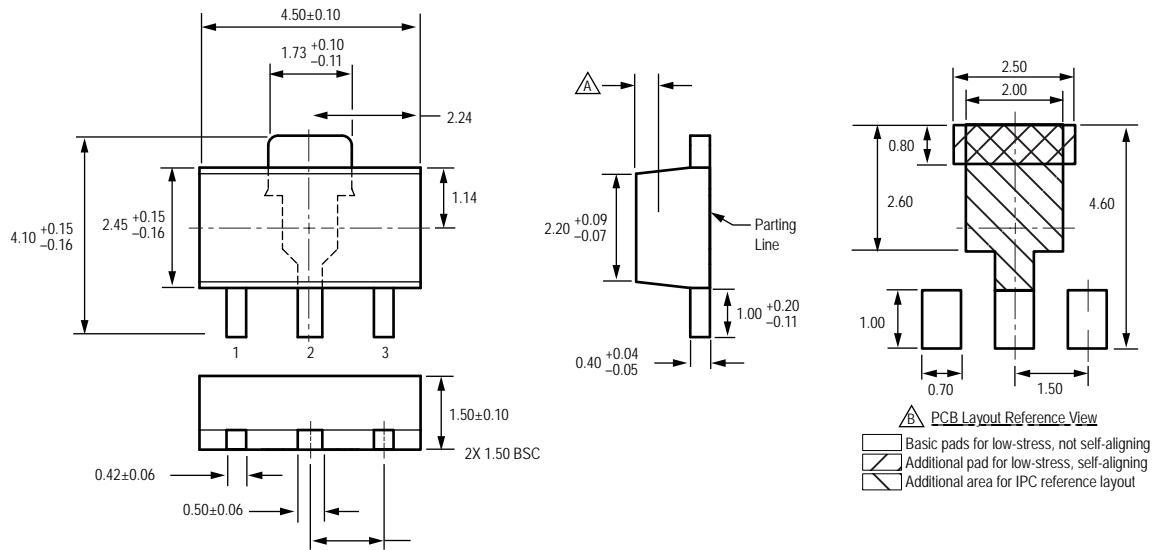


For Reference Only; not for tooling use (reference dwg. 802840)
 Dimensions in millimeters
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
 Exact case and lead configuration at supplier discretion within limits shown

- Δ Active Area Depth, 0.28 mm REF
- Δ Reference land pattern layout
 All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
- Δ Branding scale and appearance at supplier discretion
- Δ Hall element, not to scale

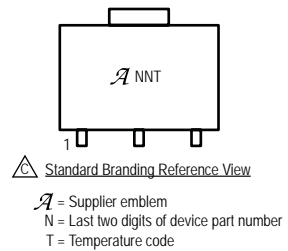
Δ PCB Layout Reference View
 Δ Standard Branding Reference View
 N = Last two digits of device part number
 T = Temperature code

Package LT, 3-Pin (SOT89/TO-243AA)



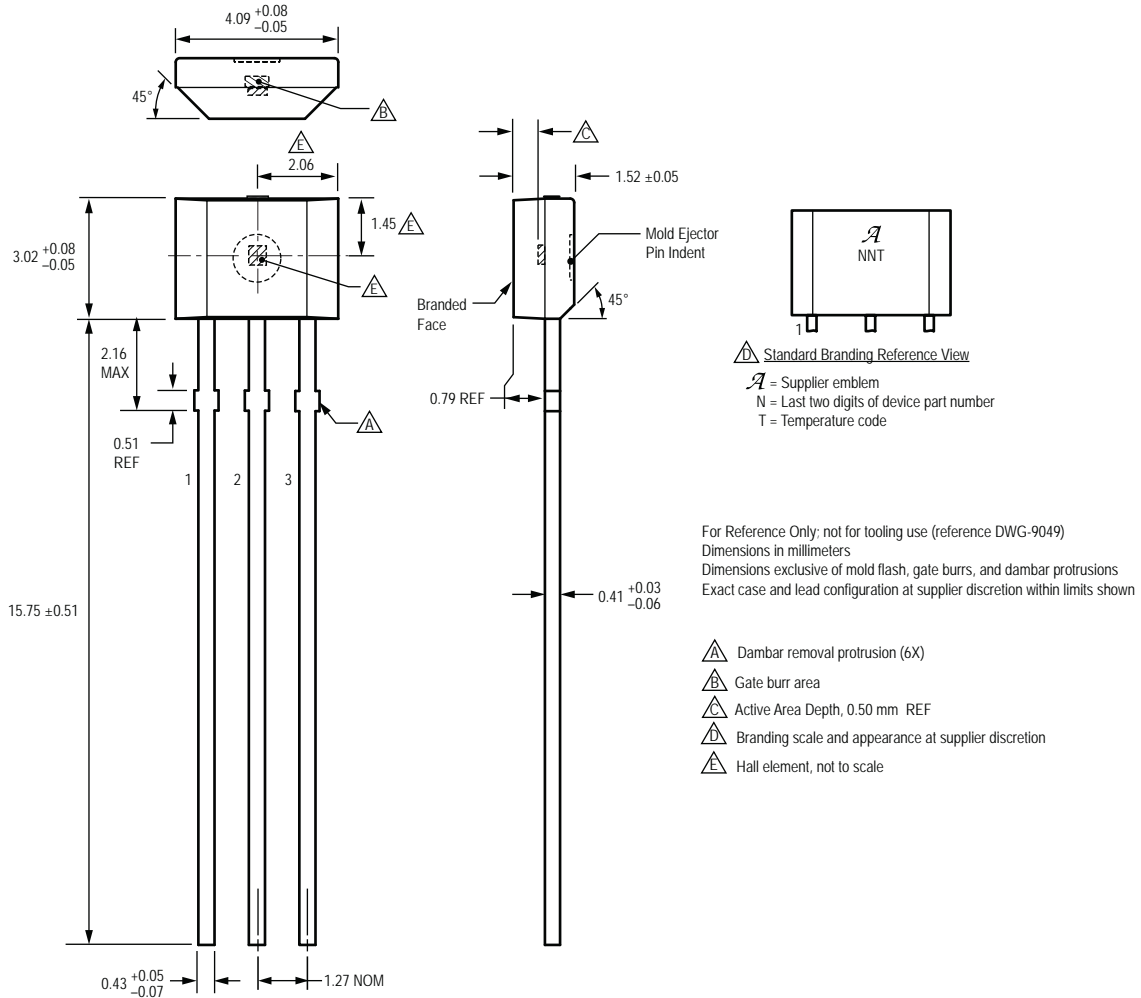
For Reference Only; not for tooling use (reference JEDEC, TO-243AA)
 Dimensions in millimeters
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
 Exact case and lead configuration at supplier discretion within limits shown

- Active Area Depth, 0.78 mm REF
- Reference land pattern layout (reference IPC7351 SOT89N);
All pads a minimum of 0.20 mm from all adjacent pads;
adjust as necessary to meet application process requirements and PCB layout tolerances
- Branding scale and appearance at supplier discretion
- Hall element, not to scale



- PCB Layout Reference View
 - Basic pads for low-stress, not self-aligning
 - Additional pad for low-stress, self-aligning
 - Additional area for IPC reference layout
- Standard Branding Reference View
 - \mathcal{A} = Supplier emblem
 - N = Last two digits of device part number
 - T = Temperature code

Package UA, 3-Pin SIP



Copyright ©2000-2010, Allegro MicroSystems, Inc.

Allegro MicroSystems, Inc. reserves the right to make, from time to time, such departures from the detail specifications as may be required to permit improvements in the performance, reliability, or manufacturability of its products. Before placing an order, the user is cautioned to verify that the information being relied upon is current.

Allegro's products are not to be used in life support devices or systems, if a failure of an Allegro product can reasonably be expected to cause the failure of that life support device or system, or to affect the safety or effectiveness of that device or system.

The information included herein is believed to be accurate and reliable. However, Allegro MicroSystems, Inc. assumes no responsibility for its use; nor for any infringement of patents or other rights of third parties which may result from its use.

For the latest version of this document, visit our website:

www.allegromicro.com

