A34M418, A34M416, A34M414

32-bit Cortex-M4F based High-performance Microcontroller

Datasheet Version 1.01

Features

Core

- High performance Cortex-M4F core

Memories

- 512/256/128KB code flash memory
- 32KB data flash memory
- 64/32KB SRAM

Clock, reset and power management

- Two main operating clocks: HCLK, PCLK
- Two system reset: cold reset, warm reset
- Power management mode: Run mode, Sleep mode, Deep sleep mode

Interrupt management

- Nested vector interrupt controller (NVIC) with 86 interrupt sources

Timers

- Watchdog Timer
- Freerun Timer
- ten general purpose timers
  - Periodic, one-shot, PWM, capture mode

Communication interfaces

- External communication ports
  - 6 UARTs, 2 I2Cs, 3 SPIs

Motor pulse-width modulation

- Two MPWM generators

Quadrature encoder interface

- Two QEI channels

1Msps ADC

- 24-channels inputs

Programmable gain amp

- Three individually operable PGA channels

Comparator

- Four comparators

Advanced encryption standard

- One AES channel

Random-number generator

- 7/8/16/32-bit CRC generator
- CRC-7, CRC-8, CRC-16, CRC-32

Development support

- SWD debug interface

Four types of package options

- LQFP120-1616 (0.5mm pitch)
- LQFP100-1414 (0.5mm pitch)
- LQFP64-1010 (0.5mm pitch)

Operating temperature

- Commercial grade (-40℃ to +85℃)

Product selection table

Table 1. Device Summary

Device name	Flash	SRAM	SPI	UART	I2C	MPWM	ADC	I/O ports	Package
A34M418YL	512KB	64KB	3	6	2	2	24	107	120LQFP-1616
A34M418VL	512KB	64KB	2	6	2	2	24	89	100LQFP-1414
A34M418RL	512KB	64KB	1	3	1	2	16	51	64LQFP-1010
A34M416VL	256KB	64KB	2	6	2	2	24	89	100LQFP-1414
A34M416RL	256KB	64KB	1	3	1	2	16	51	64LQFP-1010
A34M414VL	128KB	32KB	2	6	2	2	24	89	100LQFP-1414
A34M414RL	128KB	32KB	1	3	1	2	16	51	64LQFP-1010

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1 Description

A34M41x series is a 32-bit high-performance microcontroller with up to 512 Kbytes of flash memory. It is a powerful microcontroller which provides effective solutions to various electrical appliances which require both low power consumption and high performance.

1.1 Device overview

In this section, features of A34M41x series and peripheral counts are introduced.

Table 2. A34M41x Series Features and Peripheral Counts

Peripherals		Description
Core	CPU	• Maximum operating frequency: 120MHz • 32-bit ARM Cortex-M4F CPU • CPU register set: — Uses general-purpose registers specified by the 32-bit Thumb®-2 instruction set — Main stack pointer (MSP) and process stack pointer (PSP): R13 — Link register (LR): R14 — Program counter (PC): R15 • Data ordering format: Little-Endian • Harvard Architecture • AHB/APB
	Interrupt	• NVIC (Nested-Vectored Interrupt Controller) • Up to 86 peripheral interrupts supported. • Assignable with 16 different priority levels
	FPU	• Rendered by extending and transforming the ARMv7 floating-point arithmetic functionality • Compliant with the ANSI/IEEE 754 standard • Capable of binary floating-point arithmetic and computation

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
Memory	Code flash	• Capacity : — A34M418: 512Kbytes code flash memory — A34M416: 256Kbytes code flash memory — A34M414: 128Kbytes code flash memory • A high-capacity code flash memory built in • Max 28MHz flash access speed • 512-B, 1-KB, and 4-KB erases • Bulk erase • Read protection • Self-programming • CRC code generation and verification for the flash memory • Endurance: 10,000 cycles • Lifetime: 10 years
	Data flash	• Capacity: 32 KB • Max 28MHz access speed • 512-B, 1-KB, and 4-KB erases • CRC code generation and verification for the flash memory • Endurance: 100,000 Cycle • Lifetime: 10 years
	Boot ROM	• Executes the processor's boot mode when receiving an input at the boot pin from an external circuit • SPI and UART boot modes • In-system programming — A user can program data into the internal flash memory by setting an application board.
	SRAM	• Capacity: 64 KB/32 KB • Usable as a program's work area • High-speed execution enables the execution of time-critical codes • Part of the SRAM can be remapped into an interrupt vector area
	Endurance	• 10,000 times at room temperature • Retention for 10 years
System Control Unit (SCU)	Operating frequency	• Up to 120MHz
	Clock	• High speed internal oscillator (HSI)

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
		— 32MHz (±10% @-40℃ to +85℃) • Low speed internal oscillator (LSI) — 500KHz (±20% @-40℃ to +85℃) • External main oscillator (HSE): 4MHz to 16MHz • External sub-oscillator (LSE): 32.768KHz • Phase-locked loop (PLL) frequency generator generates a high-speed clock (up to 120MHz)
System Control Unit (SCU)	Clock monitoring	• System Fail-Safe function by Clock Monitoring — External main oscillator(HSE) — External sub oscillator(LSE) — Main system clock (MCLK)
	Operating mode	• RUN mode • SLEEP mode • STOP mode
	Reset	• nRESET pin reset • Core reset • Software reset • POR (Power On Reset) • LVR (Low Voltage Reset) • WDTR (Watch Dog Timer Reset) • Reset due to clock oscillating error
	LDO	• Low-dropout (LDO) regulator built in for low-voltage operation
	POR	• The POR generator detects an internal 1.5V voltage and generates a reset signal
	LVI	• 16 low-voltage detection levels • Supports interrupts • Supports wake-up from sleep mode
	Wake-up	• Wake-up by a general-purpose input/output (GPIO) pin • Wake-up by a free-run timer (FRT) • Wake-up by a watchdog timer (WDT) • Wake-up by a low-voltage indicator (LVI)
General Purpose I/O (GPIO)		• Input/output (I/O) port for general purposes • LQFP-120 — I/O pins: 107 • LQFP-100 — I/O pins: 89

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
		• LQFP-64 — I/O pins: 51 • Each pin can be set for one of the following modes: — Push-pull output — Open drain output — Input • The use of each pin can be set by setting the mux • Each pin can be configured as an external interrupt source, either the high-/low-level interrupt or the rising-/falling-edge interrupt • Pull-up/pull-down/debouncing can be set for each pin • Drive strength can be adjusted for each port pin • Each pin bit can be individually set/reset • Wake-up events triggered by external asynchronous inputs
Direct Memory Access Controller (DMA)		• 16-ch direct memory access (DMA) support peripherals • 8-/16-/32-bit data transfers • Compatible with 24 different types of peripherals — SPI0, SPI1, SPI2, UART0, UART1, UART2, UART3, CRC, ADC0, ADC1, ADC2, AES128
TIMER	16-bit Timer	• General-purpose 16-bit up-count timer • 10 channels — 10 timer n capture port (TnC) input channels — 10 timer n output port (TnO) output channels • Timer operating modes — Periodic timer mode — One-shot mode — PWM mode — Capture mode • Interrupt events — Timer/counter match interrupt — Timer overflow interrupt • Input clock selection — Clocks are freely selectable through the miscellaneous clock control registers (MCCRs) — External clocks are selectable • Timer signals can be generated through TnO pins

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
		• 10-bit prescaler
	WDT	• 32-bit down-count timer • Reset and periodic interrupts • Clocks are freely selectable through the miscellaneous clock control registers (MCCRs) • Eight different prescalers are selectable
	FRT	• 32-bit free-run timer — Capable of calculating the internal system time — 32-bit up-count timer • Interrupt events — Period interrupt — Overflow interrupt
Serial interface	UART	• A total of six 16450 asynchronous serial communication ports • Configurable standard asynchronous communication bits (start, stop, and parity) • Flexible communication available through programming — 5- to 8-bit data transfers — Even-/odd-/non-parity generation and checking — 1-, 1.5-, or 2-stop bit generation and checking • 8-bit fraction controller and 16-bit baud rate generator
	SPI	• Three synchronous serial communication port channels • Master/slave operation • Loop-back mode • Programmable and flexible communication — 8-/9-/16-/17-bit data transmit/receive — SPI clock speed — Both least significant bit (LSB)-first and most significant bit (MSB)-first modes available • The SPI0 channel is used when boot mode is entered
	I2C	• Standard I2C communication protocol • Two channels supported • Master and slave modes supported for each channel • 7-bit addressing supported for slave mode • SCL signal's high/low periods and SDA signal's hold time settable
Motor	MPWM	• Two MPWM generators

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
Pulse-Width Modulation		• Six channels (high and low signals of phases U, V, and W) generate different waveforms • 16-bit up-/down-counters • Six ADC trigger sources • Interrupt events — Bottom interrupts — Top (period) interrupts • Interval interrupt mode • Falling/rising dead time applicable • A special operating mode: — Phases U, V, and W are independently controlled — Different carrier counters running for phases U, V, and W — Different duties and periods configurable for phases U, V, and W — Different interrupts used for phases U, V, and W — Capture functionality • Protection and over-voltage detection supported
Quadrature Encoder Interface	QEI	• Two QEI channels • Three input pins for two phase signals and an index pulse • Programmable noise input filters • Displays counter pulses and counter direction • 32-bit up-/down-counters • Velocity capture using a timer
12-bit A/D Converter	ADC	• Three independent ADC blocks • 24 analog input channels • A number of operating modes: — Single conversion — Sequence conversion — Burst conversion — Multiple conversion • Up to eight sequential conversions supported • Software triggers supported • Three internal trigger sources (MPWM and timers) supported • Sample time and hold time are adjustable
Programmable Gain AMP	PGA	• Three individually operable PGA channels • Usable in conjunction with ADC

Table 2. A34M41x Series Features and Peripheral Counts (continued)

Peripherals		Description
Comparator	COMP	• Equipped with comparators 0 and 1, each of which has three input sources • Equipped with comparators 2 and 3, each of which has one input source • Signals from the PGA can be fed to the comparator
Advanced Encryption Standard	AES-128	• One AES channel • Compatible with direct memory access (DMA) • Input/output FIFO configurable • Input/output inversion supported
Random Number Generator	RNG	• Random-number generator • Interrupt events — Generator ready interrupt — Error interrupt
Cyclic Redundancy Check	CRC	• CRC operating modes: — CRC32 (0x04C1_1DB7) — CRC16 (0x8005) — CRC8 (0x07) — CRC7 (0x09) • Input/output data reversion supported • Compatible with DMA
Operating voltage		• 2.7V to 5.5V
Operating temperature		• Commercial grade (-40℃ to +85℃)
Package		• Three types of package options — 120-pin LQFP — 100-pin LQFP — 64-pin LQFP

1.2 Block diagram

In this section, the A34M41x series with peripherals is described in block diagram.

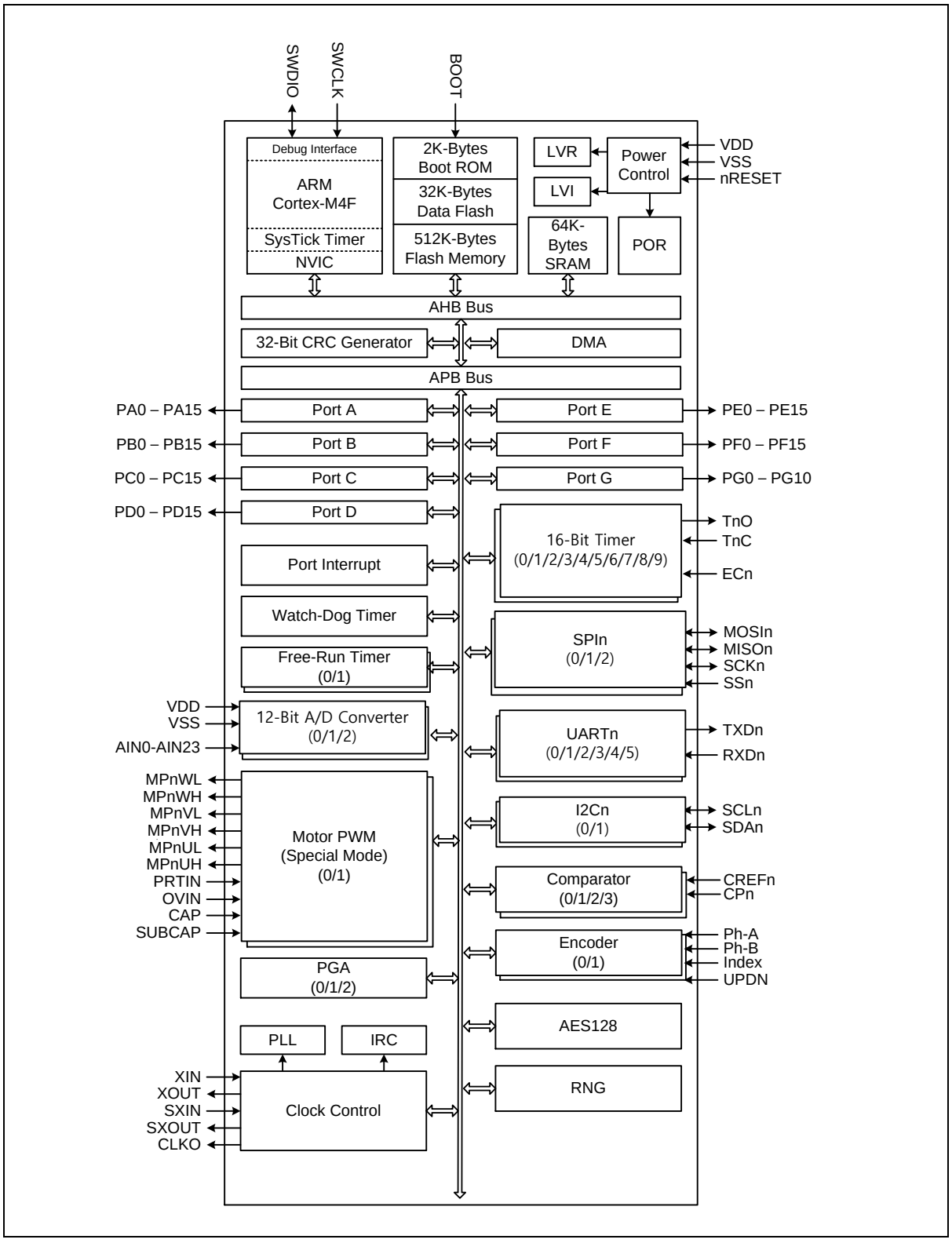


Figure 1. A34M41x Block Diagram

2 Pinouts and pin descriptions

In this chapter, pinouts and pin descriptions of the A34M41x series are introduced.

2.1 Pinouts

2.1.1 A34M418YL (120 LQFP)

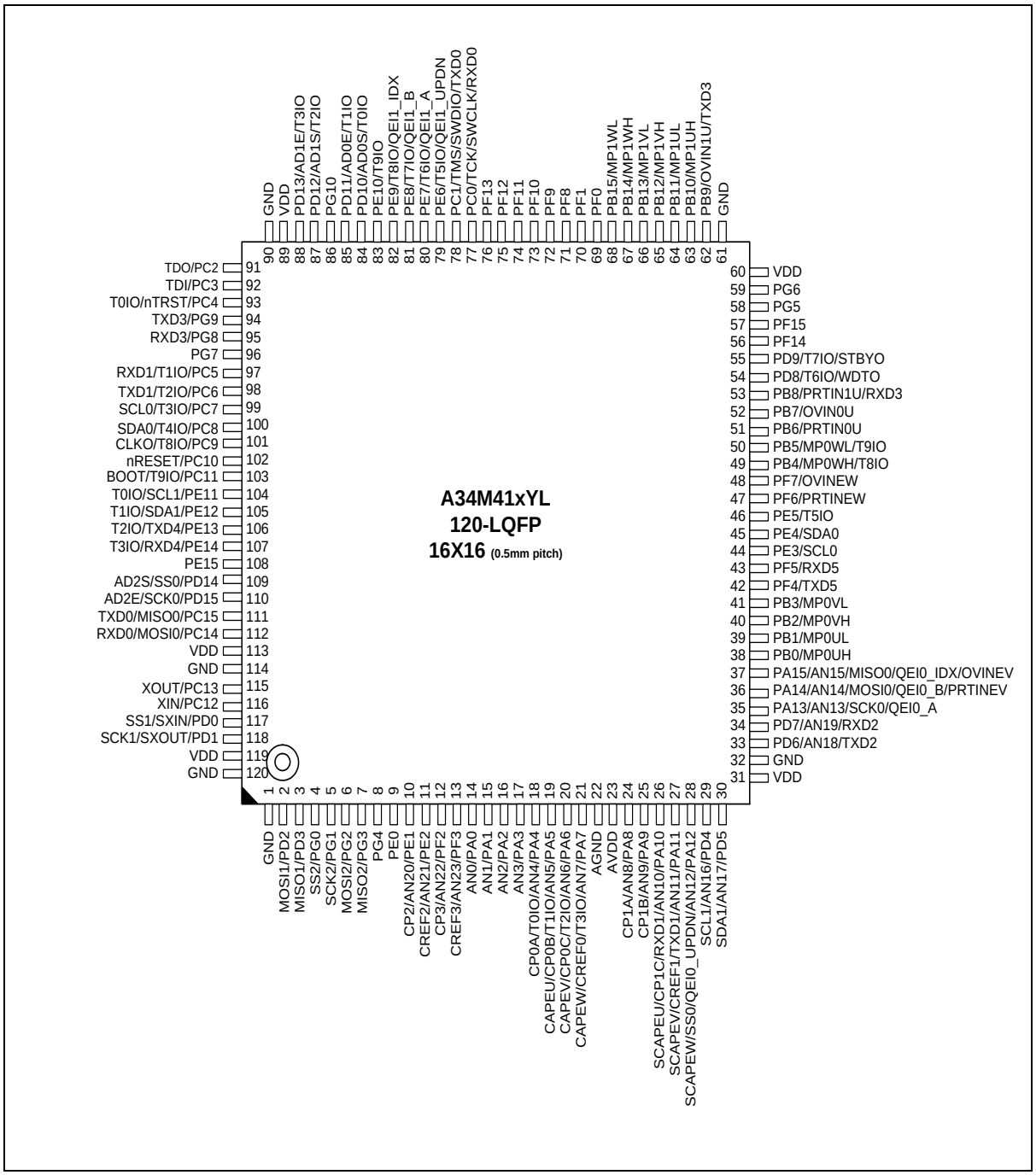


Figure 2. LQFP 120 Pinouts

2.1.2 A34M418VL/A34M416VL/A34M414VL (100 LQFP)

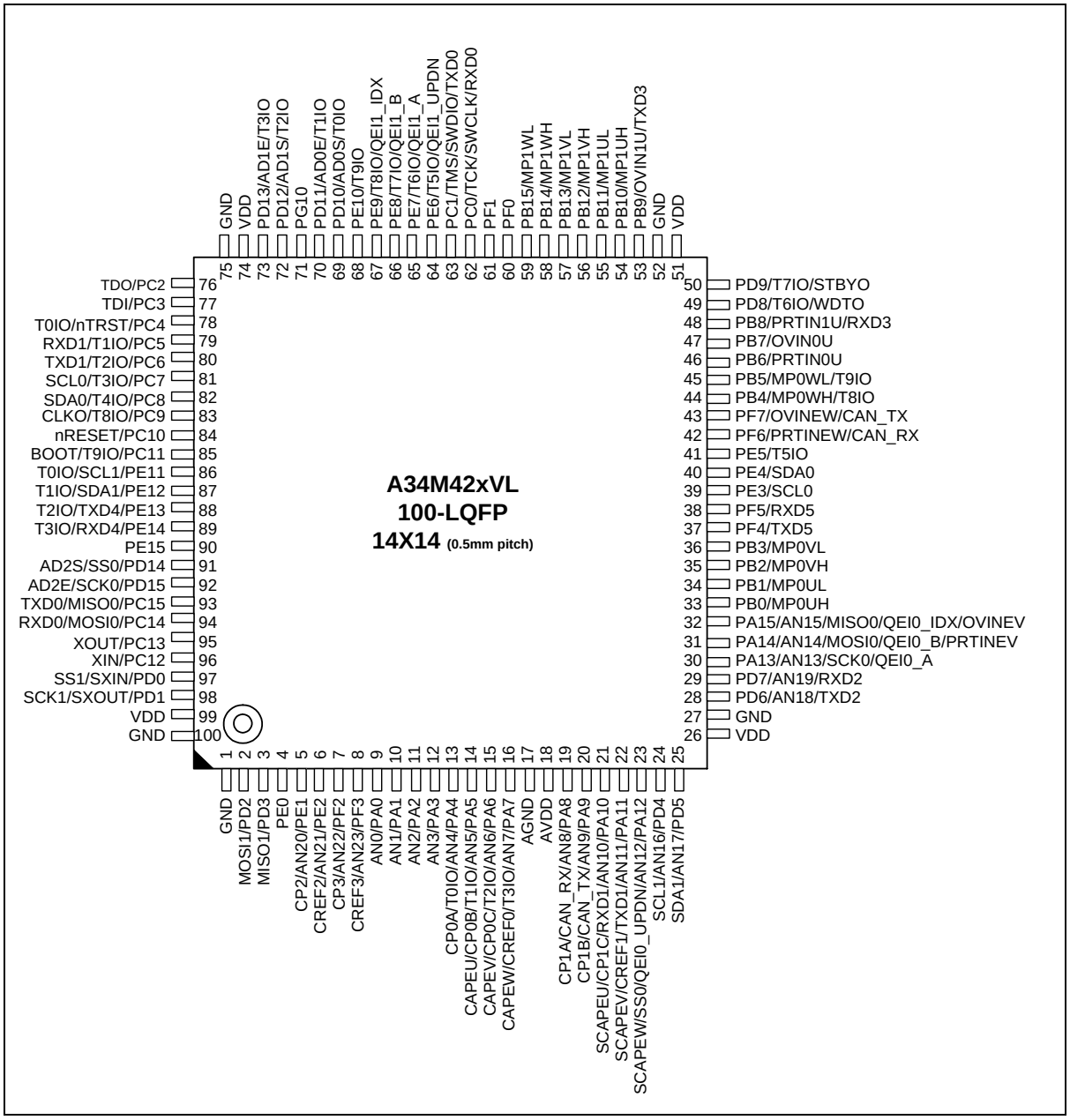


Figure 3. LQFP 100 Pinouts

2.1.3 A34M418RL/A34M416RL/A34M414RL (64 LQFP)

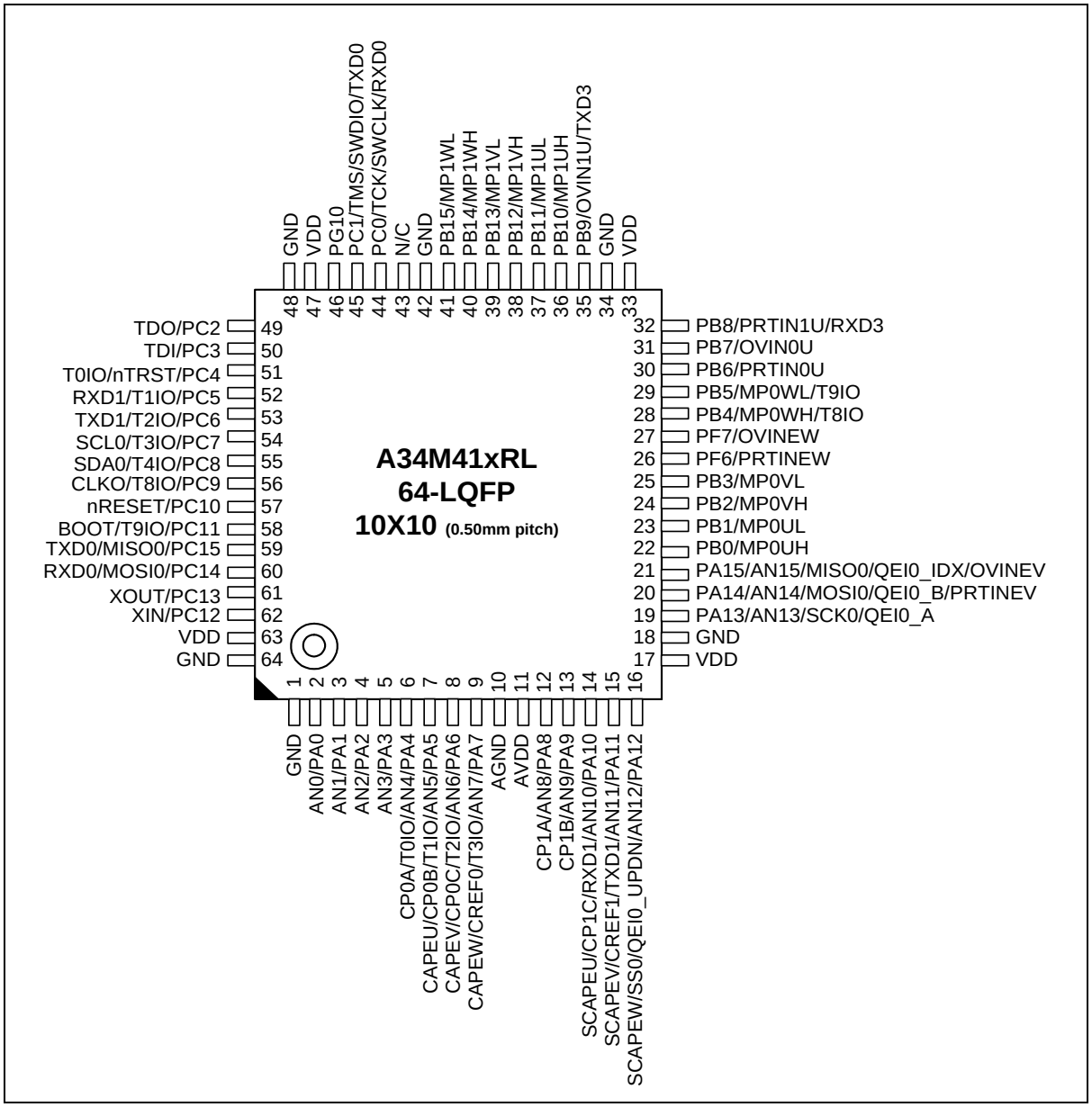


Figure 4. LQFP 64 Pinouts

2.2 Pin description

Pin configuration information in Table 3 contains two pairs of power/ground and other dedicated pins. These multi-function pins have up to five selections of functions including GPIO. Configuration including pin ordering can be changed without notice.

Table 3. Pin Description

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
1	1	1	GND	P	Ground	
2	2	-	PD2*	IOUS	PORT D Bit 2 Input/Output	
			MOSI1	IO	SPI Channel 1 Master Out/Slave In Signal	
3	3	-	PD3*	IOUS	PORT D Bit 3 Input/Output	
			MISO1	IO	SPI Channel 1 Master In/Slave Out Signal	
4	-	-	PG0*	IOUS	PORT G Bit 0 Input/Output	
			SS2	IO	SPI Channel 2 Select Signal Input/Output	
5	-	-	PG1*	IOUS	PORT G Bit 1 Input/Output	
			SCK2	IO	SPI Channel 2 Clock Signal Input/Output	
6	-	-	PG2*	IOUS	PORT G Bit 2 Input/Output	
			MOSI2	IO	SPI Channel 2 Master Out/Slave In Signal	
7	-	-	PG3*	IOUS	PORT G Bit 3 Input/Output	
			MISO2	IO	SPI Channel 2 Master In/Slave Out Signal	
8	-	-	PG4*	IOUS	PORT G Bit 4 Input/Output	
9	4	-	PE0*	IOUS	PORT E Bit 0 Input/Output	
10	5	-	PE1*	IOUS	PORT E Bit 1 Input/Output	
			AN20	IA	Analog Input 20	
			CP2	IA	Comparator Input 2	
11	6	-	PE2*	IOUS	PORT E Bit 2 Input/Output	
			AN21	IA	Analog Input 21	
			CREF2	IA	Comparator Reference Input 2	
12	7	-	PF2*	IOUS	PORT F Bit 2 Input/Output	
			AN22	IA	Analog Input 22	
			CP3	IA	Comparator Input 3	
13	8	-	PF3*	IOUS	PORT F Bit 3 Input/Output	
			AN23	IA	Analog Input 23	
			CREF3	IA	Comparator Reference Input 3	
14	9	2	PA0*	IOUS	PORT A Bit 0 Input/Output	
			AN0	IA	Analog Input 0	
15	10	3	PA1*	IOUS	PORT A Bit 1 Input/Output	
			AN1	IA	Analog Input 1	
16	11	4	PA2*	IOUS	PORT A Bit 2 Input/Output	
			AN2	IA	Analog Input 2	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
17	12	5	PA3*	IOUS	PORT A Bit 3 Input/Output	
			AN3	IA	Analog Input 3	
18	13	6	PA4*	IOUS	PORT A Bit 4 Input/Output	
			AN4	IA	Analog Input 4	
			T0IO	IO	Timer 0 Input/Output	
			CP0A	IA	Comparator Input 0A	
19	14	7	PA5*	IOUS	PORT A Bit 5 Input/Output	
			AN5	IA	Analog Input 5	
			T1IO	IO	Timer 1 Input/Output	
			CP0B	IA	Comparator Input 0B	
			CAPEU	Input	Individual PWM Capture U phase	
20	15	8	PA6*	IOUS	PORT A Bit 6 Input/Output	
			AN6	IA	Analog Input 6	
			T2IO	IO	Timer 2 Input/Output	
			CP0C	IA	Comparator Input 0C	
			CAPEV	Input	Individual PWM Capture V phase	
21	16	9	PA7*	IOUS	PORT A Bit 7 Input/Output	
			AN7	IA	Analog Input 7	
			T3IO	IO	Timer 3 Input/Output	
			CREF0	IA	Comparator Reference Input 0	
			CAPEW	Input	Individual PWM Capture W phase	
22	17	10	AGND	P	Analog Ground	
23	18	11	AVDD	P	Analog VDD	
24	19	12	PA8*	IOUS	PORT A Bit 8 Input/Output	
			AN8	IA	Analog Input 8	
			CP1A	IA	Comparator Input 1A	
25	20	13	PA9*	IOUS	PORT A Bit 9 Input/Output	
			AN9	IA	Analog Input 9	
			CP1B	IA	Comparator Input 1B	
26	21	14	PA10*	IOUS	PORT A Bit 10 Input/Output	
			AN10	IA	Analog Input 10	
			RXD1	Input	UART Channel 1 RXD Input	
			CP1C	IA	Comparator Input 1C	
			SCAPEU	Input	Individual PWM Sub Capture U phase	
27	22	15	PA11*	IOUS	PORT A Bit 11 Input/Output	
			AN11	IA	Analog Input 11	
			TXD1	Output	UART Channel 1 TXD Output	
			CREF1	IA	Comparator Reference Input 1	
			SCAPEV	Input	Individual PWM Sub Capture V phase	
28	23	16	PA12*	IOUS	PORT A Bit 12 Input/Output	
			AN12	IA	Analog Input 12	
			SS0	IO	SPI Channel 0 Select Signal Input/Output	
			QEI0_UDPN	Output	QEI0 Output of Phase Direction	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
			SCAPEW	Input	Individual PWM Sub Capture W phase	
29	24	-	PD4*	IOUS	PORT D Bit 4 Input/Output	
			AN16	IA	Analog Input 16	
			SCL1	IO	I2C Channel 1 Output	Open-drain
30	25	-	PD5*	IOUS	PORT D Bit 5 Input/Output	
			AN17	IA	Analog Input 17	
			SDA1	IO	I2C Channel 1 SDA Input/Output	Open-drain
31	26	17	VDD	P	VDD	
32	27	18	GND	P	Ground	
33	28	-	PD6*	IOUS	PORT D Bit 6 Input/Output	
			AN18	IA	Analog Input 18	
			TXD2	Output	UART Channel 2 TXD Output	
34	29	-	PD7*	IOUS	PORT D Bit 7 Input/Output	
			AN19	IA	Analog Input 19	
			RXD2	Input	UART Channel 2 RXD Input	
35	30	19	PA13*	IOUS	PORT A Bit 13 Input/Output	
			AN13	IA	Analog Input 13	
			SCK0	IO	SPI Channel 0 Clock Input/Output	
			QEI0_A	Input	Input of QEI0 PhaseA	
36	31	20	PA14*	IOUS	PORT A Bit 14 Input/Output	
			AN14	IA	Analog Input 14	
			MOSI0	IO	SPI Channel 0 Master Out/Slave In Signal	
			QEI0_B	Input	Input of QEI0 PhaseB	
			PRTINEV	Input	Individual PWM Phase V Protection Input	
37	32	21	PA15*	IOUS	PORT A Bit 15 Input/Output	
			AN15	IA	Analog Input 15	
			MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
			QEI0_IDX	Input	Input of QEI0 Index	
			OVINEV	Input	Individual PWM Phase V Over-voltage Input	
38	33	22	PB0*	IOUS	PORT B Bit 0 Input/Output	
			MP0UH	Output	PWM0 UH Output	
39	34	23	PB1*	IOUS	PORT B Bit 1 Input/Output	
			MP0UL	Output	PWM Channel 0 UL Output	
40	35	24	PB2*	IOUS	PORT B Bit 2 Input/Output	
			MP0VH	Output	PWM Channel 0 VH Output	
41	36	25	PB3*	IOUS	PORT B Bit 3 Input/Output	
			MP0VL	Output	PWM Channel 0 VL Output	
42	37	-	PF4*	IOUS	PORT F Bit 4 Input/Output	
			TXD5	Output	UART Channel 5 TXD Output	
43	38	-	PF5*	IOUS	PORT F Bit 5 Input/Output	
			RXD5	Input	UART Channel 5 RXD Input	
44	39	-	PE3*	IOUS	PORT E Bit 3 Input/Output	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
			SCL0	IO	I2C Channel 0 Output	Open-drain
45	40	-	PE4*	IOUS	PORT E Bit 4 Input/Output	
			SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain
46	41	-	PE5*	IOUS	PORT E Bit 5 Input/Output	
			T5IO	IO	Timer 5 Input/Output	
47	42	26	PF6	IOUS	PORT F Bit 6 Input/Output	
			PRTINEW	Input	Individual PWM Phase W Protection Input	
48	43	27	PF7	IOUS	PORT F Bit 7 Input/Output	
			OVINEW	Input	Individual PWM Phase W Over-voltage Input	
49	44	28	PB4*	IOUS	PORT B Bit 4 Input/Output	
			MP0WH	Output	PWM Channel 0 WH Output	
			T8IO	IO	Timer 8 Input/Output	
50	45	29	PB5*	IOUS	PORT B Bit 5 Input/Output	
			MP0WL	Output	PWM Channel 0 WL Output	
			T9IO	IO	Timer 9 Input/Output	
51	46	30	PB6*	IOUS	PORT B Bit 6 Input/Output	
			PRTIN0U	Input	PWM0 Protection Input Signal Individual PWM 0 Phase U Protection Input	
52	47	31	PB7*	IOUS	PORT B Bit 7 Input/Output	
			OVIN0U	Input	PWM0 Over-voltage Input Signal Individual PWM 0 Phase U Over voltage Input	
53	48	32	PB8*	IOUS	PORT B Bit 8 Input/Output	
			PRTIN1U	Input	PWM1 Protection Input Signal Individual PWM 1 Phase U Protection Input	
			RXD3	Input	UART Channel 3 RXD Input	
54	49	-	PD8*	IOUS	PORT D Bit 8 Input/Output	
			T6IO	IO	Timer 6 Input/Output	
			WDTO	Output	WDT Output	
55	50	-	PD9*	IOUS	PORT D Bit 9 Input/Output	
			T7IO	IO	Timer 7 Input/Output	
			STBYO	Output	Power-down Mode Indication Signal	
56	-	-	PF14	IOUS	PORT F Bit 14 Input/Output	
57	-	-	PF15	IOUS	PORT F Bit 15 Input/Output	
58	-	-	PG5	IOUS	PORT G Bit 5 Input/Output	
59	-	-	PG6	IOUS	PORT G Bit 6 Input/Output	
60	51	33	VDD	P	VDD	
61	52	34	GND	P	Ground	
62	53	35	PB9*	IOUS	PORT B Bit 9 Input/Output	
			OVIN1U	Input	PWM1 Overvoltage Input Signal Individual PWM 1 Phase U Over voltage Input	
			TXD3	Output	UART Channel 3 TXD Output	
63	54	36	PB10*	IOUS	PORT B Bit 10 Input/Output	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
			MP1UH	Output	PWM Channel 1 UH Output	
64	55	37	PB11*	IOUS	PORT B Bit 11 Input/Output	
			MP1UL	Output	PWM Channel 1 UL Output	
65	56	38	PB12*	IOUS	PORT B Bit 12 Input/Output	
			MP1VH	Output	PWM Channel 1 VH Output	
66	57	39	PB13*	IOUS	PORT B Bit 13 Input/Output	
			MP1VL	Output	PWM Channel 1 VL Output	
67	58	40	PB14*	IOUS	PORT B Bit 14 Input/Output	
			MP1WH	Output	PWM Channel 1 WH Output	
68	59	41	PB15*	IOUS	PORT B Bit 15 Input/Output	
			MP1WL	Output	PWM Channel 1 WL Output	
69	60	-	PF0	IOUS	PORT F Bit 0 Input/Output	
70	61	-	PF1	IOUS	PORT F Bit 1 Input/Output	
71	-	-	PF8	IOUS	PORT F Bit 8 Input/Output	
72	-	-	PF9	IOUS	PORT F Bit 9 Input/Output	
73	-	-	PF10	IOUS	PORT F Bit 10 Input/Output	
74	-	-	PF11	IOUS	PORT F Bit 11 Input/Output	
75	-	-	PF12	IOUS	PORT F Bit 12 Input/Output	
76	-	-	PF13	IOUS	PORT F Bit 13 Input/Output	
-	-	42	GND	P	Ground	
		43	N/C	-	N/C	
77	62	44	PC0	IOUS	PORT C Bit 0 Input/Output	
			TCK/SWCLK*	Input	JTAG TCK, SWD Clock Input	Pull-up
			RXD0	Input	UART Channel 0 RXD Input	
78	63	45	PC1	IOUS	PORT C Bit 1 Input/Output	
			TMS/SWDIO*	IO	JTAG TMS, SWD Data Input/Output	Pull-up
			TXD0	Output	UART Channel 0 TXD Output	
79	64	-	PE6*	IOUS	PORT E Bit 6 Input/Output	
			T5IO	IO	Timer 5 Input/Output	
			QEI1_UPDN	Output	QEI1 Output of Phase Direction	
80	65	-	PE7*	IOUS	PORT E Bit 7 Input/Output	
			T6IO	IO	Timer 6 Input/Output	
			QEI1_A	Input	Input of QEI1 PhaseA	
81	66	-	PE8*	IOUS	PORT E Bit 8 Input/Output	
			T7IO	IO	Timer 7 Input/Output	
			QEI1_B	Input	Input of QEI1 PhaseB	
82	67	-	PE9*	IOUS	PORT E Bit 9 Input/Output	
			T8IO	IO	Timer 8 Input/Output	
			QEI1_IDX	Input	Input of QEI1 Index	
83	68	-	PE10*	IOUS	PORT E Bit 10 Input/Output	
			T9IO	IO	Timer 9 Input/Output	
84	69	-	PD10*	IOUS	PORT D Bit 10 Input/Output	
			AD0S	Output	ADC0 Start of Conversion	

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
			T0IO	IO	Timer 0 Input/Output	
85	70	-	PD11*	IOUS	PORT D Bit 11 Input/Output	
			AD0E	Output	ADC0 End of Conversion	
			T1IO	IO	Timer 1 Input/Output	
86	71	46	PG10*	IOUS	PORT G Bit 10 Input/Output	
87	72	-	PD12*	IOUS	PORT D Bit 12 Input/Output	
			AD1S	Output	ADC1 Start of Conversion	
			T2IO	IO	Timer 2 Input/Output	
88	73	-	PD13*	IOUS	PORT D Bit 13 Input/Output	
			AD1E	Output	ADC1 End of Conversion	
			T3IO	IO	Timer 3 Input/Output	
89	74	47	VDD	P	VDD	
90	75	48	GND	P	Ground	
91	76	49	PC2	IOUS	PORT C Bit 2 Input/Output	
			TDO*	Output	JTAG TDO Output	
92	77	50	PC3	IOUS	PORT C Bit 3 Input/Output	
			TDI*	Input	JTAG TDI Input	Pull-up
93	78	51	PC4	IOUS	PORT C Bit 4 Input/Output	
			nTRST*	Input	JTAG nTRST Input	Pull-up
			T0IO	IO	Timer 0 Input/Output	
94	-	-	PG9*	IOUS	PORT G Bit 9 Input/Output	
			TXD3	Output	UART Channel 3 TXD Output	
95	-	-	PG8*	IOUS	PORT G Bit 8 Input/Output	
			RXD3	Input	UART Channel 3 RXD Input	
96	-	-	PG7	IOUS	PORT G Bit 7 Input/Output	
97	79	52	PC5*	IOUS	PORT C Bit 5 Input/Output	
			T1IO	IO	Timer 1 Input/Output	
			RXD1	Input	UART Channel 1 RXD Input	
98	80	53	PC6*	IOUS	PORT C Bit 6 Input/Output	
			T2IO	IO	Timer 2 Input/Output	
			TXD1	Output	UART Channel 1 TXD Output	
99	81	54	PC7*	IOUS	PORT C Bit 7 Input/Output	
			T3IO	IO	Timer 3 Input/Output	
			SCL0	IO	I2C Channel 0 Output	Open-drain
100	82	55	PC8*	IOUS	PORT C Bit 8 Input/Output	
			T4IO	IO	Timer 4 Input/Output	
			SDA0	IO	I2C Channel 0 SDA Input/Output	Open-drain
101	83	56	PC9*	IOUS	PORT C Bit 9 Input/Output	
			T8IO	IO	Timer 8 Input/Output	
			CLKO	Output	System Clock Output	
102	84	57	PC10	IOUS	PORT C Bit 10 Input/Output	
			nRESET*	Input	External Reset Input	Pull-up

Table 3. Pin Description (continued)

Pin no.			Pin name	Type	Description	Remark
120-pin	100-pin	64-pin				
103	85	58	PC11	IOUS	PORT C Bit 11 Input/Output	
			T9IO	IO	Timer 9 Input/Output	
			BOOT*	Input	Boot Mode Selection Input	Pull-up
104	86	-	PE11*	IOUS	PORT E Bit 11 Input/Output	
			SCL1	IO	I2C Channel 1 Output	Open-drain
			T0IO	IO	Timer 0 Input/Output	
105	87	-	PE12*	IOUS	PORT E Bit 12 Input/Output	
			SDA1	IO	I2C Channel 1 SDA Input/Output	Open-drain
			T1IO	IO	Timer 1 Input/Output	
106	88	-	PE13*	IOUS	PORT E Bit 13 Input/Output	
			TXD4	Output	UART Channel 4 TXD Output	
			T2IO	IO	Timer 2 Input/Output	
107	89	-	PE14*	IOUS	PORT E Bit 14 Input/Output	
			RXD4	Input	UART Channel 4 RXD Input	
			T3IO	IO	Timer 3 Input/Output	
108	90	-	PE15	IOUS	PORT E Bit 15 Input/Output	
109	91	-	PD14*	IOUS	PORT D Bit 14 Input/Output	
			AD2S	Output	ADC2 Start of Conversion	
			SS0	IO	SPI Channel 0 Select Signal Input/Output	
110	92	-	PD15*	IOUS	PORT D Bit 15 Input/Output	
			AD2E	Output	ADC2 End of Conversion	
			SCK0	IO	SPI Channel 0 Clock Input/Output	
111	93	59	PC15*	IOUS	PORT C Bit 15 Input/Output	
			MISO0	IO	SPI Channel 0 Master In/Slave Out Signal	
			TXD0	Output	UART Channel 0 TXD Output	
112	94	60	PC14*	IOUS	PORT C Bit 14 Input/Output	
			MOSI0	IO	SPI Channel 0 Master Out/Slave In Signal	
			RXD0	Input	UART Channel 0 RXD Input	
113	-	-	VDD	P	VDD	
114	-	-	GND	P	Ground	
115	95	61	PC13*	IOUS	PORT C Bit 13 Input/Output	
			XOUT	OA	External Crystal Oscillator Output	
116	96	62	PC12*	IOUS	PORT C Bit 12 Input/Output	
			XIN	IA	External Crystal Oscillator Input	
117	97	-	PD0*	IOUS	PORT D Bit 0 Input/Output	
			SXIN	IA	Sub Crystal Oscillator Input	
			SS1	IO	SPI Channel 1 Select Signal Input/Output	
118	98	-	PD1*	IOUS	PORT D Bit 1 Input/Output	
			SXOUT	OA	Sub Crystal Oscillator Output	
			SCK1	IO	SPI Channel 1 Clock Input/Output	
119	99	63	VDD	P	VDD	
120	100	64	GND	P	Ground	

NOTES:

1. I=Input, O=Output, U=Pull-up, D=Pull-down, S=Schmitt-Trigger Input Type, C=CMOS Input Type, A=Analog, P=Power
2. * means ‘selected pin function after reset condition’.
3. Pin order may be changed with revision notice.
4. BOOT0, nRESET, PC1 (SWDIO), PC0 (SWCLK), PC3 and PC4 are the default pull-up pins.
5. Do not configure unused pins as floating inputs.
6. After a reset, the internal pull-up for the boot pin is enabled.
7. After a reset, the internal pull-up for the serial wire clock (SWCLK) and the serial wire data I/O (SWDIO) is enabled.
8. The SWCLK and SWDIO pins should not be switched to other functions while they are being used.

3 System and memory overview

3.1 System architecture

Main system of A34M41x series consists of the followings:

- ARM® Cortex® -M4 core
- General purpose DMA
- Internal SRA, Flash memory
- Two AHB buses

3.1.1 Cortex-M4F core

The ARM® Cortex-M4F processor is a low-power processor that features low gate count, low interrupt latency, and low-cost debug. The Cortex-M4F has the same functions as the Cortex-M4 and includes optional floating point arithmetic functionality. The two processors are intended for deeply embedded applications that require fast interrupt response features.

For detailed information on the Cortex-M4F, refer to document ID061113 provided by the ARM.

3.1.2 Interrupt controller

Table 4. Interrupt Vector Map

Priority	Vector address	Interrupt source
-16	0x0000_0000	Stack Pointer
-15	0x0000_0004	Reset Handler
-14	0x0000_0008	NMI Handler
-13	0x0000_000C	Hard Fault Handler
-12	0x0000_0010	MemManage Handler
-11	0x0000_0014	BusFault Handler
-10	0x0000_0018	UsageFault Handler
-9	0x0000_001C	Reserved
-8	0x0000_0020	
-7	0x0000_0024	
-6	0x0000_0028	
-5	0x0000_002C	SVCall Handler
-4	0x0000_0030	Debug Monitor Handler
-3	0x0000_0034	Reserved
-2	0x0000_0038	PenSV Handler
-1	0x0000_003C	SysTick Handler

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
0	0x0000_0040	LVI
1	0x0000_0044	SYSCLKFAIL
2	0x0000_0048	HSEFAIL
3	0x0000_004C	LSEFAIL
4	0x0000_0050	Reserved
5	0x0000_0054	Reserved
6	0x0000_0058	WDT
7	0x0000_005C	Reserved
8	0x0000_0060	FRT0
9	0x0000_0064	FRT1
10	0x0000_0068	Reserved
11	0x0000_006C	CFMC
12	0x0000_0070	DFMC
13	0x0000_0074	Reserved
14	0x0000_0078	
15	0x0000_007C	TIMER0
16	0x0000_0080	TIMER1
17	0x0000_0084	TIMER2
18	0x0000_0088	TIMER3
19	0x0000_008C	TIMER4
20	0x0000_0090	TIMER5
21	0x0000_0094	TIMER6
22	0x0000_0098	TIMER7
23	0x0000_009C	TIMER8
24	0x0000_00A0	TIMER9
25	0x0000_00A4	Reserved
26	0x0000_00A8	
27	0x0000_00AC	RNG
28	0x0000_00B0	AES-128
29	0x0000_00B4	Reserved
30	0x0000_00B8	
31	0x0000_00BC	QEI0
32	0x0000_00C0	QEI1

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
33	0x0000_00C4	Reserved
34	0x0000_00C8	
35	0x0000_00CC	
36	0x0000_00D0	GIPOA
37	0x0000_00D4	GPIOB
38	0x0000_00D8	GPIOC
39	0x0000_00DC	GPIOD
40	0x0000_00E0	GPIOE
41	0x0000_00E4	GPIOF
42	0x0000_00E8	GPIOG
43	0x0000_00EC	Reserved
44	0x0000_00F0	
45	0x0000_00F4	MPWM0PROT
46	0x0000_00F8	MPWM0OVV
47	0x0000_00FC	MPWM0(U)
48	0x0000_0100	MPWM0(V)
49	0x0000_0104	MPWM0(W)
50	0x0000_0108	MPWM1PROT
51	0x0000_010C	MPWM1OVV
52	0x0000_0110	MPWM1(U)
53	0x0000_0114	MPWM1(V)
54	0x0000_0118	MPWM1(W)
55	0x0000_011C	SPI0
56	0x0000_0120	SPI1
57	0x0000_0124	SPI2
58	0x0000_0128	Reserved
59	0x0000_012C	
60	0x0000_0130	I2C0
61	0x0000_0134	I2C1
62	0x0000_0138	Reserved
63	0x0000_013C	UART0
64	0x0000_0140	UART1
65	0x0000_0144	UART2
66	0x0000_0148	UART3
67	0x0000_014C	UART4
68	0x0000_0150	UART5

Table 4. Interrupt Vector Map (continued)

Priority	Vector Address	Interrupt Source
69	0x0000_0154	Reserved
70	0x0000_0158	
71	0x0000_015C	
72	0x0000_0160	
73	0x0000_0164	
74	0x0000_0168	ADC0
75	0x0000_016C	ADC1
76	0x0000_0170	ADC2
77	0x0000_0174	Reserved
78	0x0000_0178	
79	0x0000_017C	COMP0
80	0x0000_0180	COMP1
81	0x0000_0184	COMP2
82	0x0000_0188	COMP3
83	0x0000_018C	Reserved
84	0x0000_0190	
85	0x0000_0194	CRC

NOTES:

1. Each interrupt has an associated priority-level register. Each of them is 2 bits wide, occupying the two MSBs of the Interrupt Priority Level Registers.

   Each Interrupt Priority Level Register occupies 1 byte (8 bits).NVIC registers in the Cortex-M4F processor can only be accessed using word-size transfers, so for each access, four Interrupt Priority Level Registers are accessed at the same time.

   ** __NVIC_PRIO_BITS = 4

2. Figure 5 is a caution when using Peripheral Interrupts. Interrupt don't work if only peripheral interrupts are enabled. Enable the function in core to enable interrupt.

   * __enable_irq > NVCI_EnableIRQ(Peripheral) > Each Peripheral Interrupt

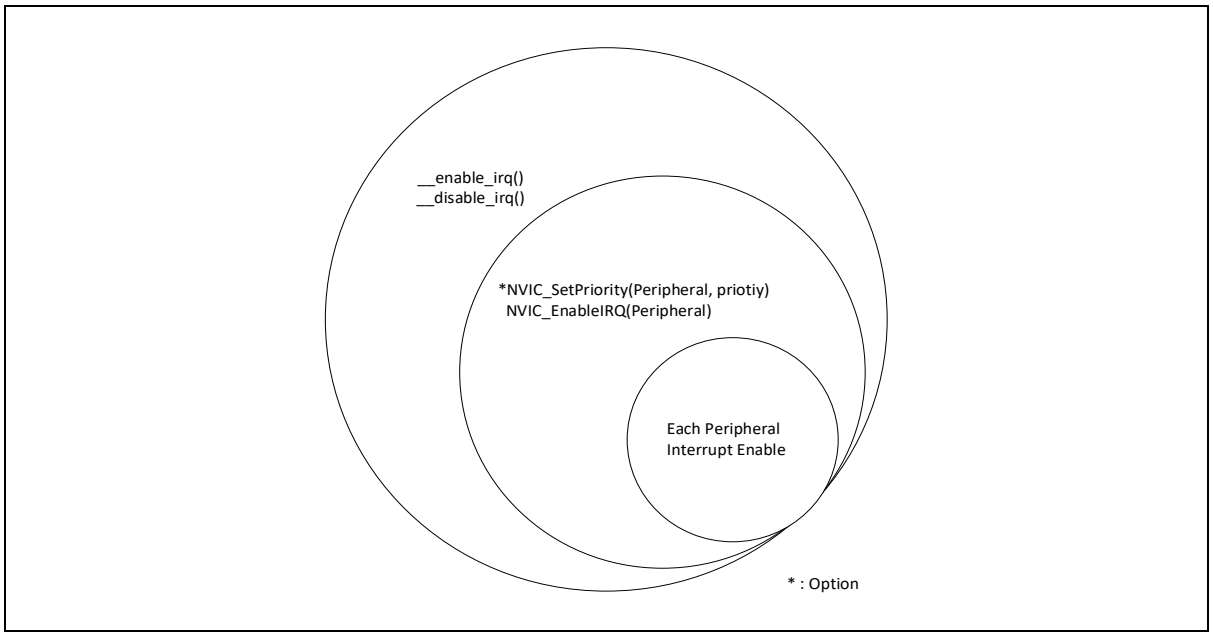


Figure 5. Interrupt Block Diagram

3.2 Floating Point Unit (FPU)

Cortex-M4 FPU is an implementation of the single precision variant of the ARMv7-M Floating-Point Extension (FPv4-SP). It provides floating-point computation functionality that is compliant with the ANSI/IEEE Std 754-2008, IEEE Standard for Binary Floating-Point Arithmetic, referred to as the IEEE 754 standard. The FPU supports all single-precision data-processing instructions and data types described in the ARM®v7-M Architecture Reference Manual.

3.3 Memory organization

Program memory, data memory, registers and I/O ports are organized in the same address space.

3.3.1 Register boundary address

Table 5 gives the boundary address assigned for each peripheral of the A34M41x series.

Table 5. A34M41x Memory Boundary Addresses

Boundary address	Memory area
0x4000_0000	SCU
0x4000_0200	WDT
0x4000_0400	DMA 0/1/2/3/4/5/6/7/8/9/10/11/12/13/14/15
0x4000_0500	AES128
0x4000_0600	FRT
0x4000_0A00	RNG
0x4000_1000	PCU A/B/C/D/E/F/G
0x4000_3000	Timer 0/1/2/3/4/5/6/7/8/9
0x4000_4000	MPWM0
0x4000_5000	MPWM1
0x4000_8000	UART 0/1/2/3/4/5
0x4000_9000	SPI 0/1/2
0x4000_A000	I2C 0/1/2
0x4000_B000	ADC 0/1/2
0x4000_B300	PGA
0x4000_B380	COMPARATOR
0x4000_B400	QEI
0x4100_0000	CFMC
0x4100_1000	DFMC
0x4100_2000	CRC
0x2000_0000	Internal SRAM

3.3.2 Memory map

Figure 6 shows addressable memory space in memory map.

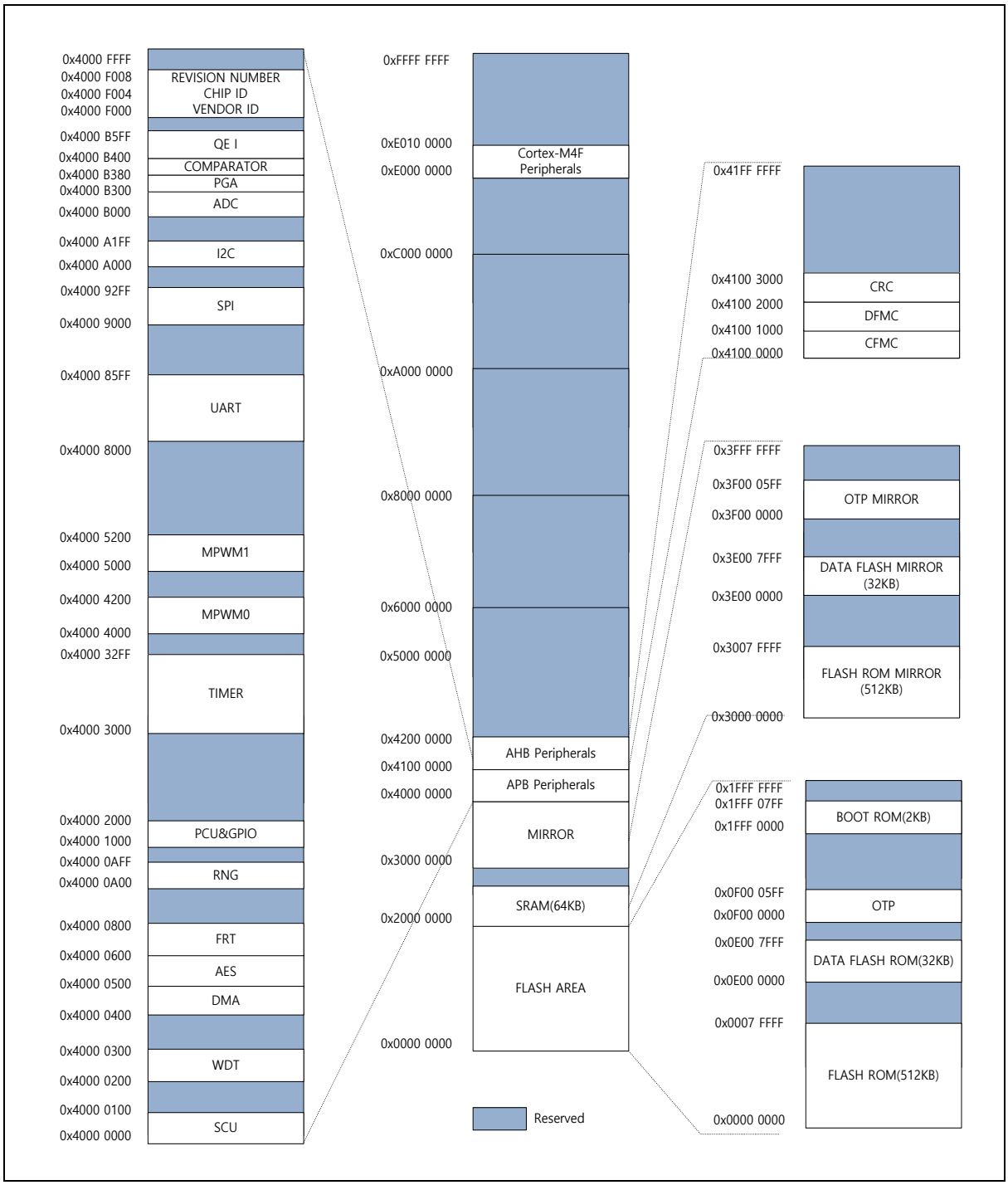


Figure 6. Memory Map

3.3.3 Embedded SRAM

The A34M41x series has a block of 0-wait on-chip SRAM. Size of the SRAM is 64KB and its base address is 0x2000_0000.

This SRAM memory area is usually used for data memory and stack memory. Sometimes the code is dumped into the SRAM memory for fast operation or flash erase/programming operation. This device does not support memory remap strategy. So jump and return are required to perform the code in SRAM memory area.

3.3.4 Flash memory overview

The A34M41x series provides internal 512KB code flash memory and a controller. This is enough to control the general system. Self-programming is available and ISP and SWD programming is also supported in boot mode or in debugging mode.

Instruction and data cache buffer are present and overcome the low bandwidth flash memory. CPU can access flash memory with one wait state up to 28MHz bus frequency.

3.3.5 Boot mode

Boot mode pins

The A34M41x series has a boot mode option to program internal flash memory. Boot mode can be entered by setting BOOT pin to 'L' at reset timing (Normal state is 'H').

Boot mode supports both of UART boot and SPI boot:

- UART boot uses TXD0/RXTD ports.
- SPI boot uses MOSI0/MISO0/SCK0/SS0 ports.

Pins for the boot mode are listed in Table 6.

Table 6. Boot Mode Pin List

Block	Pin name	Dir	Description
SYSTEM	nRESET/PC10	I	Reset input signal
	nBOOT/PC11	I	Boot mode setting pin
UART0	RXD0/PC14	I	UART boot receive data
	TXD0/PC15	O	UART boot transmit data
SPI0	SS0/PA12	I	SPI boot slave select
	SCK0/PA13	I	SPI boot clock input
	MOSI0/PA14	I	SPI boot data output
	MISO0/PA15	O	SPI boot data input

Boot mode connections

Users can design a target board using any of boot mode ports such as SPI or UART mode of UART0. Sample connection diagrams of boot mode are introduced in the following figures:

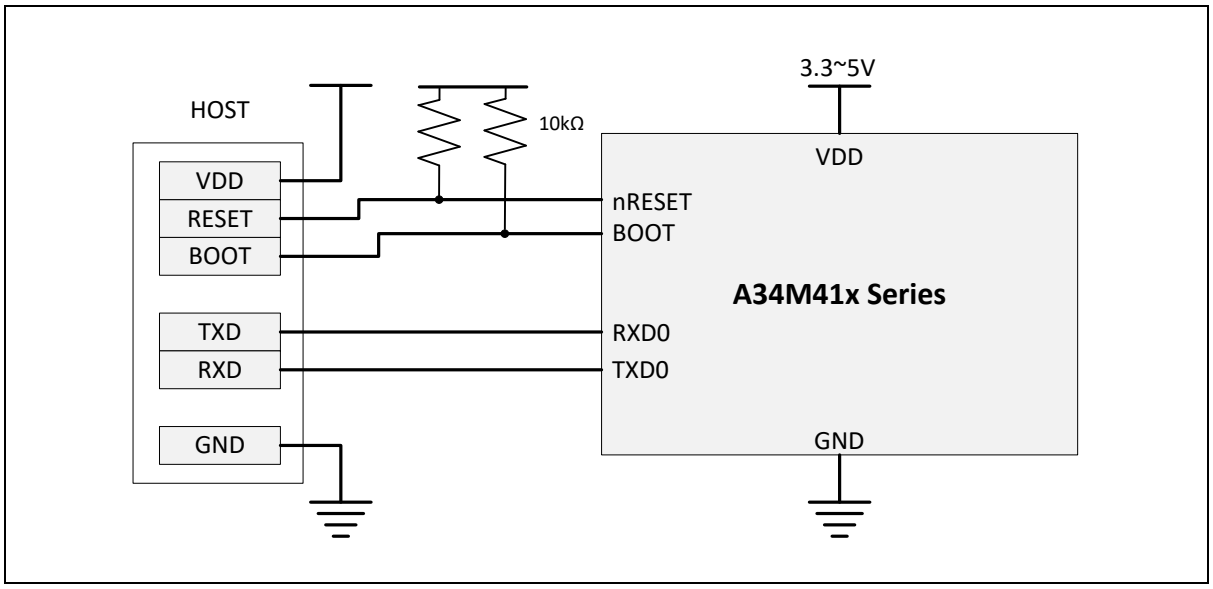


Figure 7. Connection Diagram of UART0 Boot

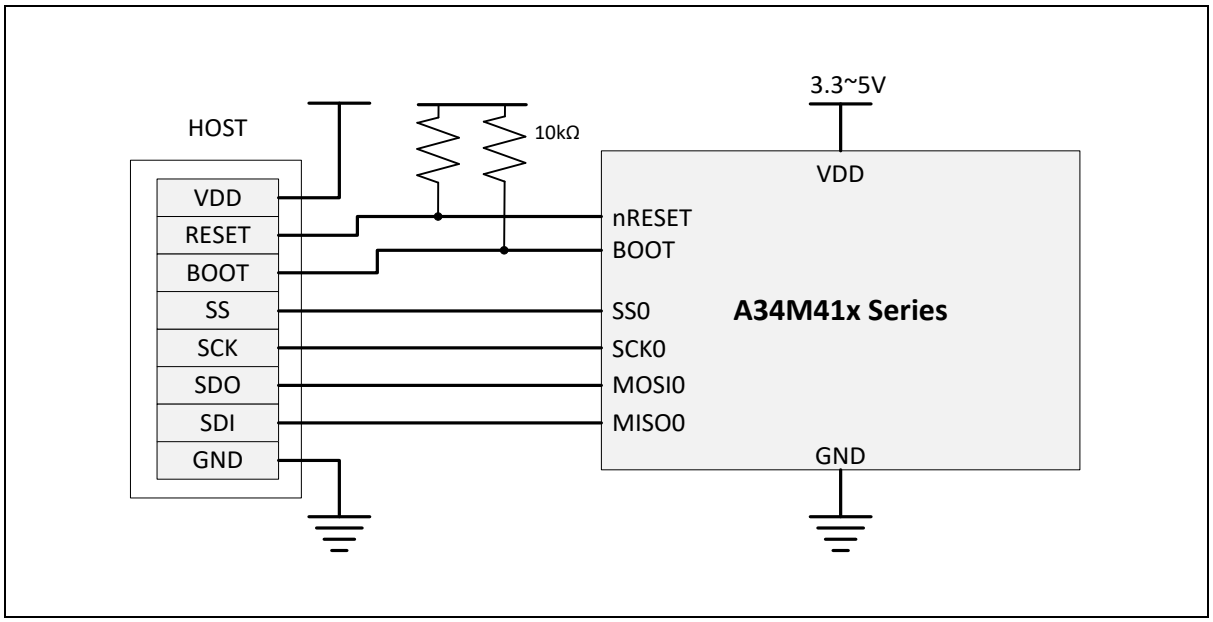


Figure 8. Connection Diagram of SPI0 Boot

SWD mode connections

Users can use SWD mode for writing with E-PGM+. This mode can be used for writing & debugging.

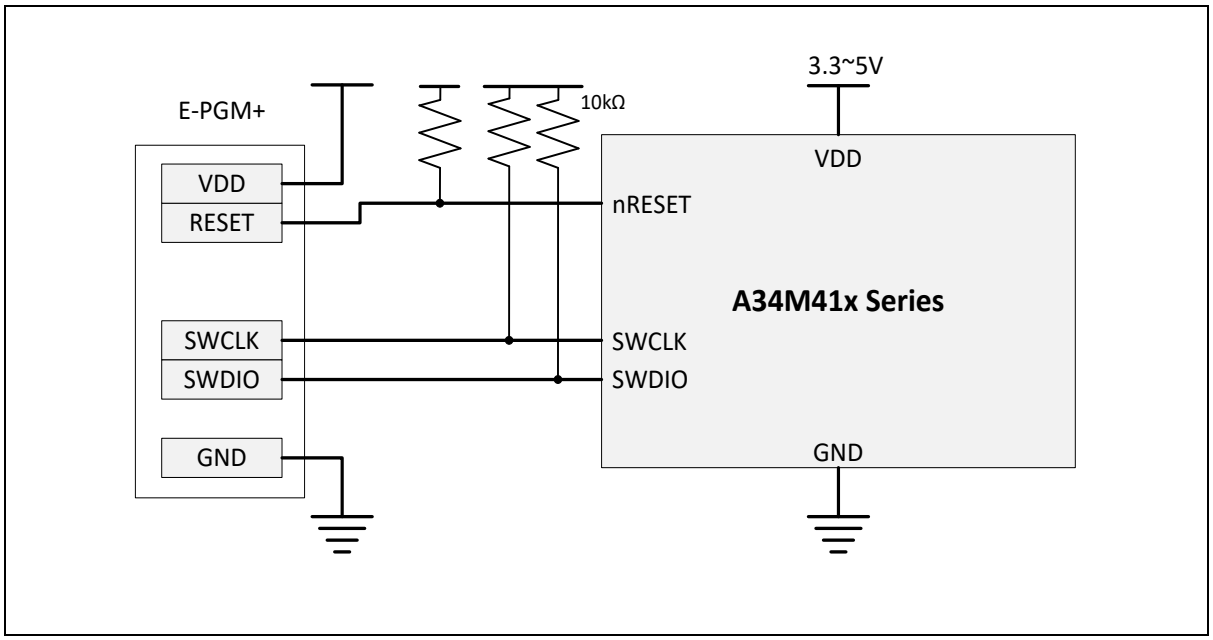


Figure 9. Connection Diagram of E-PGM+ and SWD Port

4 System Control Unit (SCU)

A34M41x series has a built-in intelligent power control block which manages system analog blocks and operating modes. System control unit (SCU) block controls an internal reset and clock signals to maintain optimize system performance and power dissipation.

Four pins in Table 7 are assigned for SCU block

Table 7. SCU Pins

Pin name	Type	Description
nRESET	I	External Reset Input
XIN/XOUT	OSC	External Crystal Oscillator
SXIN/SXOUT	OSC	External sub-Crystal Oscillator
CLKO	O	Clock Output Monitoring Signal

4.1 SCU block diagram

In this subsection, SCU block diagram is introduced in Figure 10.

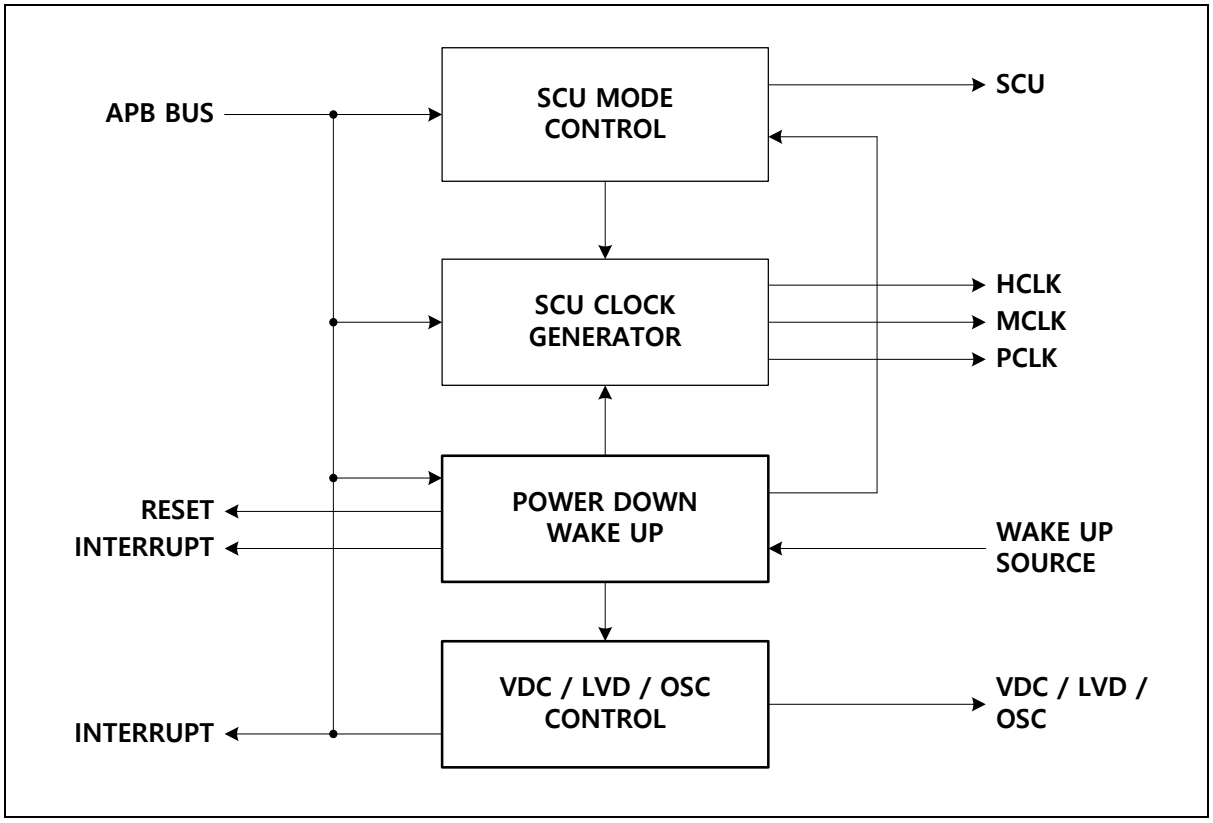


Figure 10. SCU Block Diagram

4.2 Clock system

A34M41x series has two main operating clocks. One is HCLK which produces a clock signal both for CPU and AHB bus system. The other is PCLK which produces a clock signal for peripheral systems.

A user can keep the clock system variation under software control. Through Figure 11 and Table 8, users learn about the clock system of A34M41x devices and clock sources.

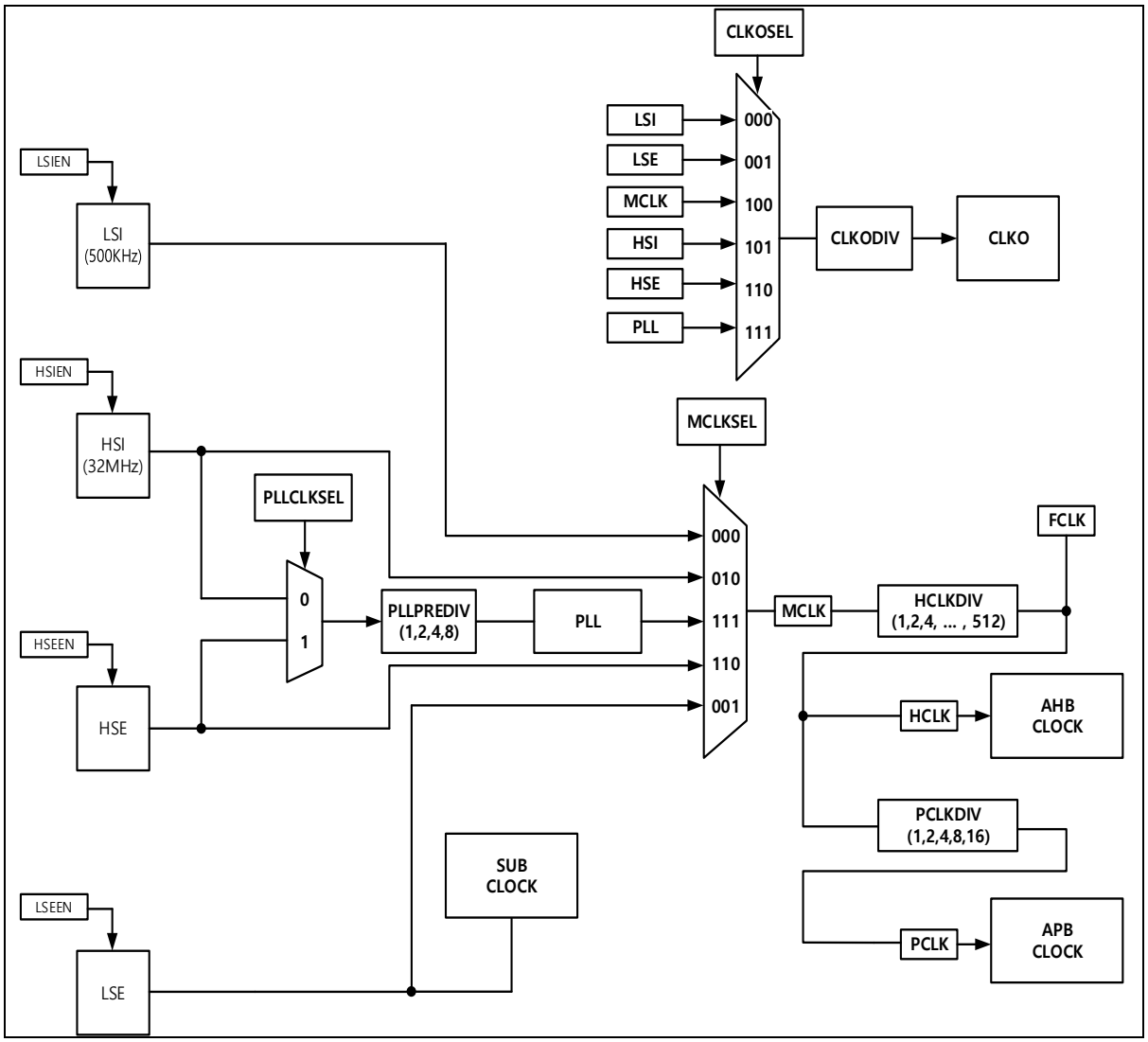


Figure 11. Clock Tree Configuration

All multiplexers switching clock sources have a glitch-free circuit in each. So a clock can be switched without glitch risks. When a user tries to change a clock mux control, both of clock sources must be alive. If one of them is not alive, clock change operation is stopped and system will be halted and not be recovered.

Table 8. Clock Sources

Clock name	Frequency	Description
HSE	4-16MHz	High Speed External Oscillator
LSE	32.768KHz	Low Speed External Oscillator
HSI	32MHz	High Speed Internal OSC
LSI	500KHz	Low Speed Internal OSC

4.2.1 Configuration of miscellaneous clocks

The A34M41x series supports the “miscellaneous clocks” feature, which allows for assigning each peripheral with a different clock source (MCLK, HSE, LSE, PLL, or HSI) at a different frequency division ratio. You can set each peripheral’s clock source and its frequency divider in the corresponding MCCR register. The supported division ratio can be one ranging from 1 to 255.

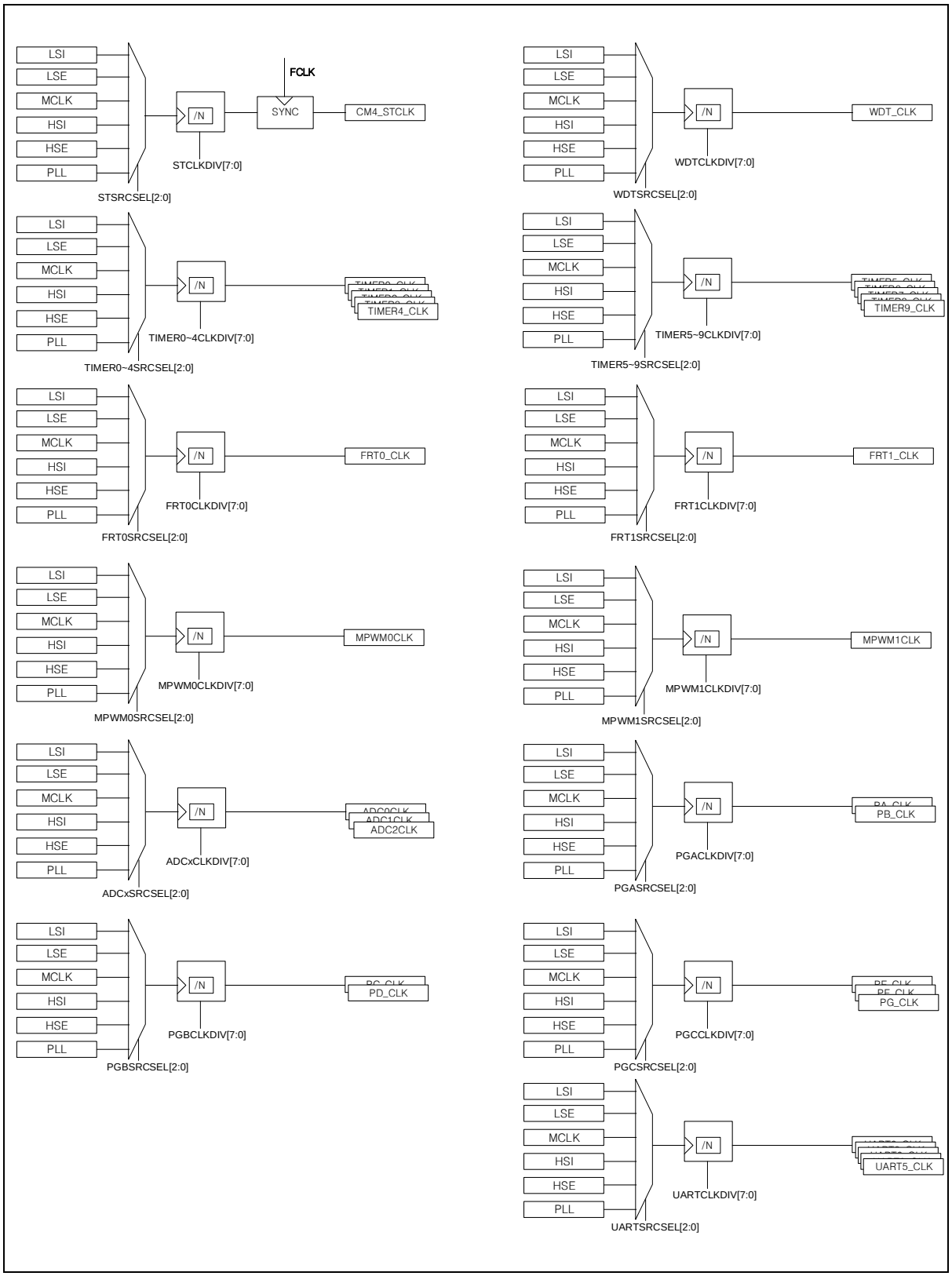


Figure 12. Configuration of Miscellaneous Clocks

4.2.2 HCLK clock domain

The HCLK is fed to the CPU and AHB. The Cortex-M4F CPU requires two clocks, the HCLK and FCLK. The FCLK stays enabled except in deep-sleep mode, whereas the HCLK can be disabled in idle mode.

The buses and memories are clocked by the HCLK. As the bus clock frequency is limited to a maximum of 120MHz, the HCLK frequency must not exceed 120MHz.

4.2.3 PCLK clock domain

The PCLK is used as a clock for any peripherals. Whether to enable or disable the PCLK for each peripheral is determined with the SCU.PCER registers; each peripheral block's registers cannot be read unless its PCLK input is enabled. And the PCLK stops operating in deep-sleep mode.

4.2.4 Clock configuration procedure

After the MCU is powered on, the LSI (500KHz) is initially enabled as the system clock source by default in the system operation sequence. Other clock sources are initially set by the user while the system is clocked by the LSI. The HSI (32MHz) can be enabled with SCU.CSCR (clock source control register). Before enabling the HSE block, the pin mux configuration should be set for XIN and XOUT. You must be careful not to affect other bits of PCC.MR and PCC.CR during this process. Once the HSE block has been enabled, you must wait for the crystal oscillation to stabilize.

The secondary oscillator (LSE) (32.768KHz) clock can be enabled with SCU.CSCR (clock source control register). Likewise with pins XIN and XOUT for the HSE, the LSE must be enabled after the pin mux configuration is set for SXIN and SXOUT and then the stabilizing time is elapsed.

The MCLK can be changed with SCU.SCCR (system clock source register). Figure 13 shows an example of how the system clock is changed.

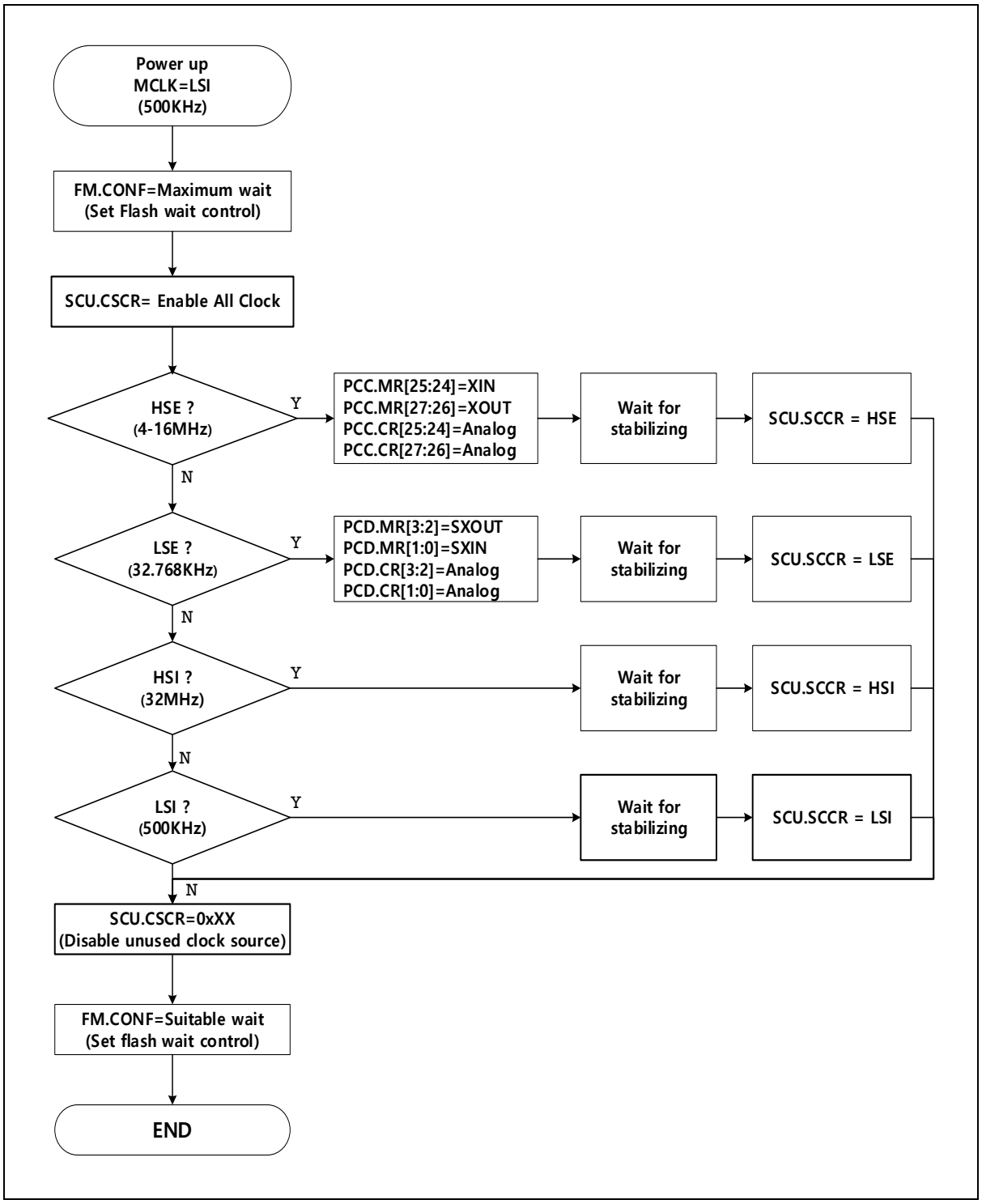


Figure 13. Clock Change Procedure

When you speed up the system clock to the maximum operating frequency, you should check flash wait control configuration. Flash read access time is one of limitation factor for performance. The wait control recommendation is suggested in Table 9.

Table 9. Flash Wait Control Recommendation

FMCONF.WAIT	FLASH access wait	Available max. system clock frequency
0000	0-clock wait	Up to 28MHz
0001	1-clock wait	Up to 56MHz
0010	2-clock wait	Up to 84MHz
0011	3-clock wait	Up to 112MHz
0100	4-clock wait	Up to 120MHz
0101	5-clock wait	Up to 120MHz
0110	6-clock wait	Up to 120MHz
0111	7-clock wait	Up to 120MHz
1000	8-clock wait	Up to 120MHz
1001	9-clock wait	Up to 120MHz
1010	10-clock wait	Up to 120MHz
1011	11-clock wait	Up to 120MHz
1100	12-clock wait	Up to 120MHz
1101	13-clock wait	Up to 120MHz
1110	14-clock wait	Up to 120MHz
1111	15-clock wait	Up to 120MHz

Figure 14 shows how to set the peripheral clock. Selecting a peripheral clock is a typical method of MCCRn and PCLK. Exceptionally WT, WDT, and RTC use other clocks than MCCRn and PCLK. (n = 1, 2, 3, 4, 5 and 6).

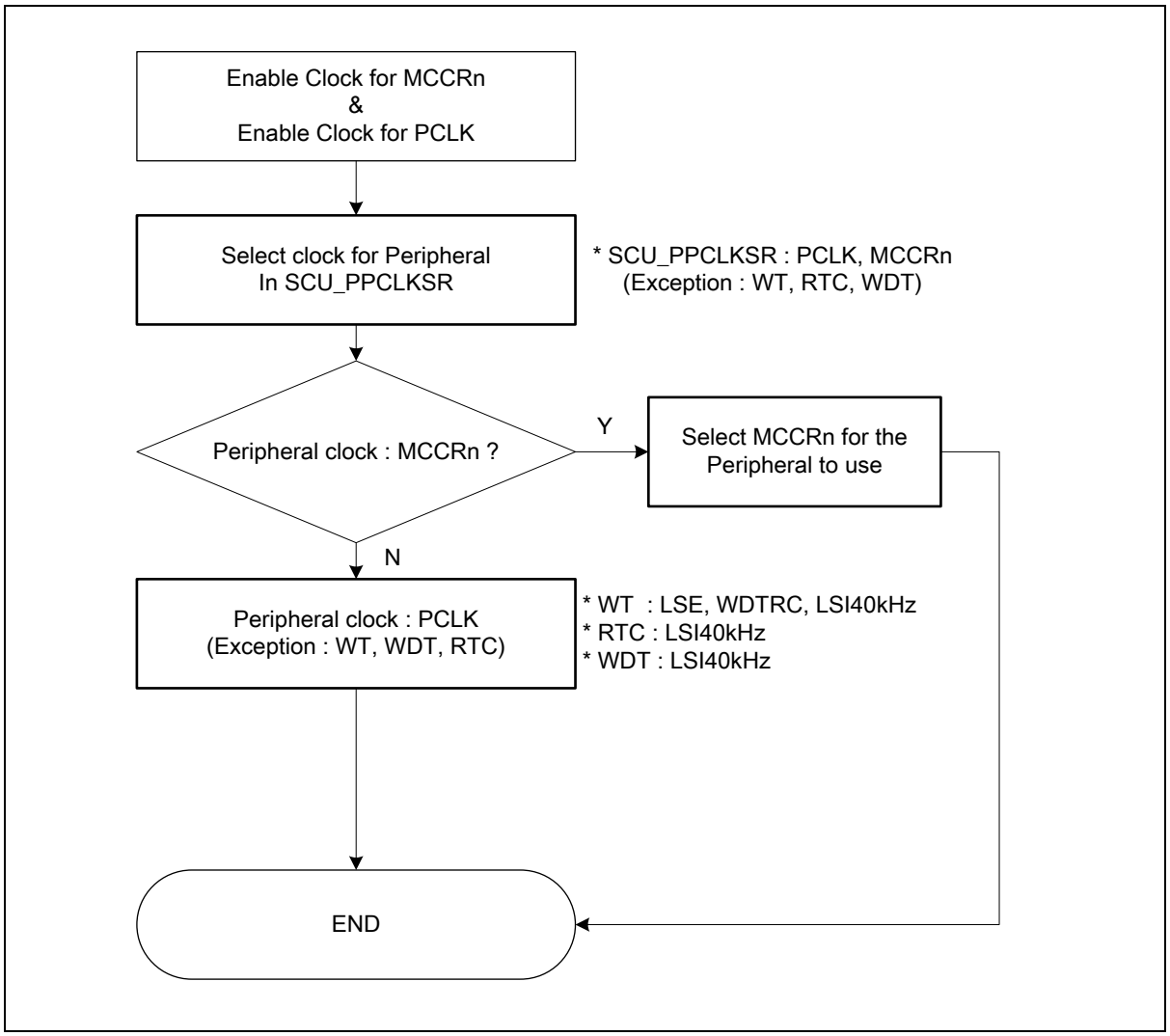


Figure 14. Peripheral Clock Select (n = 1, 2, 3, 4, 5, and 6)

Table 10. Peripheral Clock Select

Peripheral	MCCRn	PCLK
Systick	MCCR1	N/A
WDT		O
MPWM0	MCCR2	N/A
MPWM1		N/A
TIMER04	MCCR3	O
TIMER59		O
ADC	MCCR4	O
PGAD		N/A
PGBD	MCCR5	N/A
PGCD		N/A
FRT0	MCCR6	N/A
FRT1		N/A
UART	MCCR7	N/A

4.3 Reset

The A34M41x series has two system reset options. One is a cold reset that is effective during power up or down sequence. The other is a warm reset which is generated by several reset sources. A reset event makes a chip to turn to an initial state. Reset sources of the cold reset and the warm reset are listed in Table 11.

Table 11. Reset Sources of Cold Reset and Warm Reset

	Cold reset	Warm reset
Reset sources	• POR • LVR reset	• nRESET Pin • WDT reset • HSE Fail reset • LSE Fail reset • S/W reset • CPU request reset

4.3.1 Cold reset

A cold reset plays an important role during a power-up process and affects the entire process of system booting. The internal VDC becomes active as soon as the VDD is applied. The internal POR is triggered when the VDD is determined to reach 1.4V based on the amount of the internal VDC output. During the cold reset process, when the applied voltage exceeds 1.4V, the LSI clock is enabled. After the stabilization of the internal VDC level for 4.25msec, the internal logic is initialized. And then, when the external VDD voltage rises above the LVR voltage level (2.12V), the cold reset is released and, after a waiting time of 0.4ms for warm reset synchronization, booting begins.

Figure 15 shows the power-up process and the initial reset waveforms.

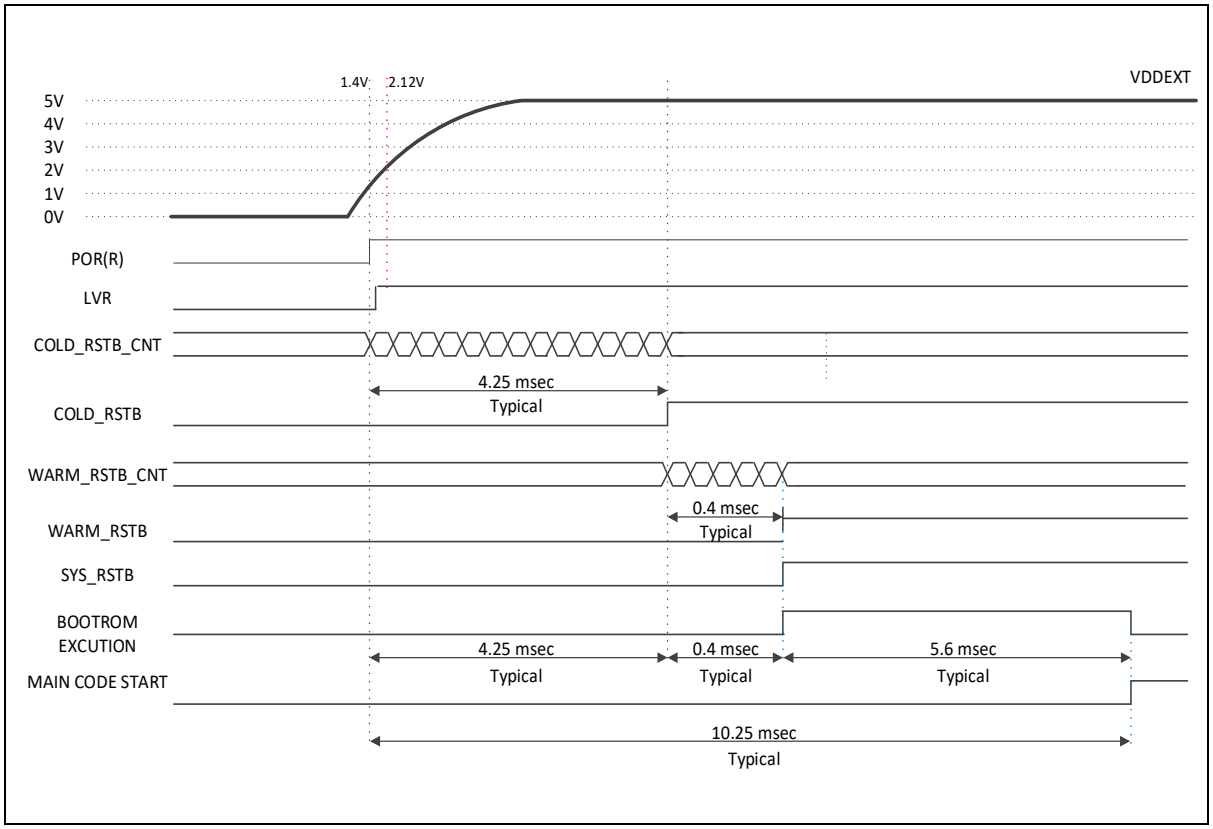


Figure 15. Power-up Procedure

4.3.2 Warm reset

A warm reset event is triggered for system initialization when the conditions of an internally set reset source are met. Warm reset sources are enabled or disabled by configuring SCU.RSER (reset source enable register), and their occurrence is written to SCU.RSSR (reset source status register). Which devices are to be initialized by a warm reset is determined by the settings of SCU.PRER (peripheral reset enable register). Using this register, a user can allow or disallow the initialization of each individual device.

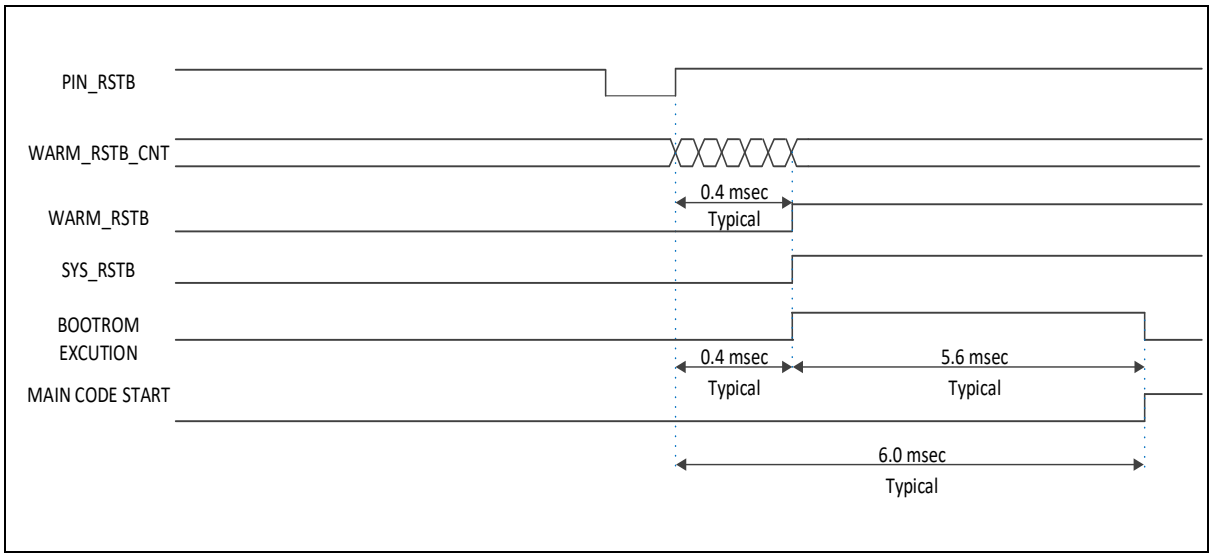


Figure 16. Warm Reset Diagram

4.3.3 LVR reset

An LVR event is triggered when the operating voltage drops below a certain level during the MCU's operation. A user can choose to set the MCU to perform a reset or an interrupt when an LVR event is triggered. This low voltage reset is a warm reset. See the description on warm resetting for details.

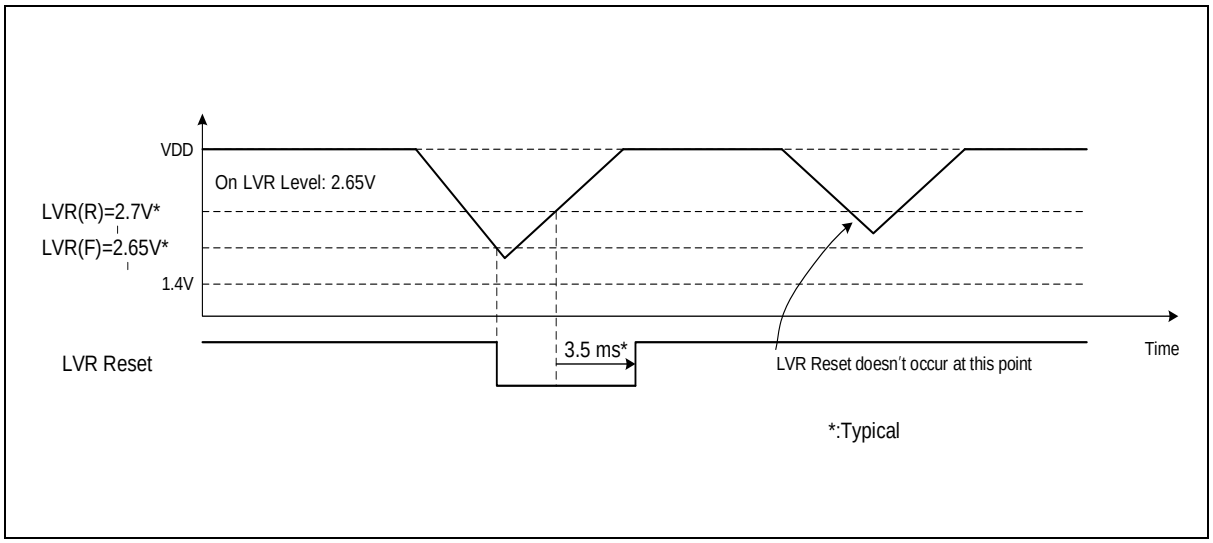


Figure 17. LVR Reset Timing Diagram

4.3.4 Reset tree

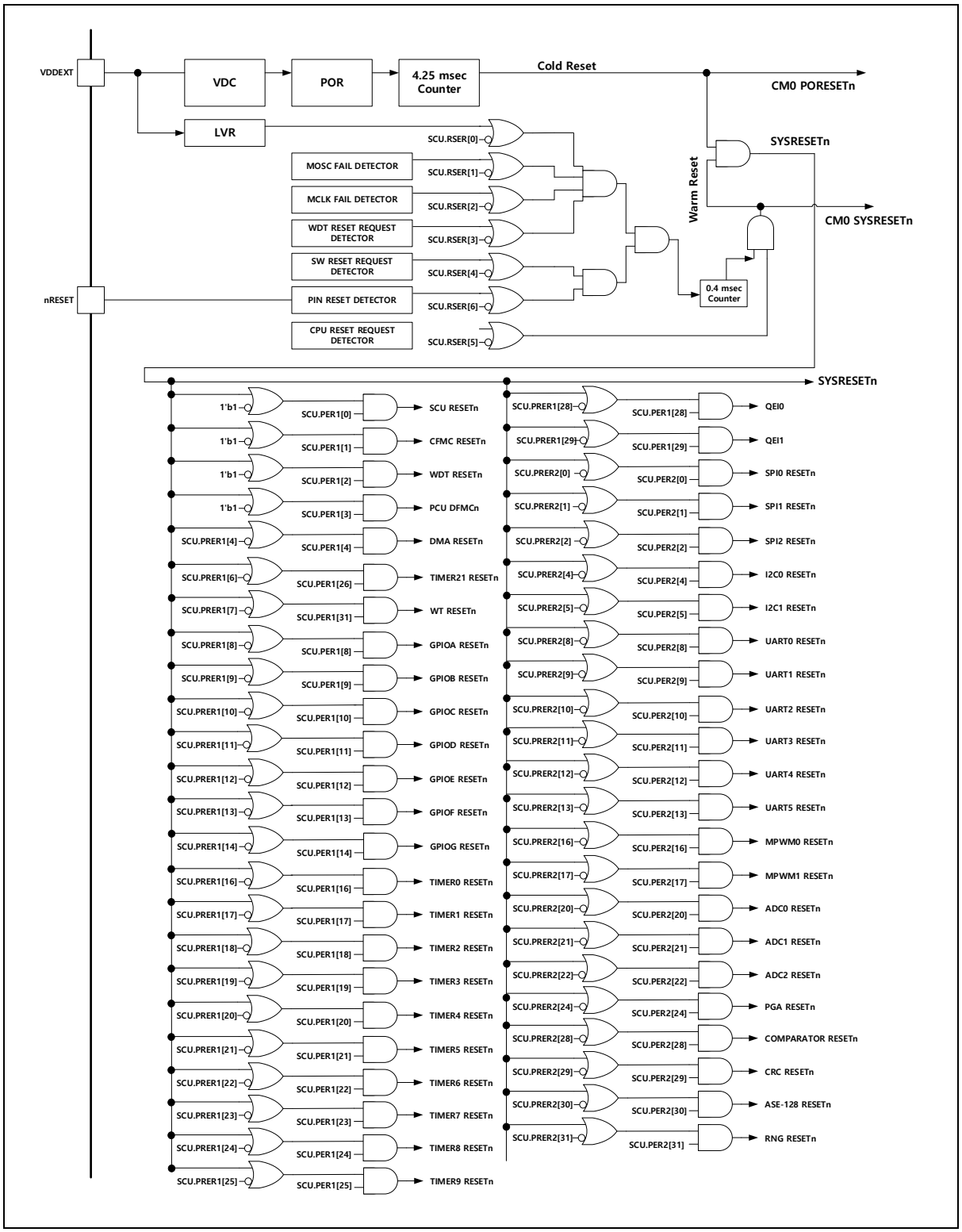


Figure 18. Reset Tree Configuration

4.4 Operation mode

INIT mode is an initial state of the chip when a reset is asserted. In RUN mode, CPU shows the maximum performance with high-speed clock system. SLEEP mode and three power down modes (STOP, STANDBY) can be used as a low power consumption mode. In the low power consumption mode, power is effectively managed to reduce power consumption by halting processor core and unused peripherals. Figure 19 describes transition between the operation modes.

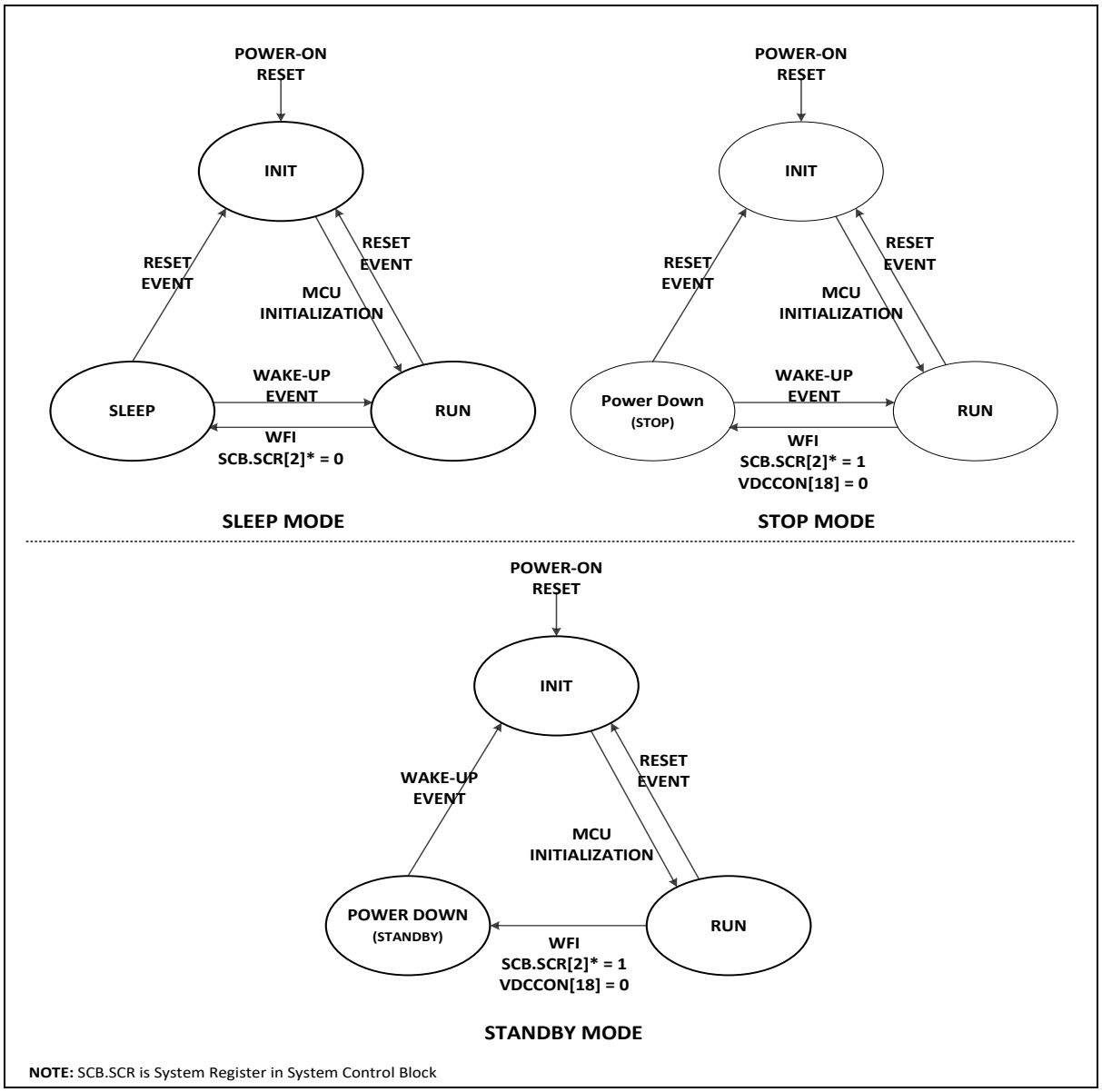


Figure 19. Transition between Operation Modes

Table 12. Operation Mode

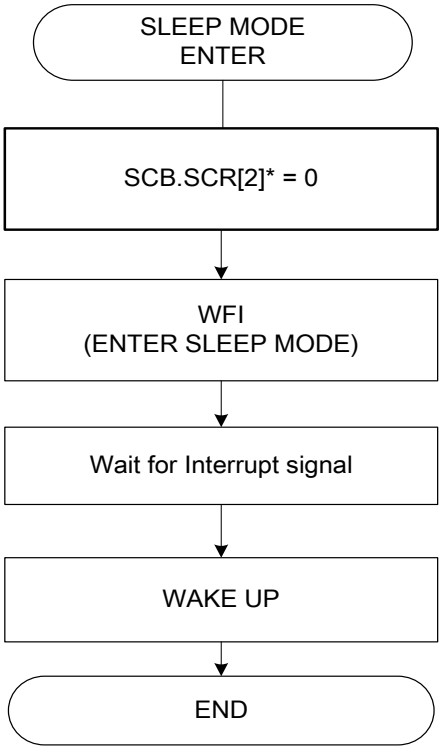
MODE	Condition	After wake-up event	After reset event
RUN	POWER ON	N/A	INIT
SLEEP	WFI (Wait for Interrupt): SCB.SCR[2]*=0	RUN	INIT
STOP	WFI (Wait for Interrupt): SCB.SCR[2]*=1	RUN	INIT
STANDBY	WFI (Wait for Interrupt): SCB.SCR[2]*=1, VDDCON[18]=1	INIT	INIT

4.4.1 RUN mode

In RUM mode, CPU and the peripheral hardware operate with a high-speed clock. After a reset followed by INIT state, the system enters in RUN mode.

4.4.2 SLEEP mode

Once the MCU enters in SLEEP mode, the CPU becomes inactive. By setting the PER and the PCER registers, a user can determine which peripherals are to be inactive in SLEEP mode.



NOTE: SCB.SCR is System Control Register in System Control Block

Figure 20. SLEEP Mode Operation Sequence

4.4.3 STOP (DEEP-SLEEP) mode

In STOP (DEEP-SLEEP) mode, all internal circuits are inactive. A special power-off phase is required to enter stop (deep-sleep) mode.

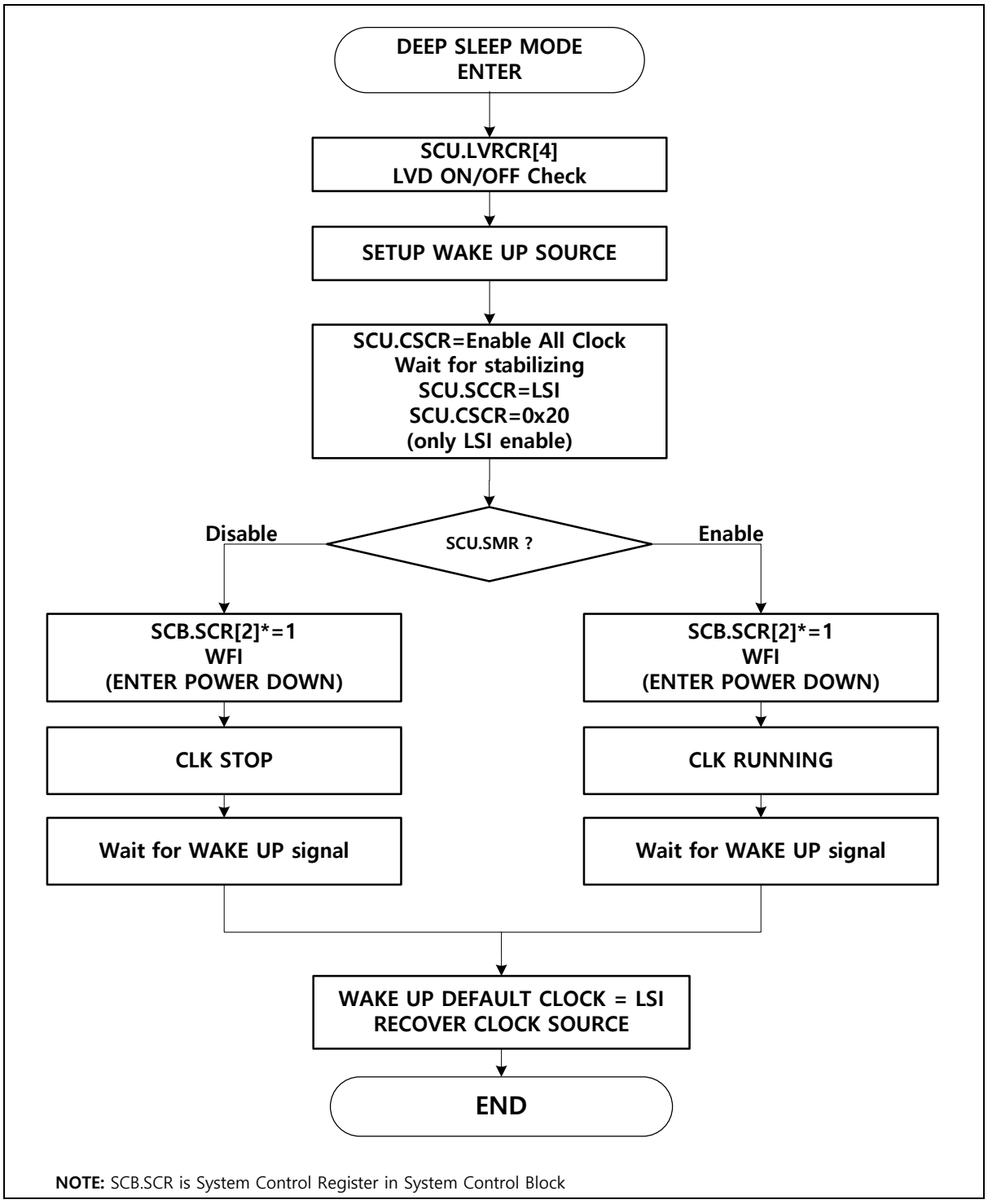


Figure 21. STOP (DEEP SLEEP) Mode Operation Sequence

Table 13 lists configurable clocks in each operating mode.

Table 13. Configurable Clocks in Each Operating Mode

Mode	Core	Peri.	IP					
			VDC	PLL	LSI	HSI	HSE	LSE
RUN	ON	User-defined	ON	User-defined	User-defined	User-defined	User-defined	User-defined
SLEEP	OFF	User-defined	OFF	User-defined	User-defined	User-defined	User-defined	User-defined
STANDBY	OFF	Only WDT, FRT	OFF	User-defined	User-defined	User-defined	User-defined	User-defined
DEEP-SLEEP1	OFF	Only WDT, FRT	OFF	OFF	User Define	OFF	OFF	User-defined
DEEP-SLEEP2	OFF	OFF	OFF	OFF	OFF	OFF	OFF	User-defined

NOTE: Unlike in DEEP-SLEEP mode, the HSE, HSI, and PLL are always enabled in STANDBY mode. Because of this, no stabilization time is required after a wake-up.

5 Port Control Unit (PCU) and GPIO

PCU: The A34M41x MCU's port control unit (PCU) block controls the external input and output (I/O) ports. By setting the PCU block registers, you can configure the pins' uses, input/output, pull-up/pull-down, and debouncing, as needed for your application.

Port Control Unit (PCU) configures and controls external I/Os as listed in the followings:

- The MUX registers define the use of each pin.
  - Input/output
  - Push-pull output
  - Open-drain output
  - Logic input
  - Analog input
- The internal pull-up resistor and open-drain mode are configurable for each pin.
- The following interrupts can be set for each pin:
  - Input level interrupt
  - Input rising-edge interrupt
  - Input falling-edge interrupt
- Up to seven GPIO interrupts are supported (GPIOA(36) through GPIOG(42)).
- Each pin can be set for debouncing.

GPIO: Pins other than the VDD, GND, and certain specific-purpose pins can be used as general-purpose input/output (GPIO) pins. The GPIO block controls the general I/O ports. Output pins can be configured by setting their bits to generate an "H" or "L" level signal, and logic input pins can be checked for their input state.

GPIO ports are controlled by GPIO block as listed in the followings:

- Output signal level (H/L) selection
- External interrupt interface
- Enables or disables pull-up/pull-down for pins

Seven pins in Table 14 are assigned for PCU and GPIO blocks.

Table 14. PCU and GPIO Pins

Pin name	Type	Description
PA	IO	PA0 – PA15
PB	IO	PB0 – PB15
PC	IO	PC0 – PC15
PD	IO	PD0 – PD15
PE	IO	PE0 – PE15
PF	IO	PF0 – PF15
PG	IO	PG0 – PG10

5.1 PCU and GPIO block diagram

Figure 22 describes PCU in block diagram.

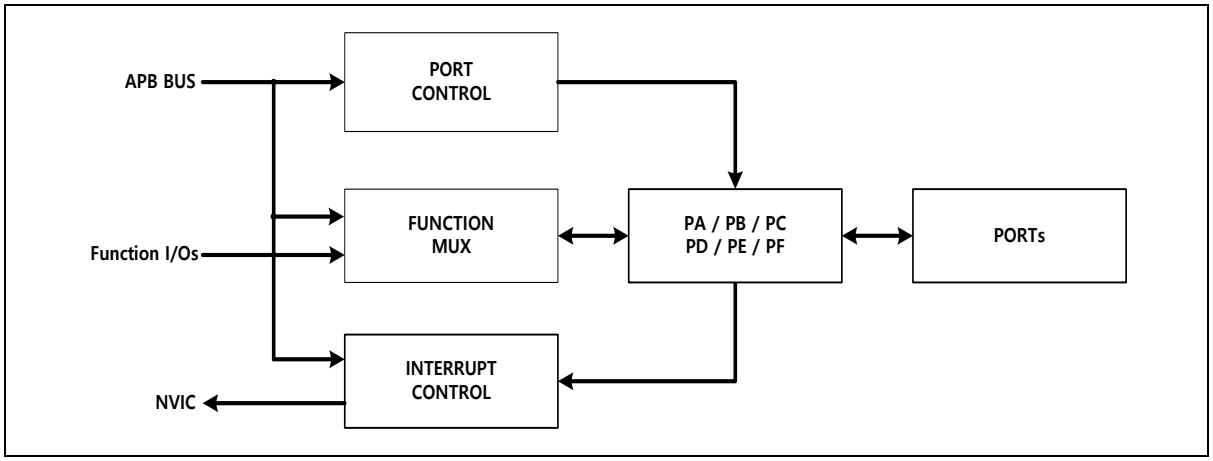


Figure 22. PCU Block Diagram

Figure 23 describes GPIO in block diagram, and Figure 24 introduces external interrupt I/O pins.

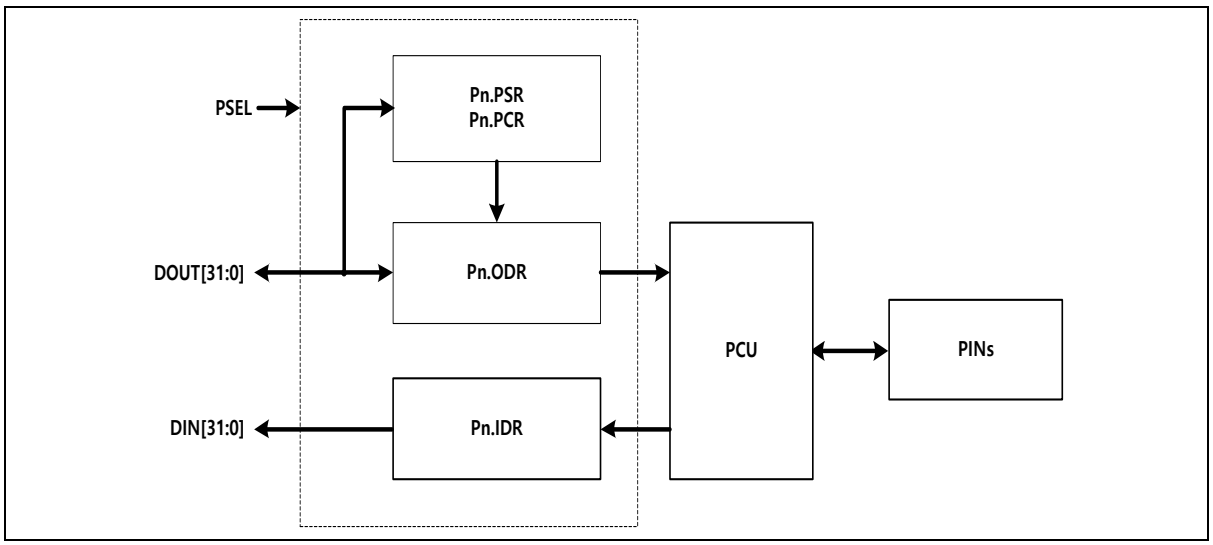


Figure 23. GPIO Block Diagram

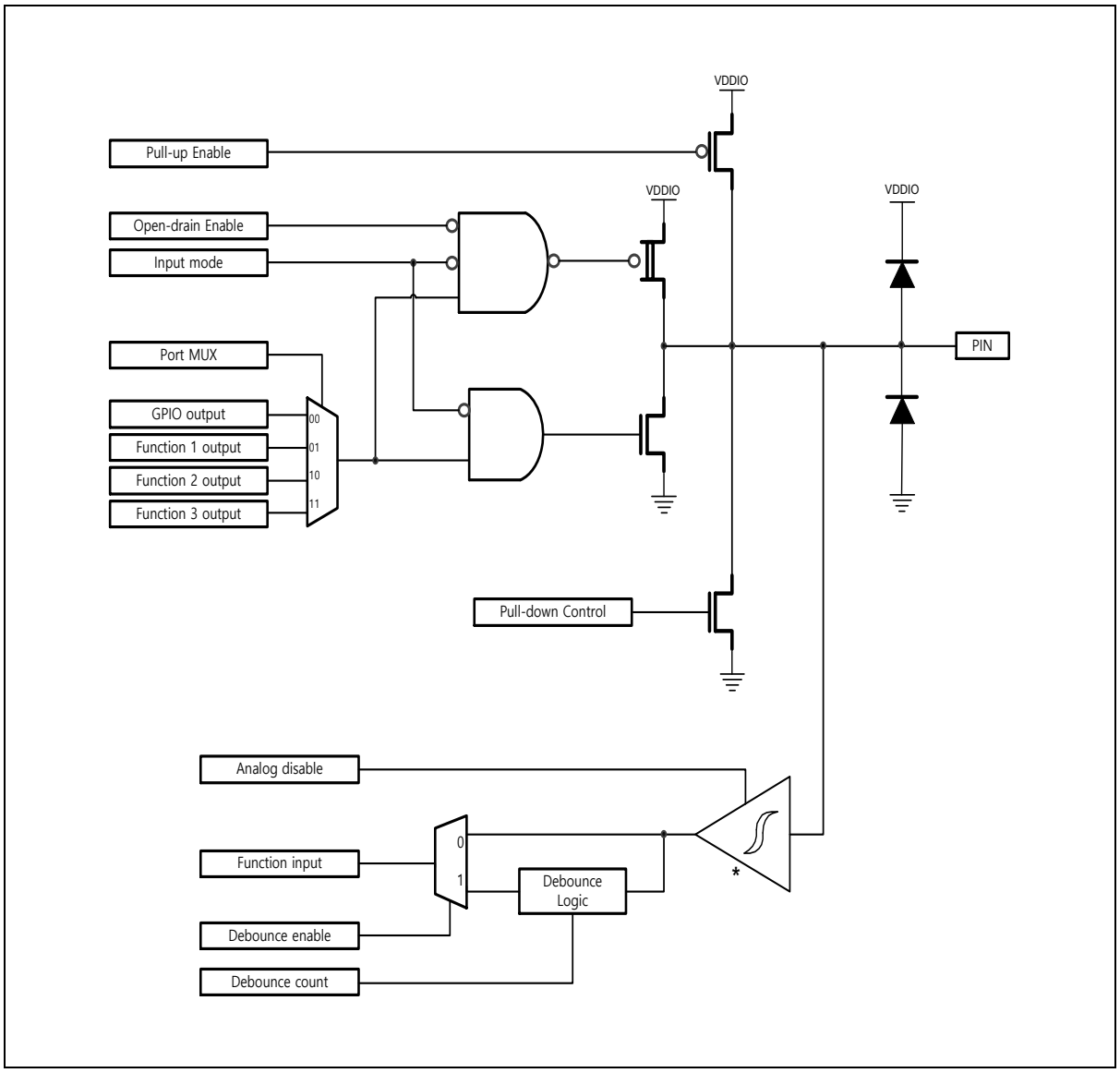


Figure 24. I/O Port Block Diagram (GPIO Pins)

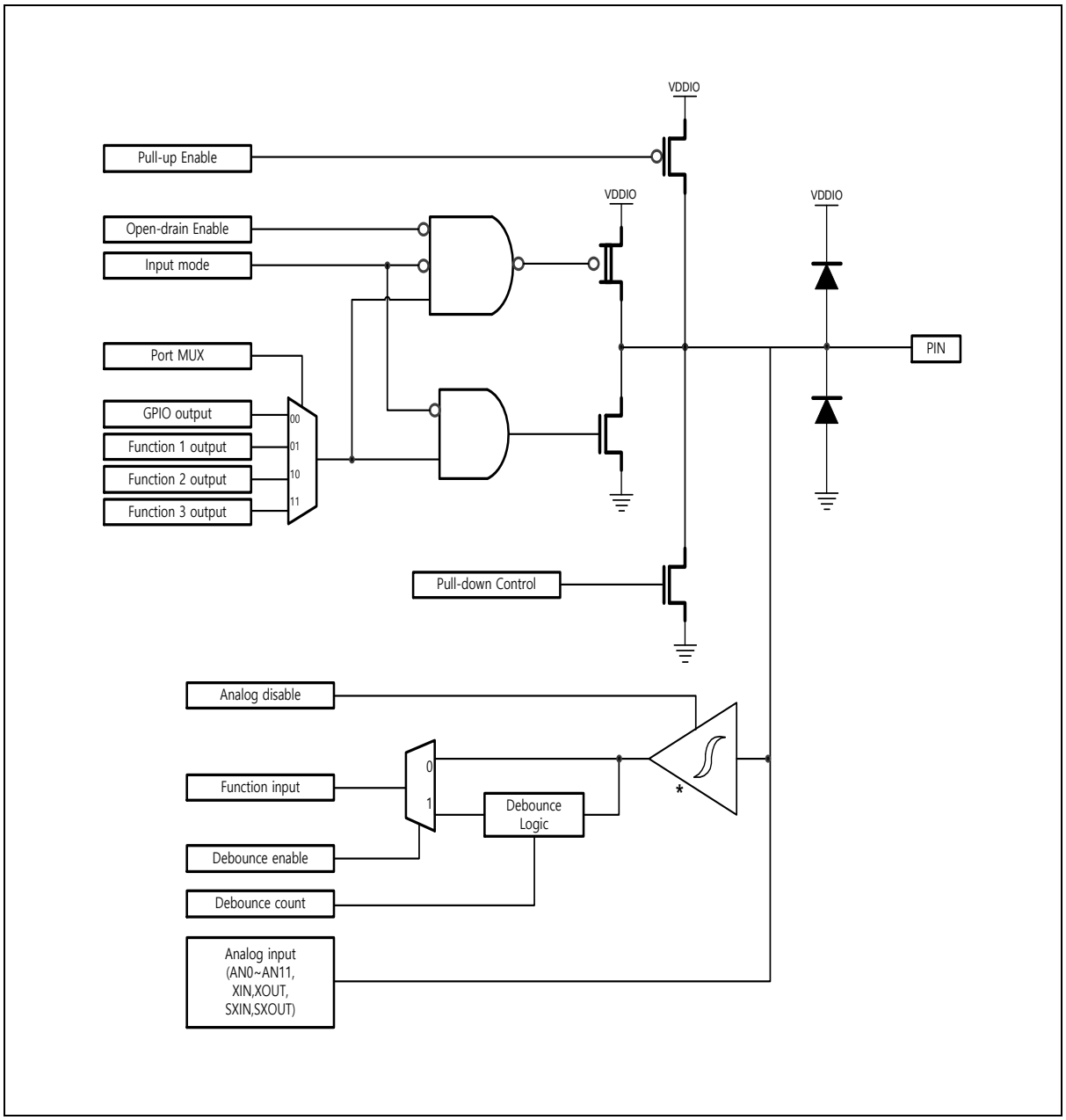


Figure 25. I/O Port Block Diagram (ADC and External Oscillator Pins)

5.2 Pin multiplexing

GPIO pins have alternative function pins. Table 15 shows pin multiplexing information.

Table 15. GPIO Alternative Function

Pin name	Alternative function				
	AF0	AF1	AF2	AF3	AF7
PA0	PA0*				AN0
PA1	PA1*				AN1
PA2	PA2*				AN2
PA3	PA3*				AN3
PA4	PA4*		T0IO		AN4/CP0A
PA5	PA5*		T1IO	CAPEU	AN5/CP0B
PA6	PA6*		T2IO	CAPEV	AN6/CP0C
PA7	PA7*		T3IO	CAPEW	AN7/CREF0
PA8	PA8*				AN8/CP1A
PA9	PA9*				AN9/CP1B
PA10	PA10*	RXD1		SCAPEU	AN10/CP1C
PA11	PA11*	TXD1		SCAPEV	AN11/CREF1
PA12	PA12*	SS0	QEI0_UPDN	SCAPEW	AN12
PA13	PA13*	SCK0	QEI0_A		AN13
PA14	PA14*	MOSI0	QEI0_B	PRTINEV	AN14
PA15	PA15*	MISO0	QEI0_IDX	OVINEV	AN15
PB0	PB0*			MP0UH	
PB1	PB1*			MP0UL	
PB2	PB2*			MP0VH	
PB3	PB3*			MP0VL	
PB4	PB4*		T8IO	MP0WH	
PB5	PB5*		T9IO	MP0WL	
PB6	PB6*			PRTIN0U	
PB7	PB7*			OVIN0U	
PB8	PB8*	RXD3		PRTIN1U	
PB9	PB9*	TXD3		OVIN1U	
PB10	PB10*			MP1UH	
PB11	PB11*			MP1UL	
PB12	PB12*			MP1VH	
PB13	PB13*			MP1VL	
PB14	PB14*			MP1WH	
PB15	PB15*			MP1WL	
PC0	PC0	RXD0		TCK/SWCLK*	
PC1	PC1	TXD0		TMS/SWDIO*	
PC2	PC2			TDO*	
PC3	PC3			TDI*	
PC4	PC4		T0IO	nTRST*	
PC5	PC5*	RXD1	T1IO		
PC6	PC6*	TXD1	T2IO		
PC7	PC7*	SCL0	T3IO		
PC8	PC8*	SDA0	T4IO		
PC9	PC9*		T8IO	CLKO	
PC10	PC10			nRESET*	
PC11	PC11		T9IO	BOOT*	
PC12	PC12*				XIN
PC13	PC13*				XOUT
PC14	PC14*	MOSI0		RXD0	
PC15	PC15*	MISO0		TXD0	

Table 15. GPIO Alternative Function (continued)

Pin name	Alternative function				
	AF0	AF1	AF2	AF3	AF7
PD0	PD0*	SS1			SXIN
PD1	PD1*	SCK1			SXOUT
PD2	PD2*	MOSI1			
PD3	PD3*	MISO1			
PD4	PD4*	SCL1			AN16
PD5	PD5*	SDA1			AN17
PD6	PD6*	TXD2			AN18
PD7	PD7*	RXD2			AN19
PD8	PD8*		T6IO	WDTO	
PD9	PD9*		T7IO	STBYO	
PD10	PD10*		T0IO	AD0S	
PD11	PD11*		T1IO	AD0E	
PD12	PD12*		T2IO	AD1S	
PD13	PD13*		T3IO	AD1E	
PD14	PD14*	SS0		AD2S	
PD15	PD15*	SCK0		AD2E	
PE0	PE0*				
PE1	PE1*				AN20/CP2
PE2	PE2*				AN21/CREF2
PE3	PE3*	SCL0			
PE4	PE4*	SDA0			
PE5	PE5*		T5IO		
PE6	PE6*		T5IO	QEI1_UPDN	
PE7	PE7*		T6IO/QEI1_A		
PE8	PE8*		T7IO/QEI1_B		
PE9	PE9*		T8IO/QEI1_IDX		
PE10	PE10*		T9IO		
PE11	PE11*	SCL1	T0IO		
PE12	PE12*	SDA1	T1IO		
PE13	PE13*	TXD4	T2IO		
PE14	PE14*	RXD4	T3IO		
PE15	PE15*				
PF0	PF0*				
PF1	PF1*				
PF2	PF2*				AN22/CP3
PF3	PF3*				AN23/CREF3
PF4	PF4*	TXD5			
PF5	PF5*	RXD5			
PF6	PF6*			PRTINEW	
PF7	PF7*			OVINEW	
PF8	PF8*				
PF9	PF9*				
PF10	PF10*				
PF11	PF11*				
PF12	PF12*				
PF13	PF13*				
PF14	PF14*				
PF15	PF15*				

Table 19. GPIO Alternative Function (continued)

Pin name	Alternative function				
	AF0	AF1	AF2	AF3	AF7
PG0	PG0*	SS2			
PG1	PG1*	SCK2			
PG2	PG2*	MOSI2			
PG3	PG3*	MISO2			
PG4	PG4*				
PG5	PG5*				
PG6	PG6*				
PG7	PG7*				
PG8	PG8*	RXD3			
PG9	PG9*	TXD3			
PG10	PG10*				

NOTE: The initial setting of each pin is marked by an asterisk (*). Unused pins are set to output from Firmware (low output is recommended).

6 Flash memory controller

The flash memory controller (FMC) is an interface controller of internal flash memories:

- Flash code memory with 128-KB, 256-KB, and 512-KB protection bits
- 512-B, 1-KB, and 4-KB erases
- 128-KB, 256-KB, and 512-KB bulk erases
- 35 ns-long flash access read time
- Zero wait (less than 28MHz), 1- to 15-wait, and cache (flash acceleration) access

Table 16. Code Flash Memory Controller Features

Item	Description		
Size	128KB	256KB	512KB
Start Address	0x0000_0000	0x0000_0000	0x0000_0000
End Address	0x0002_0000	0x0004_0000	0x0008_0000
Page Size	512-byte	512-byte	512-byte
Total Page Count	256 pages	512 pages	1024 pages
PGM Unit	512-byte	512-byte	512-byte
Erase Unit	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk	512-byte/ 1KB/ 4KB/ bulk

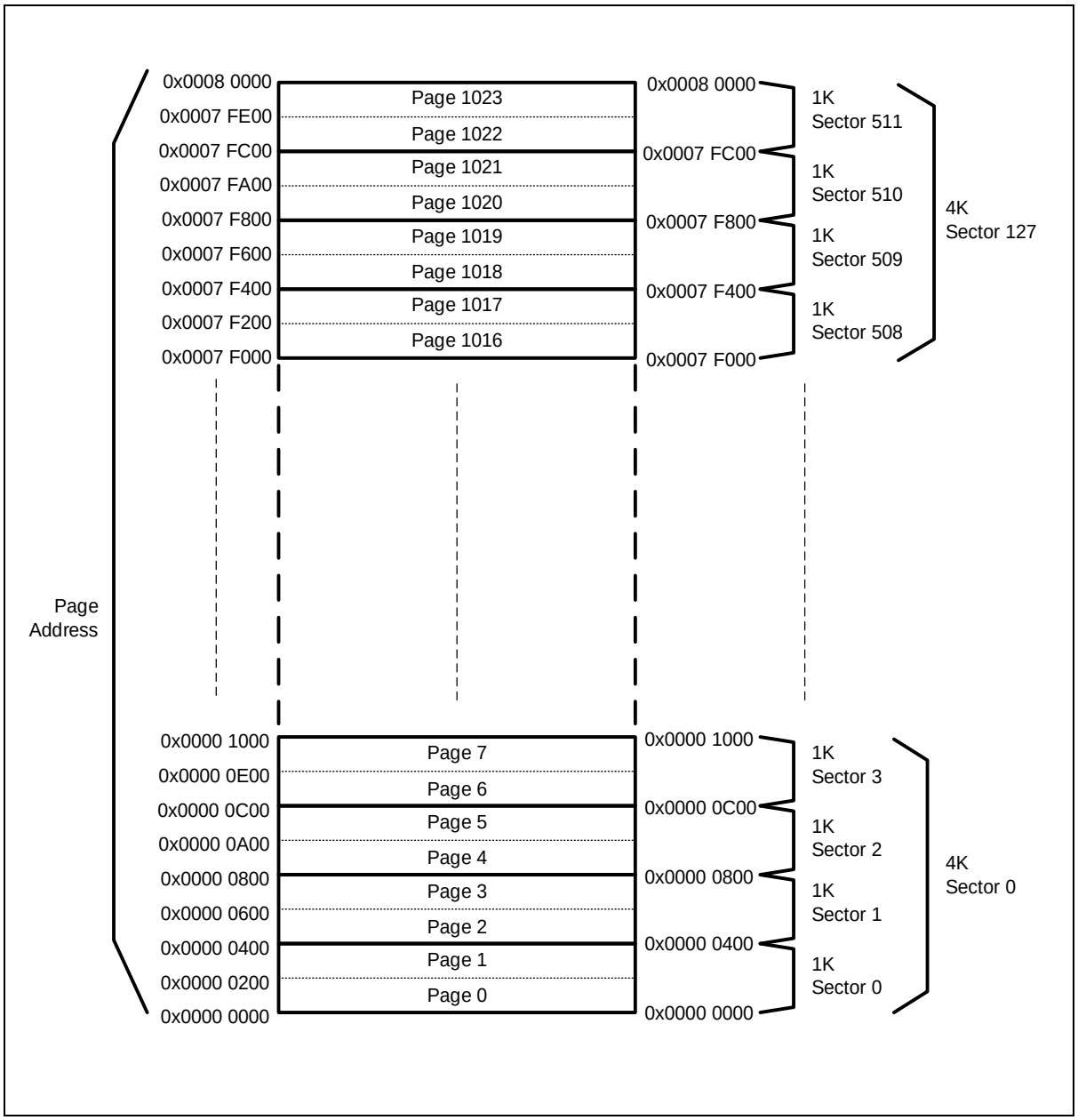


Figure 26. Code Flash Memory Map (512 KB Code Flash)

Table 17. Data Flash Memory Controller Features

Item	Description
Size	32KB
Start Address	0x0E00_0000
End Address	0x0E00_8000
Page Size	512-byte
Total Page Count	64 pages
PGM Unit	512-byte
Erase Unit	512-byte / 2KB / bulk

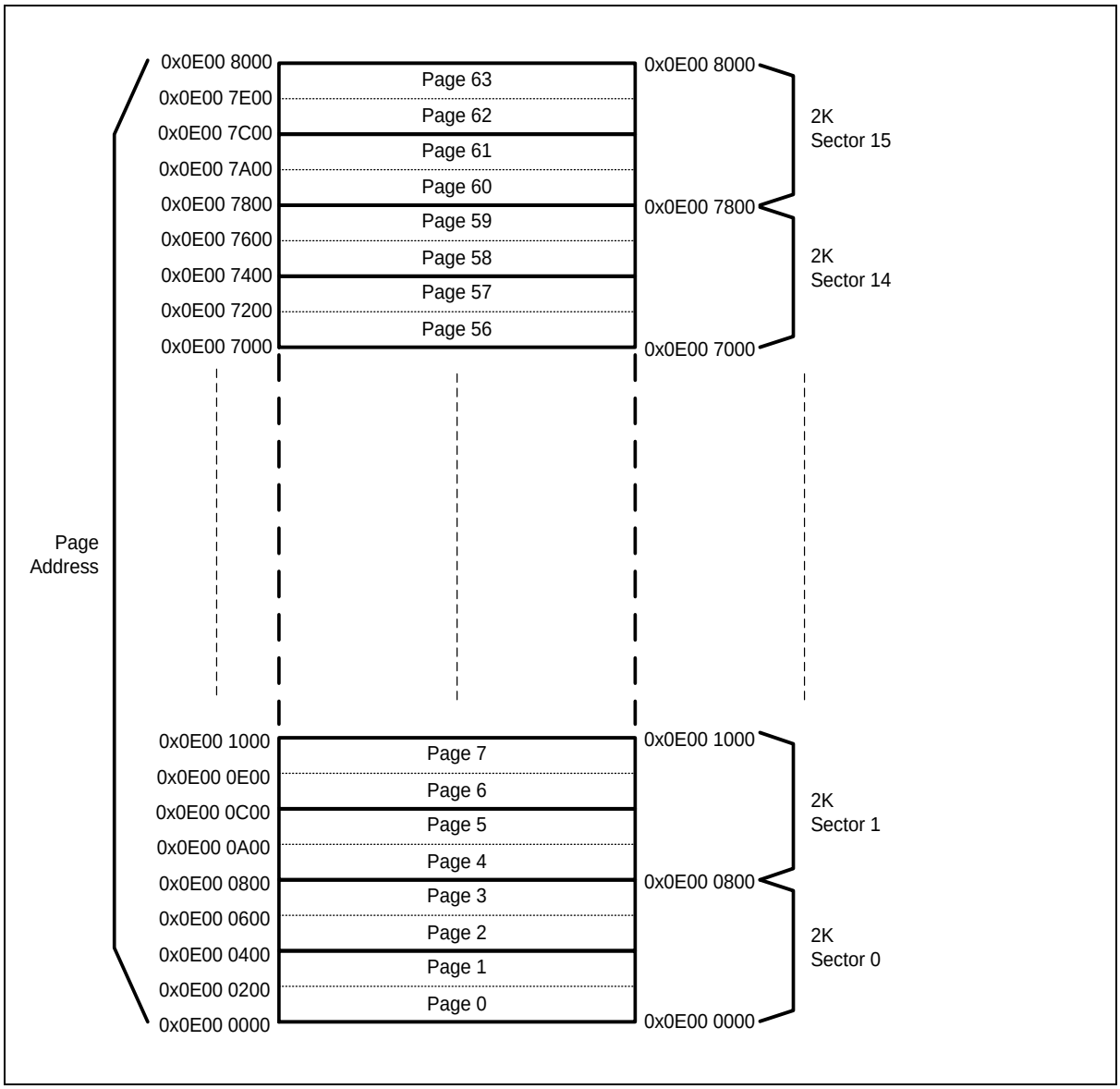


Figure 27. Data Flash Memory Map (32 KB Data Flash)

7 Internal SRAM

The A34M41x series has a zero-wait SRAM built in. The size of the SRAM is 64/32 KB. The start address of the SRAM is 0x2000_0000. The SRAM is primarily used as data memory and stack memory. Occasionally, a code is dumped into the SRAM for fast operation or to erase/write to the flash memory.

8 Direct Memory Access Controller (DMAC)

The direct memory access (DMA) controller is used for high-speed data transfers between peripherals and memories. DMA enables quick data transfers having memory to memory copying or moving of data within memory.

- 16 channels
- Only single-ended signaling supported
- 8-/16-/32-bit data transfers supported
- Various buffers with the same size supported
- DMA transfers are triggered through peripheral interrupts

8.1 Block diagram

In this section, DMAC block diagram is introduced in Figure 28.

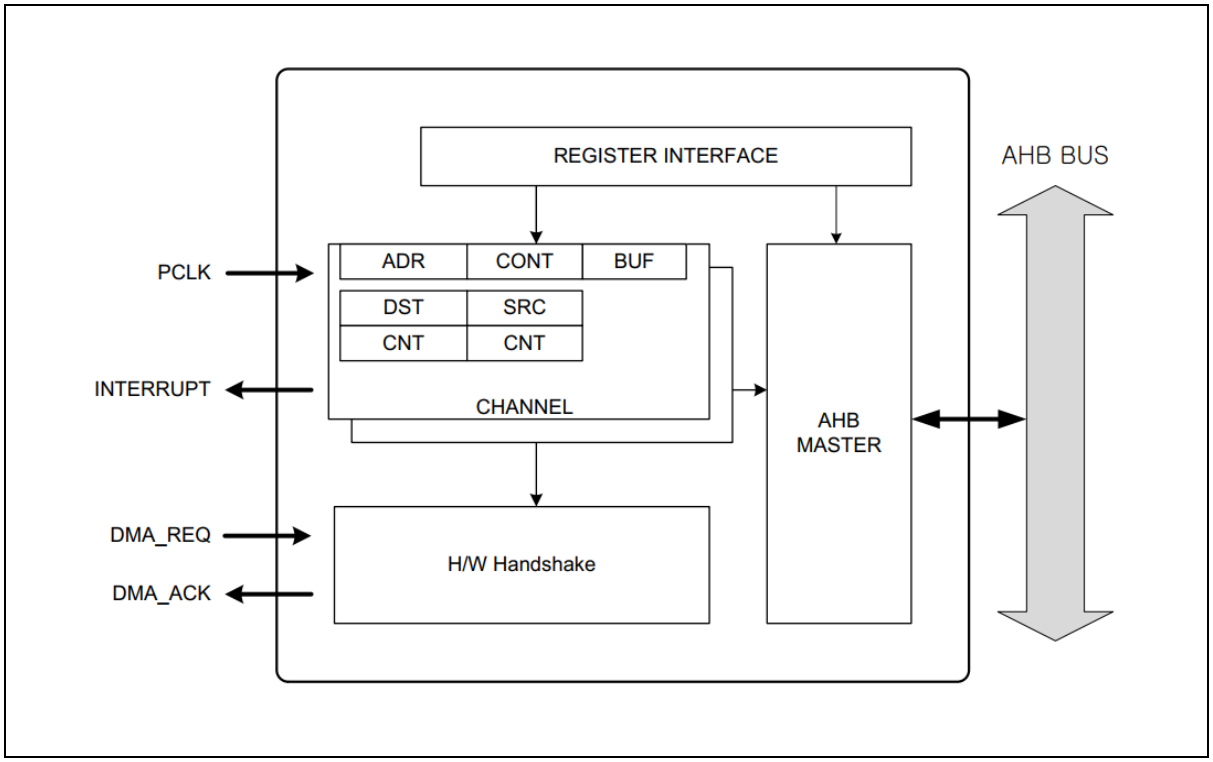


Figure 28. DMAC Block Diagram

9 Watchdog timer (WDT)

Watchdog timer (WDT) monitors the operation of the MCU and is typically used to detect software errors. When the MCU becomes uncontrollable due to a malfunction, the WDT resets the MCU to recover it.

The A34M41x series has one WDT module built in, which functions as a 32-bit down-counter. Once the WDT counts down to zero while set as a reset source, the MCU gets reset. When it is not used to monitor the MCU, it can be used as a cycle timer along with an interrupt.

WDT of A34M41x series features followings:

- A 32-bit down-counter
- WDT underflow reset supported
- Cycle timer and underflow interrupt supported
- WDT input clock sources selectable
  - PCLK
  - Clock sources selectable with the setting of SCU_MCCR1<WDTSEL[26:24>: LSI, LSE, MCLK, HSI, HSE, PLL
- Eight-level prescalers for the WDT clock
- The user can set whether to enable or disable the WDT counter in debug mode

9.1 WDT block diagram

In this section, WDT block diagram is introduced in Figure 29.

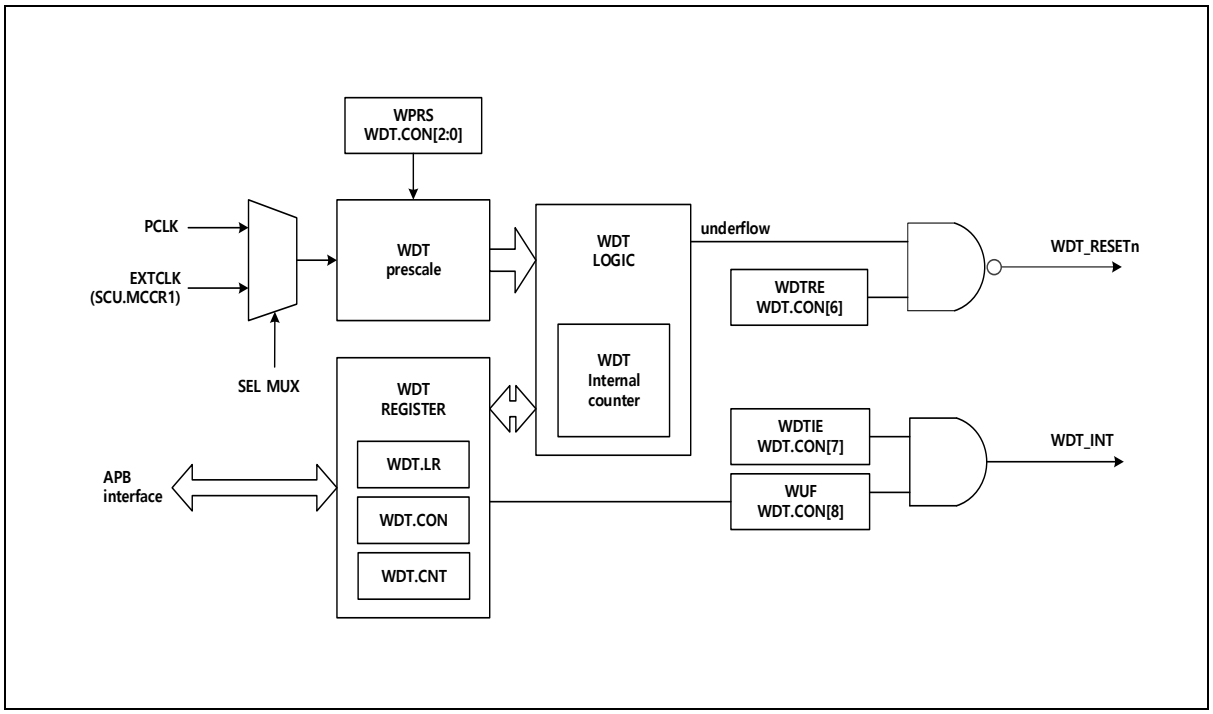


Figure 29. WDT Block Diagram

10 16-bit timer

The A34M41x series has ten channels of 16-bit timers built in. These 16-bit timers support four operating modes: periodic, PWM, one-shot, and capture modes. As the input clock source to the 16-bit timers, either a divided PCLK or an external clock can be used. Additionally, an internal 10-bit prescaler allows the user to generate various timer base clocks.

Interrupts can be triggered at regular intervals when a timer is used in periodic mode. The user can set the period and duty to form a PWM signal to be used in PWM mode. In one-shot and PWM modes, the timer can generate one PWM waveform. In capture mode, the external input signal's pulse intervals can be measured based the preset conditions. Moreover, the timer can export signals to other devices to control them. These timers are primarily used as periodic tick timers or wake-up sources.

16-bit timer of A34M41x series features the followings:

1. 16-bit up-counter timers
2. Four operating modes:
    - Periodic timer mode
    - One-shot timer mode
    - PWM mode
    - Capture mode
3. Various interrupts:
    - Match/overflow interrupts
4. Timer input clock sources selectable:
    - Four PCLK prescaler levels (1/2, 1/4, 1/16, 1/64)
    - Clock sources selectable with the setting of SCU_MCCR3: LSI, LSE, MCLK, HSI, HSE, and PLL
    - Timer clock source by an input to port TnC
5. 10-bit prescaler built in to support the timer input clock
6. PWM synchronization
    - Start delay and clear synchronization

Table 18 introduces pins assigned for 16-bit timer.

Table 18. Pin Assignment of 16-bit Timer: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
T0C	I	Timer0 capture input signal/external clock input	O	O	O
T1C	I	Timer1 capture input signal/external clock input	O	O	O
T2C	I	Timer2 capture input signal/external clock input	O	O	O
T3C	I	Timer3 capture input signal/external clock input	O	O	O
T4C	I	Timer4 capture input signal/external clock input	O	O	O
T5C	I	Timer5 capture input signal/external clock input	O	O	O
T6C	I	Timer6 capture input signal/external clock input	O	O	O
T7C	I	Timer7 capture input signal/external clock input	O	O	O
T8C	I	Timer8 capture input signal/external clock input	O	O	O
T9C	I	Timer9 capture input signal/external clock input	O	O	O
T0O	O	Timer0 timer/PWM/one-shot output	O	O	O
T1O	O	Timer1 timer/PWM/one-shot output	O	O	O
T2O	O	Timer2 timer/PWM/one-shot output	O	O	O
T3O	O	Timer3 timer/PWM/one-shot output	O	O	O
T4O	O	Timer4 timer/PWM/one-shot output	O	O	O
T5O	O	Timer5 timer/PWM/one-shot output	O	O	O
T6O	O	Timer6 timer/PWM/one-shot output	O	O	O
T7O	O	Timer7 timer/PWM/one-shot output	O	O	O
T8O	O	Timer8 timer/PWM/one-shot output	O	O	O
T9O	O	Timer9 timer/PWM/one-shot output	O	O	O

10.1 16-bit timer block diagram

In this section, 16-bit timer is described in a block diagram in Figure 30.

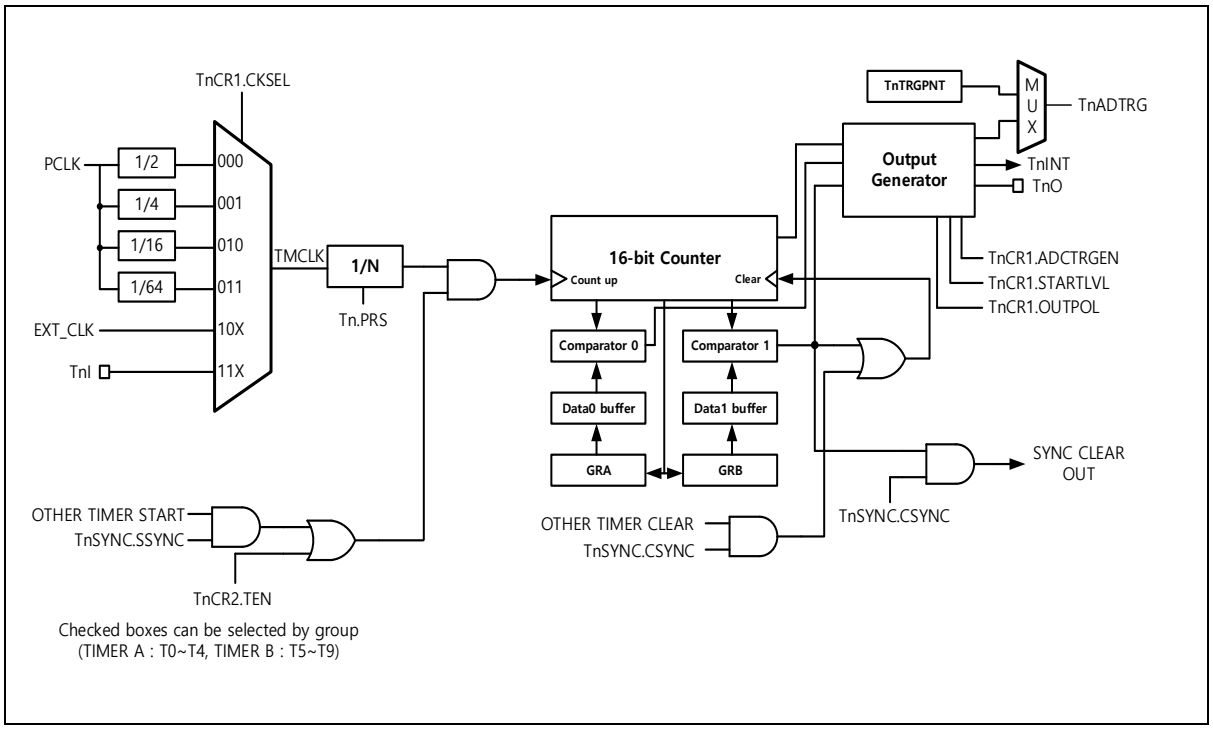


Figure 30. 16-bit Timer Block Diagram

11 Free-run timers (FRT)

The A34M41x series has two free-run timers (FRTs) built in, which are 32-bit up-count timers. These timers can run with the overflow or match interrupt according to their uses and can remain active in deep-sleep mode.

FRT of A34M41x series features the followings:

- 32-bit up-count timers
  - Capable of functioning as periodic timers (Each timer's period is configurable)
  - Free-run timer mode
- FRT overflow and match interrupts supported
- FRT input clock sources selectable
  - Clock sources selectable with the setting of SCU_MCCR6: LSI, LSE, MCLK, HSI, HSE, and PLL

11.1 FRT block diagram

In this section, FRT block diagram is introduced in Figure 31.

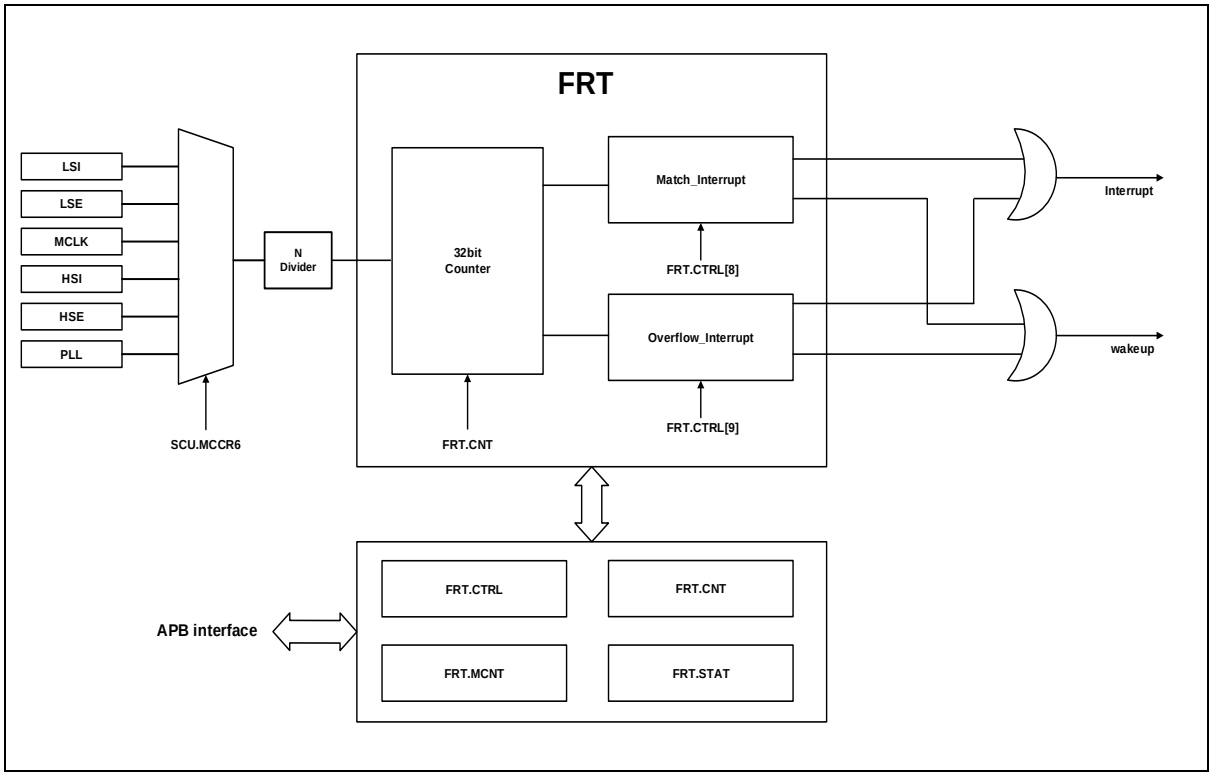


Figure 31. FRT Block Diagram

12 Universal Asynchronous Receiver/Transmitter (UART)

The A34M41x series is equipped with a six-channel UART module. These built-in UARTs transmit and receive data according to user-specified settings and read the current UART status. UART status information includes the type and conditions of the current UART transmission/reception process and can be used to check for errors (parity, overrun, framing, or break interrupts) that occur during data reception.

Each UART channel has a programmable baud-rate generator, which serves to generate an internal clock for the corresponding UART by dividing the prescaled clock by a baud-rate divisor (ranging from 1 to 65535) and then dividing the result by 16.

Additionally, the user can program interrupts that control UART communication.

UART of A34M41x series features the followings:

- A total of six 16450 asynchronous serial communication ports supported
- Configurable standard asynchronous communication bits (start, stop, and parity)
- User-programmable serial communication
  - 5, 6, 7, or 8 data bits
  - Even, odd, or no parity generation and checking
  - 1-, 1.5-, or 2-stop bit generation and checking
- A 16-bit baud-rate generator and an 8-bit fractional compensator
- Delay between data frames supported
- Transfer status indicated by the interrupt ID and line status registers
  - Stop bit error detection
  - Display of information about the current status
  - Line break generation and checking
  - Receive error diagnosis
- Loop-back control
- A priority-based interrupt system

Table 19 introduces pins assigned for the UART.

Table 19. Pin Assignment of UART: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
TXD0	O	UART channel 0 transmit output	O	O	O
RXD0	I	UART channel 0 receive input	O	O	O
TXD1	O	UART channel 1 transmit output	O	O	O
RXD1	I	UART channel 1 receive input	O	O	O
TXD2	O	UART channel 2 transmit output	O	O	O
RXD2	I	UART channel 2 receive input	O	O	O
TXD3	O	UART channel 3 transmit output	O	O	O
RXD3	I	UART channel 3 receive input	O	O	O
TXD4	O	UART channel 4 transmit output	O	O	O
RXD4	I	UART channel 4 receive input	O	O	O
TXD5	O	UART channel 5 transmit output	O	O	O
RXD5	I	UART channel 5 receive input	O	O	O

12.1 UART block diagram

In this section, UART is introduced in block diagrams.

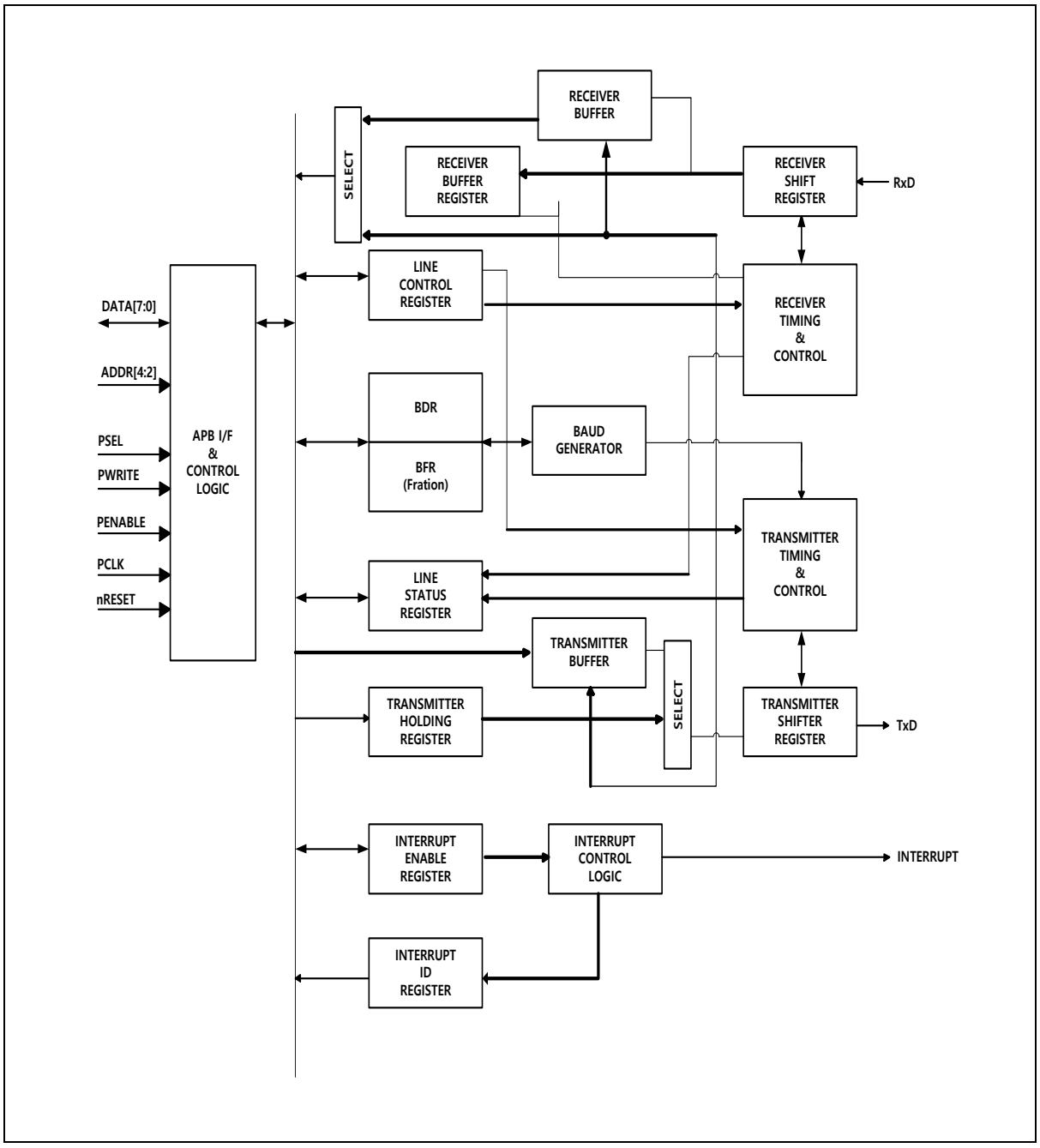


Figure 32. UART Block Diagram

13 Serial Peripheral Interface (SPI)

The A34M41x series has three serial peripheral interface (SPI) modules built in. The SPI modules are synchronized by clocks. The specifications of the transmit and receive clocks are adjustable. The SPI supports communications between one master and multiple slaves. Slaves can be selected using slave select (SS).

The SPI performs four-wire synchronous transfers via four signal terminals (SS, SCK, MOSI, and MISO). Its separate transmit and receive buffers enables full-duplex communication, which is capable of reading and writing data simultaneously.

SPI of A34M41x series features the followings:

- Selectable between the master and slave operations
- Full-duplex and four-wire synchronous transfers supported
  - SS: Slave Select
  - SCLK: Serial Clock
  - MOSI: Master Output Slave Input
  - MISO: Master Input Slave Output
- SPI clock speed and polarity adjustable
- Separate transmit and receive data registers with different data transfer sizes
  - Available transmit/receive data sizes: 8, 9, 16, and 17 bits
- Configurable interrupts triggered by the transmit status and SS signal
- Loop-back mode for internal checkups
- User-programmable start, burst, and stop delay times
- DMA transfers

Table 20 introduces pins assigned for SPI.

Table 20. Pin Assignment of SPI: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
SS0	I/O	SPI0 serial port I/O signal for slave selection	O	O	O
SCK0	I/O	SPI0 clock I/O (master: output / slave: input)	O	O	O
MOSI0	I/O	SPI0 transmit and receive data (master: output / slave: input)	O	O	O
MISO0	I/O	SPI0 transmit and receive data (master: input / slave: output)	O	O	O
SS1	I/O	SPI1 serial port I/O signal for slave selection	O	O	O
SCK1	I/O	SPI1 clock I/O (master: output / slave: input)	O	O	O
MOSI1	I/O	SPI1 transmit and receive data (master: output / slave: input)	O	O	O
MISO1	I/O	SPI1 transmit and receive data (master: input / slave: output)	O	O	O
SS2	I/O	SPI2 serial port I/O signal for slave selection	O	O	O
SCK2	I/O	SPI2 clock I/O (master: output / slave: input)	O	O	O
MOSI2	I/O	SPI2 transmit and receive data (master: output / slave: input)	O	O	O
MISO2	I/O	SPI2 transmit and receive data (master: input / slave: output)	O	O	O

13.1 SPI block diagram

In this section, SPI is described in a block diagram in Figure 33.

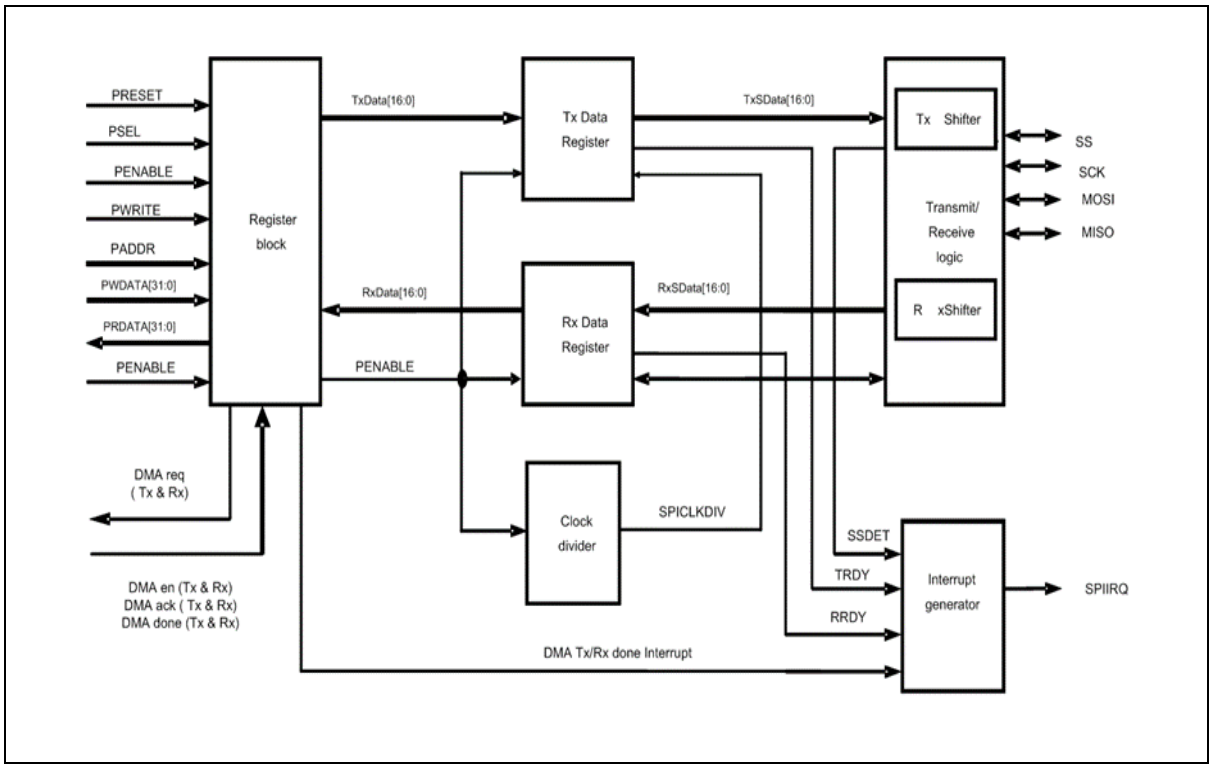


Figure 33. SPI Block Diagram

14 Inter-Integrated Circuit (I2C)

The I2C (inter-integrated circuit) interface built in the A34M41x series provides serial communications with internal and external devices via the I2C protocol. Equipped with two channels, it supports both master and slave modes and capable of transmitting and receiving data in bytes through interrupts or polling. The I2C block is used to communicate with various peripherals that have the same bus type. When using the I2C capabilities of the A34M41x series, it is recommended to configure pins SCL and SDA as open-drain and then connect an external pull-up resistor to each of them to render their output signals “high.”

I2C features the followings:

- Compliant with I2C protocol
  - Supports two channels
- Master and slave modes
- Multi-slave mode
  - 1:1 and N:N (up to 1008) slave devices
- Transfer rates configurable
  - Maximum transfer rate: 400KHz
- I2C interrupts
- 7-bit addressing
- Delay time can be set for pin SCL’s high or low waveform
- Hold time can be set for previous data
- Generates and detects STOP, START, and ACK signals

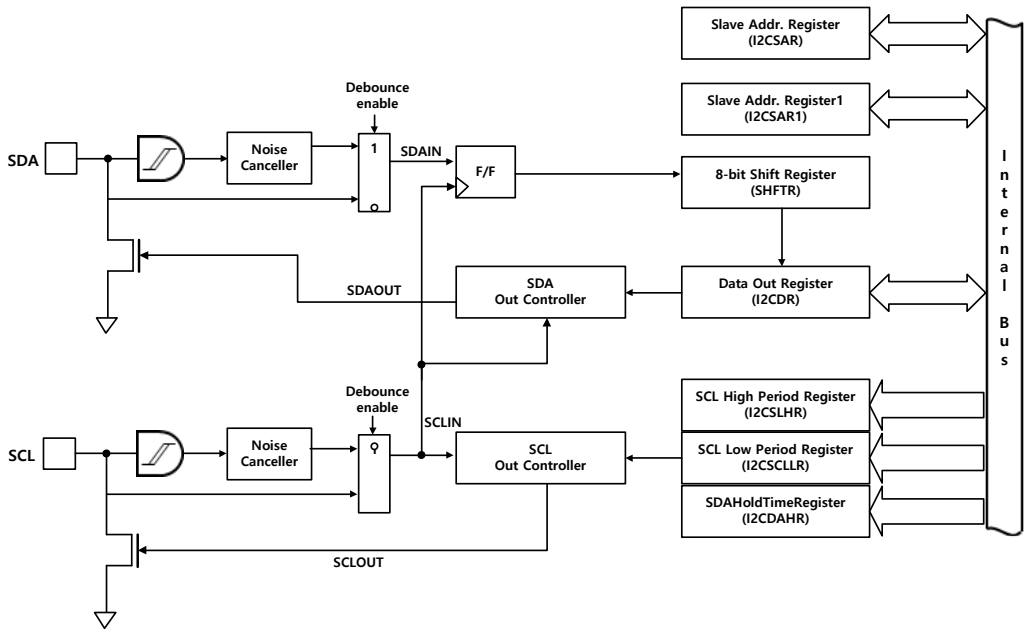
Table 21 introduces pins assigned for I2C interface.

Table 21. Pin Assignment of I2C: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
SCL0	I/O	I2C channel 0 serial clock bus line (open-drain)	O	O	O
SDA0	I/O	I2C channel 0 serial data bus line (open-drain)	O	O	O
SCL1	I/O	I2C channel 1 serial clock bus line (open-drain)	O	O	O
SDA1	I/O	I2C channel 1 serial data bus line (open-drain)	O	O	O

14.1 I2C block diagram

In this section, I2C interface block is described in a block diagram.



NOTE: When the corresponding port of I2C is a sub-function for SCL/SDA pin, the SCL/SDA pins are automatically set to the N-channel open-drain outputs and the input latch is read in the case of reading the pins. The corresponding pull-up resistor is determined by the control register.

Figure 34. I2C Block Diagram

15 Motor Pulse Width Modulation (MPWM)

The Motor PWM (MPWM) modules are programmable motor controllers optimized for three-phase AC and DC motor control applications. Each MPWM module is equipped with three channels that can generate their respective pairs of outputs. The MPWM counter is clocked from the SCU block. As the clock determines MPWM resolution and period, you must select an appropriate MPWM clock before enabling the MPWM module.

MPWM Normal Mode of A34M41x series features the followings:

- 16-bit counter
- Six output channels for motor control
- Dead-time rising or falling area
- Handling of protection and overvoltage events
- Six ADC trigger sources
- Interval interrupt mode (Only a period interrupt is used)
- Up-count and down-count modes

MPWM Individual Mode of A34M41x series features the followings:

The MPWM module supports an Individual mode to enable various applications, such as IH cookers.

- 16-bit counter
- Different periods and dead times (rising/falling) configurable for phases U, V, and W
- Handling of different protection and overvoltage events for phases U, V, and W
- Different interrupts for phases U, V, and W (except for the protection and overvoltage interrupts)
- Different protection and overvoltage events for phases U, V, and W (e.g., if protection occurs for phase V, only the phase V output becomes inactive while phases U and W remain operational).
- Capture functionality

Table 22 introduces pins assigned for MPWM.

Table 22. Pin Assignment of MPWM: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
MP0UH/L MP0VH/L MP0WH/L	O	MPWM0 H/L side output ports of phases U, V, and W	O	O	O
MP1UH/L MP1VH/L MP1WH/L	O	MPWM1 H/L side output ports of phases U, V, and W	O	O	O
PRTIN0U OVIN0U	I	MPWM0 protection and overvoltage input pins dedicated to MPWM0 phase U in Individual mode	O	O	O
PRTIN1U OVIN1U	I	MPWM1 protection and overvoltage input pins dedicated to MPWM1 phase U in Individual mode	O	O	O
PRTINEV OVINEV	I	Protection and overvoltage input pins dedicated to MPWM0/1 phase V in Individual mode	O	O	O
PRTINEW OVINEW	I	Protection and overvoltage input pins dedicated to MPWM0/1 phase W in Individual mode	O	O	O
CAPEU CAPEV CAPEW	I	Input pins in MPWM0/1 dedicated to capturing in Individual mode	O	O	O
SCAPEU SCAPEV SCAPEW	I	Input pins in MPWM0/1 dedicated to sub-capturing in Individual mode	O	O	O
Normal mode	MPWM0 Protection		MPWM1 Protection		
	PRTIN0U OVIN0U		PRTIN1U OVIN1U		

Table 22. Pin Assignment of MPWM: External Pins (continued)

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
Individual mode	U	PRTIN0U OVIN0U	PRTIN1U OVIN1U		
	V	PRTINEV	OVINEV		
	W	PRTINEW	OVINEW		

NOTE: in Individual PWM mode, V and W of PRTINE / OVINE operate simultaneously with MPWM0 and MPWM1.

15.1 MPWM block diagram

Figure 35 describes normal mode of MPWM in block diagram.

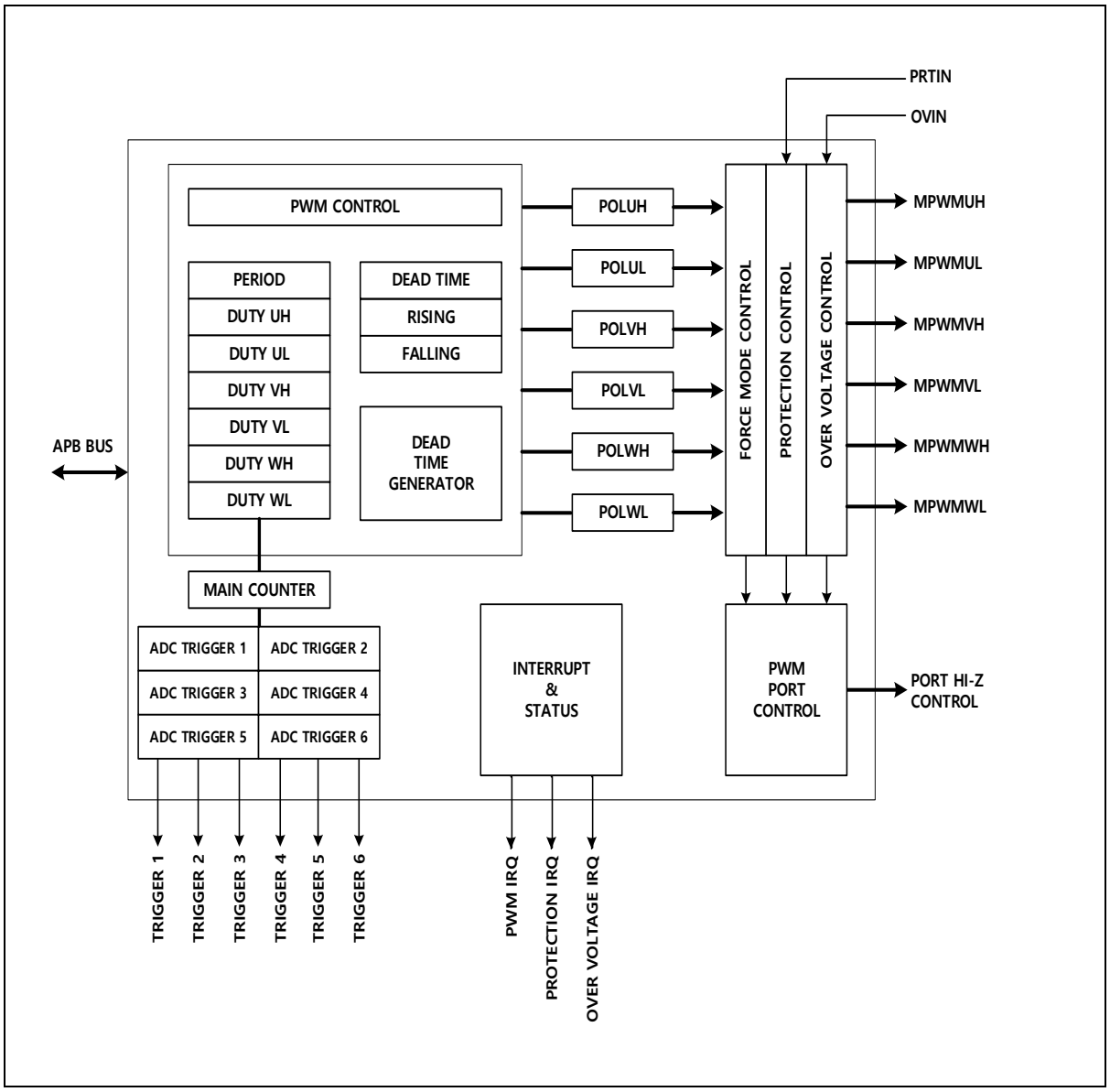


Figure 35. MPWM Block Diagram (Normal Mode)

Figure 36 describes individual mode of MPWM in block diagram.

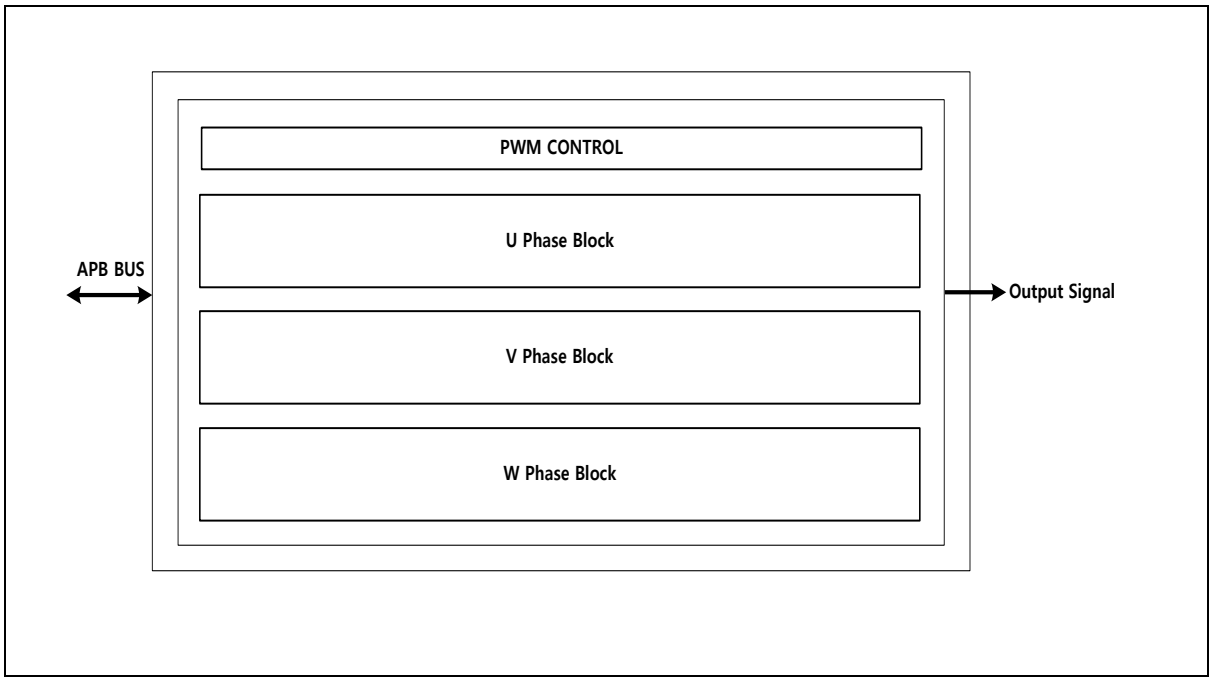


Figure 36. MPWM Block Diagram (Individual Mode)

Figure 37 describes MPWM in block diagram (detailed).

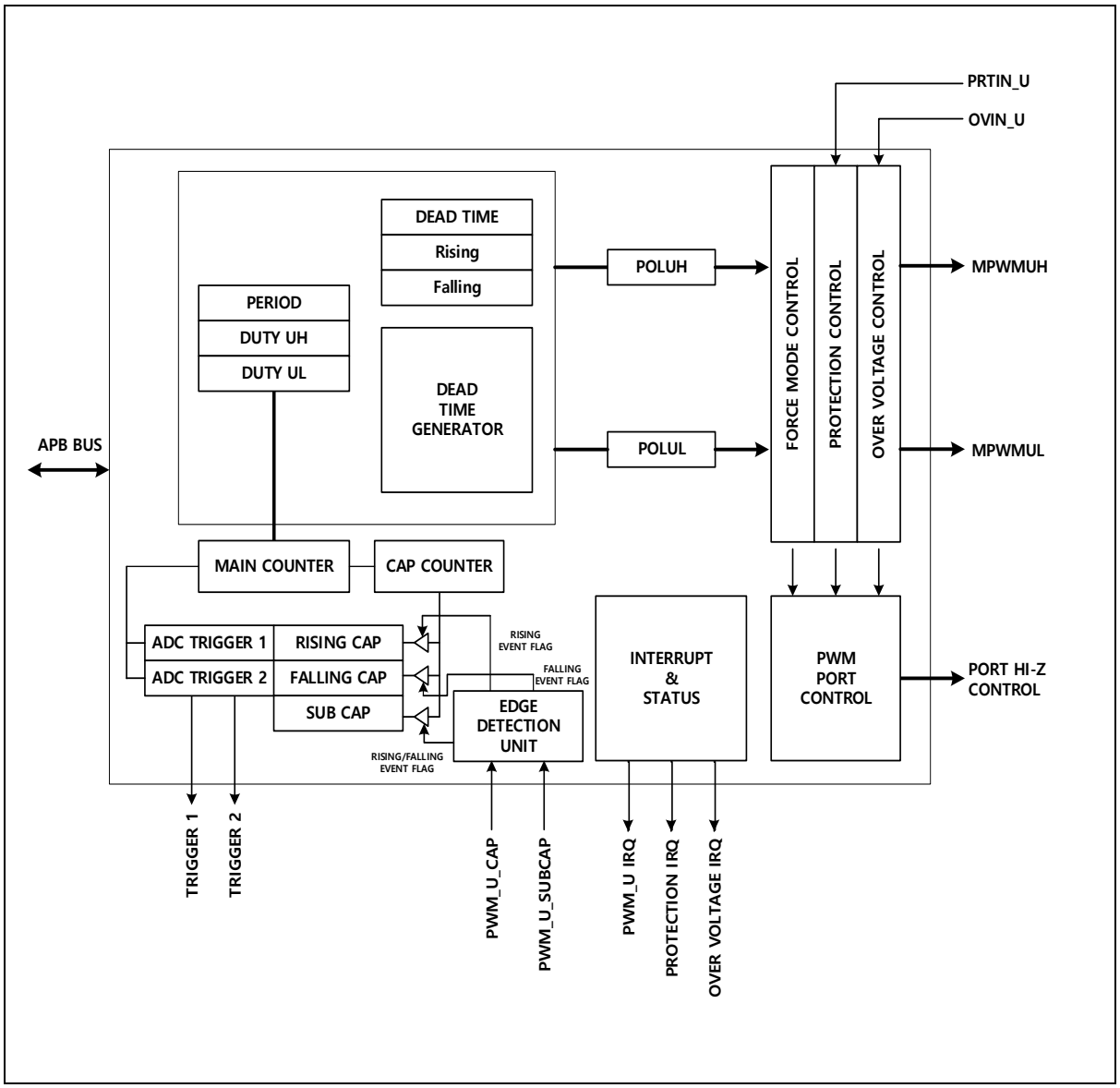


Figure 37. MPWM Block Diagram (Phase U)

NOTE: The figure above represents the phase U block only. The phase V and W blocks are identical to the phase U block. Each phase block is independently configurable; however, the protection and overvoltage interrupts are used in common.

16 Quadrature Encoder Interface (QEI)

The two-channel quadrature encoder interface (QEI) uses two pulse signals outputted from an encoder. By counting the number of relative phase pulses between these two signals, the encoder's rotational position, direction, and velocity are tracked. Additionally, an index signal is used to reset the position counter. Each QEI module consists of a decoder logic interpreting the Ph-A and Ph-B signals and up- and down-counters.

QEI of A34M41x series features the followings:

- Three input pins for two phase signals and index pulse
  - Phases A/B: Input of QEI phases A and B
  - INDEX: Input of QEI index
  - UPDN: Output of phase direction
- 32-bit up-/down-counter counting the number of rotations in each direction
- x2 and x4 count resolution for capture mode
- Position compare register and interrupt
- Index compare register and interrupt
- Velocity capture by a velocity timer
- Signals are selectable
  - Quadrature signals (Ph-A and Ph-B)
  - Clock and direction signals (Clock: Ph-A, direction: Ph-B)

Table 23 introduces pins assigned for QEI interface.

Table 23. Pin Assignment of QEI: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
QEI0_UPDN	O	QEI0 phase direction output port	O	O	O
QEI0_A QEI0_B QEI0_IDX	I	QEI0 phase-A, phase-B, and index input ports	O	O	O
QEI1_UPDN	O	QEI1 phase direction output port	O	O	X
QEI1_A QEI1_B QEI1_IDX	I	QEI1 phase-A, phase-B, and index input ports	O	O	X

16.1 QEI block diagram

Figure 38 describes normal mode of MPWM in block diagram.

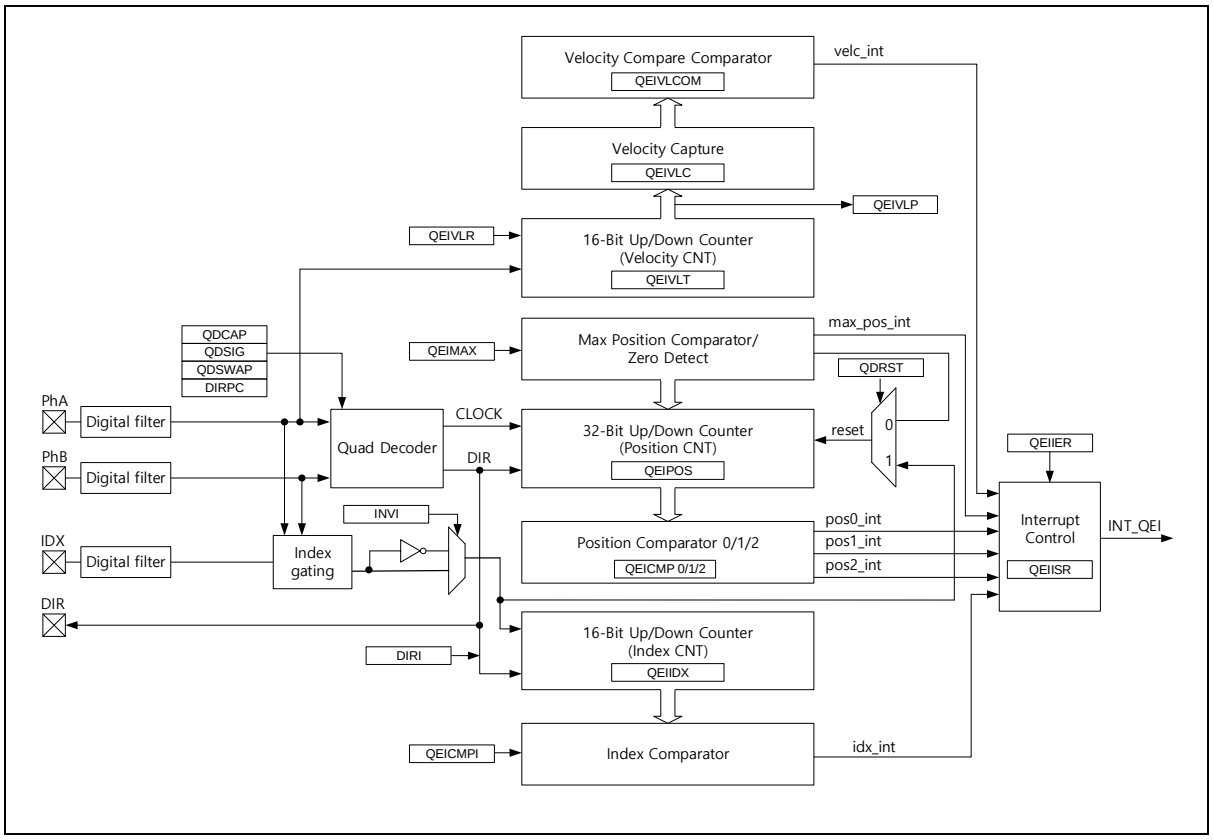


Figure 38. QEI Block Diagram

17 12-bit Analog-to-Digital Converter (ADC)

ADC block of A34M41x series consists of an independent ADC unit featuring the followings:

- 24 Channel Analog Input
- Single mode and Continuous conversion mode
- Maximum 8 sequential conversion support
- Software trigger support
- Three internal trigger source (PWM, TIMER) Support
- Adjustable sample and hold time
- 1.0 V reference voltage (ch. 22) and 1.5 V core voltage (ch. 23)

Table 24 introduces pins assigned for ADC.

Table 24. Pin Assignment of ADC: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
AVDD	P	Analog power (3.0 V to VDD)	O	O	O
AVSS	P	Analog GND	O	O	O
AD0S	O	ADC0 start of conversion	O	O	X
AD0E	O	ADC0 end of conversion	O	O	X
AD1S	O	ADC1 start of conversion	O	O	X
AD1E	O	ADC1 end of conversion	O	O	X
AD2S	O	ADC2 start of conversion	O	O	X
AD2E	O	ADC2 end of conversion	O	O	X
AN0	A	ADC input 0	O	O	O
AN1	A	ADC input 1	O	O	O
AN2	A	ADC input 2	O	O	O
AN3	A	ADC input 3	O	O	O
AN4	A	ADC input 4	O	O	O

Table 24. Pin Assignment of ADC: External Pins (continued)

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
AN5	A	ADC input 5	O	O	O
AN6	A	ADC input 6	O	O	O
AN7	A	ADC input 7	O	O	O
AN8	A	ADC input 8	O	O	O
AN9	A	ADC input 9	O	O	O
AN10	A	ADC input 10	O	O	O
AN11	A	ADC input 11	O	O	O
AN12	A	ADC input 12	O	O	O
AN13	A	ADC input 13	O	O	O
AN14	A	ADC input 14	O	O	O
AN15	A	ADC input 15	O	O	O
AN16	A	ADC input 16	O	O	X
AN17	A	ADC input 17	O	O	X
AN18	A	ADC input 18	O	O	X
AN19	A	ADC input 19	O	O	X
AN20	A	ADC input 20	O	O	X
AN21	A	ADC input 21	O	O	X
AN22	A	ADC input 22	O	O	X
AN23	A	ADC input 23	O	O	X

17.1 12-bit ADC block diagram

In this section, 12-bit ADC is described in a block diagram in Figure 39.

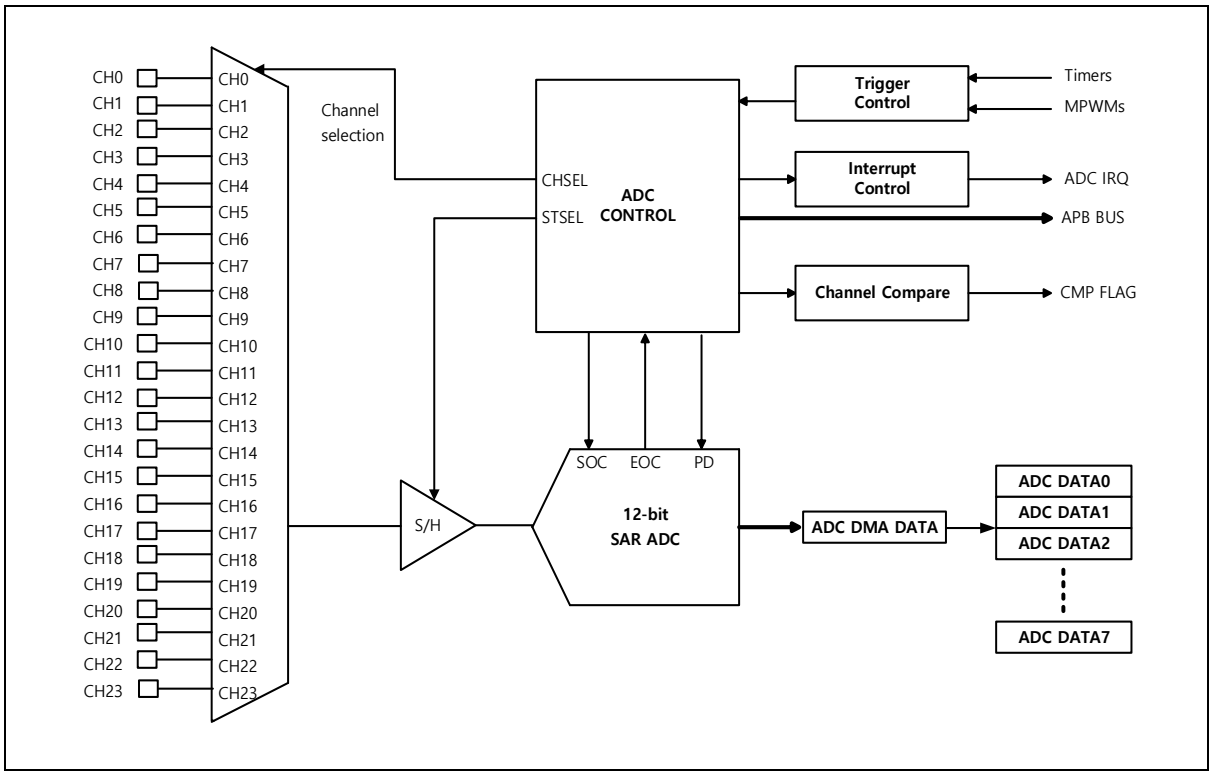


Figure 39. 12-bit ADC Block Diagram

17.2 Internal channel wiring

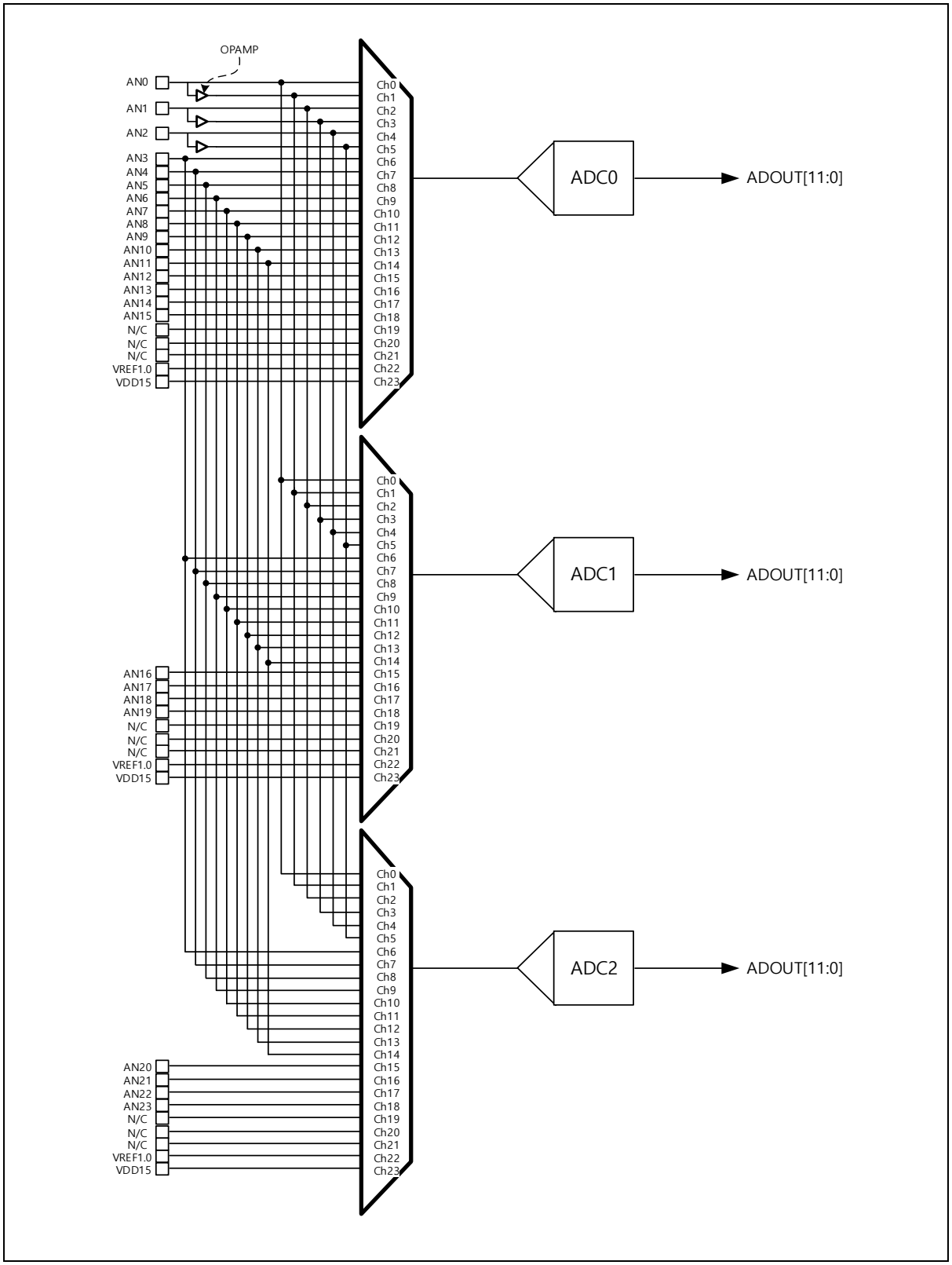


Figure 40. 12-bit ADC Internal Channel Wiring

18 Programmable Gain AMP (PGA)

The following are characteristics of the programmable gain amplifiers (PGAs) built in the A34M41x series. In the PGAn_CR register, the PGA's control signals can be set.

PGA of A34M41x series features the followings:

- Three PGAs
- PGA outputs are used in connection with ADC channels

18.1 PGA block diagram

In this section, PGA is described in a block diagram in Figure 41.

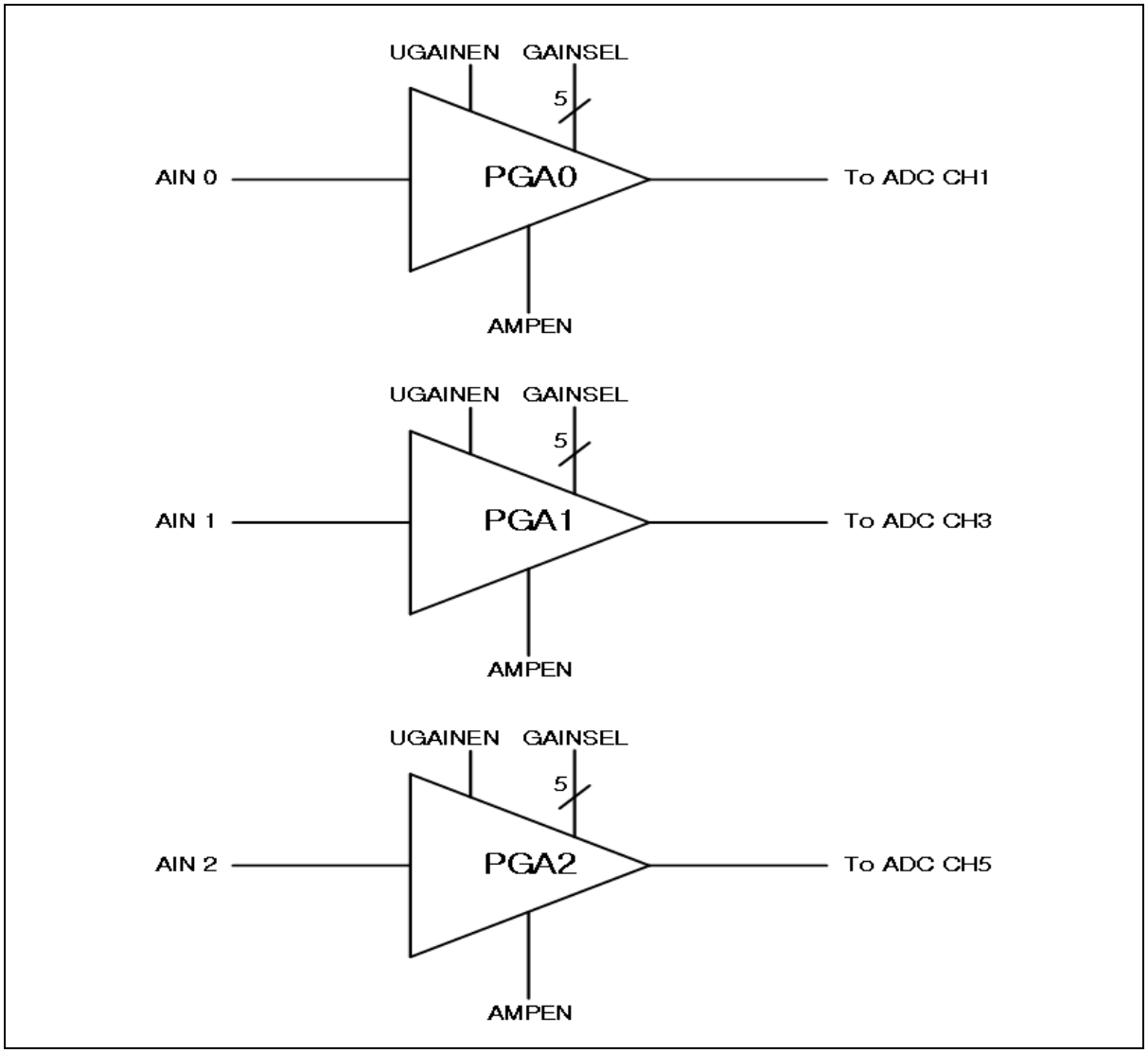


Figure 41. PGA Block Diagram

18.2 Gain table

Table 25. PGA Gain Table

GAIN[4:0]	GAIN
00000	1.200
00001	1.304
00010	1.404
00011	1.500
00100	1.600
00101	1.702
00110	1.805
00111	1.905
01000	2.000
01001	2.182
01010	2.330
01011	2.500
01100	2.667
01101	2.927
01110	3.000
01111	3.158
10000	3.478
10001	3.871
10010	4.000

19 Comparator (COMP)

The A34M41x series is equipped with four comparators. A comparator outputs a signal from its I/O pin or triggers an interrupt based on comparison between the voltages of two analog signals.

You can set comparator control signals with the COMPn_CONF register. The following are major features of the comparator module.

Comparator of A34M41x series features the followings:

- Equipped with comparators 0 and 1, each of which has three input sources (CPA, CPB, and CPC)
- Equipped with comparators 2 and 3, each of which has one input source (CP2/3)
- PGA outputs can be fed to comparators
- Interrupt polarity (falling or rising) selectable

Table 26 introduces pins assigned for Comparator.

Table 26. Pin Assignment of Comparator: External Pins

Pin name	Type	Description	Supported Packages		
			A34M418YL (LQFP-120)	A34M418VL A34M416VL A34M414VL (LQFP-100)	A34M418RL A34M416RL A34M414RL (LQFP-64)
AVDD	P	Analog VDD (3.0 V to VDD)	O	O	O
AVSS	P	Analog GND	O	O	O
CP0A	A	Comparator input 0A	O	O	O
CP0B	A	Comparator input 0B	O	O	O
CP0C	A	Comparator input 0C	O	O	O
CP1A	A	Comparator input 1A	O	O	O
CP1B	A	Comparator input 1B	O	O	O
CP1C	A	Comparator input 1C	O	O	O
CP2	A	Comparator input 2	O	O	X
CP3	A	Comparator input 3	O	O	X
CREF0	A	Comparator reference input 0	O	O	O
CREF1	A	Comparator reference input 1	O	O	O
CREF2	A	Comparator reference input 2	O	O	X
CREF3	A	Comparator reference input 3	O	O	X

19.1 Comparator block diagram

In this section, comp is described in a block diagram in Figure 42.

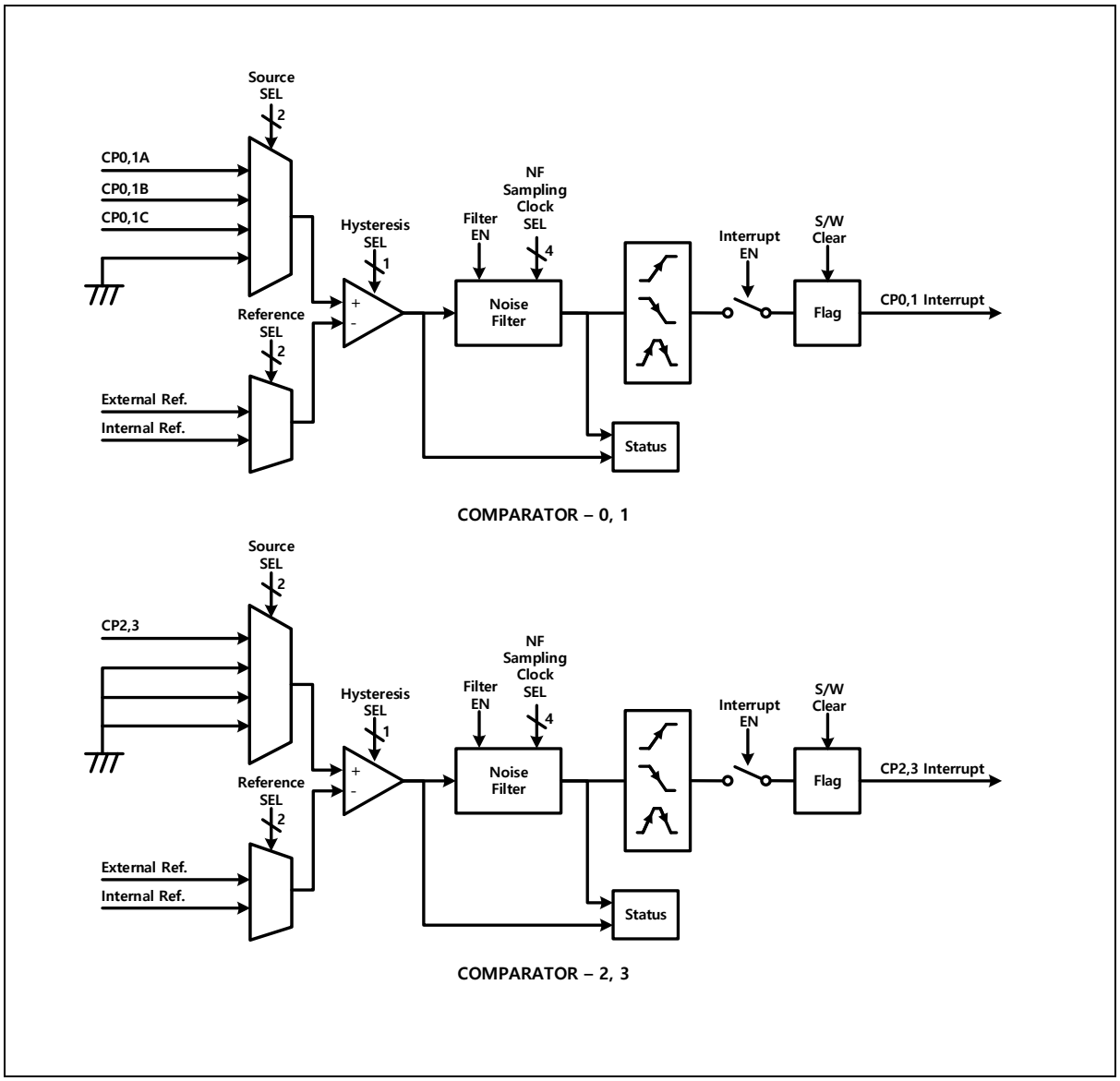


Figure 42. Comparator Block Diagram

20 Advanced Encryption Standard-128 (AES-128)

The A34M41x series has an advanced encryption standard-128 (AES-128) module built in. The AES-128 module is used to encrypt or decrypt data. Below are major features of the AES-128 block.

AES-128 of A34M41x series features the followings:

- Auto-inversion of input and output
- Input and output FIFO flush modes
- Encryption and decryption modes
- Interrupts available
- Compatible with DMA transfers

20.1 AES-128 block diagram

In this section, AES-128 is described in a block diagram in Figure 43.

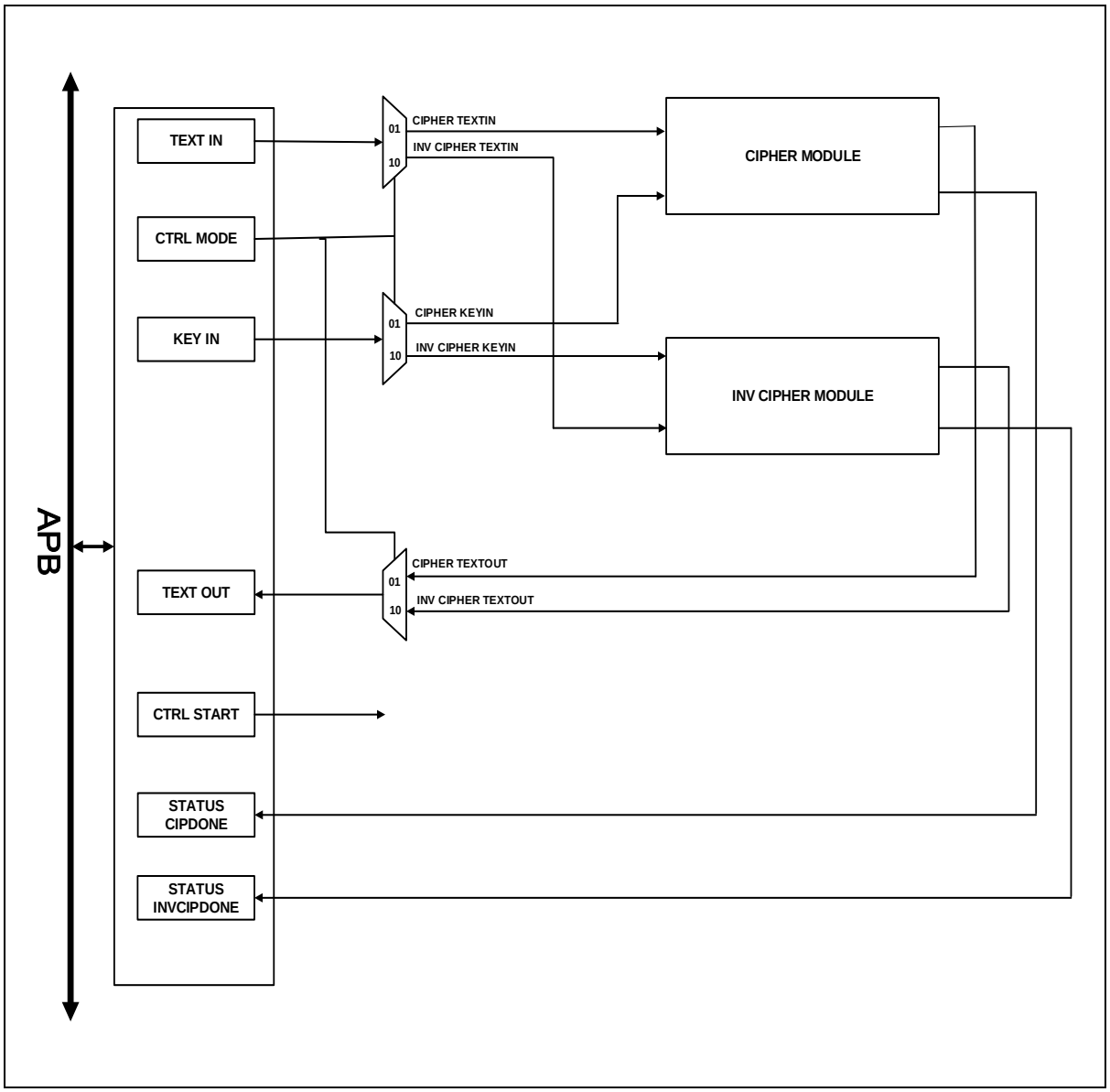


Figure 43. AES-128 Block Diagram

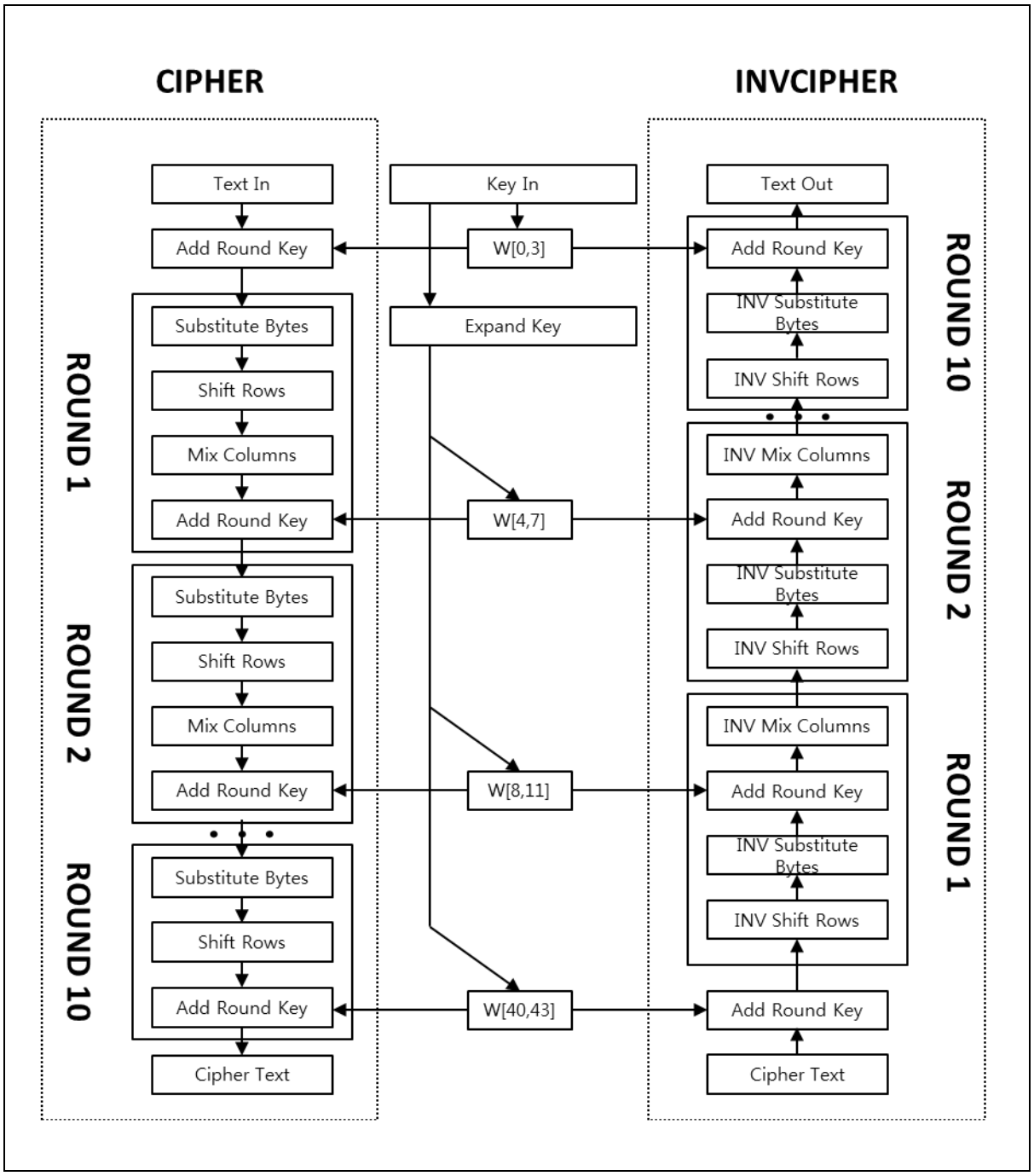


Figure 44. Cipher and Inverse Cipher Flow Diagram

21 Random Number Generator (RNG)

The A34M41x series has a random number generator (RNG) built in. You can choose to select the RNG clock. The RNG generates a random number based on the set seed value. If the user reads data before the generation of a random number is complete, an error interrupt is flagged to prevent the user from reading false data.

RNG of A34M41x series features the followings:

- Generates 32-bit random number data
- Interrupt events:
  - Error interrupt
  - Ready interrupt
- Programmable random number-generating seed

21.1 RNG block diagram

In this section, RNG is described in a block diagram in Figure 45.

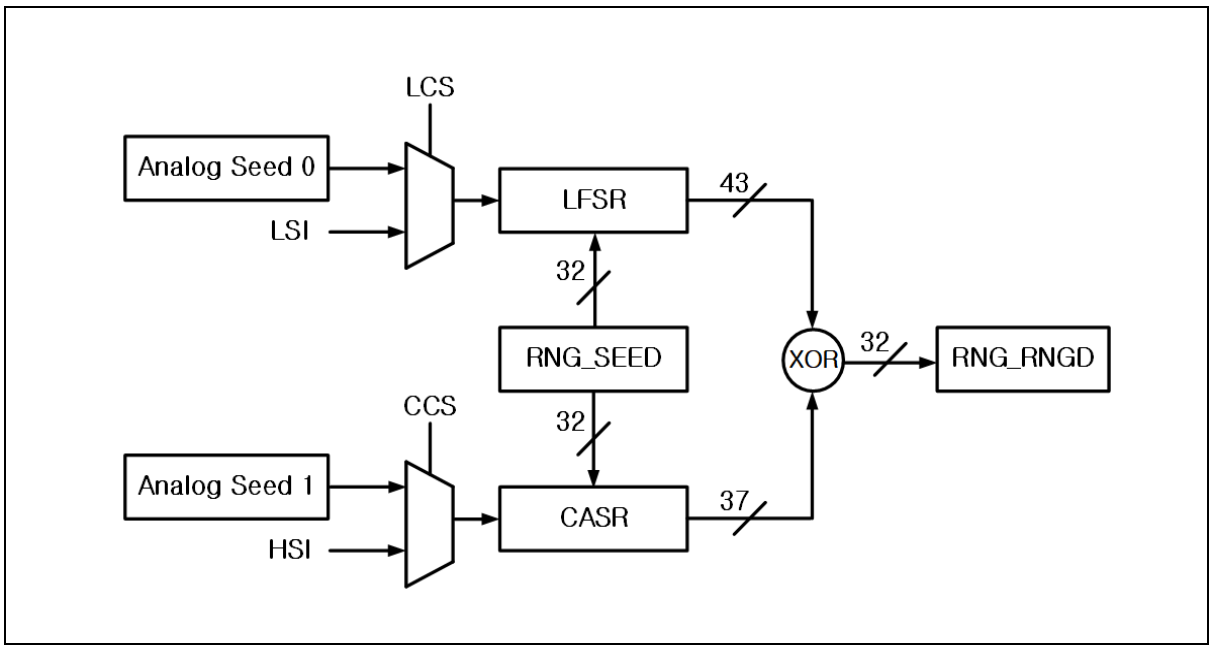


Figure 45. RNG Block Diagram

22 Cyclic Redundancy Check (CRC)

The cyclic redundancy check (CRC) module is used to load 32/16/8/7-bit CRC codes. Application programs employs CRC-based technologies to examine the integrity of data transfers, storages, and flash memories in conformance with functional safety standards.

CRC of A34M41x series features the followings:

- Automatic CRC and user CRC modes
- Handles 8-, 32-bit data size
- Input buffer to avoid bus stall during calculation
- CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size
- Reversibility option on I/O data

22.1 CRC block diagram

In this section, CRC is described in a block diagram in Figure 46.

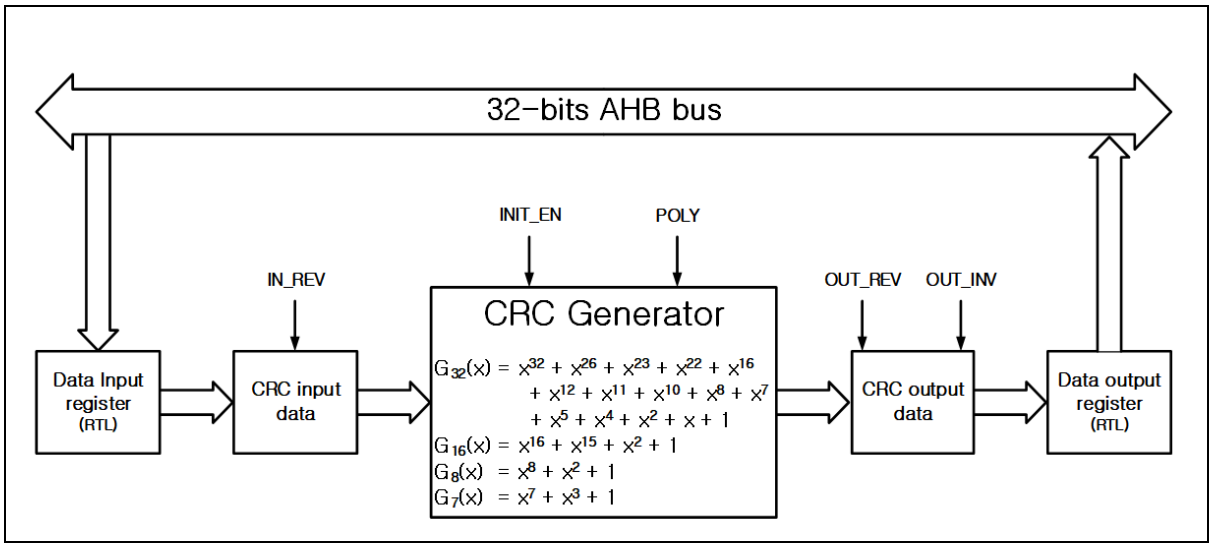


Figure 46. CRC Block Diagram

23 Electrical characteristics

23.1 Absolute maximum ratings

Absolute maximum ratings are limiting values of operating and environmental conditions which should not be exceeded under the worst possible conditions.

Table 27. Absolute Maximum Rating

Parameter	Symbol	Ratings	Unit	Remark
Supply Voltage	VDD	-0.5 – +6	V	—
Normal Pin	V_I	-0.5 – VDD+0.5	V	Voltage on any pin with respect to VSS
	V_O	-0.5 – VDD+0.5	V	
	I_{OH}	10	mA	Maximum current output sourced by (I_{OH} per I/O pin)
	ΣI_{OH}	120	mA	Maximum current (ΣI_{OH})
	I_{OL}	20	mA	Maximum current sunk by (I_{OL} per I/O pin)
	ΣI_{OL}	120	mA	Maximum current (ΣI_{OL})
	I_{IH}	1	uA	Maximum current (I_{IH})
	I_{IL}	1	uA	Maximum current (I_{IL})
Input main clock range	—	4-16	MHz	—
Storage Temperature	T_{STG}	-55 – +125	℃	—
Operating Temperature	Top	-40-+85	℃	—

23.2 Recommended operating conditions

Table 28. Recommended Operating Condition

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	Unit
Supply Voltage	VDD	—	2.7	—	5.5	V
	AVDD	—	2.7	—	5.5	V
Operating Frequency	FREQ	HSE	4	—	16	MHz
		LSE	—	32.768	—	KHz
		HSI	31.04	32	32.96	MHz
		LSI500KHz	400	500	600	KHz
Operating Temperature	Top	Top	-40	—	+85	℃

NOTE: ADC, OP-AMP dedicated voltage.

23.3 ADC characteristics

Table 29. ADC Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Operating voltage	AVDD	—	2.7	5	5.5	V
Resolution		—	—	—	12	Bit
Operating current	IDDA	AVDD = 5.0VA @f_{MCLK} = 25MHz	—	1.6	—	mA
Analog input range	V_{AN}	—	VSS	—	AVDD	V
Conversion time	t_{CONV}	—	14*MCLK	-	44*MCLK	us
Conversion rate	F_{CONV}	@AVDD > 3.6V	—	—	1.5	MHz
		@AVDD > 3.0V	—	—	1	MHz
		@AVDD > 2.7V	—	—	0.5	MHz
Operating frequency	ACLK	—	—	—	25	MHz
DC accuracy	INL	—	—	—	±4	LSB
	DNL	—	—	—	±2	LSB
Zero offset error	ZOE	TBD	—	±4	—	LSB
Full scale error	FSE	TBD	—	±4	—	LSB

23.4 Power on reset characteristics

Table 30. POR Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating current	I_{DD}	—	—	0.5	4	uA
POR set level	V_{set}	—	1.05	1.20	1.35	V
VDD Voltage Rising Time	t_R	—	0.05	—	30.0	V/ms
POR reset level	V_{reset}	—	1.00	1.10	1.20	V

23.5 Low voltage reset characteristics

Table 31. Low Voltage Reset Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	0.8	5.0	5.5	V
Detection level	V_{LVR}	T_A = –40˚C to +85˚C, Falling voltage	1.52	1.60	1.68	V
			1.61	1.69	1.77	
			1.69	1.78	1.87	
			1.81	1.90	2.00	
			1.89	1.99	2.09	
			2.01	2.12	2.23	
			2.19	2.30	2.42	
			2.35	2.47	2.59	
			2.54	2.67	2.80	
			2.89	3.04	3.19	
			3.02	3.18	3.34	
			3.41	3.59	3.77	
			3.53	3.72	3.91	
			3.83	4.03	4.23	
			3.99	4.20	4.41	
			4.26	4.48	4.70	
Hysteresis	—		—	100	200	mV
Noise cancelling time	—		—	2	—	us
Operation current	I_{DD}		—	3.5	5	uA
Operation current(STOP)	$I_{DD, STOP}$		—	2.5	3	nA

23.6 Low voltage indicator characteristics

Table 32. Low Voltage Indicator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	0.8	5.0	5.5	V
Detection level	V_{LVI}	T_A = –40°C to +85°C, Falling voltage	1.52	1.60	1.68	V
			1.61	1.69	1.77	
			1.69	1.78	1.87	
			1.81	1.90	2.00	
			1.89	1.99	2.09	
			2.01	2.12	2.23	
			2.19	2.30	2.42	
			2.35	2.47	2.59	
			2.54	2.67	2.80	
			2.89	3.04	3.19	
			3.02	3.18	3.34	
			3.41	3.59	3.77	
			3.53	3.72	3.91	
			3.83	4.03	4.23	
			3.99	4.20	4.41	
			4.26	4.48	4.70	
Hysteresis	—		—	100	200	mV
Noise cancelling time	—		—	2	—	us
Operation current	I_{DD}		—	3.5	5	uA
Operation current(STOP)	$I_{DD, STOP}$		—	2.5	3	nA

23.7 Comparator characteristics

Table 33. Comparator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.0	—	5.5	V
Input offset voltage	V_{OS}	V_{DD} = 4.5 V, V_{IN} = 1/2 V_{DD} Before offset calibration	—	10	20	mV
		V_{DD} = 4.5 V, V_{IN} = 1/2 V_{DD} Before offset calibration	—	—	5	mV
		Reflects trim error when using BGREF_1V_EXT_S.	—	—	20	mV
Hysteresis	V_{HYS}	V_{DD} = 4.5 V, HYSSEL = 0	—	5	25	mV
		V_{DD} = 4.5 V, HYSSEL = 1	—	20	60	mV
Comparator current	I_{CMP}	V_{DD} = 4.5 V	—	70	100	uA

23.8 High frequency internal RC oscillator characteristics

Table 34. High Frequency Internal RC Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		2.7	—	5.5	V
Operating current	I_{HIRC}	—	—	120	—	uA
Operating frequency	f_{32M}	—	31.04	32	32.96	MHz
	f_{16M}	—	15.52	16	16.48	MHz
Frequency error	f_E	@ 25°C	-1.2	—	1.2	%
		@ 0°C to +85°C	-3	—	3	%
		@ -40°C to 0°C	-10	—	+10	%

23.9 Low frequency internal RC oscillator characteristics

Table 35. Low Frequency (500KHz) Internal RC Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD		2.7	—	5.5	V
Operating current	I_{LIRC}	Enable	—	1.5	2	uA
		Disable	—	1	20	nA
Frequency	f_{LIRC}	VDD = 1.8V to 5.5V	400	500	600	KHz
Stabilization time	t_{LFS}	—	—	100		us

23.10 Programmable gain amp characteristics

Table 36. Programmable Gain Amp Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	—	2.7	—	5.5	V
Operating current	I_{PGA}	AV_{DD} = 5 V, 25°C	—	800	—	uA
Gain error	G_E	@ Gain = 1 ~ 4	-3		3	%
Common mode rejection ratio	CMRR	—	110	—	—	dB
Power supply rejection ratio	PSRR	—	80	—	—	dB
Gain bandwidth	f_{GB}	CL=20pF		16		MHz
Open loop voltage gain	A_V	—	—	89	—	dB
Enable time on	t_{ON}	—	—	2	—	Us

23.11 DC electrical characteristics

Table 37. DC Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH}	PA,PB,PC,PD,PE,PF,PG,nRESET, nBOOT	0.8VDD	—	—	V
Input low voltage	V_{IL}	PA,PB,PC,PD,PE,PF,PG,nRESET, nBOOT	—	—	0.2VDD	V
Output high voltage	V_{OH}	VDD=5V, I_{OH} = – 3mA	VDD-1.0	—	—	V
Output low voltage	V_{OL}	VDD=5V, I_{OL}=3mA	—	—	1.0	V
Output Low Current	I_{OL}	—	—	—	3	mA
Output High Current	I_{OH}	—	-3	—	—	mA
Input high leakage current	I_{IH}	All Input ports	—	—	4	uA
Input low leakage current	I_{IL}	All Input ports	– 4	—	—	uA
Pull-up resistor	R_{PU}	R_{MAX}:V_{DD}=3.0V R_{MIN}:V_{DD}=5V	30	—	70	KΩ

23.12 Supply current characteristics

Table 38. Supply Current Characteristics

(Temperature: -40 to +85℃)

Parameter	Symbol	Condition	Min	Typ.	Max	unit
Normal operation	IDD_{RUN}	LSI=RUN/ HSI=RUN/ HSE=8MHz LSE=32.768KHz/ MCLK=LSI	—	11	—	mA
Normal operation	IDD_{RUN}	LSI=RUN/ HSI=RUN/ HSE=8MHz LSE=32.768KHz/ MCLK=HSI	—	40	—	mA
Normal operation	IDD_{RUN}	LSI=RUN/ HSI=RUN/ HSE=8MHz LSE=32.768KHz/ MCLK=HSE	—	3.9	—	mA
Normal operation	IDD_{RUN}	LSI=RUN/ HSI=RUN/ HSE=8MHz LSE=32.768KHz/ MCLK=LSE	—	1.3	—	mA
Sleep mode	IDD_{SLEEP}	LSI=RUN/ HSI=STOP/ HSE =STOP LSE=STOP/ HCLK=LSI	—	6.3	—	mA
Sleep mode	IDD_{SLEEP}	LSI=STOP/ HSI=RUN/ HSE=STOP LSE=STOP/ HCLK=HSI	—	21	—	mA
Sleep mode	IDD_{SLEEP}	LSI=STOP/ HSI=STOP/ HSE=RUN LSE=STOP/ HCLK=HSE	—	4	—	mA
Sleep mode	IDD_{SLEEP}	LSI=STOP/ HSI=STOP/ HSE=STOP LSE=RUN/ HCLK=LSE	—	1.2	—	mA
Deep-sleep mode	IDD_{STOP}	VDC=STOP/ LVD=RUN	—	120	3,000	uA
Deep-sleep mode	IDD_{STOP}	VDC=STOP/ LVD=STOP	—	110	3,000	uA

NOTES: In deep-sleep mode, all clocks are disabled.

23.13 Internal flash ROM characteristics

Table 39. Code Flash Memory Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Read access time	t_{AC}	–	30	–	–	ns
Read cycle time	t_{AAD}	–	40	–	–	ns
Program time	t_{PROG}	–	–	–	30	us
Page erase time	t_{SER}	–	–	–	4	ms
Macro erase time	t_{MER}	–	–	–	8	ms
Endurance of write/erase	N_{FWE}	T_A=25 °C, Page unit	10,000	–	–	Times
Retention time	t_{FRT}	–	10	–	–	Years

Table 40. Data Flash Memory Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Read access time	t_{AC}	–	30	–	–	ns
Read cycle time	t_{AAD}	–	40	–	–	ns
Program time	t_{PROG}	–	–	–	30	us
Page erase time	t_{SER}	–	–	–	4	ms
Macro erase time	t_{MER}	–	–	–	8	ms
Endurance of write/erase	N_{FWE}	T_A=25 °C, Page unit	100,000	–	–	Times
Retention time	t_{FRT}	–	10	–	–	Years

23.14 Main oscillator characteristics

Table 41. Main Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Oscillator	Parameter	Conditions	Min	Typ.	Max	Units
Operating voltage	VDD	—	1.8	5.0	5.5	V
Operating current	IDD	—	—	—	2.5	mA
Power down current	I_{STOP}	—	—	0.2	30	nA
Output frequency	XOUT input frequency	VDDEXT≥1.8V NOTE1	1.0	—	4.0	MHz
		VDDEXT≥2.0V NOTE2	1.0	—	8.0	MHz
		VDDEXT≥2.2V NOTE3	1.0	—	12.0	MHz
		VDDEXT≥2.4V NOTE4	1.0	—	16	MHz
Crystal input (low)	V_{IL}	—	—	—	0.2VDD	V
Crystal input (high)	V_{IH}	—	0.8VDD	—	—	V
Crystal out (low)	V_{OL}	—	—	—	0.2VDD	V
Crystal out (high)	V_{OH}	—	0.8VDD	—	—	fff
External load cap	C_L	1M<f_{OUT}<4M	18	30	35	pf
		4M<f_{OUT}<12M	10	22	30	pf
		12M<f_{OUT}<16M	7	18	22	pf
Feedback resistance	R_{FB}	VDDEXT=5V	0.7	1.0	1.3	MΩ

NOTES:

1. EISEL = 0x3, ENFSEL = 0x0
2. EISEL = 0x2, ENFSEL = 0x1
3. EISEL = 0x1, ENFSEL = 0x2
4. EISEL = 0x0, ENFSEL = 0x3

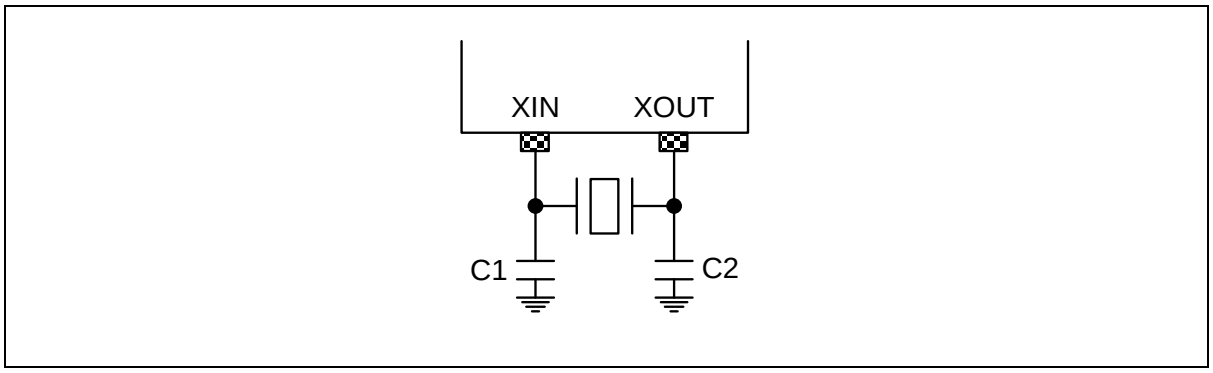


Figure 47. Crystal/Ceramic Oscillator

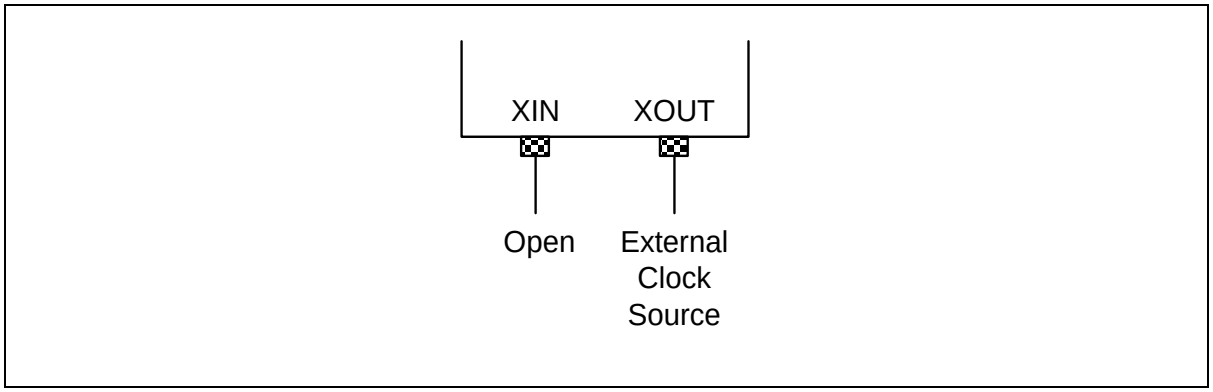


Figure 48. External Clock

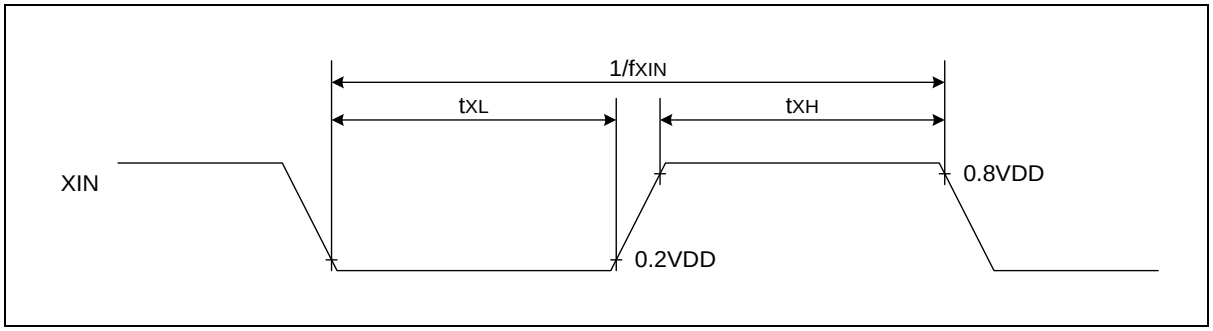


Figure 49. Clock Timing Measurement at XIN

23.15 Sub oscillator characteristics

Table 42. Sub Oscillator Characteristics

(Temperature: -40℃ to +85℃)

Oscillator	Parameter	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	–	2.7	5.0	5.5	V
Operating current	IDD	–	–	3	5	uA
Power down current	I_{STOP}	–	–	0.2	15	nA
Output frequency	f_{SUB}	–	–	32.768	–	KHz
Crystal input (low)	V_{IL}	–	–	–	0.2VDD	V
Crystal input (High)	V_{IH}	–	0.8VDD	–	–	V
Crystal out (low)	V_{OL}	–	–	–	0.2VDD	V
Crystal out (high)	V_{OH}	–	0.8VDD	–	–	fff
External load cap	R_{FB}	–	5	15	35	pF
Feedback resistance	C_L	–	7	12	24	MΩ

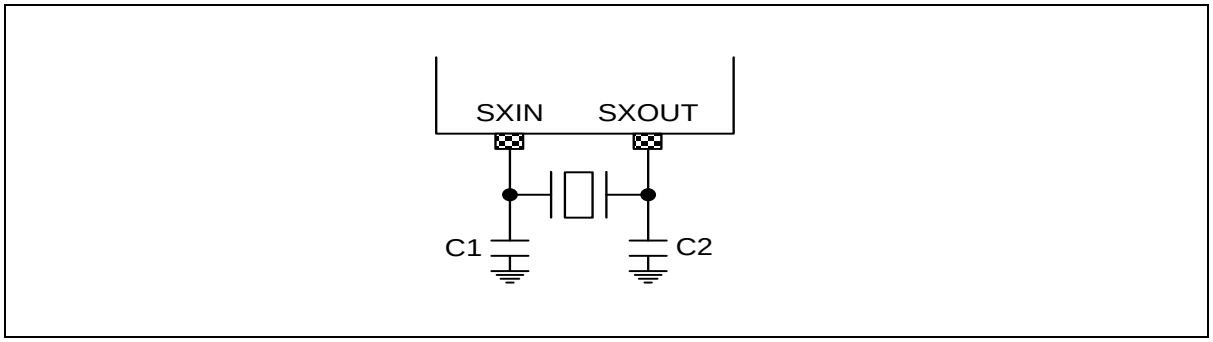


Figure 50. Crystal Oscillator

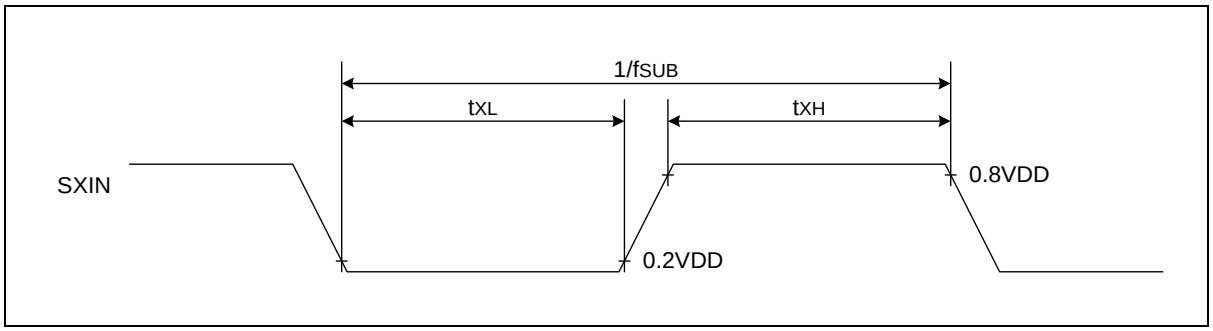


Figure 51. Clock Timing Measurement at SXIN

23.16 PLL electrical characteristics

Table 43. PLL Electrical Characteristics

(Temperature: -40℃ to +85℃)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Operating voltage	VDD	–	2.7	–	5.5	V
Operating current	I_{DD}	–	–	0.5	1	mA
Output frequency	f_{OUT}	–	48	–	120	MHz
VCO frequency	f_{VCO}	–	50	–	200	MHz
Duty	f_{DUTY}	–	40	–	60	%
Input frequency	$f_{PLLINCLK}$	–	4	8	10	MHz
P-P jitter	t_{JITTER}	@Lock State	–	–	500	ps

24 Development tools

This chapter introduces wide range of development tools for A34M41x. ABOV offers software tools, debuggers, and programmers to help a user in generating right results to match target applications. ABOV supports entire development ecosystem of the customers.

24.1 Compiler

ABOV semiconductor does not provide any compiler for A34M41x. However, since A34M41x have ARM's high-speed 32-bit Cortex-M4F Cores for their CPU, you can use all kinds of third party's standard compiler such as Keil C Compiler. These compilers' output debug information can be integrated with our A-Link and A-Link Pro. Please visit our website www.abovsemi.com for more information regarding the A-Link and A-Link Pro.

24.2 Debugger

The A-Link and A-Link Pro support ABOV Semiconductor's A34M41x MCU emulation in SWD Interface. The A-Link and A-Link Pro use two wires interfacing between PC and MCU, which is attached to user's system. The A-Link and A-Link Pro can read or change the value of MCU's internal memory and I/O peripherals. In addition, the A-Link and A-Link Pro control MCU's internal debugging logic. This means A-Link and A-Link Pro control emulation, step run, monitoring and many more functions regarding debugging.

The A-Link and A-Link Pro run underneath MS operating system such as MS-Windows NT/ 2000/ XP/ Vista/ 7/ 8/ 8.1/ 10 (32-bit, 64-bit).

Programming information using the A-Link and A-Link Pro are provided in Figure 52. More detailed information about the A-Link and A-Link Pro, please visit our website www.abovsemi.com and download the debugger S/W and documents.

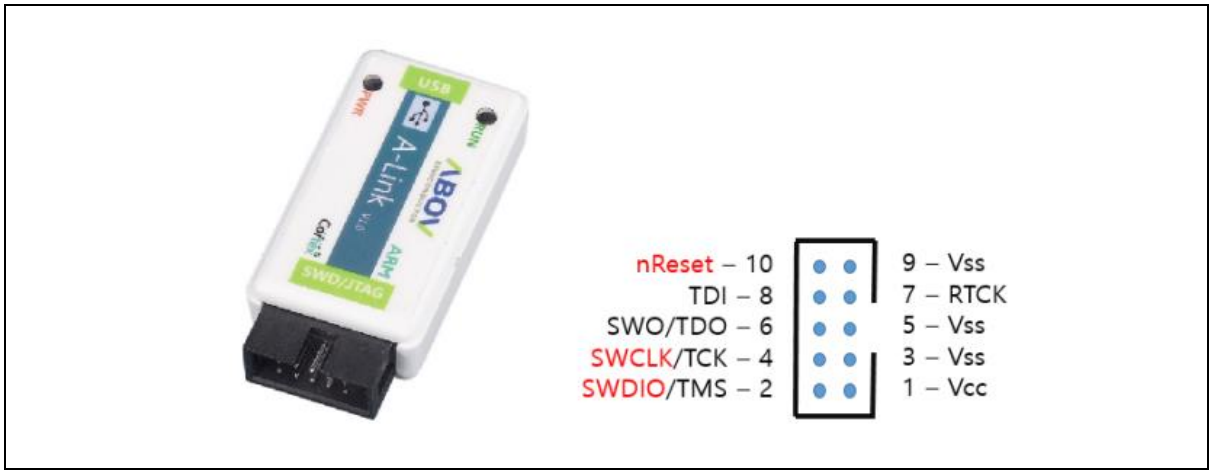


Figure 52. A-Link and Pin Descriptions

24.3 Programmer

24.3.1 E-PGM+

E-PGM+ is a single programmer, and allows a user to program on the device directly.

- Support ABOV devices
- 2~5 times faster than S-PGM+
- Main controller: 32-bit MCU @ 72MHz
- Buffer memory: 1MB

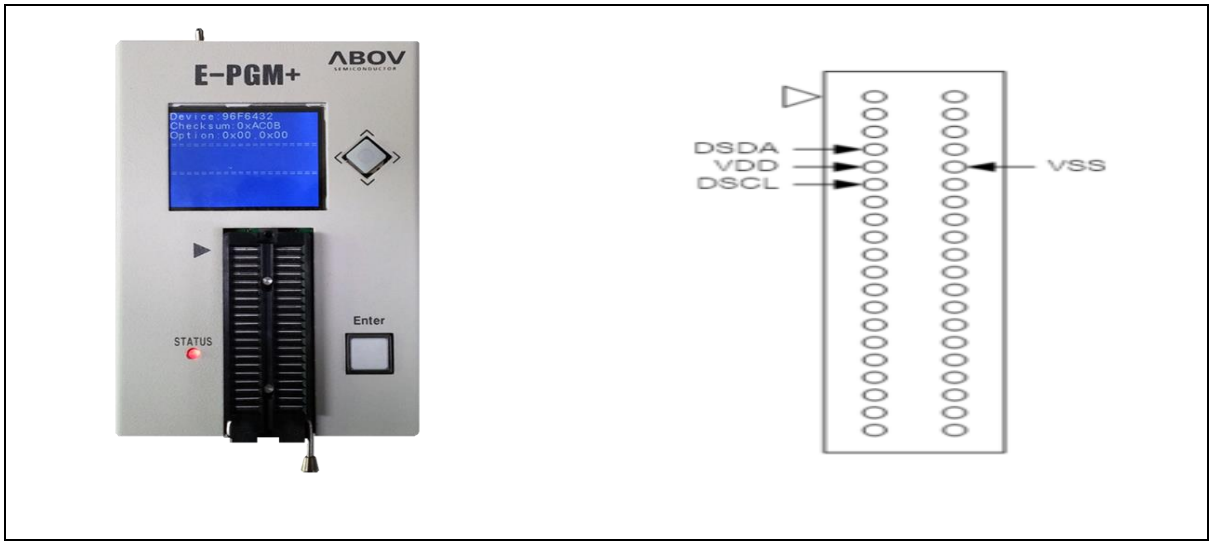


Figure 53. E-PGM+ (Single Writer) and Pin Descriptions

24.3.2 Gang programmer

E-Gang4 and E-Gang6 allows a user to program on multiple devices at a time. They run not only in PC controlled mode but also in standalone mode without PC control. USB interface is available and it is easy to connect to the handler.

Figure 54. E-Gang4 and E-Gang6 (for Mass Production)

24.4 SWD debug mode and E-PGM+ connection

Connections for SWD debugger interface or E-PGM+ is described in Figure 55.

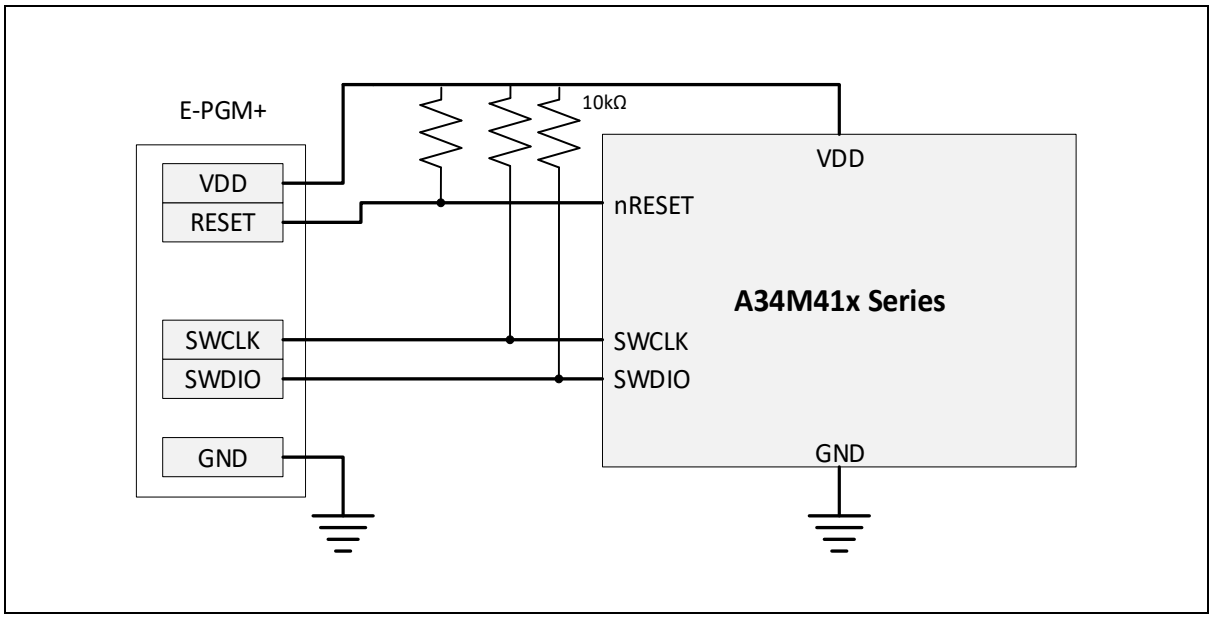


Figure 55. Connection between A34M41x Series and E-PGM+ using SWD Debugger Interface

25 Package information

This chapter provides A34M41x series package information.

25.1 120 LQFP package information

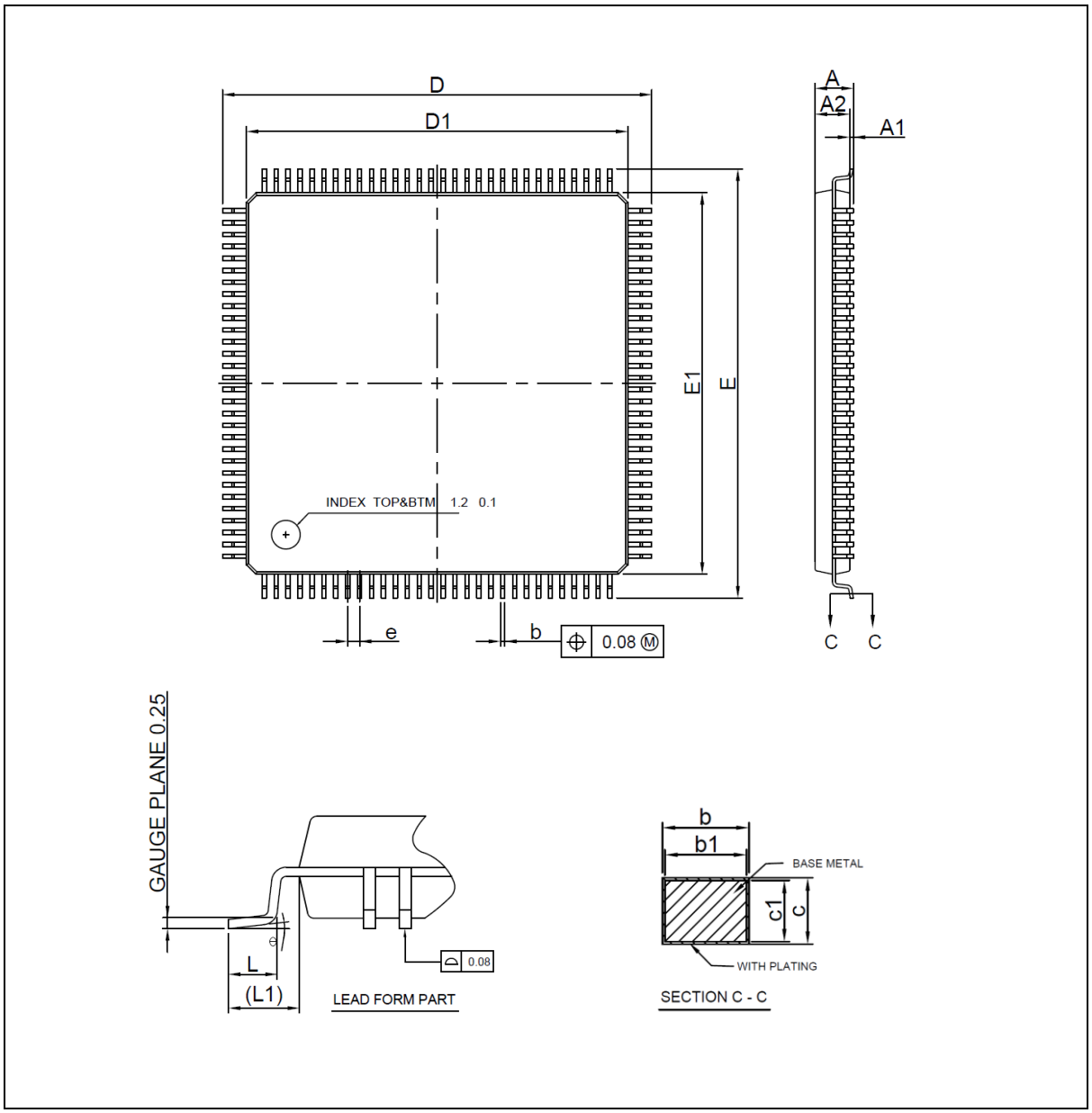


Figure 56. 120 LQFP Package Outline

Table 44. 120 LQFP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	–	0.20
c1	0.09	–	0.16
D	17.80	18.00	18.20
D1	15.80	16.00	16.20
E	17.80	18.00	18.20
E1	15.80	16.00	16.20
e	0.50 BSC		
L	0.35	0.50	0.65
L1	1.00 REF		
Θ	0°	4°	8°

NOTES:

1. All dimension refer to JEDEC standard MS-026-BCD.
2. Dimensions ‘D1’ and ‘E1’ do not include MOLD PROTRUSION. Allowable PROTRUSION is 0.25 mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including MOLD MISMATCH.
3. Dimension ‘b’ does not include DAMBAR PROTRUSION. Allowable DAMBAR PROTRUSION shall not cause the LEAD width to exceed the maximum ‘b’ dimension by more than 0.08 mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

25.2 100 LQFP package information

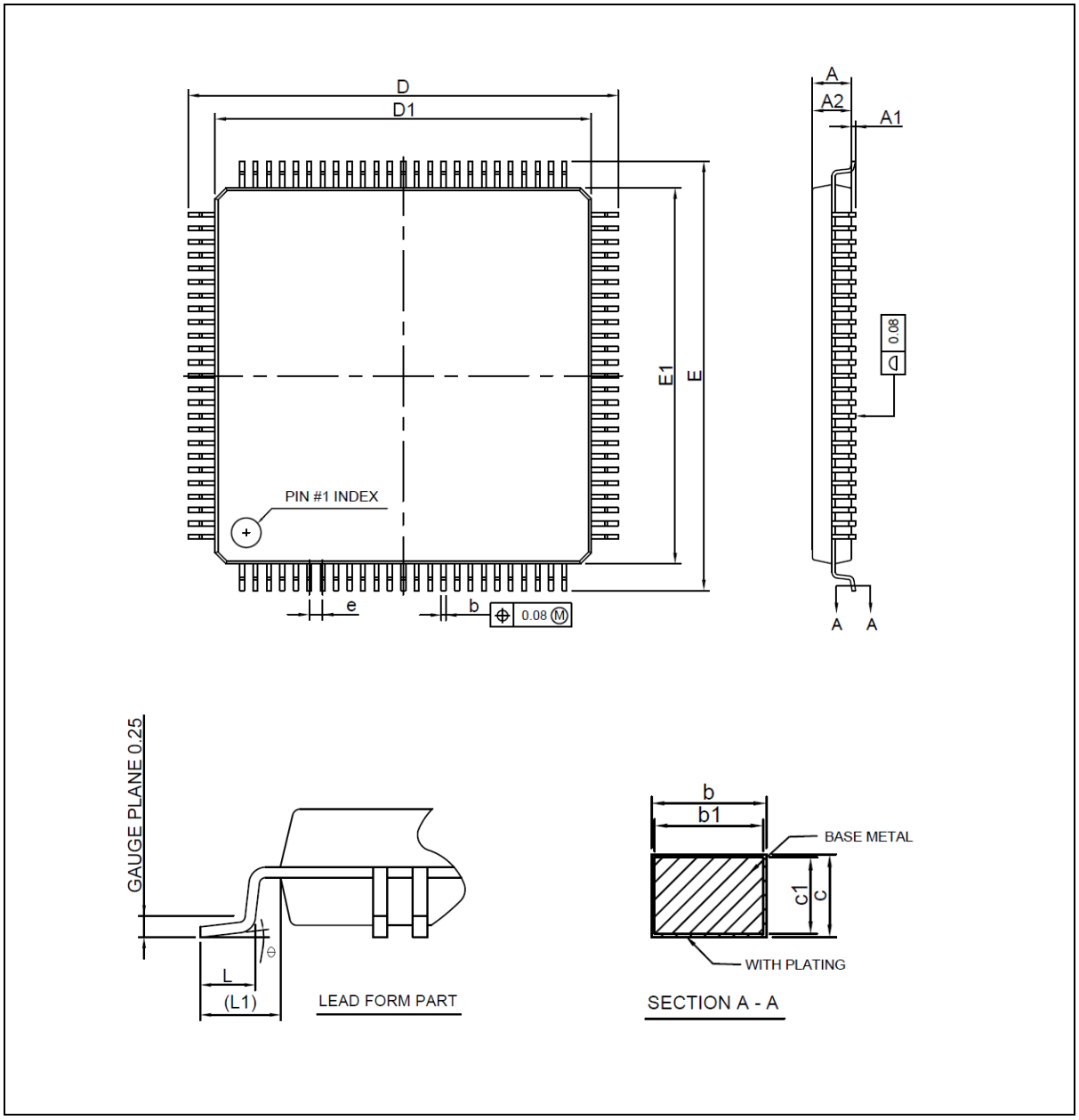


Figure 57. 100 LQFP Package Outline

Table 45. 100 LQFP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	–	0.20
c1	0.09	–	0.16
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimension refer to JEDEC standard MS-026-BCD.
2. Dimensions ‘D1’ and ‘E1’ do not include MOLD PROTRUSION. Allowable PROTRUSION is 0.25 mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including MOLD MISMATCH.
3. Dimension ‘b’ does not include DAMBAR PROTRUSION. Allowable DAMBAR PROTRUSION shall not cause the LEAD width to exceed the maximum ‘b’ dimension by more than 0.08 mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

25.3 64 LQFP package information

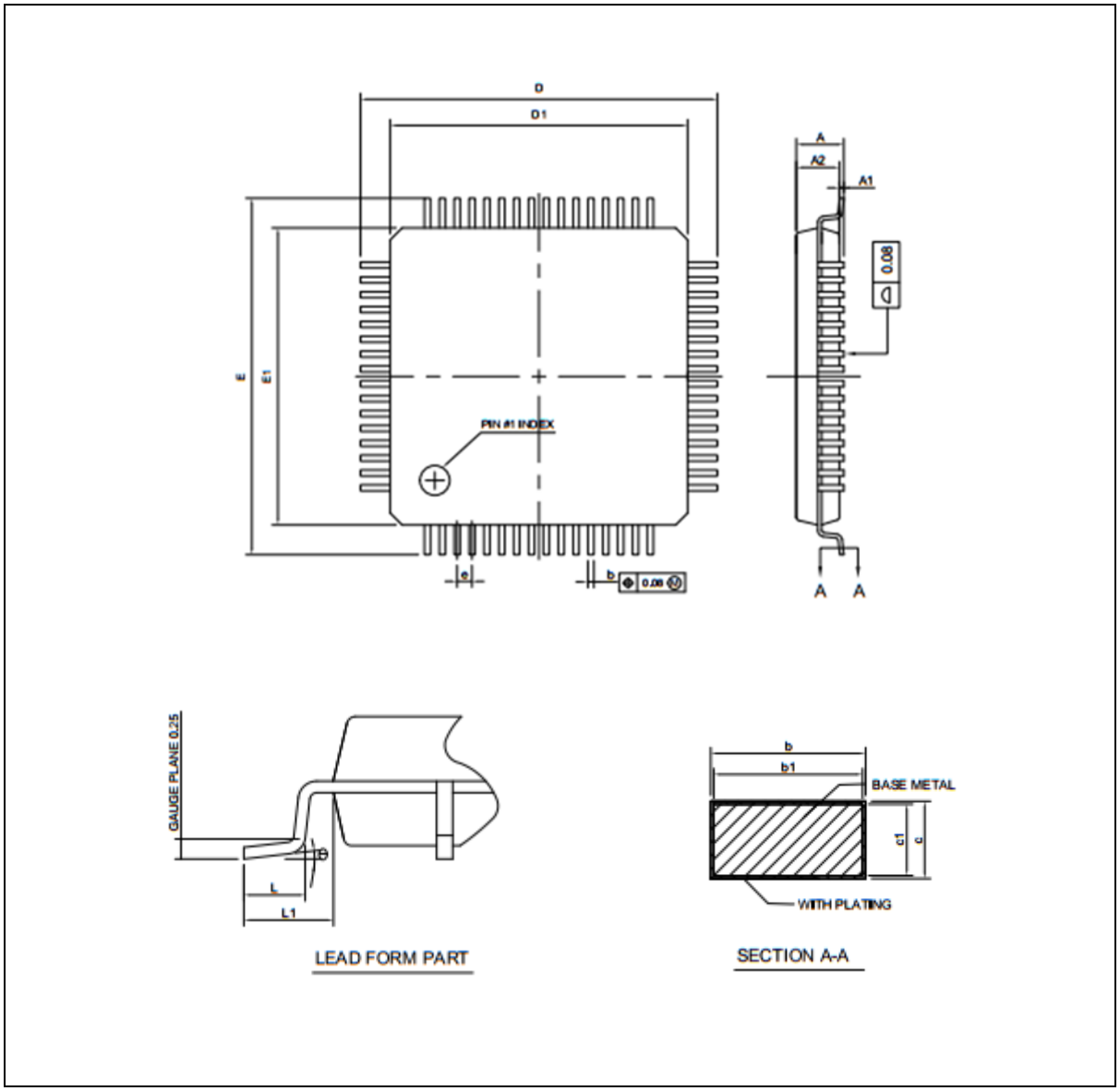


Figure 58. 64 LQFP Package Outline

Table 46. 64 LQFP Package Mechanical Data

Symbol	Dimension (mm)		
	Min.	Nom.	Max.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	–	0.20
c1	0.09	–	0.16
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
Θ	0°	3.5°	7°

NOTES:

1. All dimension refer to JEDEC standard MS-026-BCD.
2. Dimensions ‘D1’ and ‘E1’ do not include MOLD PROTRUSION. Allowable PROTRUSION is 0.25 mm per side. ‘D1’ and ‘E1’ are maximum plastic body size dimensions including MOLD MISMATCH.
3. Dimension ‘b’ does not include DAMBAR PROTRUSION. Allowable DAMBAR PROTRUSION shall not cause the LEAD width to exceed the maximum ‘b’ dimension by more than 0.08 mm.
4. ‘A1’ is defined as the distance from the seating plane to the lowest point on the package body.

26 Ordering information

Table 47. A34M41x Series Device Ordering Information

Device name	Flash	SRAM	SPI	UART	I2C	MPWM	ADC	I/O ports	Package
A34M418YL	512KB	64KB	3	6	2	2	24	107	LQFP-120
A34M418VL	512KB	64KB	2	6	2	2	24	89	LQFP-100
A34M418RL	512KB	64KB	1	3	1	2	16	51	LQFP-64
A34M416VL	256KB	64KB	2	6	2	2	24	89	LQFP-100
A34M416RL	256KB	64KB	1	3	1	2	16	51	LQFP-64
A34M414VL	128KB	32KB	2	6	2	2	24	89	LQFP-100
A34M414RL	128KB	32KB	1	3	1	2	16	51	LQFP-64

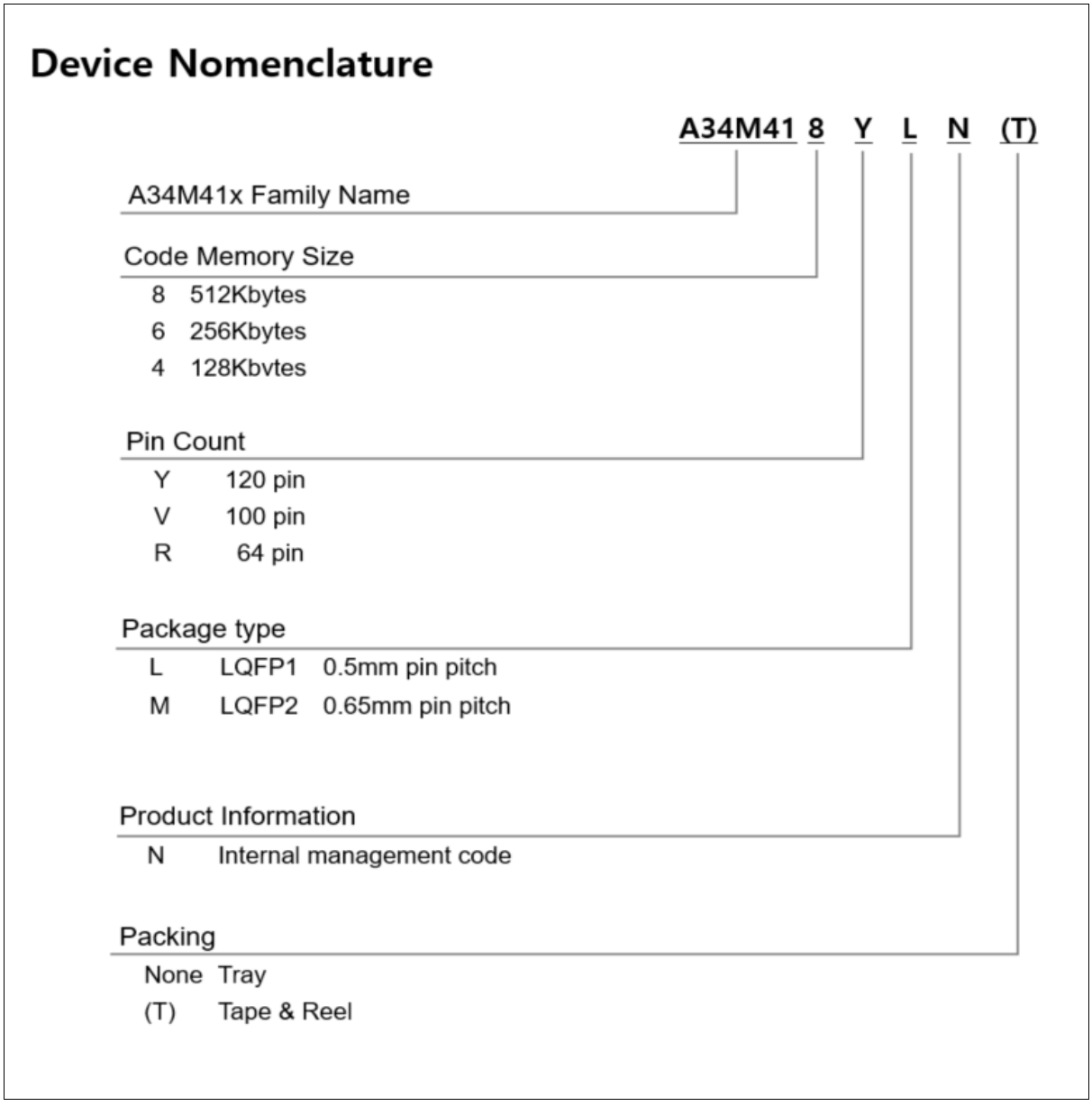


Figure 59. A34M41x Device Numbering Nomenclature

Revision history

Date	Revision	Description
Aug.2, 2019	1.00	1st creation
Jan.17,2020	1.01	Minor bug fix.

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