ProASIC™ 500K Family

Features and Benefits

High Capacity

- 100,000 to 475,000 System Gates
- 14k to 63k Bits of Two-Port SRAM
- 106 to 440 User I/Os

Performance

- 33 MHz PCI 32-bit PCI
- Internal System Performance up to 250 MHz
- External System Performance up to 100 MHz

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient Logic Cells

High Performance Routing Hierarchy

- Ultra Fast Local Network
- Efficient Long Line Network
- High Speed Very Long Line Network
- High Performance Global Network

Nonvolatile and Reprogrammable Flash Technology

- Live at Power Up
- No Configuration Device Required
- Retains Programmed Design During Power-Down/ Power-Up Cycles

I/O

- Mixed 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- 3.3V, PCI Compliance (PCI Revision 2.2)

Secure Programming

The Industry's Most Effective Security Key Prevents Read Back of Programming Bit Stream

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design Through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) with Silicon Sculptor and Flash Pro

SRAMs and FIFOs

- Up to 150 MHz Synchronous and Asynchronous Operation
- Netlist Generator Ensures Optimal Usage of Embedded Memory Blocks

Boundary Scan Test

IEEE Std. 1149.1 (JTAG) Compliant

ProASIC Product Profile

Device	A500K050	A500K130	A500K180	A500K270
Maximum System Gates	100,000	290,000	370,000	475,000
Typical Gates	43,000	105,000	150,000	215,000
Maximum Flip-Flops	5,376	12,800	18,432	26,880
Embedded RAM Bits	14k	45k	54k	63k
Embedded RAM Blocks (256 X 9)	6	20	24	28
Logic Tiles	5,376	12,800	18,432	26,880
Global Routing Resources	4	4	4	4
Maximum User I/Os	204	306	362	440
JTAG	Yes	Yes	Yes	Yes
PCI	Yes	Yes	Yes	Yes
Package (by Pin Count)				
PQFP	208	208	208	208
PBGA	272	272, 456	456	456
FBGA	144	144, 256	256	256, 676

General Description

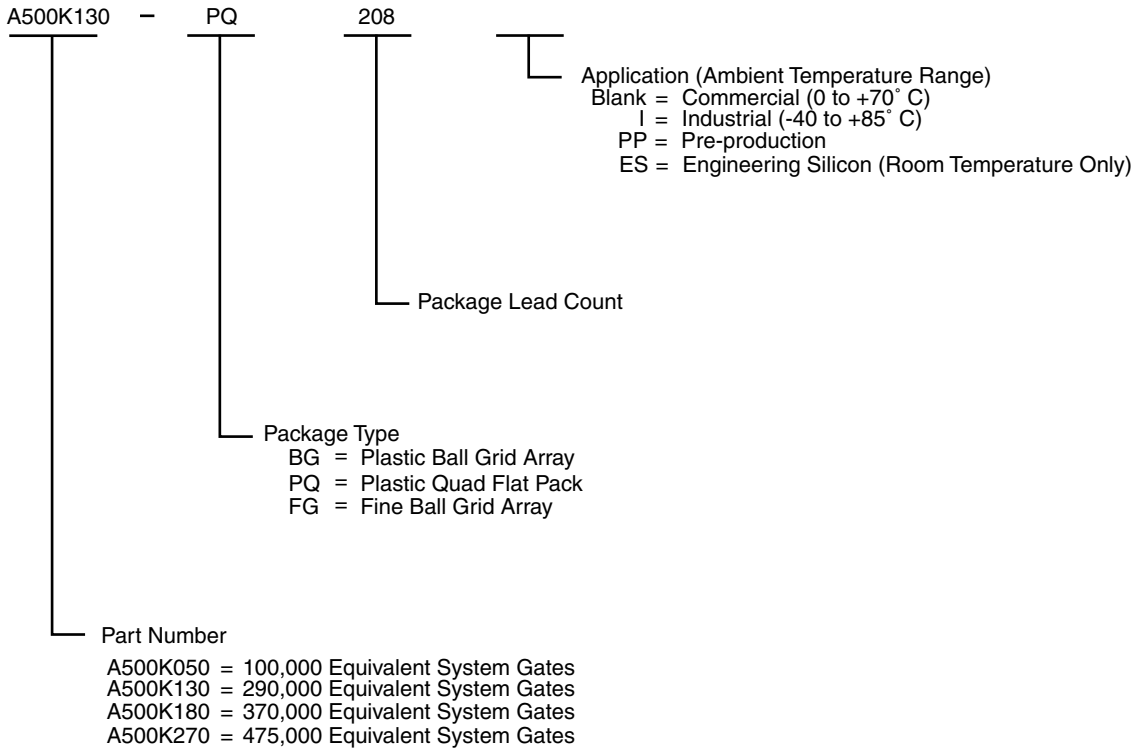
The ProASIC 500K family's nonvolatile Flash technology combines the advantages of ASICs with the benefits of programmable devices. ProASIC 500K devices shorten time-to-production by enabling designers to create high-density systems using existing ASIC or FPGA design flows and tools. ASIC migration is not necessary for any volume because the family offers cost effective reprogrammable solutions, ideal for applications in the networking, telecom, computer, and consumer markets.

The ProASIC 500K family consists of four devices ranging from 100k to 475k system gates and with up to 63k bits of embedded two-port memory. These memory blocks include hardwired FIFO circuitry as well as circuits to generate or check parity. This minimizes external logic gate count and complexity while maximizing flexibility and utility.

Process Technology

The ProASIC 500K family achieves its nonvolatile and reprogrammability through an advanced 0.25µ, four-level metal LVCMOS process enhanced with Flash technology. The use of standard CMOS design techniques to implement logic and control functions results in highly predictable performance and gate array compatibility.

Ordering Information



Product Plan

	Application	
	C	I
A500K050 Device		
144-Pin Fine Ball Grid Array (FBGA)	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔
272-Pin Plastic Ball Grid Array (PBGA)	✔	✔
A500K130 Device		
144-Pin Fine Ball Grid Array (FBGA)	✔	✔
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔
272-Pin Plastic Ball Grid Array (PBGA)	✔	✔
256-Pin Plastic Ball Grid Array (PBGA)	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔
A500K180 Device		
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔
256-Pin Plastic Ball Grid Array (PBGA)	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔
A500K270 Device		
208-Pin Plastic Quad Flat Pack (PQFP)	✔	✔
256-Pin Plastic Ball Grid Array (PBGA)	✔	✔
456-Pin Plastic Ball Grid Array (PBGA)	✔	✔
676-Pin Fine Ball Grid Array (FBGA)	✔	✔

Contact your Actel sales representative for package availability.

Applications: C = Commercial I = Industrial

Availability: ✔ = Available – Contact your Actel Sale's representative for the latest availability information.

Plastic Device Resources

	User I/Os					
Device	**PQFP 208-Pin**	**PBGA 272-Pin**	**PBGA 456-Pin**	**FBGA 144-Pin**	**FBGA 256-Pin**	**FBGA 676-Pin**
A500K050	164	204	—	106	—	—
A500K130	164	204	306	106	192	—
A500K180	164	—	362	—	192	—
A500K270	164	—	362	—	192	440

Package Definitions

PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Ball Grid Array

ProASIC 500K Architecture

The ProASIC 500K family's proprietary architecture provides granularity comparable to gate arrays. Unlike SRAM-based FPGAs that utilize look-up tables or architectural mapping during design, ProASIC device designs are directly synthesized to gates. That streamlines the design flow, increases design productivity, and eliminates dependencies on vendor-specific design tools.

The ProASIC 500K device core consists of a Sea-of-Tiles™ (Figure 1), each of which can be configured as a 3-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (See Figure 2 on page 5 and Figure 3 on page 5). Gates and larger functions are connected with four levels of routing hierarchy. Flash memory bits are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

The ProASIC 500K devices also contain embedded two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Table 3 on page 12 lists the 24 basic memory configurations.

Flash Switch

In the ProASIC Flash switch, two transistors share the floating gate which stores the programming information. One is the Flash transistor which stores programming information and in which erasing is performed. The second transistor connects/separates routing elements or configuration signal lines (Figure 2 on page 5).

Logic Tile

The logic tile cell, Figure 3 on page 5, has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra fast local and efficient long line routing resources). Any three-input one-output logic function, except a three input XOR, can be configured as one tile. Two multiplexers with feedback paths through the NAND gates allow the tile to be configured as a latch with clear or set, or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.

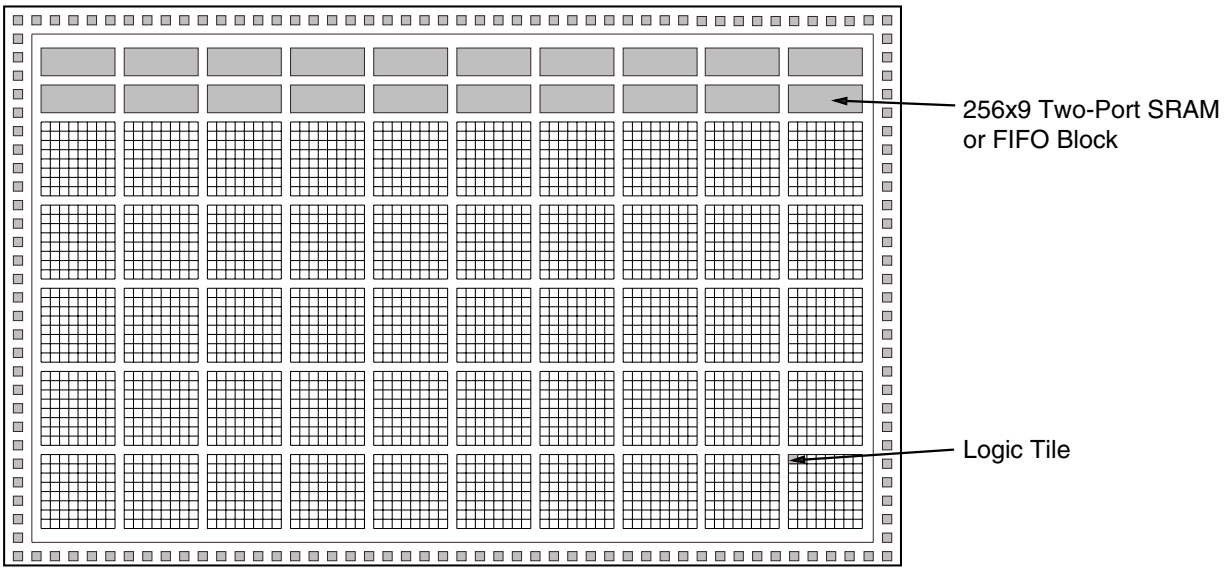


Figure 1 • *The ProASIC Device Architecture*

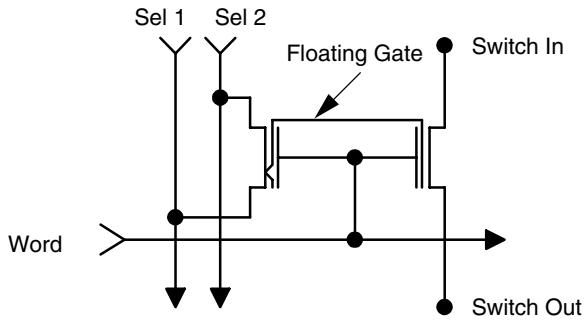


Figure 2 • *Flash Switch*

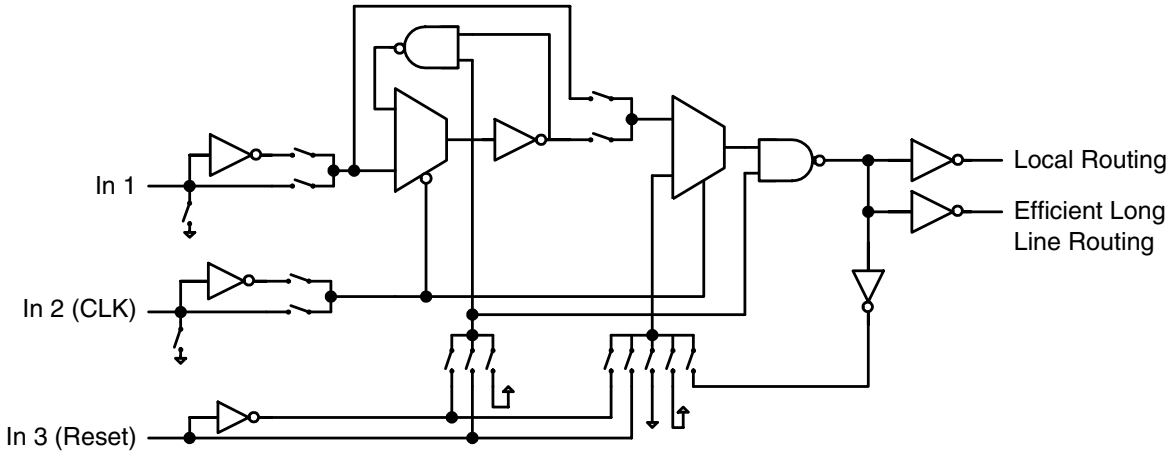


Figure 3 • *Core Logic Tile*

Routing Resources

The routing structure of the ProASIC 500K devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra fast local resources, efficient long line resources, high speed very long line resources, and high performance global networks.

The ultra fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 4 on page 6).

The efficient long line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC device (Figure 5 on page 6). Each tile can drive signals onto the efficient long line resources, while the resources can also access every input of any tile. The routing software automatically inserts active buffers to limit loading effects due to distance and fanout.

The high speed very long line resources, spanning across the entire device with minimal delay, are used to route very long or very high fanout nets. These resources run vertically and horizontally, providing multiple access to each group of tiles throughout the device (Figure 6 on page 7).

The high performance global networks' clock trees are low skew, high fanout nets that are accessible from four dedicated pins or from internal logic (Figure 7 on page 8). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically, with signals accessing every input on all tiles.

Clock Resources

ProASIC's high-drive routing structure provides four global networks, each accessible from either a dedicated global pad or a logic tile. Global lines provide optimized worst-case clock skew of 0.3ns.

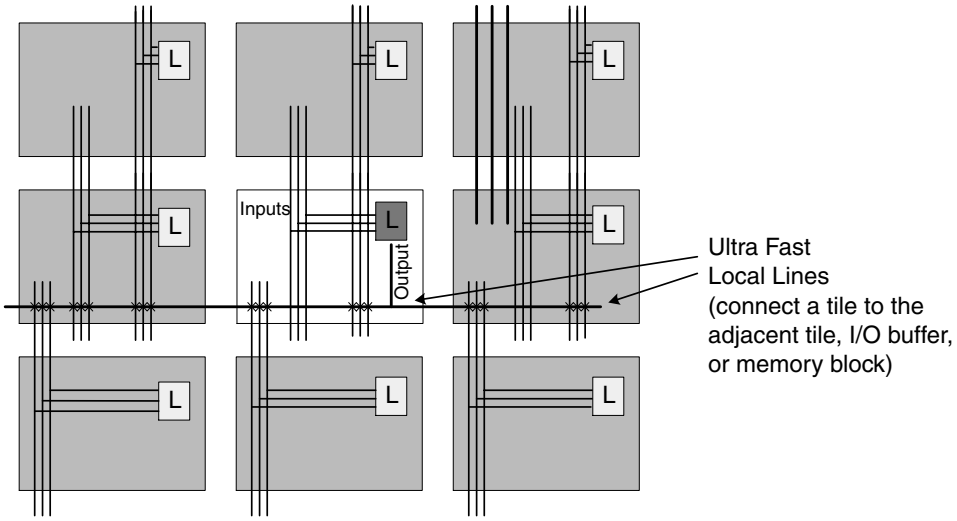


Figure 4 • *Ultra Fast Local Resources*

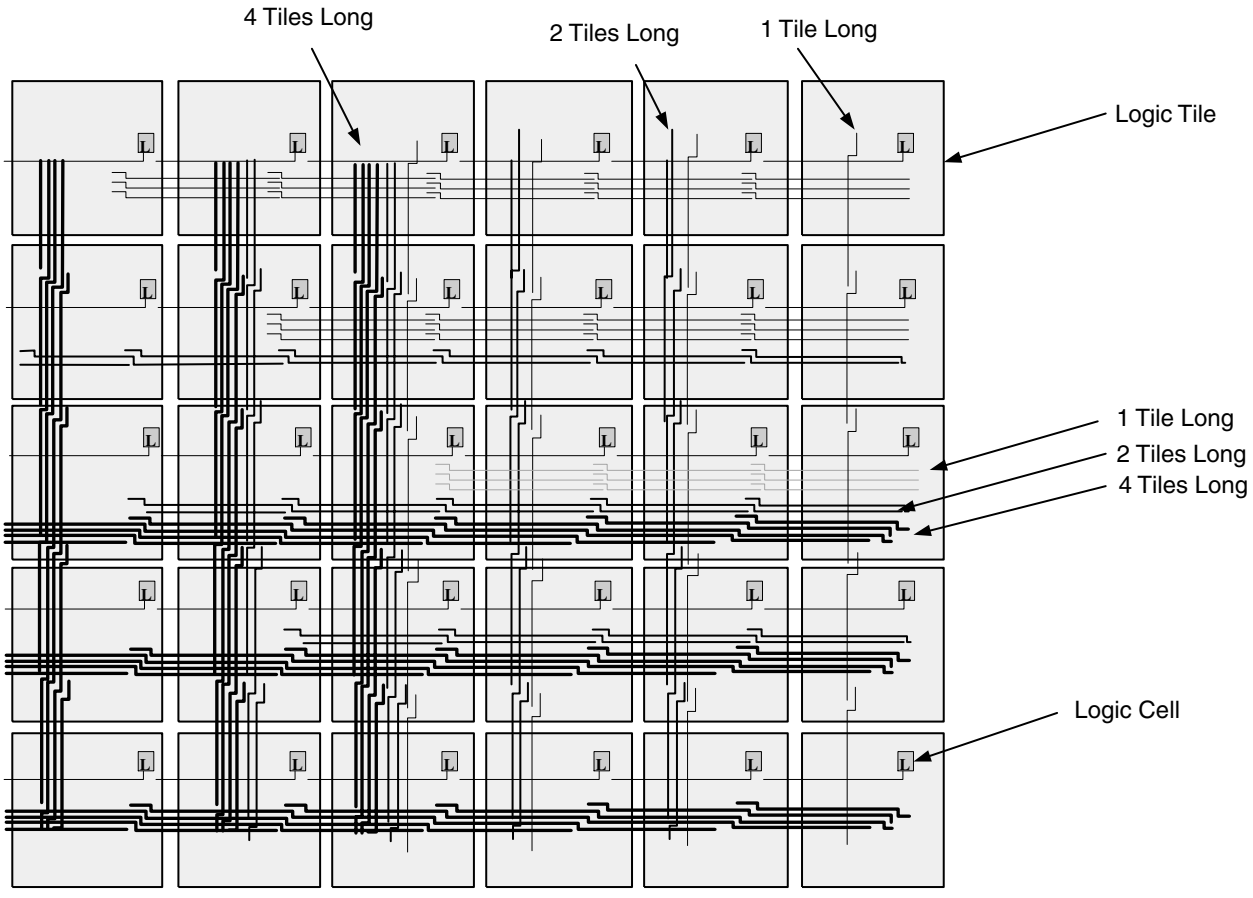


Figure 5 • *Efficient Long Line Resources*

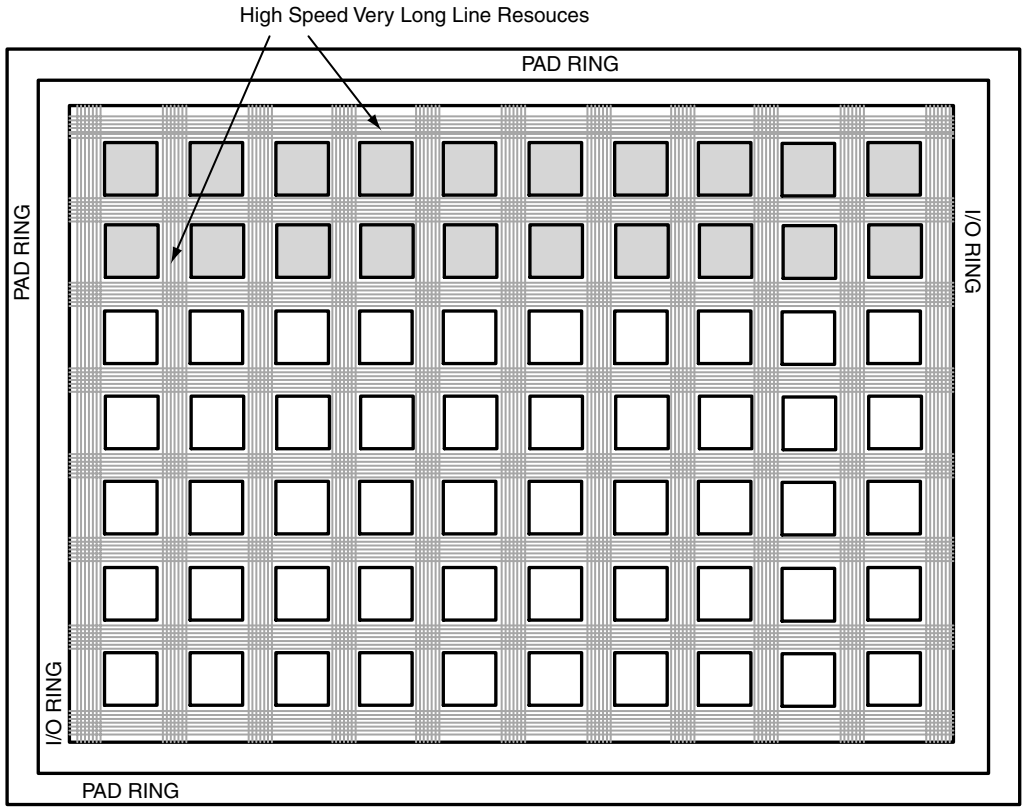


Figure 6 • *High Speed Very Long Line Resources*

Clock Trees

One of the main architectural benefits of ProASIC is the set of power and delay friendly global networks. The ProASIC family offers 4 global trees. Each of these trees is based on a network of spines and ribs that reach all the tiles in their regions (Figure 7). This flexible clock tree architecture allows users to map up to 56 different internal/external clocks in an A500K270 device (Table 1).

The flexible use of the ProASIC clock spine allows the designer to cope with several design requirements. Users implementing clock resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high fanout nets to spines. For design hints on using these features, refer to the *Efficient Use of ProASIC Clock Trees* application note.

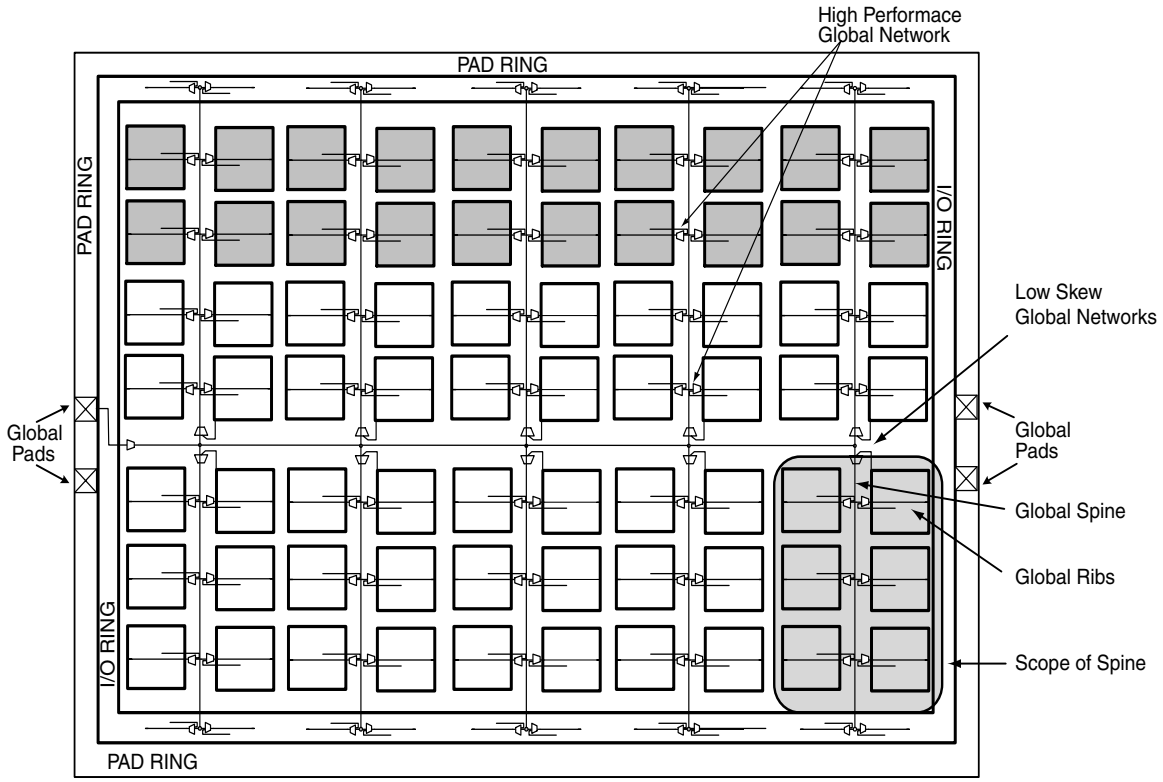


Figure 7 • *A500K130 Global Routing Resources*

Table 1 • *Number of Clock Spines*

	A500K050	A500K130	A500K180	A500K270
Top Spine Height	24	32	40	56
Tiles in Each Top Spine	768	1,024	1,280	1,792
Bottom Spine Height	32	40	56	64
Tiles in Each Bottom Spine	1,024	1,280	1,792	2,048
Global Clock Networks (Trees)	4	4	4	4
Clock Spines/Tree	6	10	12	14
Total Spines	24	40	48	56
Total Tiles	5,376	12,800	18,432	26,880

Input/Output Blocks

To meet complex system design needs, the ProASIC 500K family offers devices with a large number of I/O pins, up to 440 user I/O pins on the A500K270. If the I/O pad is powered at 3.3V, each I/O can be selectively configured at 2.5V and 3.3V threshold levels. Table 2 shows the available supply voltage configurations. Figure 8 illustrates I/O interfaces with other devices.

Table 2 • ProASIC Power Supply Voltages

V_{DDP}	2.5V	3.3V
Input Tolerance	2.5V	3.3V, 2.5V
Output Drive	2.5V	3.3V, 2.5V

Note: *V_{DDL} is always 2.5V.*

The I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a three-state driver, or a bidirectional buffer (Figure 9). I/O pads configured as inputs have the following features:

- Individually selectable 2.5V or 3.3V threshold levels[1]
- Optional pull-up resistor

I/O pads configured as outputs have the following features:

- Individually selectable 2.5V or 3.3V compliant output signals[1]
- 3.3V PCI compliant
- Ability to drive LVTTL and LVCMOS levels
- Selectable drive strengths
- Selectable slew rates
- Tristate

I/O pads configured as bidirectional buffers have the following features:

- Individually selectable 2.5V or 3.3V compliant output signals and threshold levels[1]
- 3.3V PCI compliant
- Optional pull-up resistor
- Selectable drive strengths
- Selectable slew rates
- Tristate

1. If pads are configured for 2.5V operation, they are compliant with 2.5V level signals as defined by JEDEC JESD 8-5. If pads are configured for 3.3V operation, they are compliant to the standard as defined by JEDEC JESD 8-A (LVTTL and LVCMOS).

All I/Os also include an ESD protection circuit. Each I/O is tested according to the following model:

- Human Body Model (HBM) (Per Mil Std 883 Method 3015) — 2000V

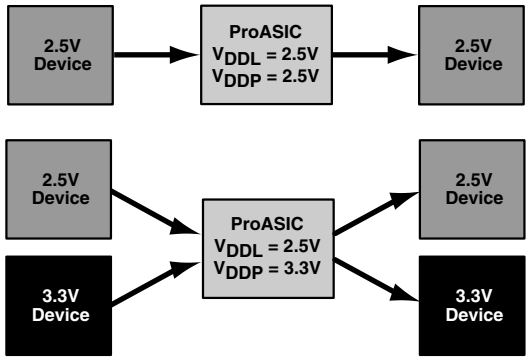


Figure 8 • I/O Interfaces

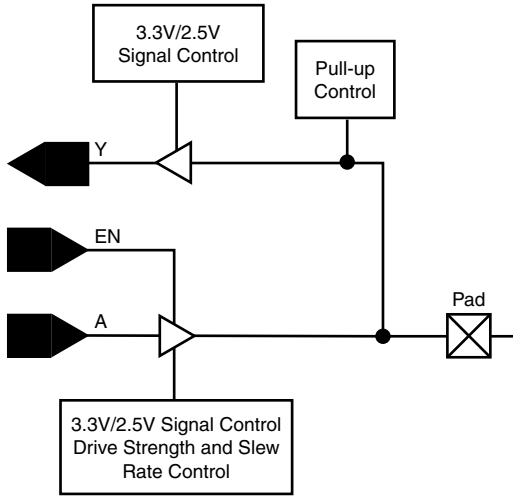


Figure 9 • I/O Block Schematic Representation

Boundary Scan

ProASIC devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic ProASIC boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 10 on page 10). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS), the optional IDCODE instructions and private instructions used for device programming and factory testing.

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO (test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI, and TRST are equipped

with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 11 on page 11. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device; this speeds up test data transfer to other devices in a test data path. The 32-bit device identification register is a shift register with four fields (LSB, ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary scan register chain which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.

Details on the implementation of boundary-scan testing on ProASIC devices can be found in the Actel application note, *Using JTAG Boundary-Scan with ProASIC Devices*.

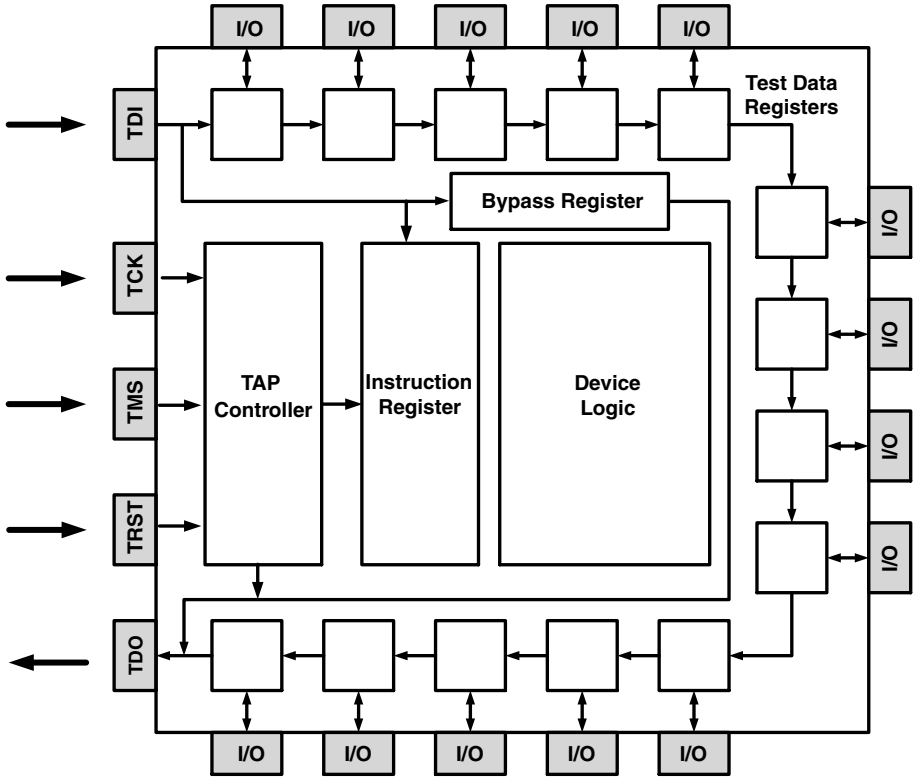


Figure 10 • *ProASIC JTAG Boundary Scan Test Logic Circuit*

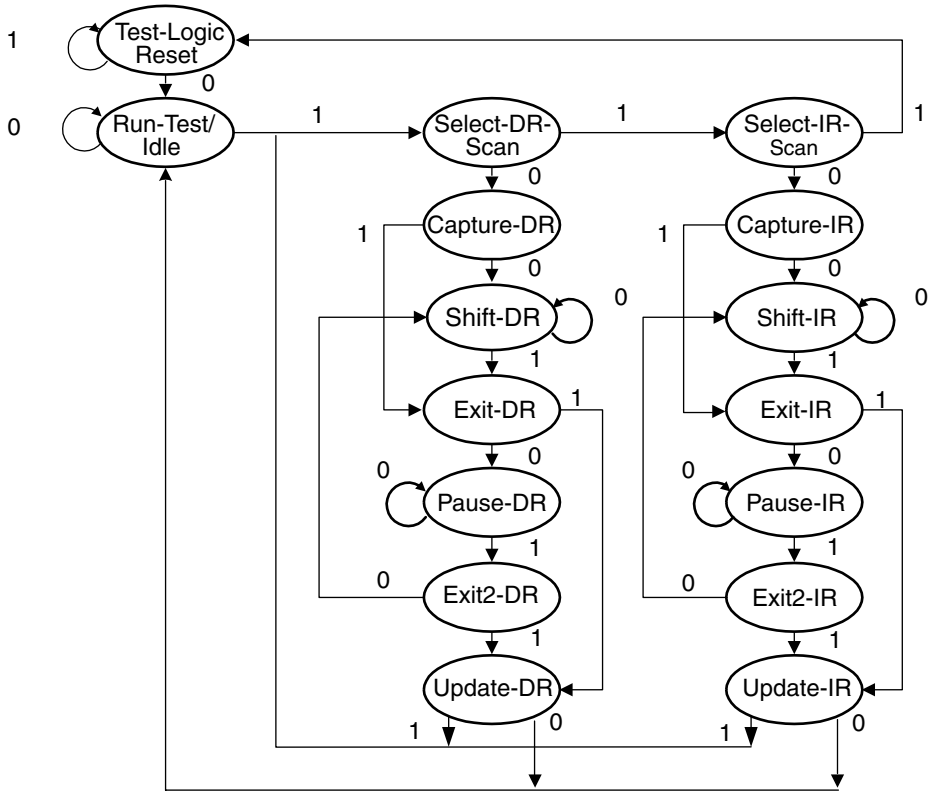


Figure 11 • TAP Controller State Diagram

User Security

The ProASIC 500K devices have read-protect bits that, once programmed, lock the entire programmed contents from being read externally. The user can only reprogram the device using the security key. This protects it from being read back and duplicated. Since programmed data is stored in nonvolatile Flash cells (which act like very small capacitors), rather than in the wiring, physical deconstruction cannot be used to compromise data. That approach would be further hampered by the placement of the flash cells, beneath the four metal layers (whose removal could not be accomplished without disturbing the charge on the floating gate). This is the highest security provided in the industry. For more information, refer to the *Design Security for Nonvolatile Flash and Antifuse FPGAs* white paper for more information.

Embedded Memory Floorplan

The embedded memory is located across the top of the device (see Figure 1 on page 4) in 256x9 blocks. Depending upon the device, 6 to 28 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory or combined (using dedicated memory routing resources) to form larger, more complex memories.

Embedded Memory Configurations

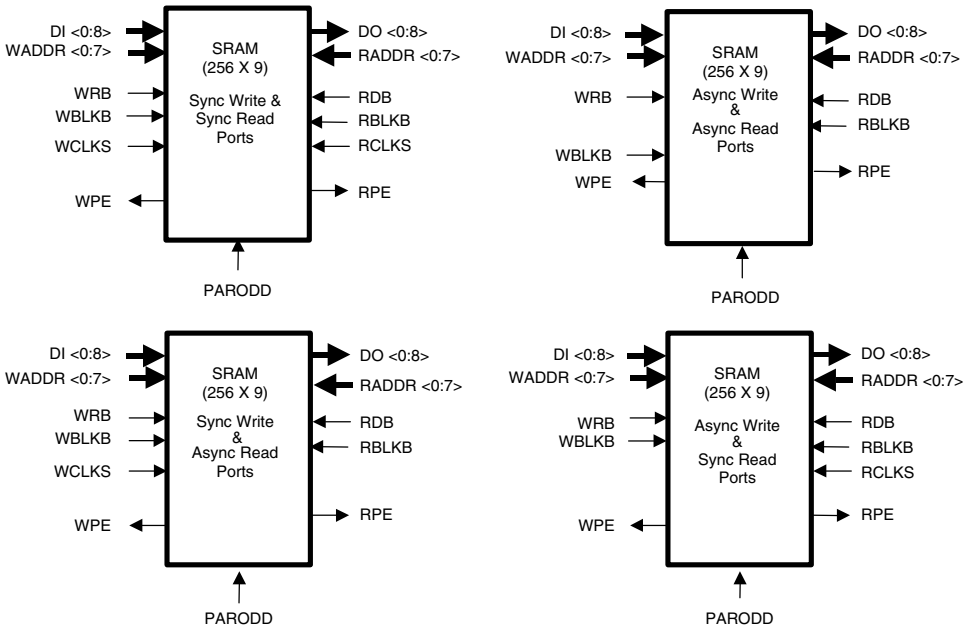
The embedded memory in the ProASIC 500K family provides great configuration flexibility. While other programmable vendors typically use single port memories that can only be transformed into two-port memories by sacrificing half the memory, each ProASIC block is designed and optimized as a two-port memory (1 read, 1 write). This provides 63k bits of total memory for two-port and single port usage in the A500K270 device.

Each memory can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports (Table 3 on page 12). Multiple write ports are not supported. Additional characteristics include programmable flags as well as parity check and generation. Figure 12 and Figure 13 on page 13 show the block diagrams of the basic SRAM and FIFO blocks. These memories are designed to operate up to 133 MHz when operated individually. Each block contains a 256 word deep by 9-bit wide (1 read, 1 write) memory. The memory blocks may be combined in parallel to form wider memories or stacked to form deeper memories (Figure 14 on page 14). This provides optimal bit widths of 9 (1 block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1024. Refer to the *Macro Library Guide* for more information.

Figure 15 on page 14 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to generate three memories of various widths and depths. Figure 16 on page 14 shows how memory can be doubled up to create extra read ports. In this example, 10 out of 28 blocks of the A500K270 yield an effective 6,912 bits of multiple port memories. The ACTgen™ software facilitates building wider and deeper memories for optimal memory usage.

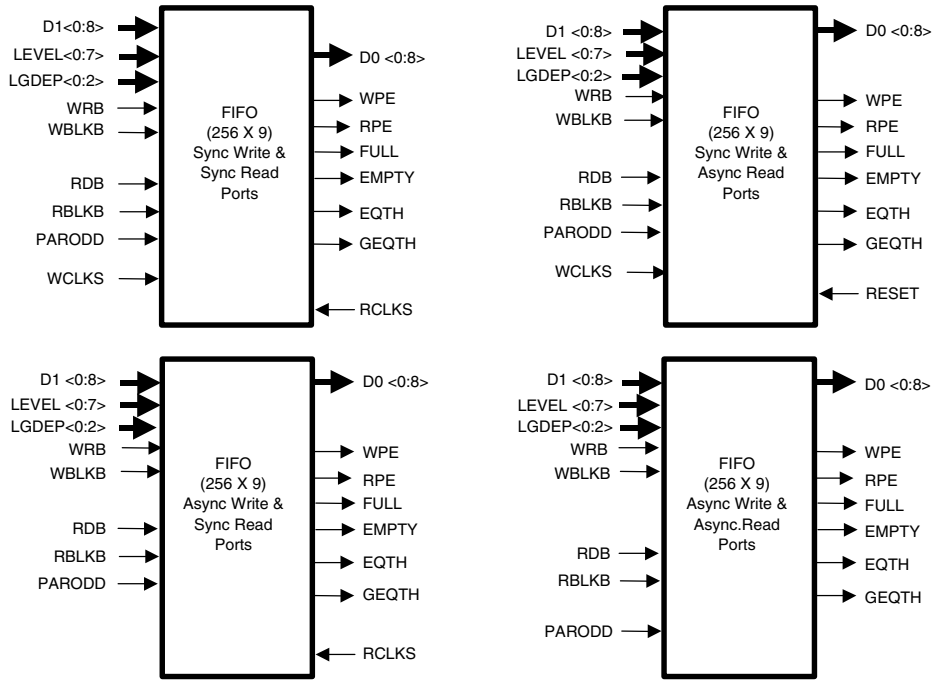
Table 3 • *Basic Memory Configurations*

Type	Write Access	Read Access	Parity	Library Cell Name
RAM	Asynchronous	Asynchronous	Checked	RAM256x9AA
RAM	Asynchronous	Asynchronous	Generated	RAM256x9AAP
RAM	Asynchronous	Synchronous Transparent	Checked	RAM256xAST
RAM	Asynchronous	Synchronous Transparent	Generated	RAM256xASTP
RAM	Asynchronous	Synchronous Pipelined	Checked	RAM256x9ASR
RAM	Asynchronous	Synchronous Pipelined	Generated	RAM256x9ASRP
RAM	Synchronous	Asynchronous	Checked	RAM256x9SA
RAM	Synchronous	Asynchronous	Generated	RAM256xSAP
RAM	Synchronous	Synchronous Transparent	Checked	RAM256x9SST
RAM	Synchronous	Synchronous Transparent	Generated	RAM256x9SSTP
RAM	Synchronous	Synchronous Pipelined	Checked	RAM256x9SSR
RAM	Synchronous	Synchronous Pipelined	Generated	RAM256x9SSRP
FIFO	Asynchronous	Asynchronous	Checked	FIFO256xAA
FIFO	Asynchronous	Asynchronous	Generated	FIFO256x9AAP
FIFO	Asynchronous	Synchronous Transparent	Checked	FIFO256xAST
FIFO	Asynchronous	Synchronous Transparent	Generated	FIFO256x9ASTP
FIFO	Asynchronous	Synchronous Pipelined	Checked	FIFO256x9ASR
FIFO	Asynchronous	Synchronous Pipelined	Generated	FIFO256x9ASRP
FIFO	Synchronous	Asynchronous	Checked	FIFO256x9SA
FIFO	Synchronous	Asynchronous	Generated	FIFO256xSAP
FIFO	Synchronous	Synchronous Transparent	Checked	FIFO256x9SST
FIFO	Synchronous	Synchronous Transparent	Generated	FIFO256x9SSTP
FIFO	Synchronous	Synchronous Pipelined	Checked	FIFO256x9SSR
FIFO	Synchronous	Synchronous Pipelined	Generated	FIFO256x9SSRP



Note: *For memory block interface signal definitions, see Table 4 on page 28.*

Figure 12 • Example SRAM Block Diagrams



Note: *For memory block FIFO signal definitions, see Table 5 on page 34.*

Figure 13 • Basic FIFO Block Diagrams

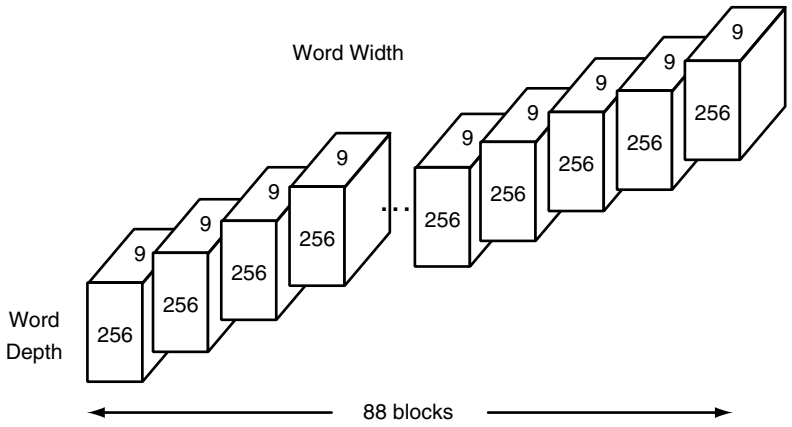


Figure 14 • A500K270 Memory Block Architecture

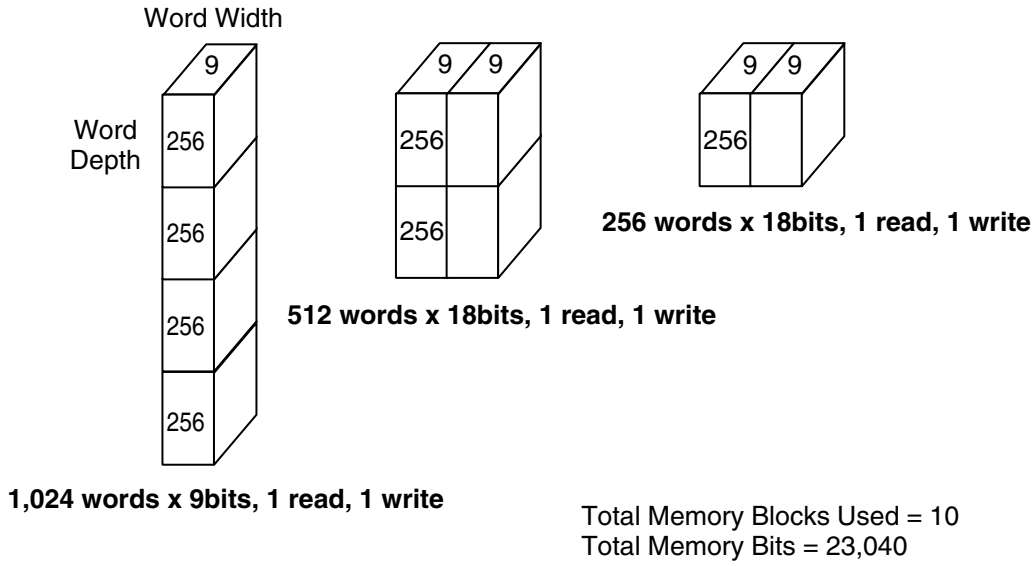


Figure 15 • Example Showing Memories with Different Width and Depth

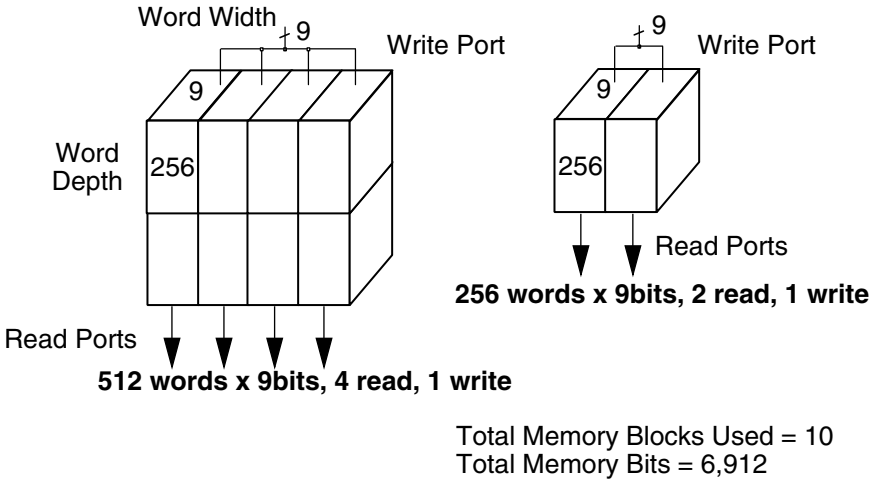


Figure 16 • Multiport Memory Usage

Design Environment

ProASIC devices are supported by Actel's Designer Series software, as well as all of the industry standard third party CAE tools. Unlike other FPGA vendors, no special HDL instantiation or device related attributes are needed when using the standard VHDL or Verilog HDL design flow with ProASIC. As a result, designers can utilize the technology independent of HDL code for ProASIC devices. This feature and the ASIC-like design flow ensure a seamless transition to an ASIC implementation, if production volumes warrant a migration to a gate array or a standard cell product (Figure 17).

ACTgen automatically generates memories and FIFOs with all the various options (width, depth, access mode, parity checking or generation, flags, etc.). For a synchronous read port, the user can choose whether the output is pipelined or transparent. ACTgen allows any bit width up to 252 (for the A500K270 device). ACTgen also enables optimal memory stacking in 256-word increments. However, any word depth may be combined for up to 7,168 words. ACTgen allows the user to generate distributed memory.

Place and route is performed by Actel's Designer software. Available for UNIX workstations and PC platforms, Designer software accepts standard netlists in Verilog, VHDL, and in EDIF format, performs timing driven place and route of the design into the selected device/package, and provides postlayout timing information for backannotated simulation or static timing analysis. The Designer software also contains very powerful layout capabilities for the experienced user. A very comprehensive set of floor planning, timing, and routing constraints gives users optimal control over the tools' capabilities, enabling them to meet their tight design requirements. Users have access to constraints that allow them full control of the resources management. See the *Designer User's Guide* for various constraints and their uses.

The ProASIC devices are also fully supported by Actel's Libero design tool suite. Libero is a design management environment that integrates the needed design tools, streamlines the design flow, manages all design and log files, and passes the necessary design data between tools. Libero includes Synplify, ViewDraw, Actel's Designer Series, ModelSim HDL Simulator, and WaveFormer Lite.

Once the design is finalized, the programming bitstream is downloaded into the device programmer for ProASIC part programming. ProASIC 500K devices can be programmed with the Silicon Sculptor II and Flash Pro programmers. On-board programming is also available. Refer to the *In-System Programming ProASIC 500K with Silicon Sculptor* application note for more information.

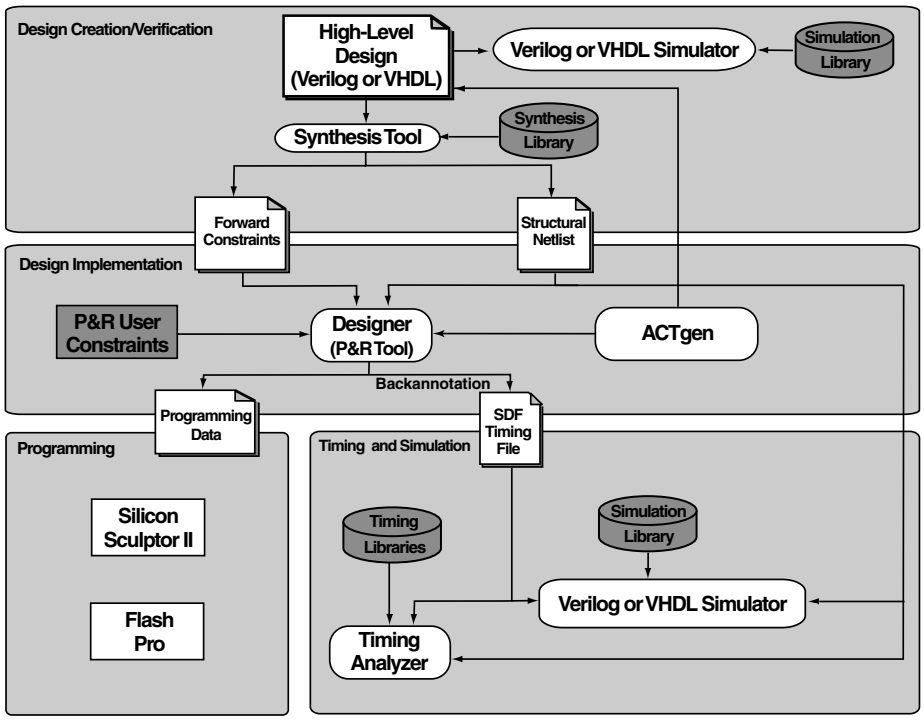


Figure 17 • *ProASIC Design Flow*

Package Thermal Characteristics

The ProASIC 500K family is available in a number of package types. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance indicates the ability of a package to conduct heat away from the silicon, through the package, to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja (Θ_{ja}). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature (T_J), maximum ambient operating temperature (T_A), and junction-to-ambient thermal resistance Θ_{ja}. Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

Θ_{ja} is a function of the rate (in linear feet per minute – lfpm) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used.

Package Type	Pin Count	Θ_{jc}	Θ_{ja} Still Air	Θ_{ja} 300 ft/min	Units
Plastic Quad Flat Pack (PQFP)	208	8	30	23	°C/W
PQFP with Heatspreader	208	3.8	20	17	°C/W
Plastic Ball Grid Array (PBGA)	272	3	20	16.5	°C/W
Plastic Ball Grid Array (PBGA)	456	3	18	14.5	°C/W
Fine Ball Grid Array (FBGA)	144	3.8	38.8	26.7	°C/W
Fine Ball Grid Array (FBGA)	256	3.0	30	25	°C/W

Calculating Power Dissipation

ProASIC device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

$$P_{total} = P_{dc} + P_{ac}$$

where:

P_{dc} = 10 mW

P_{ac} = $P_{clock} + P_{storage} + P_{logic} + P_{ios} + P_{memory}$

P_{clock} = $(P1 + P2 * s) * Fs$

where:

P1 = 2500 uW/MHz
the basic power consumption of the clock-tree normalized per MHz of the clock

P2 = 1.0 uW/MHz
the extra power consumption of the clock-tree per storage-tile normalized per MHz of the clock

s = the number of storage tiles clocked by this clock

Fs = the clock frequency

$$P_{storage} = P5 * ms * Fs$$

where:

P5 = 1.0 uW/MHz
the average power consumption of a storage-tile normalized per MHz of its output

ms = the number of storage tiles switching at each Fs cycle

Fs = the clock frequency

$$P_{logic} = P3 * mc * Fs$$

where:

P3 = 3.0 uW/MHz
the average power consumption of a logic-tile normalized per MHz of its output

mc = the number of logic tiles switching at each Fs cycle

Fs = the clock frequency

$$P_{ios} = (P4 + C_{load} * V_{ddp}\text{^}2) * p * Fp$$

where:

P4 = 15.0 uW/MHz
the average power consumption of an output-pad normalized per MHz of its output (internal power-load is not included)

C_{load} = the output load

p = the number of outputs

Fp = the average output frequency

$$P_{memory} = P6 * N_{mem} * F_{mem}$$

where:

P6 = 100.0 uW/MHz
is the average power consumption of a memory block normalized per MHz of the clock

N_{mem} = the number of RAM/FIFO blocks (1 block = 256 words * 9 bits)

F_{mem} = the clock frequency of the memory

The following is an example using a shift register design with 13,440 storage tiles and 0 logic tile. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz for a A500K270.

Fs = 10 MHz

s = 13,440

=> Pclock = $(P1 + P2 * s) * Fs$ = 159.4 mW

ms = 13,440 (in a shift register 100% of storage-tiles are toggling at each clock cycle and Fs = 10 MHz

=> Pstorage = $P5 * ms * Fs$ = 134.4 mW

mc = 0 (no logic tile in this shift-register)

=> P_{logic} = 0 mW

Fp = 5 MHz

C_{load} = 40 pF

V_{DDP} = 3.3 V

and p = 24

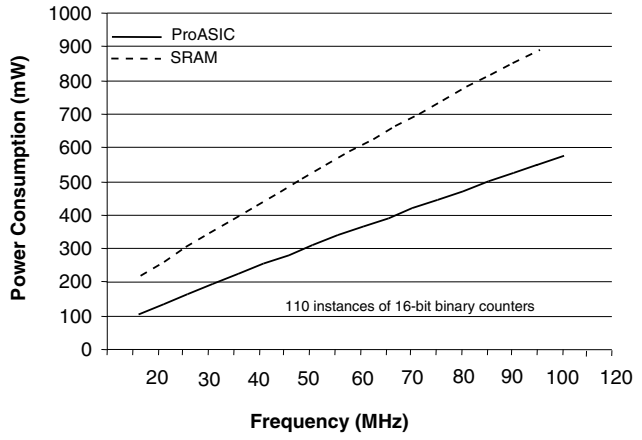
=> $P_{ios} = (P4 + Cload * V_{ddp}\text{^}2) * p * Fp$ = 54.1 mW

N_{mem} = 0 (no RAM/FIFO in this shift-register)

=> P_{memory} = 0 mW

- $P_{ac} = P_{clock} + P_{storage} + P_{logic} + P_{ios} + P_{memory}$ = 347.9 mW
- P_{dc} = 10 mW
- $P_{total} = P_{dc} + P_{ac}$ = 357.9 mW

Power Consumption of a 500K Device



Operating Conditions

Absolute Maximum Ratings

Parameter	Condition	Minimum	Maximum	Units
Supply Voltage Core (V_{DDL})		–0.3	3.0	V
Supply Voltage I/O Ring (V_{DDP})		–0.3	4.0	V
DC Input Voltage		–0.3	V_{DDP} + 0.3	V
PCI DC Input Voltage		–0.5	V_{DDP} + 0.5	V
DC Input Clamp Current	V_{IN} < 0 or V_{IN}> V_{DDP}	–10	+10	mA

Note: Stresses beyond those listed in the Absolute Maximum Ratings table can cause permanent damage to the device. Exposure to maximum rated conditions for extended periods can adversely affect device reliability. Operation of the device at these conditions or any others beyond those listed in the Recommended Operating Conditions is not implied.

Programming and Storage Temperature LImits

Product Grade	Programming Cycles	Program Retention	Storage Temperature	
			Min.	Max.
Commercial	50	20 years	–55°C	110°C
Industrial	50	20 years	–55°C	110°C

Supply Voltages

Mode	V_{DDL}	V_{DDP}	V_{PP}	V_{PN}
Single Voltage	2.5V	2.5V	2.5V ≤ V_{pp} ≤ 16.5V	–12V≤ V_{PN} ≤ 0V
Mixed Voltage	2.5V	3.3V	3.3V ≤ V_{pp} ≤ 16.5V	–12V ≤V_{PN} ≤ 0V

Recommended Operating Conditions

Parameter	Symbol	Limits
Commercial		
DC Supply Voltage (2.5V I/Os)	V_{DDL} & V_{DDP}	2.3V to 2.7V
DC Supply Voltage (Mixed 2.5V and 3.3V I/Os)	V_{DDP} V_{DDL}	3.0V to 3.6V 2.3V to 2.7V
Operating Ambient Temperature Range	T_A	0°C to 70°C
Maximum Operating Junction Temperature	T_J	110°C
Maximum Clock Frequency	f_{CLOCK}	250 MHz
Maximum RAM Frequency	f_{RAM}	150 MHz
Industrial		
DC Supply Voltage (2.5V I/Os)	V_{DDL} & V_{DDP}	2.3V to 2.7V
DC Supply Voltage (Mixed 2.5V and 3.3V I/Os)	V_{DDP} V_{DDL}	3.0V to 3.6V 2.3V to 2.7V
Operating Ambient Temperature Range	T_A	–40°C to 85°C
Maximum Operating Junction Temperature	T_J	110°C
Maximum Clock Frequency	f_{CLOCK}	250 MHz
Maximum RAM Frequency	f_{RAM}	150 MHz

DC Electrical Specifications (V_{DDP} = 2.5V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP}, V_{DDL}	Supply Voltage		2.3		2.7	V
V_{OH}	Output High Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OH} = –2.0 mA I_{OH} = –4.0 mA I_{OH} = –8.0 mA I_{OH} = –1.0 mA I_{OH} = –2.0 mA I_{OH} = –4.0 mA	 2.1 2.0 1.7 2.1 2.0 1.7			V
V_{OL}	Output Low Voltage High Drive (OB25LPH) Low Drive (OB25LPL)	 I_{OL} = 5.0 mA I_{OL} = 10.0 mA I_{OL} = 15.0 mA I_{OL} = 2.0 mA I_{OL} = 3.5 mA I_{OL} = 5.0 mA			 0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage		1.7		V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.7	V
$\lvert I_{IN} \rvert$ [2]	Input Current	with pull-up without pull-up	25		250 10	µA µA
I_{DDQ}	Quiescent Supply Current	$V_{IN} = V_{SS}$ [3] or V_{DDL}		4.0	10	mA
I_{OZ}	3-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DDL}			10	µA
$\lvert I_{OSH} \rvert$ [2]	Output Short Circuit Current High High Drive (OB25LPH) Low Drive (OB25LPL)	 $V_{IN} = V_{SS}$ $V_{IN} = V_{SS}$			 120 100	mA
I_{OSL}	Output Short Circuit Current Low High Drive (OB25LPH) Low Drive (OB25LPL)	 $V_{IN} = V_{DDP}$ $V_{IN} = V_{DDP}$			 100 30	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Junction Temperature: –40 to +110°C.*
2. *Current is negative.*
3. *No pull-up resistor.*

DC Electrical Specifications (V_{DDP} = 3.3V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{DDP}	Supply Voltage		3.0		3.6	V
V_{DDL}	Supply Voltage, Logic Array		2.3		2.7	V
V_{OH}	Output High Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	 I_{OH} = –5.0 mA I_{OH} = –10.0 mA I_{OH} = –2.5 mA I_{OH} = –5.0 mA	 0.9V_{DDP} 2.4 0.9V_{DDP} 2.4			V
	Output High Voltage 2.5V I/O, High Drive (OB25H) 2.5V I/O, Low Drive (OB25L)	I_{OH} = –200µA I_{OH} = –10.0 mA I_{OH} = –2.0 mA I_{OH} = –100µA I_{OH} = –1.0 mA I_{OH} = –2.0 mA	2.1 2.0 1.7 2.1 2.0 1.7			V
V_{OL}	Output High Voltage 3.3V I/O, High Drive (OB33P) 3.3V I/O, Low Drive (OB33L)	 I_{OL} = 7.5 mA I_{OL} = 12.0 mA I_{OL} = 4.0 mA I_{OL} = 5.0 mA	 		0.1V_{DDP} 0.4 0.1V_{DDP} 0.4	V
	Output High Voltage 2.5V I/O, High Drive (OB25H) 2.5V I/O, Low Drive (OB25L)	I_{OL} = 5.0 mA I_{OL} = 12.0 mA I_{OL} = 16.0 mA I_{OL} = 2.5 mA I_{OL} = 5.0 mA I_{OL} = 8.0 mA	 		0.2 0.4 0.7 0.2 0.4 0.7	V
V_{IH}	Input High Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		 2 1.7		 V_{DDP} + 0.3 V_{DDP} + 0.3	V
V_{IL}	Input Low Voltage 3.3V LVTTL/LVCMOS 2.5V Mode		 –0.3 –0.3		 0.8 0.7	V
$\lvert I_{IN} \rvert$ [2]	Input Current LVTTL/LVCMOS LVTTL/LVCMOS	 with pull-up without pull-up	 30		 300 10	 µA µA
I_{DDQ}	Quiescent Supply Current	V_{IN} = V_{SS} [3] or V_{DDL}		4.0	10	mA
I_{DDQI} [4]	Incremental Quiescent Supply Current			70	400	µA
I_{OZ}	3-State Output Leakage Current	V_{OH} = V_{SS} or V_{DDL}			10	µA

Notes:

1. *All process conditions. Junction Temperature: –40 to +110°C.*
2. *Current is negative.*
3. *No pull-up resistor.*
4. *I_{DDQ} is augmented by I_{DDQI} for each 2.5V I/O when operating in a mixed voltage environment.*

DC Electrical Specifications (V_{DDP} = 3.3V) (Continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$\lvert I_{OSH} \rvert$ [2]	Output Short Circuit Current High 3.3V High Drive 3.3 Low Drive 2.5V High Drive 2.5 Low Drive				 200 140 120 100	mA
I_{OSL}	Output Short Circuit Current Low 3.3V High Drive 3.3 Low Drive 2.5V High Drive 2.5 Low Drive				 160 150 160 50	mA
$C_{I/O}$	I/O Pad Capacitance				10	pF
C_{CLK}	Clock Input Pad Capacitance				10	pF

Notes:

1. *All process conditions. Junction Temperature: –40 to +110°C.*
2. *Current is negative.*
3. *No pull-up resistor.*
4. *I_{DDQ} is augmented by I_{DDQI} for each 2.5V I/O when operating in a mixed voltage environment.*

DC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
V_{DDL}	Supply Voltage for Core		2.3	2.7	V
V_{DDP}	Supply Voltage for I/O Ring		3.0	3.6	V
V_{IH}	Input High Voltage		$0.5V_{DPP}$	V_{DPP} + 0.5	V
V_{IL}	Input Low Voltage		–0.5	$0.3V_{DDP}$	V
I_{IPU}	Input Pull-up Voltage[1]		$0.7V_{DDP}$		V
I_{IL}	Input Leakage Current[2]	$0 < V_{IN} < V_{CCI}$	–10	+10	µA
V_{OH}	Output High Voltage	I_{OUT} = –500 µA	$0.9V_{DPP}$		V
V_{OL}	Output Low Voltage	I_{OUT} = 1500 µA		$0.1V_{DPP}$	V
C_{IN}	Input Pin Capacitance[3]			10	pF
C_{CLK}	CLK Pin Capacitance		5	12	pF

Notes:

1. *This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization should assure that the input buffer is conducting minimum current at this input voltage.*
2. *Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.*
3. *Absolute maximum pin capacitance for a PCI input is 10 pF (except for CLK).*

AC Specifications (3.3V PCI Operation)

Symbol	Parameter	Condition	Min.	Max.	Units
$I_{OH(AC)}$	Switching Current High	$0 < V_{OUT} \le 0.3V_{CCI}$ [1]	$-12V_{CCI}$		mA
		$0.3V_{CCI} \le V_{OUT} < 0.9V_{CCI}$ [1]	$(-17.1 + (V_{DDP} - V_{OUT}))$		mA
		$0.7V_{CCI} < V_{OUT} < V_{CCI}$ [1, 2]		Equation A on page 23	
	(Test Point)	$V_{OUT} = 0.7V_{CC}$ [2]		$-32V_{CCI}$	mA
$I_{OL(AC)}$	Switching Current Low	$V_{CCI} > V_{OUT} \ge 0.6V_{CCI}$ [1]	$16V_{DDP}$		mA
		$0.6V_{CCI} > V_{OUT} > 0.1V_{CCI}$ [1]	$(26.7V_{OUT})$		mA
		$0.18V_{CCI} > V_{OUT} > 0$ [1, 2]		Equation B on page 23	
	(Test Point)	$V_{OUT} = 0.18V_{CC}$ [2]		$38V_{CCI}$	mA
I_{CL}	Low Clamp Current	$-3 < V_{IN} \le -1$	$-25 + (V_{IN} + 1)/0.015$		mA
I_{CH}	High Clamp Current	$V_{CCI} + 4 > V_{IN} \ge V_{CCI} + 1$	$25 + (V_{IN} - V_{DDP} - 1)/0.015$		mA
$slew_R$	Output Rise Slew Rate	$0.2V_{CCI}$ to $0.6V_{CCI}$ load [3]	1	4	V/ns
$slew_F$	Output Fall Slew Rate	$0.6V_{CCI}$ to $0.2V_{CCI}$ load [3]	1	4	V/ns

Notes:

1. *Refer to the V/I curves in Figure 18 on page 23. Switching current characteristics for REQ# and GNT# are permitted to be one half of that specified here; i.e., half size output drivers may be used on these signals. This specification does not apply to CLK and RST#, which are system outputs. "Switching Current High" specifications are not relevant to SERR#, INTA#, INTB#, INTC#, and INTD#, which are open drain outputs.*
2. *Maximum current requirements must be met as drivers pull beyond the last step voltage. Equations defining these maximums (A and B) are provided with the respective diagrams in Figure 18 on page 23. The equation defined maxima should be met by design. In order to facilitate component testing, a maximum current test point is defined for each side of the output driver.*
3. *This parameter is to be interpreted as the cumulative edge rate across the specified range, rather than the instantaneous rate at any point within the transition range. The specified load (diagram below) is optional; i.e., the designer may elect to meet this parameter with an unloaded output per the latest revision of the PCI Local Bus Specification. However, adherence to both maximum and minimum parameters is required (the maximum is no longer simply a guideline). Rise slew rate does not apply to open drain outputs.*

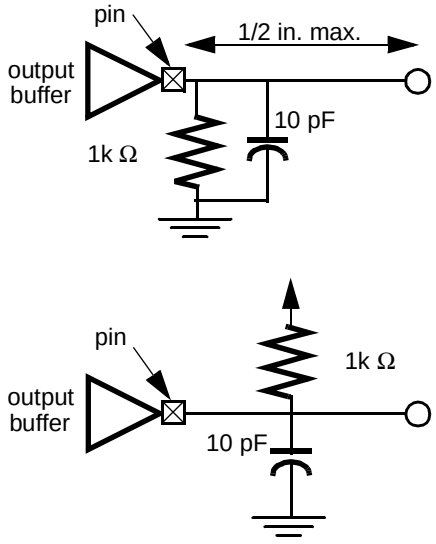


Figure 18 shows the 3.3V PCI V/I curve and the minimum and maximum PCI drive characteristics of the ProASIC family.

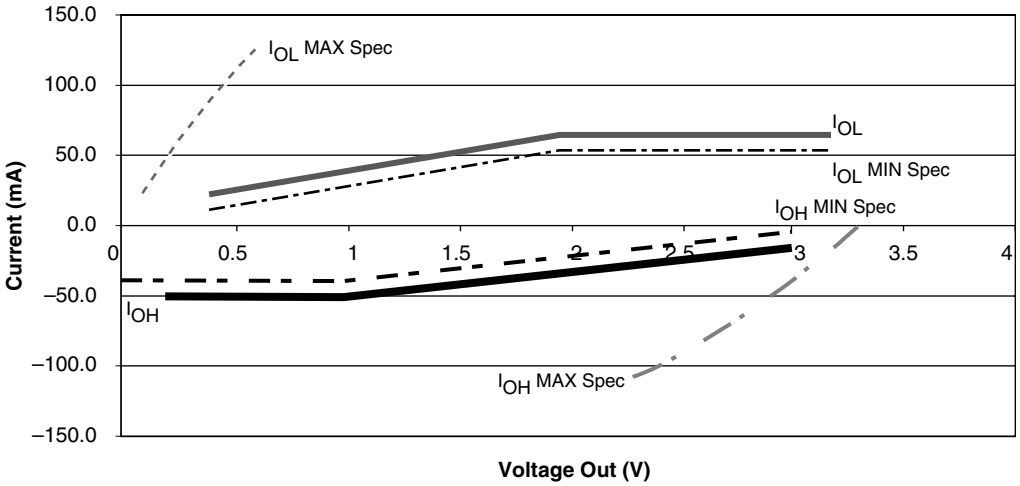


Figure 18 • 3.3V PCI V/I Curve for ProASIC Family

Equation A

$$I_{OH} = (98.0/V_{CCI}) * (V_{OUT} - V_{CCI}) * (V_{OUT} + 0.4V_{CCI})$$
$$\text{for } 0.7\ V_{CCI} < V_{OUT} < V_{CCI}$$

Equation B

$$I_{OL} = (256/V_{CCI}) * V_{OUT} * (V_{CCI} - V_{OUT})$$
$$\text{for } 0V < V_{OUT} < 0.18\ V_{CCI}$$

Timing Characteristics

Timing characteristics for ProASIC 500K devices fall into three categories: family dependent, device dependent, and design-dependent. The input and output buffer characteristics are common to all ProASIC 500K family members. Internal routing delays are device-dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are completed. Design timing attributes may then be determined by using Timer, the Static Analysis tool embedded into Designer software, or performing simulation with post-layout delays using ModelSim Simulator integrated into Libero design environment.

Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most critical timing paths. Critical nets are determined by net property assignment prior to placement and routing. Up to 6 percent of the nets in a design may be designated as critical, while more than 90% of the nets in a design are typical. User's can control priorities between critical nets and use routing constraints, such as set_critical to focus the routing optimization on the most critical ones. Please see the *Designer User's Guide* for more information on using constraints.

Very Long Lines

Some nets in the design are very long lines marked using VLLs, which are special routing resources that span multiple rows, columns, or modules. This increases capacitance and resistance, resulting in longer net delays for macros connected to long tracks. Typically, up to 6 percent of nets in a fully utilized device require long tracks. Very long lines contribute between 4 and 8.4ns routing delay depending on the fanout. This additional delay is represented statistically in higher fanout routing delays.

Timing Derating

Since ProASIC 500K devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications).

Temperature and Voltage Derating Factors

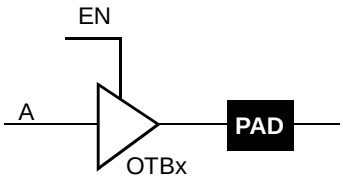
(Normalized to Worst-Case Commercial, T_J = 70°C, V_{CCA} = 2.3V)

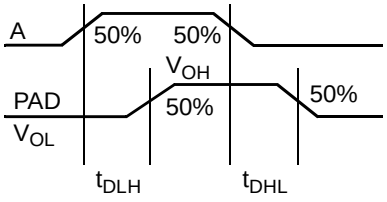
	Junction Temperature (T_J)							
V_{CCA}	–55°C	–40°C	0°C	25°C	70°C	85°C	110°C	125°C
2.3V	0.84	0.86	0.91	0.94	1.00	1.02	1.05	1.07
2.5V	0.81	0.83	0.87	0.90	0.96	0.98	1.01	1.02
2.7V	0.77	0.79	0.84	0.86	0.92	0.93	0.96	0.98

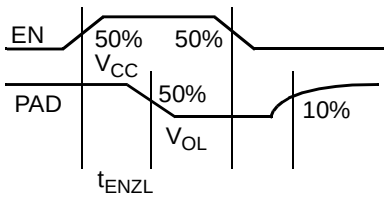
Slew Rates Measured at C_{out} = 10pF (Total Output Load), Nominal Power Supplies and 25°C

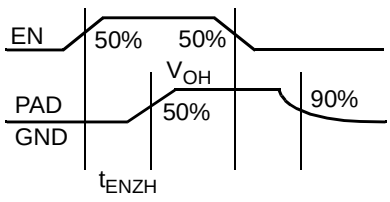
Type	Trig. Lev.	Rising Edge	Slew Rate	Falling Edge	Slew Rate
		pS	V/nS	pS	V/nS
OB33PH	20%-60%	397	3.33	390	-3.38
OB33PN	20%-60%	463	2.85	450	-2.93
OB33PL	20%-60%	567	2.33	527	-2.51
OB33LH	20%-60%	467	2.83	700	-1.89
OB33LN	20%-60%	620	2.13	767	-1.72
OB33LL	20%-60%	813	1.62	1100	-1.20
OB25HH	20%-60%	750	1.33	310	-3.23
OB25HN	20%-60%	850	1.18	390	-2.56
OB25HL	20%-60%	1310	0.76	510	-1.96
OB25LH	20%-60%	793	1.26	430	-2.33
OB25LN	20%-60%	870	1.15	730	-1.37
OB25LL	20%-60%	1287	0.78	1037	-0.96
OB25LPHH	20%-60%	470	2.13	433	-2.31
OB25LPHN	20%-60%	533	1.81	527	-1.90
OB25LPHL	20%-60%	770	1.30	753	-1.33
OB25LPLH	20%-60%	597	1.68	707	-1.42
OB25LPLN	20%-60%	873	1.15	760	-1.32
OB25LPLL	20%-60%	1153	0.87	1563	-0.54

Tristate Buffer Delays









Tristate Buffer Delays

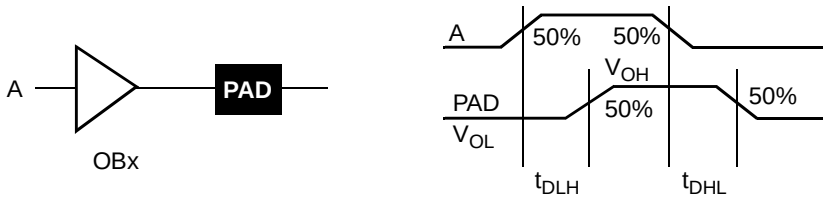
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max t_{DLH}	Max t_{DHL}	Max t_{ENZH}	Max t_{ENZL}	Units
OTB33PH	3.3V, PCI Output Current, High Slew Rate	4.2	4.1	4.2	3.67	ns
OTB33PN	3.3V, PCI Output Current, Nominal Slew Rate	4.7	5.9	4.8	5.3	ns
OTB33PL	3.3V, PCI Output Current, Low Slew Rate	5.3	7.0	5.3	6.6	ns
OTB33LH	3.3V, Low Output Current, High Slew Rate	6.0	6.6	6.0	5.9	ns
OTB33LN	3.3V, Low Output Current, Nominal Slew Rate	6.7	9.2	6.7	8.9	ns
OTB33LL	3.3V, Low Output Current, Low Slew Rate	7.5	12.0	7.5	11.8	ns
OTB25HH	2.5V, High Output Current, High Slew Rate	6.9	3.6	6.9	3.4	ns
OTB25HN	2.5V, High Output Current, Nominal Slew Rate	7.2	5.2	7.2	4.9	ns
OTB25HL	2.5V, High Output Current, Low Slew Rate	8.2	6.4	8.2	6.1	ns
OTB25LH	2.5V, Low Output Current, High Slew Rate	10.4	5.5	10.4	5.2	ns
OTB25LN	2.5V, Low Output Current, Nominal Slew Rate	11.0	8.3	11.0	8.1	ns
OTB25LL	2.5V, Low Output Current, Low Slew Rate	11.9	10.9	11.9	11.7	ns
OTB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.1	5.1	5.1	4.4	ns
OTB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	6.0	7.7	6.0	7.4	ns
OTB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	6.9	9.8	6.8	9.3	ns
OTB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	7.4	8.6	7.4	7.8	ns
OTB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	8.6	12.6	8.5	12.3	ns
OTB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	9.8	17.0	9.8	16.7	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*
3. *t_{ENZH} = Enable-to-Pad, Z to HIGH*
4. *t_{ENZL} = Enable-to-Pad, Z to LOW*

Output Buffer Delays



Output Buffer Delays

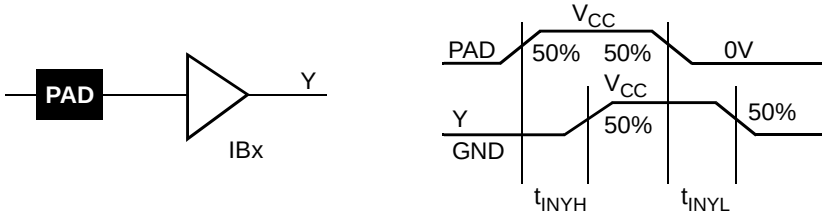
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max. t_{DLH}	Max. t_{DHL}	Units
OB33PH	3.3V, PCI Output Current, High Slew Rate	4.2	4.1	ns
OB33PN	3.3V, PCI Output Current, Nominal Slew Rate	4.7	5.9	ns
OB33PL	3.3V, PCI Output Current, Low Slew Rate	5.3	7.1	ns
OB33LH	3.3V, Low Output Current, High Slew Rate	6.0	6.6	ns
OB33LN	3.3V, Low Output Current, Nominal Slew Rate	6.7	9.2	ns
OB33LL	3.3V, Low Output Current, Low Slew Rate	7.5	12.1	ns
OB25HH	2.5V, High Output Current, High Slew Rate	6.9	3.6	ns
OB25HN	2.5V, High Output Current, Nominal Slew Rate	7.2	5.2	ns
OB25HL	2.5V, High Output Current, Low Slew Rate	8.2	6.4	ns
OB25LH	2.5V, Low Output Current, High Slew Rate	10.4	5.5	ns
OB25LN	2.5V, Low Output Current, Nominal Slew Rate	11.0	8.3	ns
OB25LL	2.5V, Low Output Current, Low Slew Rate	11.9	10.9	ns
OB25LPHH	2.5V, Low Power, High Output Current, High Slew Rate	5.1	5.1	ns
OB25LPHN	2.5V, Low Power, High Output Current, Nominal Slew Rate	6.0	7.7	ns
OB25LPHL	2.5V, Low Power, High Output Current, Low Slew Rate	6.9	9.8	ns
OB25LPLH	2.5V, Low Power, Low Output Current, High Slew Rate	7.4	8.6	ns
OB25LPLN	2.5V, Low Power, Low Output Current, Nominal Slew Rate	8.6	12.6	ns
OB25LPLL	2.5V, Low Power, Low Output Current, Low Slew Rate	9.8	17.0	ns

Notes:

1. *t_{DLH} = Data-to-Pad HIGH*
2. *t_{DHL} = Data-to-Pad LOW*

Input Buffer Delays



Input Buffer Delays

(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
IB25	2.5V, CMOS Input Levels, No Pull-up Resistor	2.2	0.7	ns
IB25LP	2.5V, CMOS Input Levels, Low Power	2.2	1.4	ns
IB33	3.3V, CMOS Input Levels, No Pull-up Resistor	1.9	1.0	ns

Notes:

1. *t_{INYH} = Input Pad-to-Y HIGH*
2. *t_{INYL} = Input Pad-to-Y LOW*

Global Input Buffer Delays
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Macro Type	Description	Max. t_{INYH}	Max. t_{INYL}	Units
GL25	2.5V, CMOS Input Levels	2.1	1.6	ns
GL25LP	2.5V, CMOS Input Levels	2.3	2.3	ns
GL33	3.3V, CMOS Input Levels	3.8	1.2	ns
GL25U	2.5V, CMOS Input Levels, with Pull-up Resistor	2.1	1.6	ns
GL25LPU	2.5V, CMOS Input Levels, Low Power, with Pull-up Resistor	2.3	2.3	ns
GL33U	3.3V, CMOS Input Levels, with Pull-up Resistor	3.8	1.2	ns

Predicted Global Routing Delay*
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

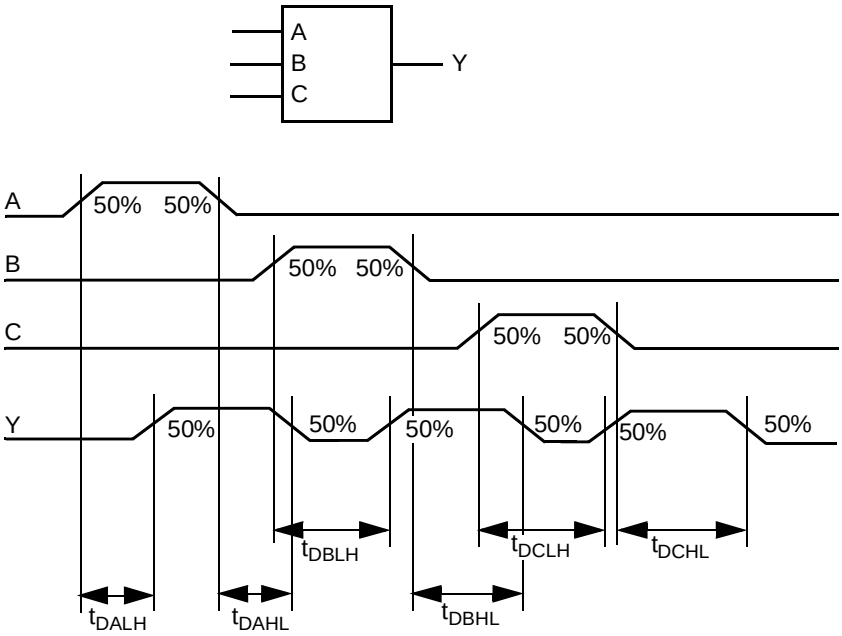
Parameter	Description	Max.	Units
t_{RCKH}	Input Low to High (fully loaded row—32 inputs)	1.2	ns
t_{RCKL}	Input High to Low (fully loaded row—32 inputs)	1.1	ns
t_{RCKH}	Input Low to High (minimally loaded row—1 input)	0.9	ns
t_{RCKL}	Input High to Low (minimally loaded row—1 input)	0.9	ns

** The timing delay difference between tile locations is less than 15ps.*

Global Routing Skew
(Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, f_{CLOCK} = 250 MHz)

Parameter	Description	Max.	Units
t_{RCKSWH}	Maximum Skew Low to High	0.3	ns
t_{RCKSHH}	Maximum Skew High to Low	0.3	ns

Module Delays



Sample Macrocell Library Listing
(Worst-Case Commercial Conditions, V_{DDL} = 2.3V, T_J = 70° C)

Cell Name	Description	Maximum Intrinsic Delay	Minimum Setup/Hold	Units
NAND2	2-Input NAND	0.4		ns
AND2	2-Input AND	0.4		ns
NOR3	3-Input NOR	0.4		ns
MUX2L	2-1 Mux with Active Low Select	0.4		ns
OA21	2-Input OR into a 2-Input AND	0.4		ns
XOR2	2-Input Exclusive OR	0.3		ns
LDL	Active Low Latch (LH/HL)	D: 0.3/0.2	t_{setup} 0.5 t_{hold} 0.2	ns
DFFL	Negative Edge-Triggered D-type Flip-Flop (LH/HL)	CLK-Q: 0.4/0.4	t_{setup} 0.4 t_{hold} 0.2	ns

Note: *Assumes fanout of two.*

Embedded Memory Specifications

This section focuses on the embedded memory of the ProASIC 500K family. It describes the SRAM and FIFO interface signals and includes timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 4 and Table 5 on page 34). Refer to Table 3 on page 12 for basic RAM configurations. Simultaneous Read and Write to the same location must be done with care. On such accesses the DI bus is output to the DO bus.

Enclosed Timing Diagrams—SRAM Mode:

- Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Asynchronous RAM Write
- Asynchronous RAM Read, Address Controlled, RDB=0
- Asynchronous RAM Read, RDB Controlled
- Synchronous RAM Write

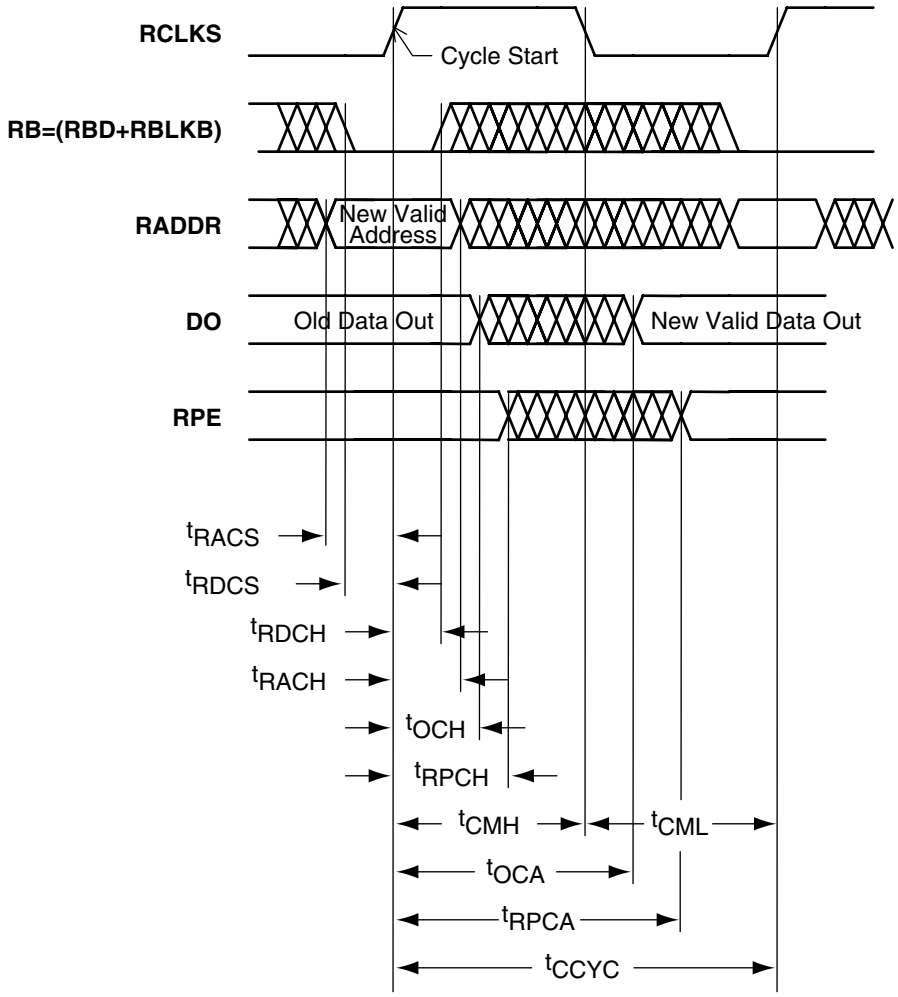
Note: *The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. However, if clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). This makes processing of this data in the same clock cycle nearly impossible. Most designers solve this problem by adding registers at all outputs of the memory to push the data processing into the next clock cycle. In this setup, the whole cycle time can be used to process the data. To simplify the use of this kind of memory setup these registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.*

Table 4 • *Memory Block SRAM Interface Signals*

SRAM Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used on synchronization on write side
RCLKS	1	IN	Read clock used on synchronization on read side
RADDR<0:7>	8	IN	Read address
RBLKB	1	IN	Negative true read block select
RDB	1	IN	Negative true read pulse
WADDR<0:7>	8	IN	Write address
WBLKB	1	IN	Negative true write block select
DI<0:8>	9	IN	Input data bits <0:8>, <8> can be used for parity in
WRB	1	IN	Negative true write pulse
DO<0:8>	9	OUT	Output data bits <0:8>, <8> can be used for parity out
RPE	1	OUT	Read parity error
WPE	1	OUT	Write parity error
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

Note: *Not all signals shown are used in all modes.*

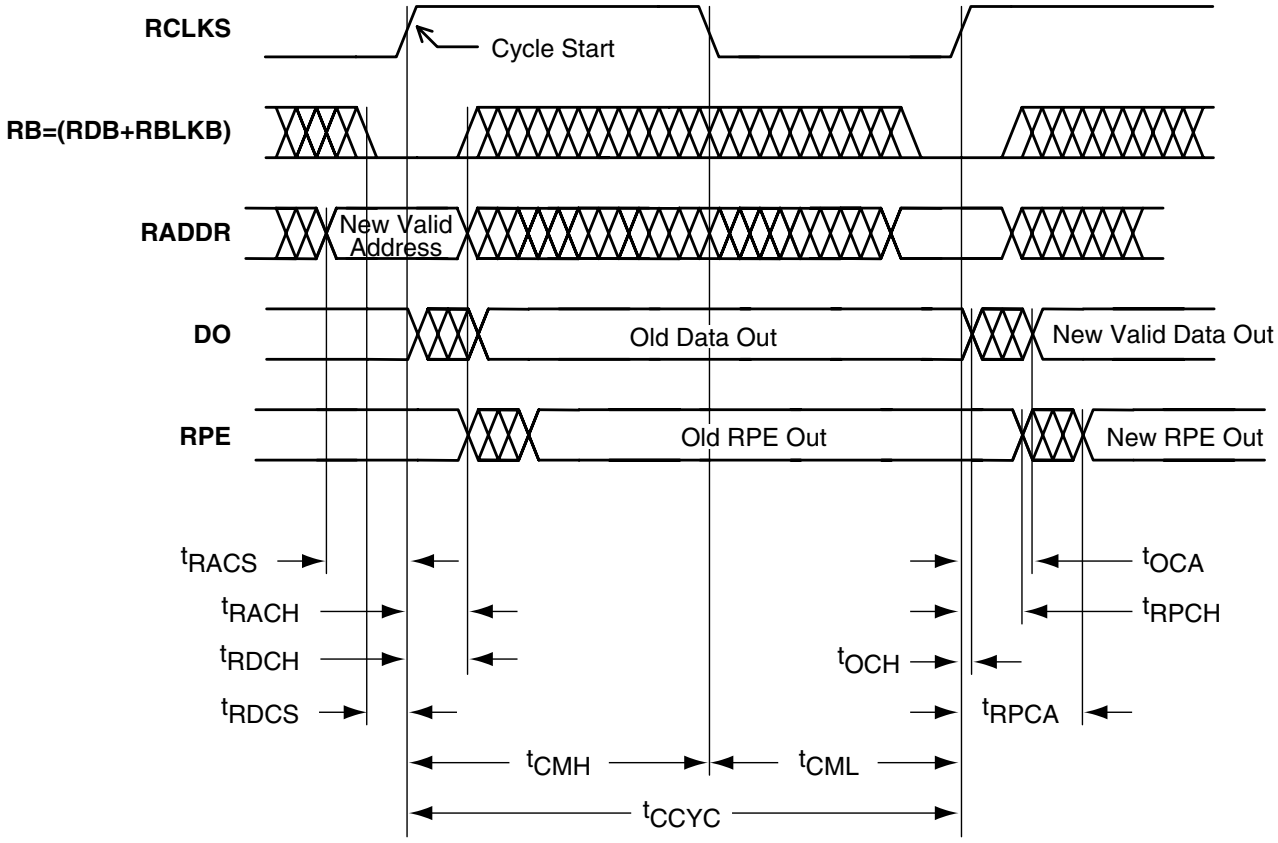
Synchronous RAM Read, Access Timed Output Strobe (Synchronous Transparent)



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	

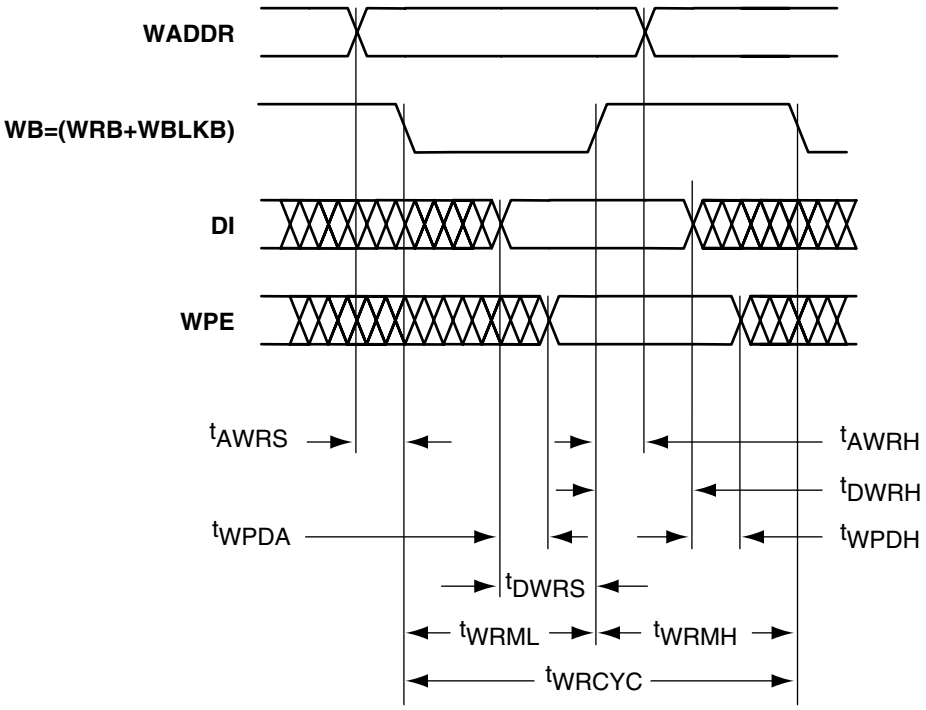
Synchronous RAM Read, Pipeline Mode Outputs (Synchronous Pipelined)



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		.75	ns	
RACH	RADDR hold from RCLKS ↑	0.5		ns	
RACS	RADDR setup to RCLKS ↑	1.0		ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	

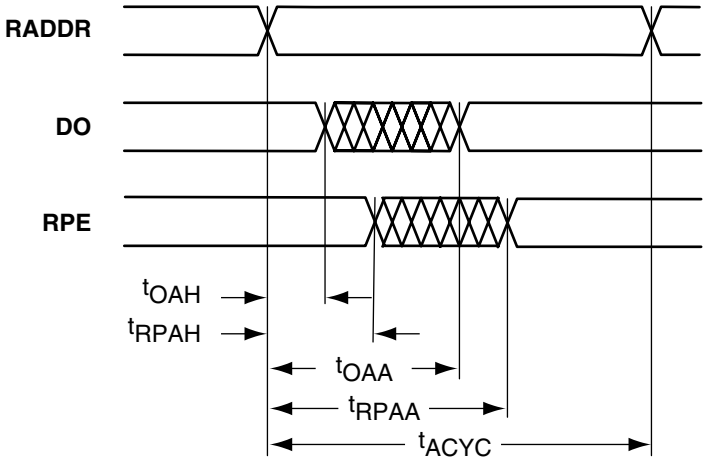
Asynchronous RAM Write



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
AWRH	WADDR hold from WB ↑	1.0		ns	
AWRS	WADDR setup to WB ↓	0.5		ns	
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
WPDA	WPE access from DI	3.0		ns	WPE is invalid while
WPDH	WPE hold from DI		1.0	ns	PARGEN is active
WRCYC	Cycle time	7.5		ns	
WRMH	WB high phase	3.0		ns	Inactive
WRML	WB low phase	3.0		ns	Active

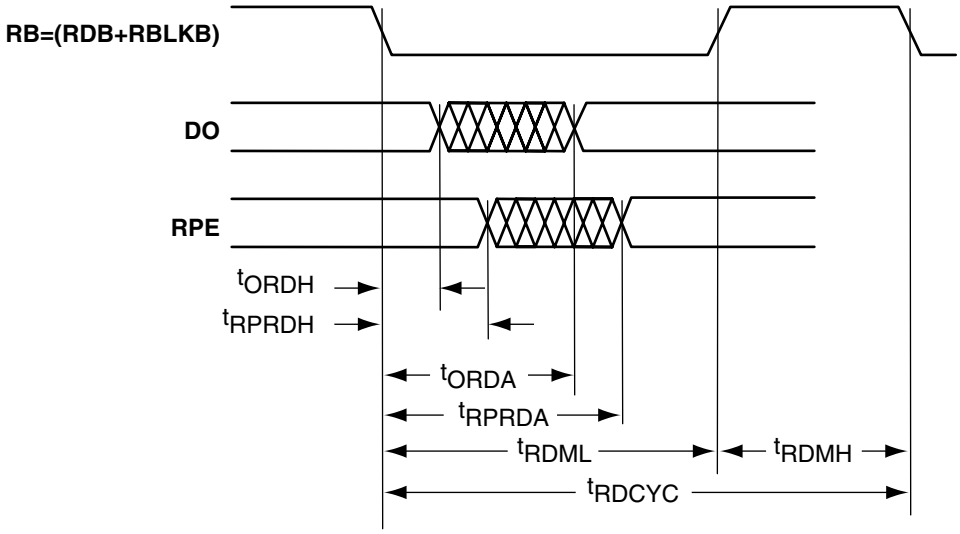
Asynchronous RAM Read, Address Controlled, RDB=0



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ACYC	Read cycle time	7.5		ns	
OAA	New DO access from RADDR stable	7.5		ns	
OAH	Old DO hold from RADDR stable		3.0	ns	
RPAA	New RPE access from RADDR stable	10.0		ns	
RPAH	Old RPE hold from RADDR stable		3.0	ns	

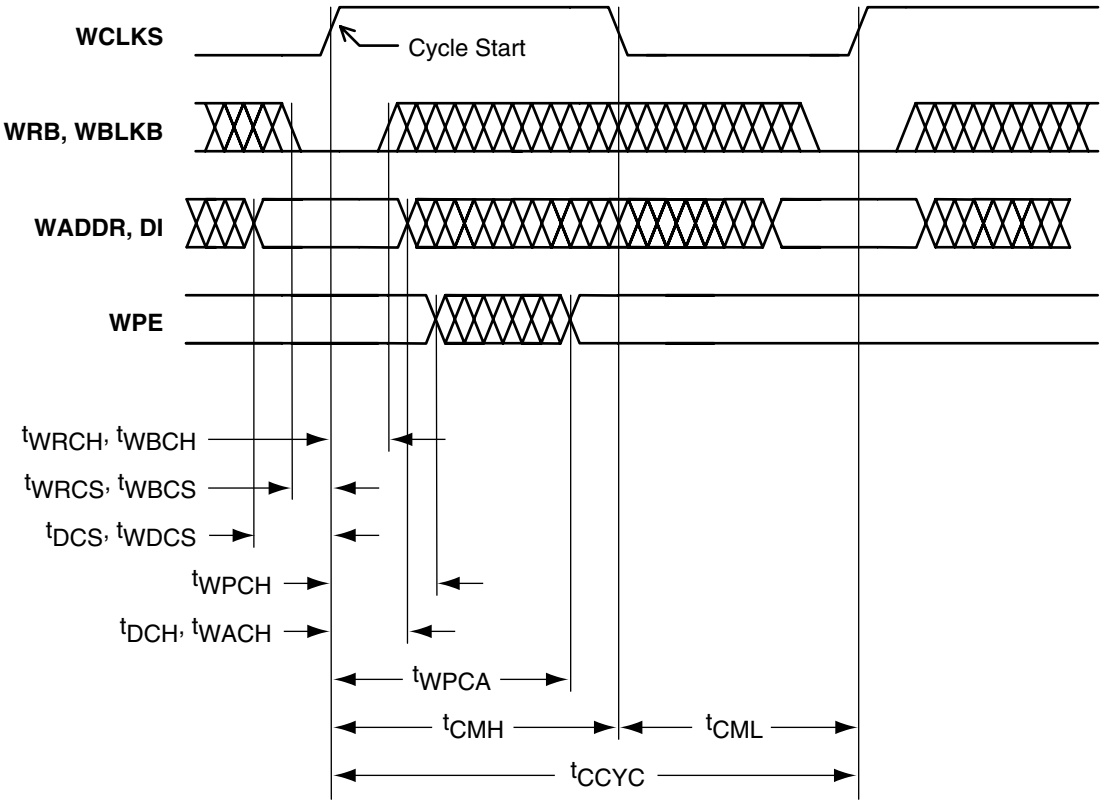
Asynchronous RAM Read, RDB Controlled



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDMH	RB high phase	3.0		ns	Inactive setup to new cycle
RDML	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		3.0	ns	

Synchronous RAM Write



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
WACH	WADDR hold from WCLKS ↑	0.5		ns	
WDCS	WADDR setup to WCLKS ↑	1.0		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note: *On simultaneous read and write accesses to the same location DI is output to DO.*

Asynchronous FIFO Full and Empty Transitions

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write (read) operation changes from inhibited to accepted after the read (write) signal which causes the transition from full (empty) to not full (empty) is indeterminate. This indeterminate period starts 1ns after the RB (WB) transition which deactivates full (not empty). For slow cycles, the indeterminate period ends 3ns after the RB (WB) transition. For fast cycles, this period ends either 3ns or (7.5ns - t_{RDL} (t_{WRL})) after the RB (WB) transition, whichever is later.

The timing diagram for write is shown in Figure 19 on page 35. The timing diagram for read is shown in Figure 20 on page 35. For basic RAM configurations, see Table 3 on page 12. For memory block interface signals, see Table 4 on page 28, and for memory block FIFO signals, see Table 5.

Enclosed Timing Diagrams—FIFO Mode:

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

Table 5 • *Memory Block FIFO Interface Signals*

FIFO Signal	Bits	In/Out	Description
WCLKS	1	IN	Write clock used to synchronize write side
RCLKS	1	IN	Read clock used to synchronize read side
LEVEL <0:7>	8	IN	Direct configuration implements static flag logic
RBLKB	1	IN	Active low read block select
RDB	1	IN	Active low read pulse
RESET	1	IN	Active low reset for FIFO pointers
WBLKB	1	IN	Active low write block select
DI<0:8>	9	IN	Input data bits <0:8>, <8> can be used for parity in.
WRB	1	IN	Active low write pulse
FULL, EMPTY	2	OUT	FIFO flags. FULL prevents write and EMPTY prevents read
EQTH, GEQTH	2	OUT	EQTH is true when the FIFO holds (LEVEL) words. GEQTH is true when the FIFO holds (LEVEL) words or more
DO<0:8>	9	OUT	Output data bits <0:8>, <8> can be used for parity out.
RPE	1	OUT	Read parity error
WPE	1	OUT	Write parity error
LGDEP <0:2>	3	IN	Configures DEPTH of the FIFO to $2^{(LGDEP+1)}$
PARODD	1	IN	Selects odd parity generation/detect when high, even when low

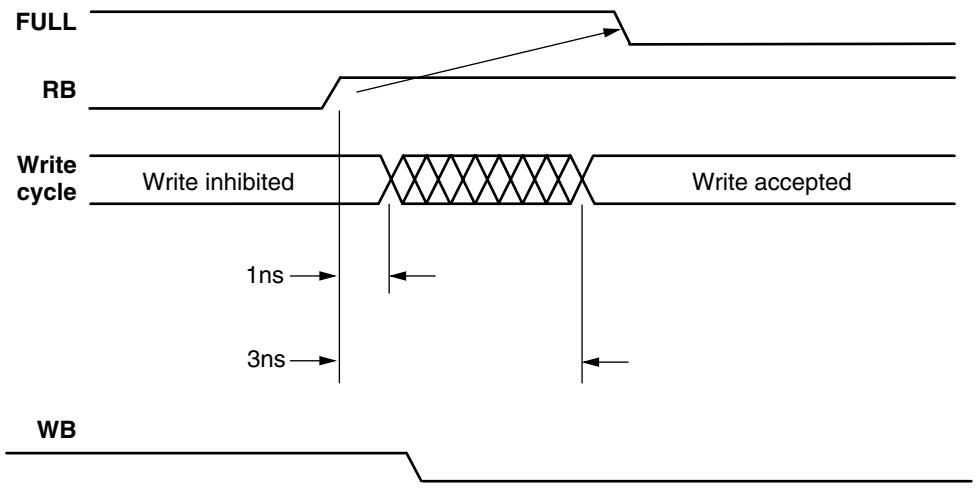


Figure 19 • *Write Timing Diagram*

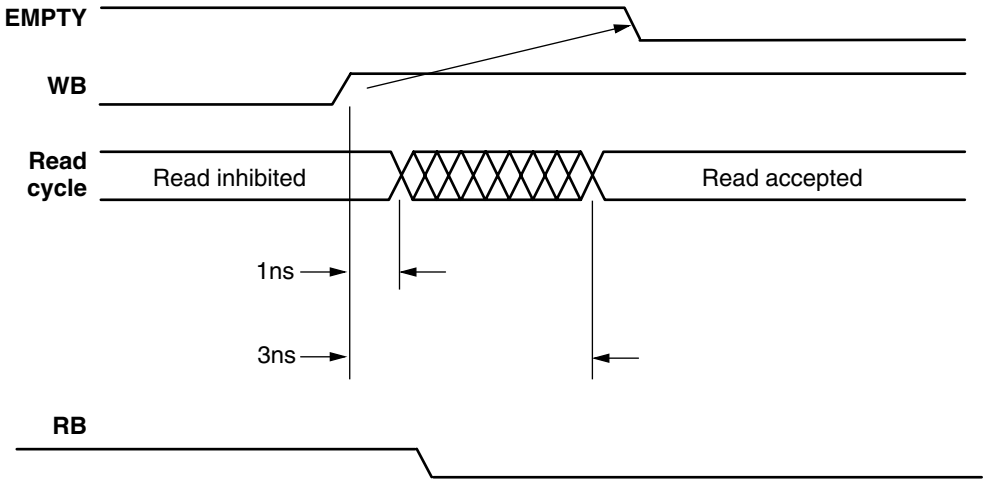
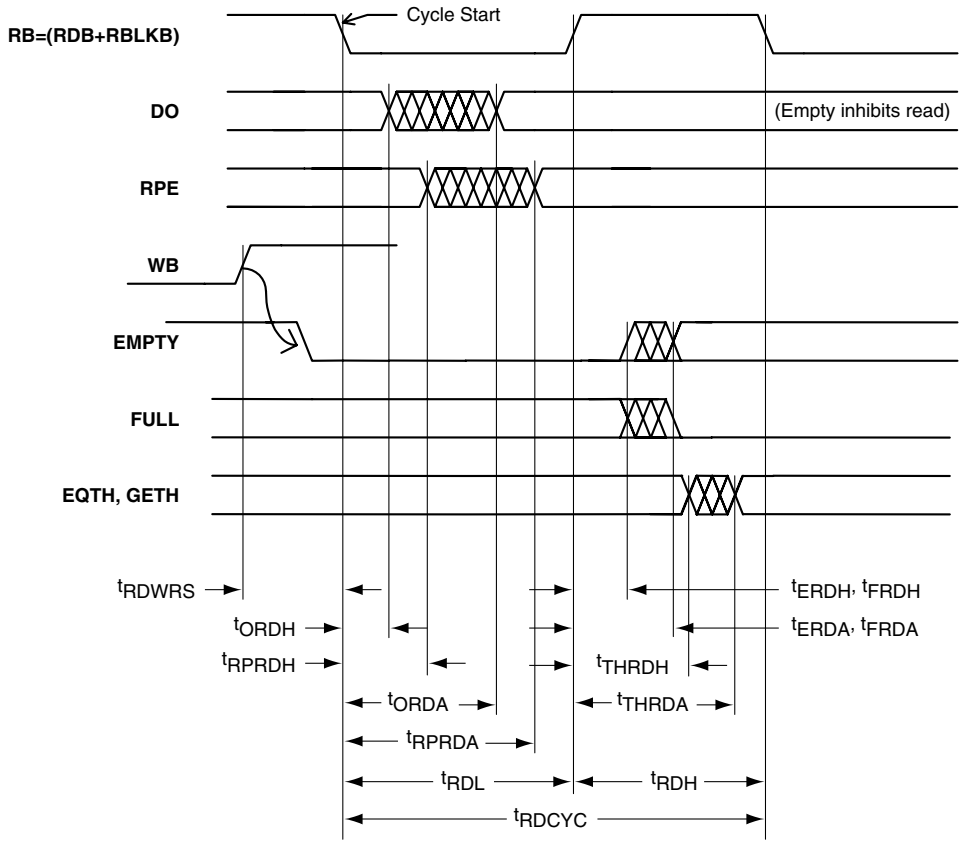


Figure 20 • *Read Timing Diagram*

Asynchronous FIFO Read



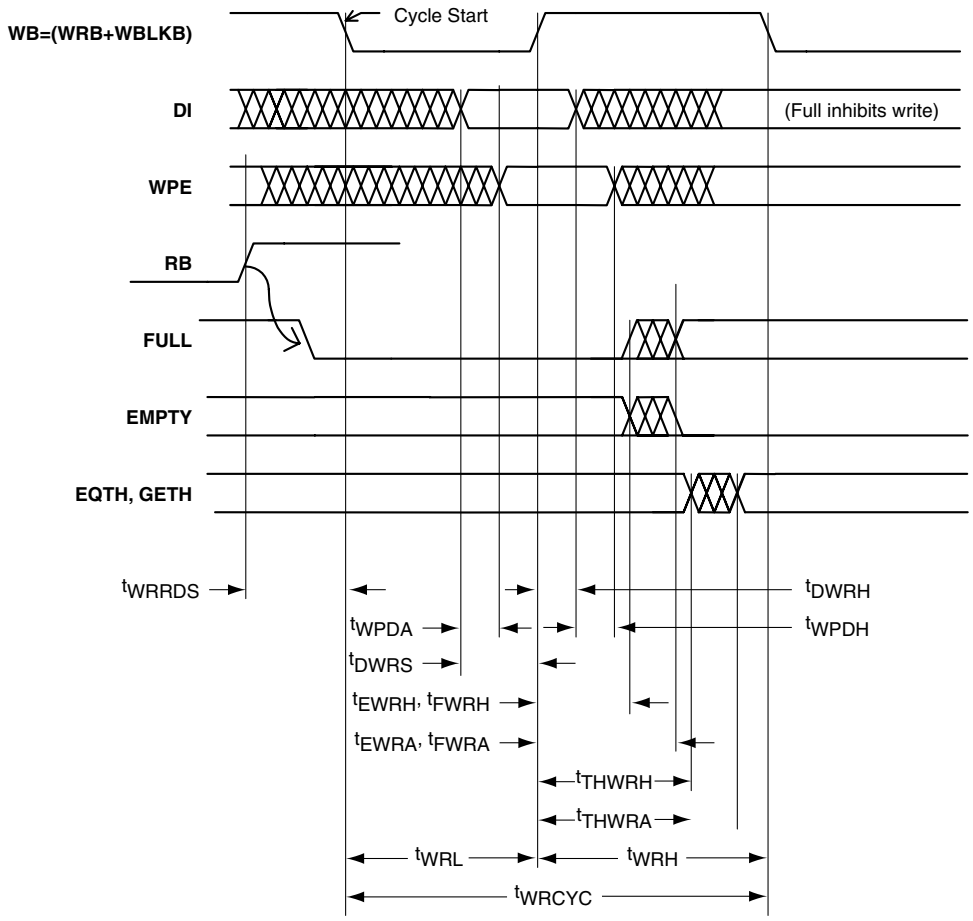
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
ERDH, FRDH, THRDH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
ERDA	New EMPTY access from RB ↑	3.0[1]		ns	
FRDA	FULL↓ access from RB ↑	3.0[1]		ns	
ORDA	New DO access from RB ↓	7.5		ns	
ORDH	Old DO valid from RB ↓		3.0	ns	
RDCYC	Read cycle time	7.5		ns	
RDWRS	WB ↑, clearing EMPTY, setup to	3.0[2]		ns	Enabling the read operation
	RB ↓		1.0	ns	Inhibiting the read operation
RDH	RB high phase	3.0		ns	Inactive
RDL	RB low phase	3.0		ns	Active
RPRDA	New RPE access from RB ↓	9.5		ns	
RPRDH	Old RPE valid from RB ↓		4.0	ns	
THRDA	EQTH or GETH access from RB↑	4.5		ns	

Notes:

1. *At fast cycles, ERDA & FRDA = MAX ((7.5ns – RDL), 3.0ns)*
2. *At fast cycles, RDWRS (for enabling read) = MAX ((7.5ns – WRL), 3.0ns)*

Asynchronous FIFO Write



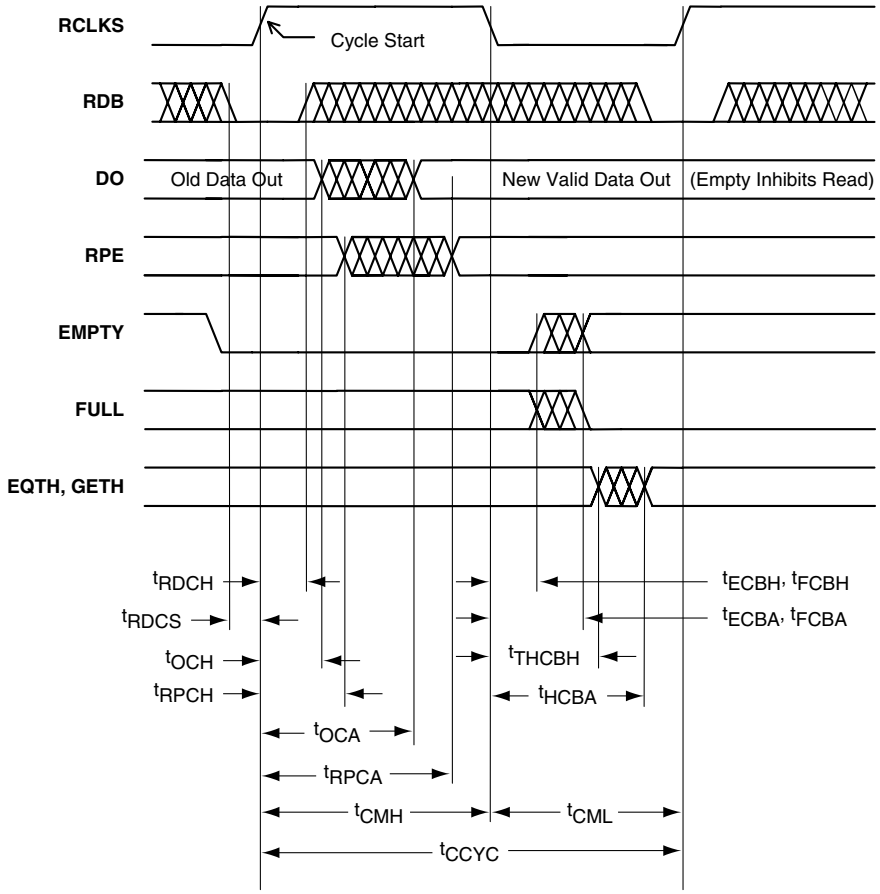
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
DWRH	DI hold from WB ↑	1.5		ns	
DWRS	DI setup to WB ↑	0.5		ns	PARGEN is inactive
DWRS	DI setup to WB ↑	2.5		ns	PARGEN is active
EWRH, FWRH, THWRH	Old EMPTY, FULL, EQTH, & GETH valid hold time after WB ↑		0.5	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
EWRA	EMPTY ↓ access from WB ↑	3.0[1]		ns	
FWRA	New FULL access from WB ↑	3.0[1]		ns	
THWRA	EQTH or GETH access from WB ↑	4.5		ns	
WPDA	WPE access from DI	3.0		ns	WPE is invalid while PARGEN is active
WPDH	WPE hold from DI		1.0	ns	
WRCYC	Cycle time	7.5		ns	
WRRDS	RB ↑, clearing FULL, setup to WB ↓	3.0[2]		ns	Enabling the write operation
			1.0		Inhibiting the write operation
WRH	WB high phase	3.0		ns	Inactive
WRL	WB low phase	3.0		ns	Active

Notes:

1. *At fast cycles, EWRA, FWRA = MAX ((7.5ns – WRL), 3.0ns)*
2. *At fast cycles, WRRDS (for enabling write) = MAX ((7.5ns – RDL), 3.0ns)*

Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



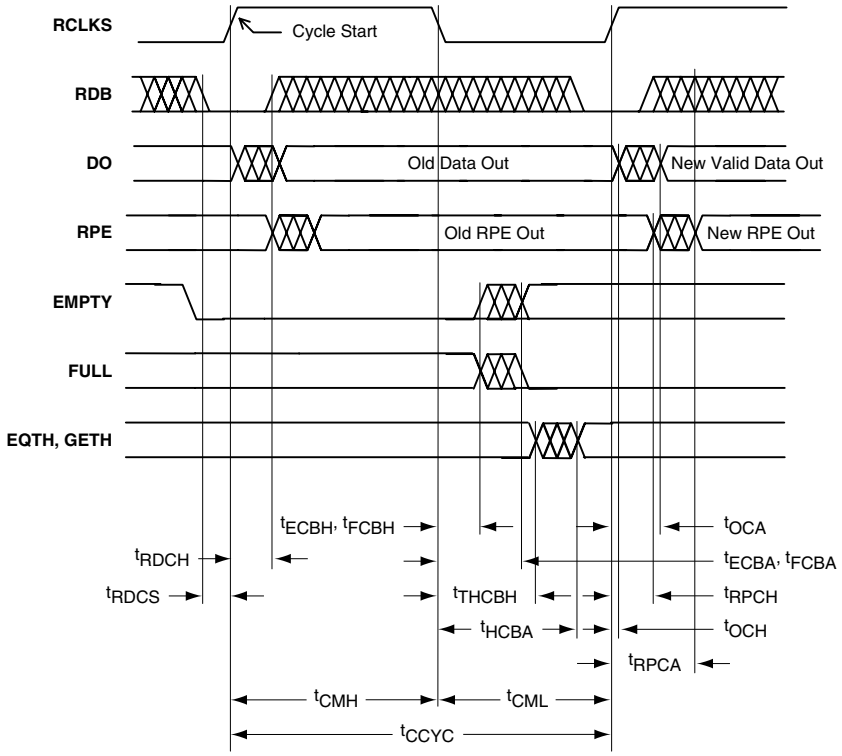
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	7.5		ns	
OCH	Old DO valid from RCLKS ↑		3.0	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	9.5		ns	
RPCH	Old RPE valid from RCLKS ↑		3.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX ((7.5ns – CMH), 3.0ns)

Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



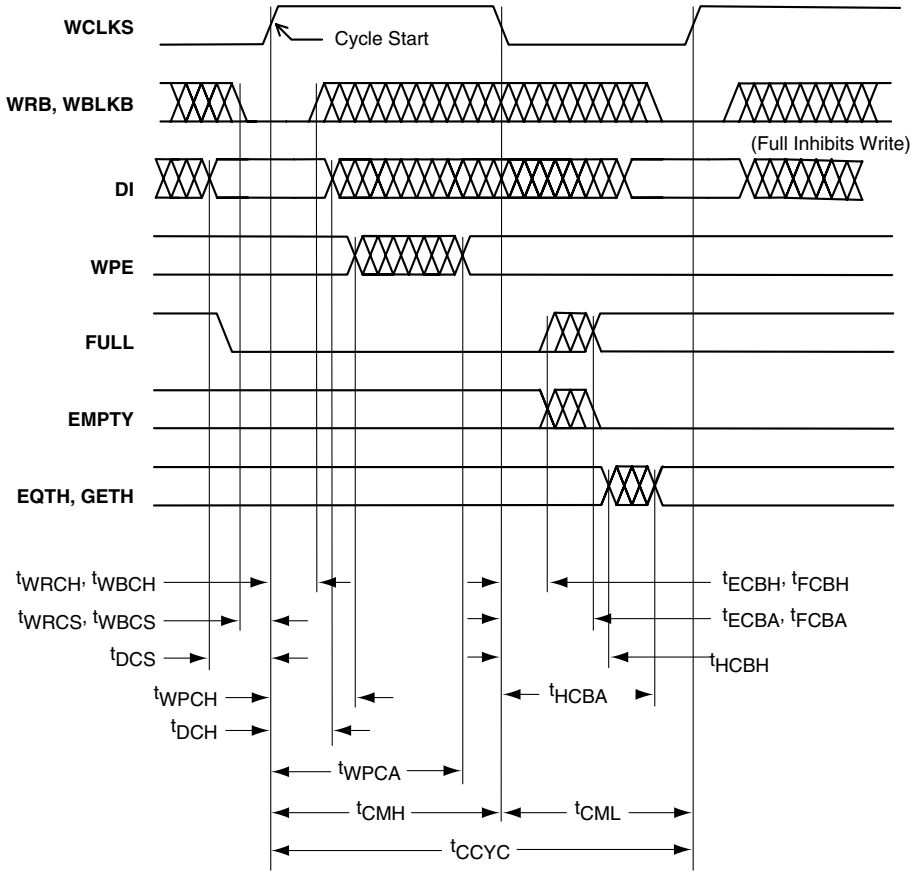
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
ECBA	New EMPTY access from RCLKS ↓	3.0[1]		ns	
FCBA	FULL ↓ access from RCLKS ↓	3.0[1]		ns	
ECBH, FCBH, THCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
OCA	New DO access from RCLKS ↑	2.0		ns	
OCH	Old DO valid from RCLKS ↑		0.75	ns	
RDCH	RDB hold from RCLKS ↑	0.5		ns	
RDCS	RDB setup to RCLKS ↑	1.0		ns	
RPCA	New RPE access from RCLKS ↑	4.0		ns	
RPCH	Old RPE valid from RCLKS ↑		1.0	ns	
HCBA	EQTH or GETH access from RCLKS ↓	4.5		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX ((7.5ns – CMS), 3.0ns)

Synchronous FIFO Write



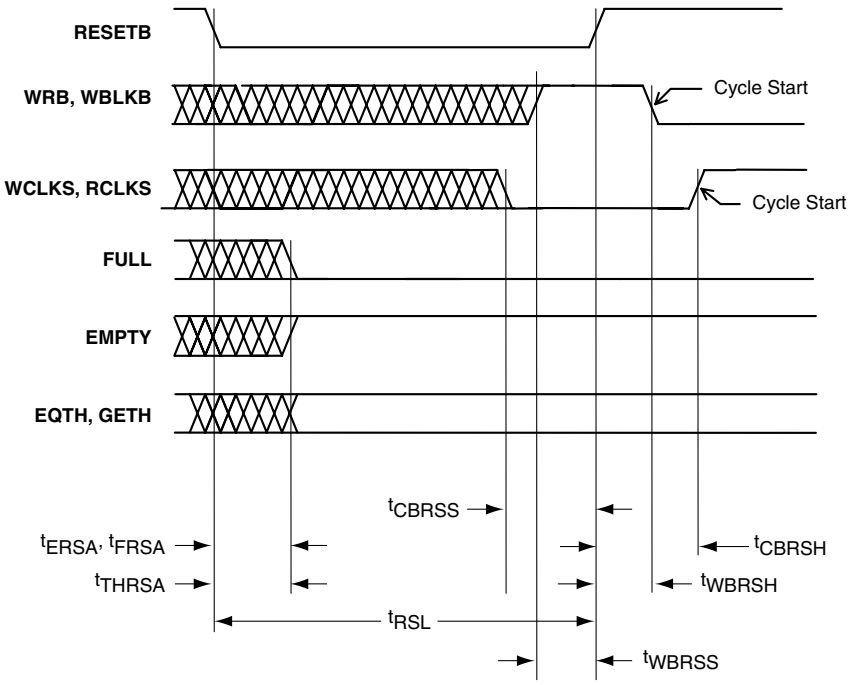
T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CCYC	Cycle time	7.5		ns	
CMH	Clock high phase	3.0		ns	
CML	Clock low phase	3.0		ns	
DCH	DI hold from WCLKS ↑	0.5		ns	
DCS	DI setup to WCLKS ↑	1.0		ns	
FCBA	New FULL access from WCLKS ↓	3.0[1]		ns	
ECBA	EMPTY↓ access from WCLKS ↓	3.0[1]		ns	
ECBH, FCBH, HCBH	Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS ↓		1.0	ns	Empty/full/thresh are invalid from the end of hold until the new access is complete
HCBA	EQTH or GETH access from WCLKS ↓	4.5		ns	
WPCA	New WPE access from WCLKS ↑	3.0		ns	WPE is invalid while PARGEN is active
WPCH	Old WPE valid from WCLKS ↑		0.5	ns	
WRCH, WBCH	WRB & WBLKB hold from WCLKS ↑	0.5		ns	
WRCS, WBCS	WRB & WBLKB setup to WCLKS ↑	1.0		ns	

Note:

1. At fast cycles, ECBA & FCBA = MAX ((7.5ns – CMH), 3.0ns)

FIFO Reset



T_J = 0°C to 110°C; V_{DDL} = 2.3V to 2.7V

Symbol t_{xxx}	Description	Min.	Max.	Units	Notes
CBRSH	WCLKS or RCLKS ↑ hold from RESETB ↑	1.5		ns	Synchronous mode only
CBRSS	WCLKS or RCLKS ↓ setup to RESETB ↑	1.5		ns	Synchronous mode only
ERSA	New EMPTY ↑ access from RESETB ↓	3.0		ns	
FRSA	FULL ↓ access from RESETB ↓	3.0		ns	
RSL	RESETB low phase	7.5		ns	
THRSA	EQTH or GETH access from RESETB ↓	4.5		ns	
WBRSH	WB ↓ hold from RESETB ↑	1.5		ns	Asynchronous mode only
WBRSS	WB ↑ setup to RESETB ↑	1.5		ns	Asynchronous mode only

Pin Description

I/O **User Input/Output**

The I/O pin functions as an input, output, three-state, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

N/C **No Connect**

To maintain compatibility with future Actel ProASIC products it is recommended that this pin not be connected to the circuitry on the board.

GL **Global Input Pin**

Low skew input pin for clock or other global signals. Input only. This pin can be configured with a pull-up resistor.

GND **Ground**

Common ground supply voltage.

V_{DDL} **Logic Array Power Supply Pin**

2.5V supply voltage.

V_{DDP} **I/O Pad Power Supply Pin**

2.5V or 3.3V supply voltage.

V_{PP} **Programming Supply Pin**

This pin must be connected to V_{DDP} during normal operation, or it can remain at 16.5V in an ISP application. This pin must not float.

V_{PN} **Programming Supply Pin**

This pin must be connected to GND during normal operation, or it can remain at –12V in an ISP application. This pin must not float.

TMS **Test Mode Select**

The TMS pin controls the use of Boundary Scan circuitry.

TCK **Test Clock**

Clock input pin for Boundary Scan.

TDI **Test Data In**

Serial input for Boundary Scan.

TDO **Test Data Out**

Serial output for Boundary Scan.

TRST **Test Reset Input**

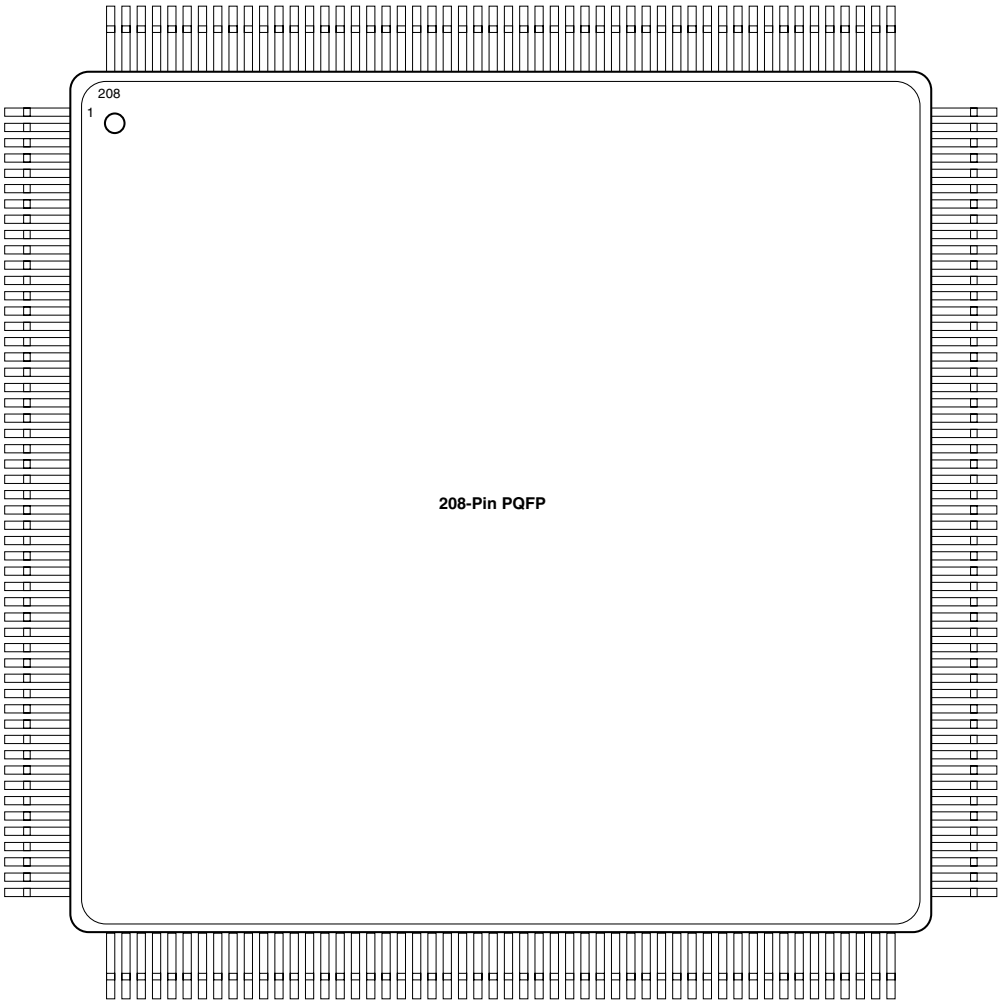
Asynchronous, active low input pin for resetting Boundary Scan circuitry.

RCK **Running Clock**

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

Package Pin Assignments

208-Pin PQFP



208-Pin PQFP

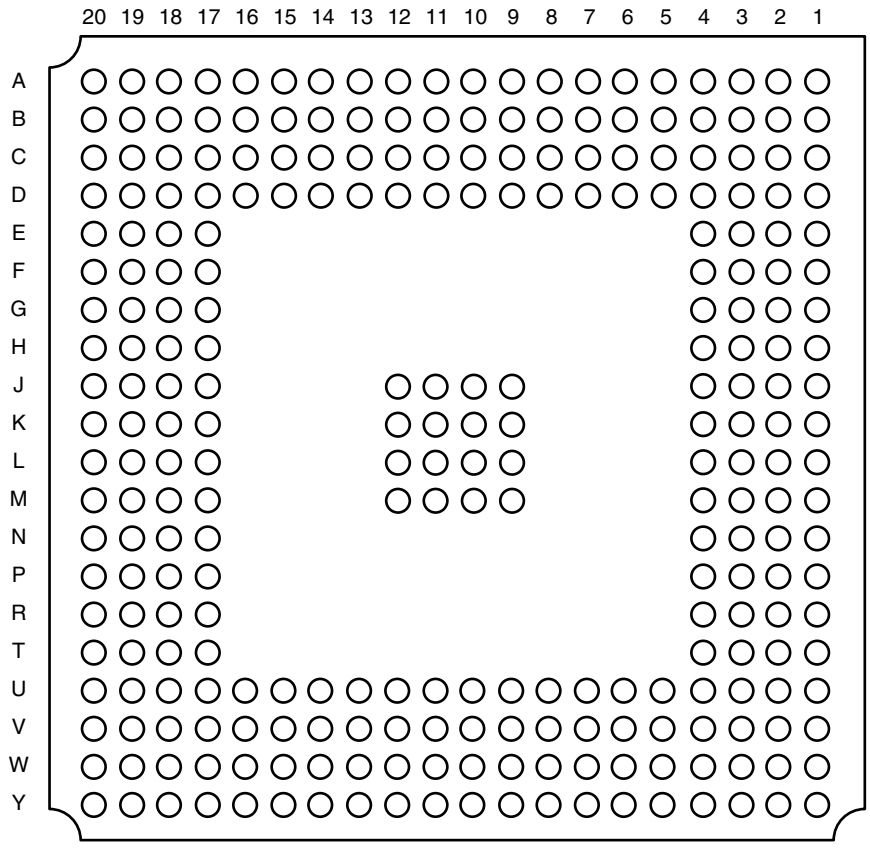
Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
1	GND	GND	GND	GND
2	I/O	I/O	I/O	I/O
3	I/O	I/O	I/O	I/O
4	I/O	I/O	I/O	I/O
5	I/O	I/O	I/O	I/O
6	I/O	I/O	I/O	I/O
7	I/O	I/O	I/O	I/O
8	I/O	I/O	I/O	I/O
9	I/O	I/O	I/O	I/O
10	I/O	I/O	I/O	I/O
11	I/O	I/O	I/O	I/O
12	I/O	I/O	I/O	I/O
13	I/O	I/O	I/O	I/O
14	I/O	I/O	I/O	I/O
15	I/O	I/O	I/O	I/O
16	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
17	GND	GND	GND	GND
18	I/O	I/O	I/O	I/O
19	I/O	I/O	I/O	I/O
20	I/O	I/O	I/O	I/O
21	I/O	I/O	I/O	I/O
22	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
23	I/O	I/O	I/O	I/O
24	I/O	I/O	I/O	I/O
25	GL	GL	GL	GL
26	GL	GL	GL	GL
27	I/O	I/O	I/O	I/O
28	I/O	I/O	I/O	I/O
29	GND	GND	GND	GND
30	I/O	I/O	I/O	I/O
31	I/O	I/O	I/O	I/O
32	I/O	I/O	I/O	I/O
33	I/O	I/O	I/O	I/O
34	I/O	I/O	I/O	I/O
35	I/O	I/O	I/O	I/O
36	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
37	I/O	I/O	I/O	I/O
38	I/O	I/O	I/O	I/O
39	I/O	I/O	I/O	I/O
40	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
41	GND	GND	GND	GND
42	I/O	I/O	I/O	I/O
43	I/O	I/O	I/O	I/O
44	I/O	I/O	I/O	I/O
45	I/O	I/O	I/O	I/O
46	I/O	I/O	I/O	I/O
47	I/O	I/O	I/O	I/O
48	I/O	I/O	I/O	I/O
49	I/O	I/O	I/O	I/O
50	I/O	I/O	I/O	I/O
51	I/O	I/O	I/O	I/O
52	GND	GND	GND	GND
53	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
54	I/O	I/O	I/O	I/O
55	I/O	I/O	I/O	I/O
56	I/O	I/O	I/O	I/O
57	I/O	I/O	I/O	I/O
58	I/O	I/O	I/O	I/O
59	I/O	I/O	I/O	I/O
60	I/O	I/O	I/O	I/O
61	I/O	I/O	I/O	I/O
62	I/O	I/O	I/O	I/O
63	I/O	I/O	I/O	I/O
64	I/O	I/O	I/O	I/O
65	GND	GND	GND	GND
66	I/O	I/O	I/O	I/O
67	I/O	I/O	I/O	I/O
68	I/O	I/O	I/O	I/O
69	I/O	I/O	I/O	I/O
70	I/O	I/O	I/O	I/O
71	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
72	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
73	I/O	I/O	I/O	I/O
74	I/O	I/O	I/O	I/O
75	I/O	I/O	I/O	I/O
76	I/O	I/O	I/O	I/O
77	I/O	I/O	I/O	I/O
78	I/O	I/O	I/O	I/O
79	I/O	I/O	I/O	I/O
80	I/O	I/O	I/O	I/O
81	GND	GND	GND	GND
82	I/O	I/O	I/O	I/O
83	I/O	I/O	I/O	I/O
84	I/O	I/O	I/O	I/O
85	I/O	I/O	I/O	I/O
86	I/O	I/O	I/O	I/O
87	I/O	I/O	I/O	I/O
88	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
89	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
90	I/O	I/O	I/O	I/O
91	I/O	I/O	I/O	I/O
92	I/O	I/O	I/O	I/O
93	I/O	I/O	I/O	I/O
94	I/O	I/O	I/O	I/O
95	I/O	I/O	I/O	I/O
96	I/O	I/O	I/O	I/O
97	GND	GND	GND	GND
98	I/O	I/O	I/O	I/O
99	I/O	I/O	I/O	I/O
100	I/O	I/O	I/O	I/O
101	TCK	TCK	TCK	TCKO
102	TDI	TDI	TDI	TDI
103	TMS	TMS	TMS	TMS
104	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

208-Pin PQFP (Continued)

Pin Number	A500K050 Function	A500K130 Function	A500K180 Function	A500K270 Function
105	GND	GND	GND	GND
106	V_{PP}	V_{PP}	V_{PP}	V_{PP}
107	V_{PN}	V_{PN}	V_{PN}	V_{PN}
108	TDO	TDO	TDO	TDO
109	TRST	TRST	TRST	TRST
110	RCK	RCK	RCK	RCK
111	I/O	I/O	I/O	I/O
112	I/O	I/O	I/O	I/O
113	I/O	I/O	I/O	I/O
114	I/O	I/O	I/O	I/O
115	I/O	I/O	I/O	I/O
116	I/O	I/O	I/O	I/O
117	I/O	I/O	I/O	I/O
118	I/O	I/O	I/O	I/O
119	I/O	I/O	I/O	I/O
120	I/O	I/O	I/O	I/O
121	I/O	I/O	I/O	I/O
122	GND	GND	GND	GND
123	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
124	I/O	I/O	I/O	I/O
125	I/O	I/O	I/O	I/O
126	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
127	I/O	I/O	I/O	I/O
128	I/O	I/O	I/O	I/O
129	I/O	I/O	I/O	I/O
130	GND	GND	GND	GND
131	I/O	I/O	I/O	I/O
132	I/O	I/O	I/O	I/O
133	GL	GL	GL	GL
134	GL	GL	GL	GL
135	I/O	I/O	I/O	I/O
136	I/O	I/O	I/O	I/O
137	I/O	I/O	I/O	I/O
138	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
139	I/O	I/O	I/O	I/O
140	I/O	I/O	I/O	I/O
141	GND	GND	GND	GND
142	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
143	I/O	I/O	I/O	I/O
144	I/O	I/O	I/O	I/O
145	I/O	I/O	I/O	I/O
146	I/O	I/O	I/O	I/O
147	I/O	I/O	I/O	I/O
148	I/O	I/O	I/O	I/O
149	I/O	I/O	I/O	I/O
150	I/O	I/O	I/O	I/O
151	I/O	I/O	I/O	I/O
152	I/O	I/O	I/O	I/O
153	I/O	I/O	I/O	I/O
154	I/O	I/O	I/O	I/O
155	I/O	I/O	I/O	I/O
156	GND	GND	GND	GND
157	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
158	I/O	I/O	I/O	I/O
159	I/O	I/O	I/O	I/O
160	I/O	I/O	I/O	I/O
161	I/O	I/O	I/O	I/O
162	GND	GND	GND	GND
163	I/O	I/O	I/O	I/O
164	I/O	I/O	I/O	I/O
165	I/O	I/O	I/O	I/O
166	I/O	I/O	I/O	I/O
167	I/O	I/O	I/O	I/O
168	I/O	I/O	I/O	I/O
169	I/O	I/O	I/O	I/O
170	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
171	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
172	I/O	I/O	I/O	I/O
173	I/O	I/O	I/O	I/O
174	I/O	I/O	I/O	I/O
175	I/O	I/O	I/O	I/O
176	I/O	I/O	I/O	I/O
177	I/O	I/O	I/O	I/O
178	GND	GND	GND	GND
179	I/O	I/O	I/O	I/O
180	I/O	I/O	I/O	I/O
181	I/O	I/O	I/O	I/O
182	I/O	I/O	I/O	I/O
183	I/O	I/O	I/O	I/O
184	I/O	I/O	I/O	I/O
185	I/O	I/O	I/O	I/O
186	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}
187	V_{DDL}	V_{DDL}	V_{DDL}	V_{DDL}
188	I/O	I/O	I/O	I/O
189	I/O	I/O	I/O	I/O
190	I/O	I/O	I/O	I/O
191	I/O	I/O	I/O	I/O
192	I/O	I/O	I/O	I/O
193	I/O	I/O	I/O	I/O
194	I/O	I/O	I/O	I/O
195	GND	GND	GND	GND
196	I/O	I/O	I/O	I/O
197	I/O	I/O	I/O	I/O
198	I/O	I/O	I/O	I/O
199	I/O	I/O	I/O	I/O
200	I/O	I/O	I/O	I/O
201	I/O	I/O	I/O	I/O
202	I/O	I/O	I/O	I/O
203	I/O	I/O	I/O	I/O
204	I/O	I/O	I/O	I/O
205	I/O	I/O	I/O	I/O
206	I/O	I/O	I/O	I/O
207	I/O	I/O	I/O	I/O
208	V_{DDP}	V_{DDP}	V_{DDP}	V_{DDP}

Package Pin Assignments (Continued)

272-Pin PBGA (Bottom View)



272-Pin PBGA

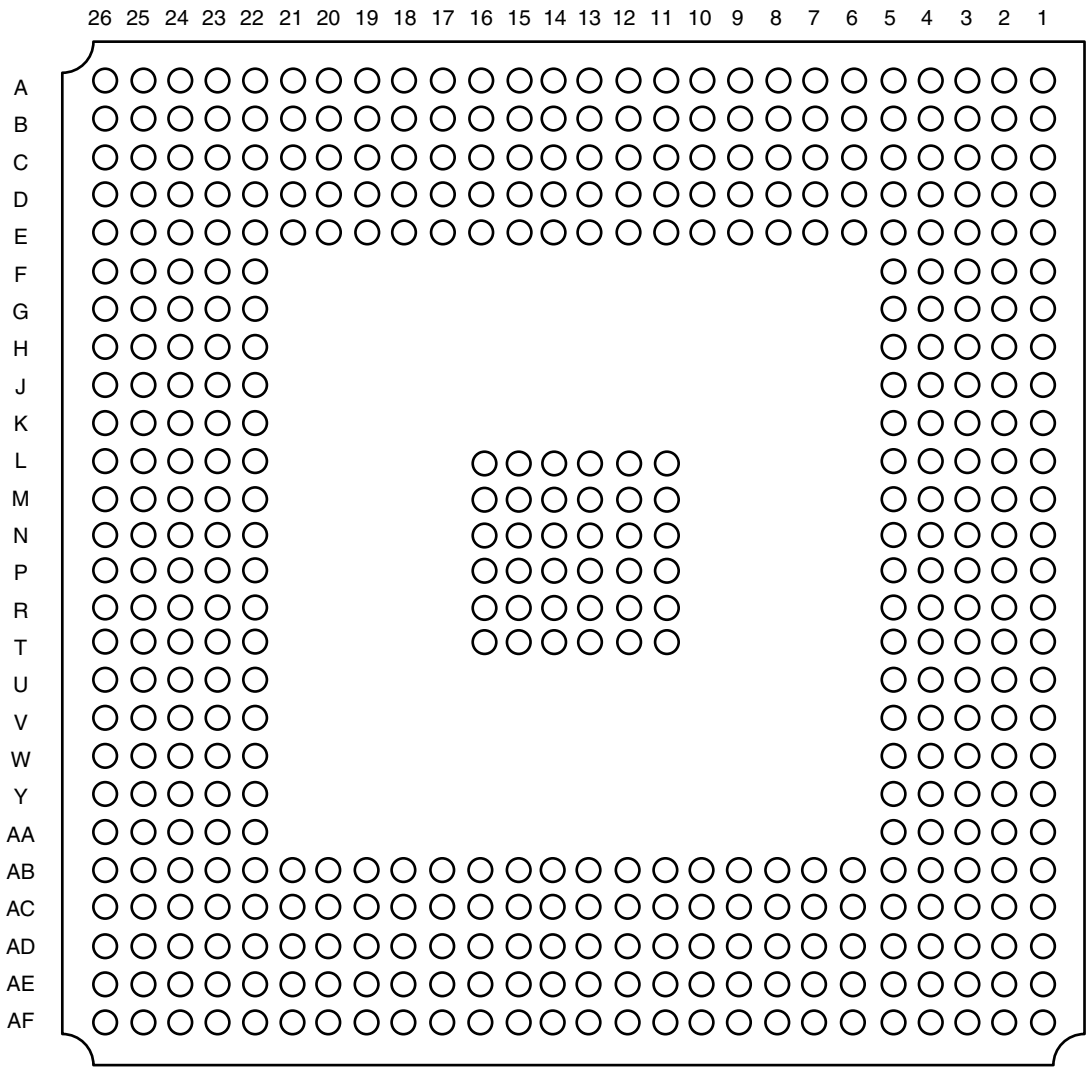
Pin Number	A500K050 Function	A500K130 Function
A1	I/O	I/O
A2	I/O	I/O
A3	I/O	I/O
A4	I/O	I/O
A5	I/O	I/O
A6	I/O	I/O
A7	I/O	I/O
A8	I/O	I/O
A9	I/O	I/O
A10	I/O	I/O
A11	I/O	I/O
A12	I/O	I/O
A13	I/O	I/O
A14	I/O	I/O
A15	I/O	I/O
A16	I/O	I/O
A17	I/O	I/O
A18	I/O	I/O
A19	I/O	I/O
A20	I/O	I/O
B1	I/O	I/O
B2	I/O	I/O
B3	I/O	I/O
B4	I/O	I/O
B5	I/O	I/O
B6	I/O	I/O
B7	I/O	I/O
B8	I/O	I/O
B9	I/O	I/O
B10	I/O	I/O
B11	I/O	I/O
B12	I/O	I/O
B13	I/O	I/O
B14	I/O	I/O
B15	I/O	I/O
B16	I/O	I/O
B17	I/O	I/O
B18	I/O	I/O
B19	I/O	I/O
B20	I/O	I/O
C1	I/O	I/O
C2	I/O	I/O
C3	I/O	I/O
C4	I/O	I/O
C5	I/O	I/O
C6	I/O	I/O
C7	I/O	I/O
C8	I/O	I/O
C9	I/O	I/O
C10	I/O	I/O
C11	I/O	I/O
C12	I/O	I/O
C13	I/O	I/O
C14	I/O	I/O
C15	I/O	I/O
C16	I/O	I/O
C17	I/O	I/O
C18	I/O	I/O
C19	I/O	I/O
C20	I/O	I/O
D1	I/O	I/O
D2	I/O	I/O
D3	I/O	I/O
D4	V_{DDP}	V_{DDP}
D5	V_{DDP}	V_{DDP}
D6	V_{DDP}	V_{DDP}
D7	I/O	I/O
D8	V_{DDL}	V_{DDL}
D9	V_{DDL}	V_{DDL}
D10	V_{DDL}	V_{DDL}
D11	V_{DDL}	V_{DDL}
D12	V_{DDL}	V_{DDL}
D13	V_{DDL}	V_{DDL}
D14	I/O	I/O
D15	V_{DDP}	V_{DDP}
D16	V_{DDP}	V_{DDP}
D17	V_{DDP}	V_{DDP}
D18	I/O	I/O
D19	I/O	I/O
D20	I/O	I/O
E1	I/O	I/O
E2	I/O	I/O
E3	I/O	I/O
E4	V_{DDP}	V_{DDP}
E17	V_{DDP}	V_{DDP}
E18	I/O	I/O
E19	I/O	I/O
E20	I/O	I/O
F1	I/O	I/O
F2	I/O	I/O
F3	I/O	I/O
F4	V_{DDP}	V_{DDP}
F17	V_{DDP}	V_{DDP}
F18	I/O	I/O
F19	I/O	I/O
F20	I/O	I/O
G1	I/O	I/O
G2	I/O	I/O
G3	I/O	I/O
G4	I/O	I/O
G17	I/O	I/O
G18	I/O	I/O
G19	I/O	I/O
G20	I/O	I/O
H1	I/O	I/O
H2	I/O	I/O
H3	I/O	I/O
H4	I/O	I/O
H17	I/O	I/O
H18	I/O	I/O
H19	I/O	I/O
H20	GL	GL
J1	I/O	I/O
J2	GL	GL
J3	GL	GL
J4	V_{DDL}	V_{DDL}
J9	GND	GND
J10	GND	GND
J11	GND	GND
J12	GND	GND
J17	V_{DDL}	V_{DDL}
J18	GL	GL
J19	I/O	I/O
J20	I/O	I/O
K1	I/O	I/O
K2	I/O	I/O
K3	I/O	I/O
K4	V_{DDL}	V_{DDL}
K9	GND	GND
K10	GND	GND
K11	GND	GND
K12	GND	GND
K17	V_{DDL}	V_{DDL}
K18	I/O	I/O
K19	I/O	I/O
K20	I/O	I/O
L1	I/O	I/O
L2	I/O	I/O

272-Pin PBGA (Continued)

Pin Number	A500K050 Function	A500K130 Function
L3	I/O	I/O
L4	V_{DDL}	V_{DDL}
L9	GND	GND
L10	GND	GND
L11	GND	GND
L12	GND	GND
L17	V_{DDL}	V_{DDL}
L18	I/O	I/O
L19	I/O	I/O
L20	I/O	I/O
M1	I/O	I/O
M2	I/O	I/O
M3	I/O	I/O
M4	V_{DDL}	V_{DDL}
M9	GND	GND
M10	GND	GND
M11	GND	GND
M12	GND	GND
M17	V_{DDL}	V_{DDL}
M18	I/O	I/O
M19	I/O	I/O
M20	I/O	I/O
N1	I/O	I/O
N2	I/O	I/O
N3	I/O	I/O
N4	V_{DDL}	V_{DDL}
N17	V_{DDL}	V_{DDL}
N18	I/O	I/O
N19	I/O	I/O
N20	I/O	I/O
P1	I/O	I/O
P2	I/O	I/O
P3	I/O	I/O
P4	V_{DDP}	V_{DDP}
P17	V_{DDP}	V_{DDP}
P18	I/O	I/O
P19	I/O	I/O
P20	I/O	I/O
R1	I/O	I/O
R2	I/O	I/O
R3	I/O	I/O
R4	V_{DDP}	V_{DDP}
R17	V_{DDP}	V_{DDP}
R18	I/O	I/O
R19	I/O	I/O
R20	I/O	I/O
T1	I/O	I/O
T2	I/O	I/O
T3	I/O	I/O
T4	V_{DDP}	V_{DDP}
T17	V_{DDP}	V_{DDP}
T18	I/O	I/O
T19	I/O	I/O
T20	I/O	I/O
U1	I/O	I/O
U2	I/O	I/O
U3	I/O	I/O
U4	V_{DDP}	V_{DDP}
U5	V_{DDP}	V_{DDP}
U6	V_{DDP}	V_{DDP}
U7	I/O	I/O
U8	V_{DDL}	V_{DDL}
U9	V_{DDL}	V_{DDL}
U10	V_{DDL}	V_{DDL}
U11	V_{DDL}	V_{DDL}
U12	V_{DDL}	V_{DDL}
U13	V_{DDL}	V_{DDL}
U14	I/O	I/O
U15	V_{DDP}	V_{DDP}
U16	V_{DDP}	V_{DDP}
U17	V_{DDP}	V_{DDP}
U18	RCK	RCK
U19	I/O	I/O
U20	I/O	I/O
V1	I/O	I/O
V2	I/O	I/O
V3	I/O	I/O
V4	I/O	I/O
V5	I/O	I/O
V6	I/O	I/O
V7	I/O	I/O
V8	I/O	I/O
V9	I/O	I/O
V10	I/O	I/O
V11	I/O	I/O
V12	I/O	I/O
V13	I/O	I/O
V14	I/O	I/O
V15	I/O	I/O
V16	I/O	I/O
V17	TMS	TMS
V18	TDO	TDO
V19	I/O	I/O
V20	I/O	I/O
W1	I/O	I/O
W2	I/O	I/O
W3	I/O	I/O
W4	I/O	I/O
W5	I/O	I/O
W6	I/O	I/O
W7	I/O	I/O
W8	I/O	I/O
W9	I/O	I/O
W10	I/O	I/O
W11	I/O	I/O
W12	I/O	I/O
W13	I/O	I/O
W14	I/O	I/O
W15	I/O	I/O
W16	I/O	I/O
W17	TCK	TCK
W18	V_{PP}	V_{PP}
W19	TRST	TRST
W20	I/O	I/O
Y1	I/O	I/O
Y2	I/O	I/O
Y3	I/O	I/O
Y4	I/O	I/O
Y5	I/O	I/O
Y6	I/O	I/O
Y7	I/O	I/O
Y8	I/O	I/O
Y9	I/O	I/O
Y10	I/O	I/O
Y11	I/O	I/O
Y12	I/O	I/O
Y13	I/O	I/O
Y14	I/O	I/O
Y15	I/O	I/O
Y16	I/O	I/O
Y17	I/O	I/O
Y18	TDI	TDI
Y19	V_{PN}	V_{PN}
Y20	I/O	I/O

Package Pin Assignments (Continued)

456-Pin PBGA (Bottom View)



456-Pin PBGA

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
A1	V_{DDP}	V_{DDP}	V_{DDP}
A2	V_{DDP}	V_{DDP}	V_{DDP}
A3	NC	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	NC	I/O	I/O
A7	I/O	I/O	I/O
A8	NC	I/O	I/O
A9	NC	I/O	I/O
A10	I/O	I/O	I/O
A11	NC	I/O	I/O
A12	NC	I/O	I/O
A13	I/O	I/O	I/O
A14	NC	I/O	I/O
A15	NC	I/O	I/O
A16	I/O	I/O	I/O
A17	NC	I/O	I/O
A18	NC	I/O	I/O
A19	I/O	I/O	I/O
A20	NC	I/O	I/O
A21	NC	I/O	I/O
A22	I/O	I/O	I/O
A23	NC	I/O	I/O
A24	NC	I/O	I/O
A25	V_{DDP}	V_{DDP}	V_{DDP}
A26	V_{DDP}	V_{DDP}	V_{DDP}
AA1	I/O	I/O	I/O
AA2	I/O	I/O	I/O
AA3	I/O	I/O	I/O
AA4	I/O	I/O	I/O
AA5	V_{DDL}	V_{DDL}	V_{DDL}
AA22	V_{DDL}	V_{DDL}	V_{DDL}
AA23	I/O	I/O	I/O
AA24	I/O	I/O	I/O
AA25	I/O	I/O	I/O
AA26	NC	I/O	I/O
AB1	NC	I/O	I/O
AB2	I/O	I/O	I/O
AB3	I/O	I/O	I/O
AB4	I/O	I/O	I/O
AB5	V_{DDL}	V_{DDL}	V_{DDL}
AB6	V_{DDL}	V_{DDL}	V_{DDL}
AB7	V_{DDL}	V_{DDL}	V_{DDL}
AB8	I/O	I/O	I/O
AB9	I/O	I/O	I/O
AB10	I/O	I/O	I/O
AB11	I/O	I/O	I/O
AB12	I/O	I/O	I/O
AB13	I/O	I/O	I/O
AB14	I/O	I/O	I/O
AB15	I/O	I/O	I/O
AB16	I/O	I/O	I/O
AB17	I/O	I/O	I/O
AB18	I/O	I/O	I/O
AB19	I/O	I/O	I/O
AB20	V_{DDL}	V_{DDL}	V_{DDL}
AB21	V_{DDL}	V_{DDL}	V_{DDL}
AB22	V_{DDL}	V_{DDL}	V_{DDL}
AB23	I/O	I/O	I/O
AB24	I/O	I/O	I/O
AB25	I/O	I/O	I/O
AB26	I/O	I/O	I/O
AC1	I/O	I/O	I/O
AC2	I/O	I/O	I/O
AC3	I/O	I/O	I/O
AC4	V_{DDP}	V_{DDP}	V_{DDP}
AC5	I/O	I/O	I/O
AC6	I/O	I/O	I/O
AC7	I/O	I/O	I/O
AC8	I/O	I/O	I/O
AC9	I/O	I/O	I/O
AC10	I/O	I/O	I/O
AC11	I/O	I/O	I/O
AC12	I/O	I/O	I/O
AC13	I/O	I/O	I/O
AC14	I/O	I/O	I/O
AC15	I/O	I/O	I/O
AC16	I/O	I/O	I/O
AC17	I/O	I/O	I/O
AC18	I/O	I/O	I/O
AC19	I/O	I/O	I/O
AC20	I/O	I/O	I/O
AC21	TMS	TMS	TMS
AC22	TDO	TDO	TDO
AC23	V_{DDP}	V_{DDP}	V_{DDP}
AC24	RCK	RCK	RCK
AC25	I/O	I/O	I/O
AC26	NC	I/O	I/O
AD1	NC	I/O	I/O
AD2	I/O	I/O	I/O
AD3	V_{DDP}	V_{DDP}	V_{DDP}
AD4	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
AD5	I/O	I/O	I/O
AD6	I/O	I/O	I/O
AD7	I/O	I/O	I/O
AD8	I/O	I/O	I/O
AD9	I/O	I/O	I/O
AD10	I/O	I/O	I/O
AD11	I/O	I/O	I/O
AD12	I/O	I/O	I/O
AD13	I/O	I/O	I/O
AD14	I/O	I/O	I/O
AD15	I/O	I/O	I/O
AD16	I/O	I/O	I/O
AD17	I/O	I/O	I/O
AD18	I/O	I/O	I/O
AD19	I/O	I/O	I/O
AD20	I/O	I/O	I/O
AD21	TCK	TCK	TCK
AD22	V_{PP}	V_{PP}	V_{PP}
AD23	I/O	I/O	I/O
AD24	V_{DDP}	V_{DDP}	V_{DDP}
AD25	I/O	I/O	I/O
AD26	NC	I/O	I/O
AE1	V_{DDP}	V_{DDP}	V_{DDP}
AE2	V_{DDP}	V_{DDP}	V_{DDP}
AE3	I/O	I/O	I/O
AE4	I/O	I/O	I/O
AE5	I/O	I/O	I/O
AE6	I/O	I/O	I/O
AE7	I/O	I/O	I/O
AE8	I/O	I/O	I/O
AE9	I/O	I/O	I/O
AE10	I/O	I/O	I/O
AE11	I/O	I/O	I/O
AE12	I/O	I/O	I/O
AE13	I/O	I/O	I/O
AE14	I/O	I/O	I/O
AE15	I/O	I/O	I/O
AE16	I/O	I/O	I/O
AE17	I/O	I/O	I/O
AE18	I/O	I/O	I/O
AE19	I/O	I/O	I/O
AE20	I/O	I/O	I/O
AE21	I/O	I/O	I/O
AE22	I/O	I/O	I/O
AE23	V_{PN}	V_{PN}	V_{PN}
AE24	TRST	TRST	TRST

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
AE25	V_{DDP}	V_{DDP}	V_{DDP}
AE26	V_{DDP}	V_{DDP}	V_{DDP}
AF1	V_{DDP}	V_{DDP}	V_{DDP}
AF2	V_{DDP}	V_{DDP}	V_{DDP}
AF3	NC	I/O	I/O
AF4	NC	I/O	I/O
AF5	I/O	I/O	I/O
AF6	NC	I/O	I/O
AF7	NC	I/O	I/O
AF8	I/O	I/O	I/O
AF9	NC	I/O	I/O
AF10	NC	I/O	I/O
AF11	I/O	I/O	I/O
AF12	NC	I/O	I/O
AF13	NC	I/O	I/O
AF14	I/O	I/O	I/O
AF15	NC	I/O	I/O
AF16	NC	I/O	I/O
AF17	I/O	I/O	I/O
AF18	NC	I/O	I/O
AF19	NC	I/O	I/O
AF20	I/O	I/O	I/O
AF21	NC	I/O	I/O
AF22	I/O	I/O	I/O
AF23	TDI	TDI	TDI
AF24	NC	I/O	I/O
AF25	V_{DDP}	V_{DDP}	V_{DDP}
AF26	V_{DDP}	V_{DDP}	V_{DDP}
B1	V_{DDP}	V_{DDP}	V_{DDP}
B2	V_{DDP}	V_{DDP}	V_{DDP}
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	I/O	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	I/O	I/O	I/O
B16	I/O	I/O	I/O
B17	I/O	I/O	I/O
B18	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
B19	I/O	I/O	I/O
B20	I/O	I/O	I/O
B21	I/O	I/O	I/O
B22	I/O	I/O	I/O
B23	I/O	I/O	I/O
B24	I/O	I/O	I/O
B25	V_{DDP}	V_{DDP}	V_{DDP}
B26	V_{DDP}	V_{DDP}	V_{DDP}
C1	V_{DDP}	V_{DDP}	V_{DDP}
C2	I/O	I/O	I/O
C3	V_{DDP}	V_{DDP}	V_{DDP}
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
C17	I/O	I/O	I/O
C18	I/O	I/O	I/O
C19	I/O	I/O	I/O
C20	I/O	I/O	I/O
C21	I/O	I/O	I/O
C22	I/O	I/O	I/O
C23	I/O	I/O	I/O
C24	V_{DDP}	V_{DDP}	V_{DDP}
C25	I/O	I/O	I/O
C26	NC	I/O	I/O
D1	NC	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	V_{DDP}	V_{DDP}	V_{DDP}
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
D17	I/O	I/O	I/O
D18	I/O	I/O	I/O
D19	I/O	I/O	I/O
D20	I/O	I/O	I/O
D21	I/O	I/O	I/O
D22	I/O	I/O	I/O
D23	V_{DDP}	V_{DDP}	V_{DDP}
D24	I/O	I/O	I/O
D25	I/O	I/O	I/O
D26	I/O	I/O	I/O
E1	NC	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	V_{DDL}	V_{DDL}	V_{DDL}
E6	V_{DDL}	V_{DDL}	V_{DDL}
E7	V_{DDL}	V_{DDL}	V_{DDL}
E8	V_{DDL}	V_{DDL}	V_{DDL}
E9	I/O	I/O	I/O
E10	I/O	I/O	I/O
E11	I/O	I/O	I/O
E12	I/O	I/O	I/O
E13	I/O	I/O	I/O
E14	I/O	I/O	I/O
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
E17	I/O	I/O	I/O
E18	I/O	I/O	I/O
E19	I/O	I/O	I/O
E20	V_{DDL}	V_{DDL}	V_{DDL}
E21	V_{DDL}	V_{DDL}	V_{DDL}
E22	V_{DDL}	V_{DDL}	V_{DDL}
E23	I/O	I/O	I/O
E24	I/O	I/O	I/O
E25	I/O	I/O	I/O
E26	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	I/O	I/O	I/O
F5	V_{DDL}	V_{DDL}	V_{DDL}
F22	V_{DDL}	V_{DDL}	V_{DDL}

456-Pin PBGA (Continued)

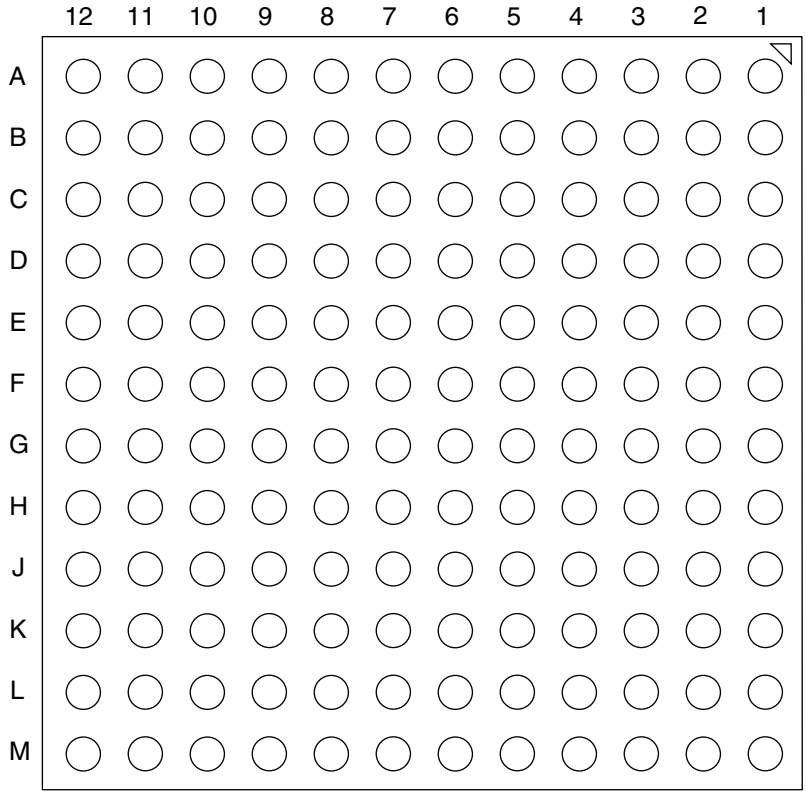
Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
F23	I/O	I/O	I/O
F24	I/O	I/O	I/O
F25	I/O	I/O	I/O
F26	NC	I/O	I/O
G1	NC	I/O	I/O
G2	I/O	I/O	I/O
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	V_{DDL}	V_{DDL}	V_{DDL}
G22	V_{DDL}	V_{DDL}	V_{DDL}
G23	I/O	I/O	I/O
G24	I/O	I/O	I/O
G25	I/O	I/O	I/O
G26	I/O	I/O	I/O
H1	NC	I/O	I/O
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	V_{DDL}	V_{DDL}	V_{DDL}
H22	V_{DDL}	V_{DDL}	V_{DDL}
H23	I/O	I/O	I/O
H24	I/O	I/O	I/O
H25	I/O	I/O	I/O
H26	NC	I/O	I/O
J1	I/O	I/O	I/O
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J22	I/O	I/O	I/O
J23	I/O	I/O	I/O
J24	I/O	I/O	I/O
J25	I/O	I/O	I/O
J26	NC	I/O	I/O
K1	NC	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	I/O	I/O	I/O
K22	I/O	I/O	I/O
K23	I/O	I/O	I/O
K24	I/O	I/O	I/O
K25	I/O	I/O	I/O
K26	I/O	I/O	I/O
L1	NC	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	I/O	I/O	I/O
L11	GND	GND	GND
L12	GND	GND	GND
L13	GND	GND	GND
L14	GND	GND	GND
L15	GND	GND	GND
L16	GND	GND	GND
L22	I/O	I/O	I/O
L23	I/O	I/O	I/O
L24	I/O	I/O	I/O
L25	I/O	I/O	I/O
L26	NC	I/O	I/O
M1	GL	GL	GL
M2	GL	GL	GL
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M11	GND	GND	GND
M12	GND	GND	GND
M13	GND	GND	GND
M14	GND	GND	GND
M15	GND	GND	GND
M16	GND	GND	GND
M22	GL	GL	GL
M23	I/O	I/O	I/O
M24	I/O	I/O	I/O
M25	I/O	I/O	I/O
M26	NC	I/O	I/O
N1	NC	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N11	GND	GND	GND
N12	GND	GND	GND
N13	GND	GND	GND
N14	GND	GND	GND
N15	GND	GND	GND
N16	GND	GND	GND
N22	I/O	I/O	I/O
N23	GL	GL	GL
N24	I/O	I/O	I/O
N25	I/O	I/O	I/O
N26	I/O	I/O	I/O

456-Pin PBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
P1	NC	I/O	I/O
P2	I/O	I/O	I/O
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	I/O	I/O	I/O
P11	GND	GND	GND
P12	GND	GND	GND
P13	GND	GND	GND
P14	GND	GND	GND
P15	GND	GND	GND
P16	GND	GND	GND
P22	I/O	I/O	I/O
P23	I/O	I/O	I/O
P24	I/O	I/O	I/O
P25	I/O	I/O	I/O
P26	NC	I/O	I/O
R1	I/O	I/O	I/O
R2	I/O	I/O	I/O
R3	I/O	I/O	I/O
R4	I/O	I/O	I/O
R5	I/O	I/O	I/O
R11	GND	GND	GND
R12	GND	GND	GND
R13	GND	GND	GND
R14	GND	GND	GND
R15	GND	GND	GND
R16	GND	GND	GND
R22	I/O	I/O	I/O
R23	I/O	I/O	I/O
R24	I/O	I/O	I/O
R25	I/O	I/O	I/O
R26	NC	I/O	I/O
T1	NC	I/O	I/O
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	I/O	I/O	I/O
T5	I/O	I/O	I/O
T11	GND	GND	GND
T12	GND	GND	GND
T13	GND	GND	GND
T14	GND	GND	GND
T15	GND	GND	GND
T16	GND	GND	GND
T22	I/O	I/O	I/O
T23	I/O	I/O	I/O
T24	I/O	I/O	I/O
T25	I/O	I/O	I/O
T26	I/O	I/O	I/O
U1	NC	I/O	I/O
U2	I/O	I/O	I/O
U3	I/O	I/O	I/O
U4	I/O	I/O	I/O
U5	I/O	I/O	I/O
U22	I/O	I/O	I/O
U23	I/O	I/O	I/O
U24	I/O	I/O	I/O
U25	I/O	I/O	I/O
U26	NC	I/O	I/O
V1	I/O	I/O	I/O
V2	I/O	I/O	I/O
V3	I/O	I/O	I/O
V4	I/O	I/O	I/O
V5	I/O	I/O	I/O
V22	I/O	I/O	I/O
V23	I/O	I/O	I/O
V24	I/O	I/O	I/O
V25	I/O	I/O	I/O
V26	NC	I/O	I/O
W1	NC	I/O	I/O
W2	I/O	I/O	I/O
W3	I/O	I/O	I/O
W4	I/O	I/O	I/O
W5	V_{DDL}	V_{DDL}	V_{DDL}
W22	V_{DDL}	V_{DDL}	V_{DDL}
W23	I/O	I/O	I/O
W24	I/O	I/O	I/O
W25	I/O	I/O	I/O
W26	I/O	I/O	I/O
Y1	NC	I/O	I/O
Y2	I/O	I/O	I/O
Y3	I/O	I/O	I/O
Y4	I/O	I/O	I/O
Y5	V_{DDL}	V_{DDL}	V_{DDL}
Y22	V_{DDL}	V_{DDL}	V_{DDL}
Y23	I/O	I/O	I/O
Y24	I/O	I/O	I/O
Y25	I/O	I/O	I/O
Y26	NC	I/O	I/O

Package Assignments (Continued)

144-FBGA (Bottom View)



144-pin FBGA

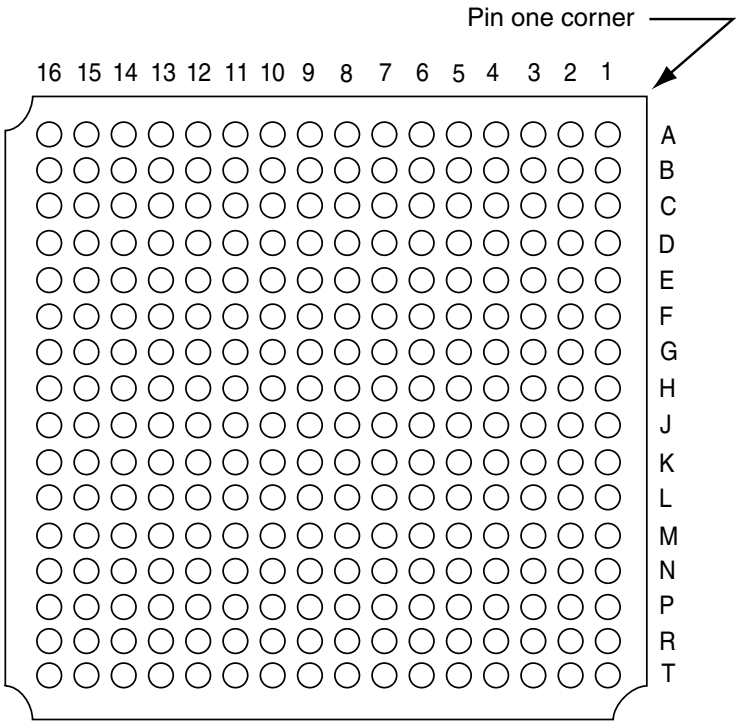
Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function
A1	I/O	I/O	D1	I/O	I/O	G1	I/O	I/O
A2	I/O	I/O	D2	I/O	I/O	G2	GND	GND
A3	I/O	I/O	D3	I/O	I/O	G3	I/O	I/O
A4	I/O	I/O	D4	I/O	I/O	G4	I/O	I/O
A5	I/O	I/O	D5	I/O	I/O	G5	GND	GND
A6	GND	GND	D6	I/O	I/O	G6	GND	GND
A7	I/O	I/O	D7	I/O	I/O	G7	GND	GND
A8	V_{DDL}	V_{DDL}	D8	I/O	I/O	G8	I/O	I/O
A9	I/O	I/O	D9	I/O	I/O	G9	I/O	I/O
A10	I/O	I/O	D10	I/O	I/O	G10	I/O	I/O
A11	I/O	I/O	D11	I/O	I/O	G11	I/O	I/O
A12	I/O	I/O	D12	I/O	I/O	G12	I/O	I/O
B1	I/O	I/O	E1	V_{DDL}	V_{DDL}	H1	V_{DDL}	V_{DDL}
B2	GND	GND	E2	I/O	I/O	H2	I/O	I/O
B3	I/O	I/O	E3	I/O	I/O	H3	I/O	I/O
B4	I/O	I/O	E4	V_{DDP}	V_{DDP}	H4	I/O	I/O
B5	I/O	I/O	E5	I/O	I/O	H5	V_{DDL}	V_{DDL}
B6	I/O	I/O	E6	V_{DDP}	V_{DDP}	H6	I/O	I/O
B7	I/O	I/O	E7	V_{DDP}	V_{DDP}	H7	I/O	I/O
B8	I/O	I/O	E8	I/O	I/O	H8	I/O	I/O
B9	I/O	I/O	E9	V_{DDP}	V_{DDP}	H9	I/O	I/O
B10	I/O	I/O	E10	V_{DDL}	V_{DDL}	H10	V_{DDP}	V_{DDP}
B11	GND	GND	E11	I/O	I/O	H11	I/O	I/O
B12	I/O	I/O	E12	I/O	I/O	H12	V_{DDL}	V_{DDL}
C1	I/O	I/O	F1	GL	GL	J1	I/O	I/O
C2	GL	GL	F2	I/O	I/O	J2	I/O	I/O
C3	I/O	I/O	F3	I/O	I/O	J3	V_{DDP}	V_{DDP}
C4	V_{DDL}	V_{DDL}	F4	I/O	I/O	J4	I/O	I/O
C5	I/O	I/O	F5	GND	GND	J5	I/O	I/O
C6	I/O	I/O	F6	GND	GND	J6	I/O	I/O
C7	I/O	I/O	F7	GND	GND	J7	V_{DDL}	V_{DDL}
C8	I/O	I/O	F8	I/O	I/O	J8	TCK	TCK
C9	I/O	I/O	F9	GL	GL	J9	I/O	I/O
C10	I/O	I/O	F10	GND	GND	J10	TDO	TDO
C11	I/O	I/O	F11	I/O	I/O	J11	I/O	I/O
C12	I/O	I/O	F12	GL	GL	J12	I/O	I/O

144-pin FBGA (Continued)

Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function	Pin Number	A500K050 Function	A500K130 Function
K1	I/O	I/O	L1	GND	GND	M1	I/O	I/O
K2	I/O	I/O	L2	I/O	I/O	M2	I/O	I/O
K3	I/O	I/O	L3	I/O	I/O	M3	I/O	I/O
K4	I/O	I/O	L4	I/O	I/O	M4	I/O	I/O
K5	I/O	I/O	L5	V_{DDP}	V_{DDP}	M5	I/O	I/O
K6	I/O	I/O	L6	I/O	I/O	M6	I/O	I/O
K7	GND	GND	L7	I/O	I/O	M7	I/O	I/O
K8	I/O	I/O	L8	I/O	I/O	M8	I/O	I/O
K9	I/O	I/O	L9	TMS	TMS	M9	TDI	TDI
K10	GND	GND	L10	RCK	RCK	M10	V_{DDP}	V_{DDP}
K11	I/O	I/O	L11	I/O	I/O	M11	V_{PP}	V_{PP}
K12	I/O	I/O	L12	TRST	TRST	M12	V_{PN}	V_{PN}

Package Assignments (Continued)

256-FBGA (Bottom View)



256-pin FBGA

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
A1	GND	GND	GND
A2	I/O	I/O	I/O
A3	I/O	I/O	I/O
A4	I/O	I/O	I/O
A5	I/O	I/O	I/O
A6	I/O	I/O	I/O
A7	I/O	I/O	I/O
A8	I/O	I/O	I/O
A9	I/O	I/O	I/O
A10	I/O	I/O	I/O
A11	I/O	I/O	I/O
A12	I/O	I/O	I/O
A13	I/O	I/O	I/O
A14	I/O	I/O	I/O
A15	I/O	I/O	I/O
A16	GND	GND	GND
B1	I/O	I/O	I/O
B2	I/O	I/O	I/O
B3	I/O	I/O	I/O
B4	I/O	I/O	I/O
B5	I/O	I/O	I/O
B6	I/O	I/O	I/O
B7	I/O	I/O	I/O
B8	I/O	I/O	I/O
B9	I/O	I/O	I/O
B10	I/O	I/O	I/O
B11	I/O	I/O	I/O
B12	I/O	I/O	I/O
B13	I/O	I/O	I/O
B14	I/O	I/O	I/O
B15	I/O	I/O	I/O
B16	I/O	I/O	I/O
C1	I/O	I/O	I/O
C2	I/O	I/O	I/O
C3	I/O	I/O	I/O
C4	I/O	I/O	I/O
C5	I/O	I/O	I/O
C6	I/O	I/O	I/O
C7	I/O	I/O	I/O

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
C8	I/O	I/O	I/O
C9	I/O	I/O	I/O
C10	I/O	I/O	I/O
C11	I/O	I/O	I/O
C12	I/O	I/O	I/O
C13	I/O	I/O	I/O
C14	I/O	I/O	I/O
C15	I/O	I/O	I/O
C16	I/O	I/O	I/O
D1	I/O	I/O	I/O
D2	I/O	I/O	I/O
D3	I/O	I/O	I/O
D4	I/O	I/O	I/O
D5	I/O	I/O	I/O
D6	I/O	I/O	I/O
D7	I/O	I/O	I/O
D8	I/O	I/O	I/O
D9	I/O	I/O	I/O
D10	I/O	I/O	I/O
D11	I/O	I/O	I/O
D12	I/O	I/O	I/O
D13	I/O	I/O	I/O
D14	I/O	I/O	I/O
D15	I/O	I/O	I/O
D16	I/O	I/O	I/O
E1	I/O	I/O	I/O
E2	I/O	I/O	I/O
E3	I/O	I/O	I/O
E4	I/O	I/O	I/O
E5	I/O	I/O	I/O
E6	V_{DDP}	V_{DDP}	V_{DDP}
E7	V_{DDP}	V_{DDP}	V_{DDP}
E8	I/O	I/O	I/O
E9	I/O	I/O	I/O
E10	V_{DDP}	V_{DDP}	V_{DDP}
E11	V_{DDP}	V_{DDP}	V_{DDP}
E12	I/O	I/O	I/O
E13	I/O	I/O	I/O
E14	I/O	I/O	I/O

256-pin FBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
E15	I/O	I/O	I/O
E16	I/O	I/O	I/O
F1	I/O	I/O	I/O
F2	I/O	I/O	I/O
F3	I/O	I/O	I/O
F4	I/O	I/O	I/O
F5	V_{DDP}	V_{DDP}	V_{DDP}
F6	GND	GND	GND
F7	V_{DDL}	V_{DDL}	V_{DDL}
F8	V_{DDL}	V_{DDL}	V_{DDL}
F9	V_{DDL}	V_{DDL}	V_{DDL}
F10	V_{DDL}	V_{DDL}	V_{DDL}
F11	GND	GND	GND
F12	V_{DDP}	V_{DDP}	V_{DDP}
F13	I/O	I/O	I/O
F14	I/O	I/O	I/O
F15	I/O	I/O	I/O
F16	I/O	I/O	I/O
G1	I/O	I/O	I/O
G2	I/O	I/O	I/O
G3	I/O	I/O	I/O
G4	I/O	I/O	I/O
G5	V_{DDP}	V_{DDP}	V_{DDP}
G6	V_{DDL}	V_{DDL}	V_{DDL}
G7	GND	GND	GND
G8	GND	GND	GND
G9	GND	GND	GND
G10	GND	GND	GND
G11	V_{DDL}	V_{DDL}	V_{DDL}
G12	V_{DDP}	V_{DDP}	V_{DDP}
G13	I/O	I/O	I/O
G14	I/O	I/O	I/O
G15	I/O	I/O	I/O
G16	I/O	I/O	I/O
H1	GL	GL	GL
H2	I/O	I/O	I/O
H3	I/O	I/O	I/O
H4	I/O	I/O	I/O
H5	I/O	I/O	I/O
H6	V_{DDL}	V_{DDL}	V_{DDL}
H7	GND	GND	GND
H8	GND	GND	GND
H9	GND	GND	GND
H10	GND	GND	GND
H11	V_{DDL}	V_{DDL}	V_{DDL}
H12	I/O	I/O	I/O
H13	I/O	I/O	I/O
H14	I/O	I/O	I/O
H15	I/O	I/O	I/O
H16	GL	GL	GL
J1	GL	GL	GL
J2	I/O	I/O	I/O
J3	I/O	I/O	I/O
J4	I/O	I/O	I/O
J5	I/O	I/O	I/O
J6	V_{DDL}	V_{DDL}	V_{DDL}
J7	GND	GND	GND
J8	GND	GND	GND
J9	GND	GND	GND
J10	GND	GND	GND
J11	V_{DDL}	V_{DDL}	V_{DDL}
J12	I/O	I/O	I/O
J13	I/O	I/O	I/O
J14	I/O	I/O	I/O
J15	I/O	I/O	I/O
J16	GL	GL	GL
K1	I/O	I/O	I/O
K2	I/O	I/O	I/O
K3	I/O	I/O	I/O
K4	I/O	I/O	I/O
K5	V_{DDP}	V_{DDP}	V_{DDP}
K6	V_{DDL}	V_{DDL}	V_{DDL}
K7	GND	GND	GND
K8	GND	GND	GND
K9	GND	GND	GND
K10	GND	GND	GND
K11	V_{DDL}	V_{DDL}	V_{DDL}
K12	V_{DDP}	V_{DDP}	V_{DDP}

256-pin FBGA (Continued)

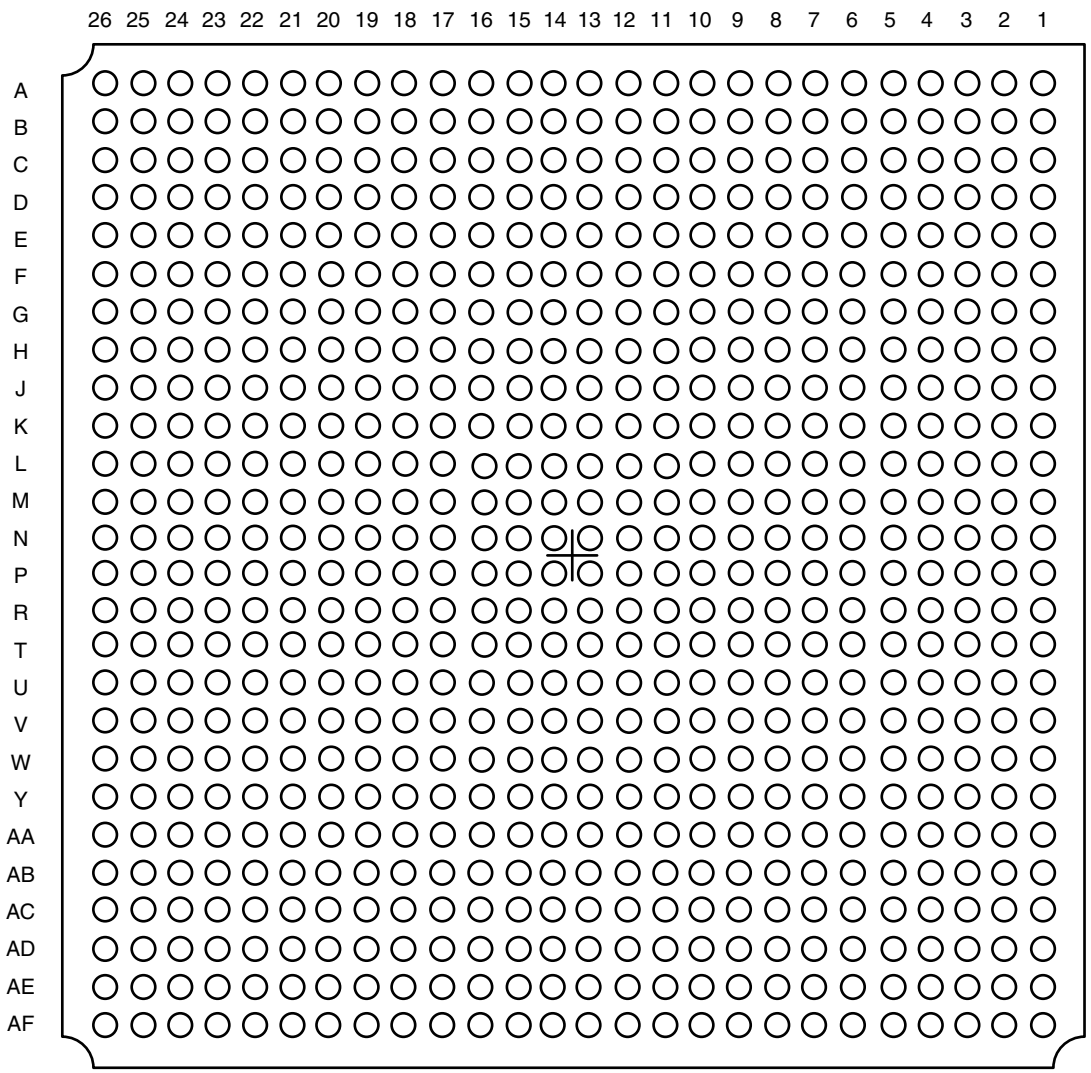
Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
K13	I/O	I/O	I/O
K14	I/O	I/O	I/O
K15	I/O	I/O	I/O
K16	I/O	I/O	I/O
L1	I/O	I/O	I/O
L2	I/O	I/O	I/O
L3	I/O	I/O	I/O
L4	I/O	I/O	I/O
L5	V_{DDP}	V_{DDP}	V_{DDP}
L6	GND	GND	GND
L7	V_{DDL}	V_{DDL}	V_{DDL}
L8	V_{DDL}	V_{DDL}	V_{DDL}
L9	V_{DDL}	V_{DDL}	V_{DDL}
L10	V_{DDL}	V_{DDL}	V_{DDL}
L11	GND	GND	GND
L12	V_{DDP}	V_{DDP}	V_{DDP}
L13	I/O	I/O	I/O
L14	I/O	I/O	I/O
L15	I/O	I/O	I/O
L16	I/O	I/O	I/O
M1	I/O	I/O	I/O
M2	I/O	I/O	I/O
M3	I/O	I/O	I/O
M4	I/O	I/O	I/O
M5	I/O	I/O	I/O
M6	V_{DDP}	V_{DDP}	V_{DDP}
M7	V_{DDP}	V_{DDP}	V_{DDP}
M8	I/O	I/O	I/O
M9	I/O	I/O	I/O
M10	V_{DDP}	V_{DDP}	V_{DDP}
M11	V_{DDP}	V_{DDP}	V_{DDP}
M12	I/O	I/O	I/O
M13	I/O	I/O	I/O
M14	I/O	I/O	I/O
M15	I/O	I/O	I/O
M16	I/O	I/O	I/O
N1	I/O	I/O	I/O
N2	I/O	I/O	I/O
N3	I/O	I/O	I/O
N4	I/O	I/O	I/O
N5	I/O	I/O	I/O
N6	I/O	I/O	I/O
N7	I/O	I/O	I/O
N8	I/O	I/O	I/O
N9	I/O	I/O	I/O
N10	I/O	I/O	I/O
N11	I/O	I/O	I/O
N12	I/O	I/O	I/O
N13	I/O	I/O	I/O
N14	RCK	RCK	RCK
N15	I/O	I/O	I/O
N16	I/O	I/O	I/O
P1	I/O	I/O	I/O
P2	I/O	I/O	I/O
P3	I/O	I/O	I/O
P4	I/O	I/O	I/O
P5	I/O	I/O	I/O
P6	I/O	I/O	I/O
P7	I/O	I/O	I/O
P8	I/O	I/O	I/O
P9	I/O	I/O	I/O
P10	I/O	I/O	I/O
P11	I/O	I/O	I/O
P12	I/O	I/O	I/O
P13	TCK	TCK	TCK
P14	V_{PP}	V_{PP}	V_{PP}
P15	TRST	TRST	TRST
P16	I/O	I/O	I/O
R1	I/O	I/O	I/O
R2	I/O	I/O	I/O
R3	I/O	I/O	I/O
R4	I/O	I/O	I/O
R5	I/O	I/O	I/O
R6	I/O	I/O	I/O
R7	I/O	I/O	I/O
R8	I/O	I/O	I/O
R9	I/O	I/O	I/O
R10	I/O	I/O	I/O

256-pin FBGA (Continued)

Pin Number	A500K130 Function	A500K180 Function	A500K270 Function
R11	I/O	I/O	I/O
R12	I/O	I/O	I/O
R13	I/O	I/O	I/O
R14	TDI	TDI	TDI
R15	V_{PN}	V_{PN}	V_{PN}
R16	TDO	TDO	TDO
T1	GND	GND	GND
T2	I/O	I/O	I/O
T3	I/O	I/O	I/O
T4	I/O	I/O	I/O
T5	I/O	I/O	I/O
T6	I/O	I/O	I/O
T7	I/O	I/O	I/O
T8	I/O	I/O	I/O
T9	I/O	I/O	I/O
T10	I/O	I/O	I/O
T11	I/O	I/O	I/O
T12	I/O	I/O	I/O
T13	I/O	I/O	I/O
T14	I/O	I/O	I/O
T15	TMS	TMS	TMS
T16	GND	GND	GND

Package Assignments (Continued)

676-pin FBGA (Bottom View)



676-Pin FBGA

Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function
A1	GND	AA13	I/O	AB25	I/O	AD11	I/O	AE23	I/O
A2	GND	AA14	I/O	AB26	I/O	AD12	I/O	AE24	I/O
A3	I/O	AA15	I/O	AC1	I/O	AD13	I/O	AE25	GND
A4	I/O	AA16	I/O	AC2	I/O	AD14	I/O	AE26	GND
A5	I/O	AA17	I/O	AC3	I/O	AD15	I/O	AF1	GND
A6	I/O	AA18	I/O	AC4	I/O	AD16	I/O	AF2	GND
A7	I/O	AA19	I/O	AC5	GND	AD17	I/O	AF3	GND
A8	I/O	AA20	I/O	AC6	I/O	AD18	I/O	AF4	GND
A9	I/O	AA21	TDO	AC7	I/O	AD19	I/O	AF5	I/O
A10	I/O	AA22	GND	AC8	I/O	AD20	I/O	AF6	I/O
A11	I/O	AA23	GND	AC9	GND	AD21	I/O	AF7	I/O
A12	I/O	AA24	I/O	AC10	I/O	AD22	I/O	AF8	I/O
A13	I/O	AA25	I/O	AC11	I/O	AD23	TDI	AF9	I/O
A14	I/O	AA26	I/O	AC12	I/O	AD24	V_{PN}	AF10	I/O
A15	I/O	AB1	I/O	AC13	I/O	AD25	I/O	AF11	I/O
A16	I/O	AB2	I/O	AC14	I/O	AD26	I/O	AF12	I/O
A17	I/O	AB3	I/O	AC15	I/O	AE1	GND	AF13	I/O
A18	I/O	AB4	I/O	AC16	I/O	AE2	GND	AF14	I/O
A19	I/O	AB5	I/O	AC17	I/O	AE3	GND	AF15	I/O
A20	I/O	AB6	GND	AC18	I/O	AE4	I/O	AF16	I/O
A21	I/O	AB7	GND	AC19	I/O	AE5	I/O	AF17	I/O
A22	I/O	AB8	I/O	AC20	I/O	AE6	I/O	AF18	I/O
A23	I/O	AB9	I/O	AC21	I/O	AE7	I/O	AF19	I/O
A24	I/O	AB10	I/O	AC22	TMS	AE8	I/O	AF20	I/O
A25	GND	AB11	I/O	AC23	RCK	AE9	I/O	AF21	I/O
A26	GND	AB12	I/O	AC24	I/O	AE10	I/O	AF22	I/O
AA1	I/O	AB13	I/O	AC25	I/O	AE11	I/O	AF23	I/O
AA2	I/O	AB14	I/O	AC26	I/O	AE12	I/O	AF24	I/O
AA3	I/O	AB15	I/O	AD1	I/O	AE13	I/O	AF25	GND
AA4	I/O	AB16	I/O	AD2	I/O	AE14	I/O	AF26	GND
AA5	I/O	AB17	I/O	AD3	I/O	AE15	I/O	B1	GND
AA6	GND	AB18	I/O	AD4	I/O	AE16	I/O	B2	GND
AA7	I/O	AB19	I/O	AD5	I/O	AE17	I/O	B3	GND
AA8	I/O	AB20	I/O	AD6	I/O	AE18	I/O	B4	GND
AA9	I/O	AB21	TCK	AD7	I/O	AE19	I/O	B5	I/O
AA10	I/O	AB22	TRST	AD8	I/O	AE20	I/O	B6	I/O
AA11	I/O	AB23	I/O	AD9	I/O	AE21	I/O	B7	I/O
AA12	I/O	AB24	I/O	AD10	I/O	AE22	I/O	B8	I/O

676-Pin FBGA (Continued)

Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function
B9	I/O	C21	I/O	E7	I/O	F19	I/O	H5	I/O
B10	I/O	C22	I/O	E8	I/O	F20	I/O	H6	I/O
B11	I/O	C23	I/O	E9	I/O	F21	I/O	H7	V_{DDP}
B12	I/O	C24	I/O	E10	I/O	F22	I/O	H8	V_{DDL}
B13	I/O	C25	I/O	E11	I/O	F23	I/O	H9	V_{DDP}
B14	I/O	C26	I/O	E12	I/O	F24	I/O	H10	V_{DDP}
B15	I/O	D1	I/O	E13	I/O	F25	I/O	H11	V_{DDP}
B16	I/O	D2	I/O	E14	I/O	F26	I/O	H12	V_{DDP}
B17	I/O	D3	GND	E15	I/O	G1	I/O	H13	V_{DDP}
B18	I/O	D4	I/O	E16	I/O	G2	I/O	H14	V_{DDP}
B19	I/O	D5	I/O	E17	I/O	G3	I/O	H15	V_{DDP}
B20	I/O	D6	I/O	E18	I/O	G4	I/O	H16	V_{DDP}
B21	I/O	D7	I/O	E19	I/O	G5	I/O	H17	V_{DDP}
B22	I/O	D8	I/O	E20	I/O	G6	I/O	H18	V_{DDP}
B23	I/O	D9	I/O	E21	I/O	G7	I/O	H19	V_{DDL}
B24	I/O	D10	I/O	E22	I/O	G8	V_{DDL}	H20	V_{DDL}
B25	GND	D11	I/O	E23	I/O	G9	NC	H21	I/O
B26	GND	D12	I/O	E24	I/O	G10	NC	H22	I/O
C1	GND	D13	I/O	E25	I/O	G11	NC	H23	I/O
C2	GND	D14	I/O	E26	I/O	G12	NC	H24	I/O
C3	GND	D15	I/O	F1	I/O	G13	NC	H25	I/O
C4	GND	D16	I/O	F2	I/O	G14	NC	H26	I/O
C5	I/O	D17	I/O	F3	I/O	G15	NC	J1	I/O
C6	I/O	D18	I/O	F4	I/O	G16	NC	J2	I/O
C7	I/O	D19	I/O	F5	GND	G17	NC	J3	I/O
C8	I/O	D20	I/O	F6	I/O	G18	NC	J4	I/O
C9	I/O	D21	I/O	F7	NC	G20	NC	J5	I/O
C10	I/O	D22	I/O	F8	I/O	G19	V_{DDP}	J6	I/O
C11	I/O	D23	I/O	F9	I/O	G21	I/O	J7	NC
C12	I/O	D24	I/O	F10	I/O	G22	I/O	J8	V_{DDP}
C13	I/O	D25	I/O	F11	I/O	G23	I/O	J9	V_{DDL}
C14	I/O	D26	I/O	F12	I/O	G24	I/O	J10	V_{DDL}
C15	I/O	E1	I/O	F13	I/O	G25	I/O	J11	V_{DDL}
C16	I/O	E2	I/O	F14	I/O	G26	I/O	J12	V_{DDL}
C17	I/O	E3	I/O	F15	I/O	H1	I/O	J13	V_{DDL}
C18	I/O	E4	I/O	F16	I/O	H2	I/O	J14	V_{DDL}
C19	I/O	E5	I/O	F17	I/O	H3	I/O	J15	V_{DDL}
C20	I/O	E6	I/O	F18	I/O	H4	I/O	J16	V_{DDL}

676-Pin FBGA (Continued)

Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function	Pin Number	A500K270 Function
J17	V_{DDL}	L3	I/O	M15	GND	P1	GL	R13	GND
J18	V_{DDL}	L4	I/O	M16	GND	P2	I/O	R14	GND
J19	V_{DDP}	L5	I/O	M17	GND	P3	I/O	R15	GND
J20	NC	L6	I/O	M18	V_{DDL}	P4	I/O	R16	GND
J21	I/O	L7	NC	M19	V_{DDP}	P5	I/O	R17	GND
J22	I/O	L8	V_{DDP}	M20	NC	P6	I/O	R18	V_{DDL}
J23	I/O	L9	V_{DDL}	M21	I/O	P7	NC	R19	V_{DDP}
J24	I/O	L10	GND	M22	I/O	P8	V_{DDP}	R20	NC
J25	I/O	L11	GND	M23	I/O	P9	V_{DDL}	R21	I/O
J26	I/O	L12	GND	M24	I/O	P10	GND	R22	I/O
K1	I/O	L13	GND	M25	I/O	P11	GND	R23	I/O
K2	I/O	L14	GND	M26	I/O	P12	GND	R24	I/O
K3	I/O	L15	GND	N1	GL	P13	GND	R25	I/O
K4	I/O	L16	GND	N2	I/O	P14	GND	R26	I/O
K5	I/O	L17	GND	N3	I/O	P15	GND	T1	I/O
K6	I/O	L18	V_{DDL}	N4	I/O	P16	GND	T2	I/O
K7	NC	L19	V_{DDP}	N5	I/O	P17	GND	T3	I/O
K8	V_{DDP}	L20	NC	N6	I/O	P18	V_{DDL}	T4	I/O
K9	V_{DDL}	L21	I/O	N7	NC	P19	V_{DDP}	T5	I/O
K10	GND	L22	I/O	N8	V_{DDP}	P20	NC	T6	I/O
K11	GND	L23	I/O	N9	V_{DDL}	P21	I/O	T7	NC
K12	GND	L24	I/O	N10	GND	P22	I/O	T8	V_{DDP}
K13	GND	L25	I/O	N11	GND	P23	I/O	T9	V_{DDL}
K14	GND	L26	I/O	N12	GND	P24	I/O	T10	GND
K15	GND	M1	I/O	N13	GND	P25	I/O	T11	GND
K16	GND	M2	I/O	N14	GND	P26	I/O	T12	GND
K17	GND	M3	I/O	N15	GND	R1	I/O	T13	GND
K18	V_{DDL}	M4	I/O	N16	GND	R2	I/O	T14	GND
K19	V_{DDP}	M5	I/O	N17	GND	R3	I/O	T15	GND
K20	NC	M6	I/O	N18	V_{DDL}	R4	I/O	T16	GND
K21	I/O	M7	NC	N19	V_{DDP}	R5	I/O	T17	GND
K22	I/O	M8	V_{DDP}	N20	NC	R6	I/O	T18	V_{DDL}
K23	I/O	M9	V_{DDL}	N21	I/O	R7	NC	T19	V_{DDP}
K24	I/O	M10	GND	N22	GL	R8	V_{DDP}	T20	NC
K25	I/O	M11	GND	N23	I/O	R9	V_{DDL}	T21	I/O
K26	I/O	M12	GND	N24	I/O	R10	GND	T22	I/O
L1	I/O	M13	GND	N25	GL	R11	GND	T23	I/O
L2	I/O	M14	GND	N26	I/O	R12	GND	T24	I/O

676-Pin FBGA (Continued)

Pin Number	A500K270 Function
T25	I/O
T26	I/O
U1	I/O
U2	I/O
U3	I/O
U4	I/O
U5	I/O
U6	I/O
U7	NC
U8	V_{DDP}
U9	V_{DDL}
U10	GND
U11	GND
U12	GND
U13	GND
U14	GND
U15	GND
U16	GND
U17	GND
U18	V_{DDL}
U19	V_{DDP}
U20	NC
U21	I/O
U22	I/O
U23	I/O
U24	I/O
U25	I/O
U26	I/O
V1	I/O
V2	I/O
V3	I/O
V4	I/O
V5	I/O
V6	I/O
V7	NC
V8	V_{DDP}
V9	V_{DDL}
V10	V_{DDL}
V11	V_{DDL}
V12	V_{DDL}
V13	V_{DDL}
V14	V_{DDL}
V15	V_{DDL}
V16	V_{DDL}
V17	V_{DDL}
V18	V_{DDL}
V19	V_{DDP}
V20	NC
V21	I/O
V22	I/O
V23	I/O
V24	I/O
V25	I/O
V26	I/O
W1	I/O
W2	I/O
W3	I/O
W4	I/O
W5	I/O
W6	I/O
W7	V_{DDL}
W8	V_{DDL}
W9	V_{DDP}
W10	V_{DDP}
W11	V_{DDP}
W12	V_{DDP}
W13	V_{DDP}
W14	V_{DDP}
W15	V_{DDP}
W16	V_{DDP}
W17	V_{DDP}
W18	V_{DDP}
W19	V_{DDL}
W20	V_{DDP}
W21	I/O
W22	I/O
W23	I/O
W24	I/O
W25	I/O
W26	I/O
Y1	I/O
Y2	I/O
Y3	I/O
Y4	I/O
Y5	I/O
Y6	I/O
Y7	I/O
Y8	V_{DDP}
Y9	NC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	NC
Y15	NC
Y16	NC
Y17	NC
Y18	NC
Y19	V_{DDL}
Y20	V_{PP}
Y21	I/O
Y22	I/O
Y23	I/O
Y24	I/O
Y25	I/O
Y26	I/O

List of Changes

The following table lists critical changes that were made in the current version of the document.

Previous version	Changes in current version (v3.0)	Page
v2.0	WDATA has been changed to DI, and RDATA has been changed to DO to make them consistent with the signal names found in the *Macro Library Guide*.	
Preliminary v1.1	The "Product Plan" on page 3 has been updated to include the 256-FBGA package.	page 3
	The "Plastic Device Resources" on page 3 has been updated to include the 256-FBGA package.	page 3
	Figure 12 and Figure 13 on page 13 have been updated.	page 13
	The "Design Environment" on page 15 and Figure 17 on page 15 have been updated.	page 15
	Package Thermal Characteristics table on page 16 has been updated to include the 256-FBGA package.	page 16
	The "Calculating Power Dissipation" on page 17 has been changed.	page 17
	The "Programming and Storage Temperature LImits" on page 18 is new.	page 18
	The "DC Electrical Specifications (V_{DDP} = 2.5V)" on page 19 has been updated.	page 19
	The "DC Electrical Specifications (V_{DDP} = 3.3V)" on page 20 has been updated.	page 20
	The Table 4 on page 28 has been updated.	page 28
	The Table 5 on page 34 has been updated.	page 34
	The "256-FBGA (Bottom View)" on page 58 is new.	page 58
Preliminary v1.0	In the "676-pin FBGA (Bottom View)" on page 63, the functions for pins N1, N22, N25, and P1 have changed from I/O to GL	page 59
Advanced v.4	The section, "Clock Trees" on page 8 is new.	page 8
	The table, "DC Electrical Specifications (V_{DDP} = 3.3V)" on page 20 is new.	page 18
	The table, "AC Specifications (3.3V PCI Operation)" on page 22 is new.	page 20
	The table, the "Slew Rates Measured at Cout = 10pF (Total Output Load), Nominal Power Supplies and 25°C" on page 24 is new.	page 22
	The numbers found in the "Tristate Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, fCLOCK = 250 MHz)" on page 25 have changed.	page 23
	The numbers found in the "Output Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, fCLOCK = 250 MHz)" on page 26 have changed.	page 24
	The numbers found in the "Input Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, fCLOCK = 250 MHz)" on page 26 have changed.	page 24
	The numbers found in the "Global Input Buffer Delays (Worst-Case Commercial Conditions, V_{DDP} = 3.0V, V_{DDL} = 2.3V, T_J = 70°C, fCLOCK = 250 MHz)" on page 27 have changed.	page 25
	The "144-FBGA (Bottom View)" on page 55 for A500K050 is new.	pages 53-55
	The "676-pin FBGA (Bottom View)" on page 63 for A500K130 and A500K270 are new.	pages 56-60

Data Sheet Categories

In order to provide the latest information to designers, some data sheets are published before data has been fully characterized. These data sheets are marked as “Advanced” or Preliminary” data sheets. The definition of these categories are as follows:

Advanced

The data sheet contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

Preliminary

The data sheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

The data sheet contains information that is considered to be final.

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5172140-7/2.02