A5268

3A, 28V, 340KHz Synchronous Rectified Step-Down Converter

■ General Description

The A5268 is a fixed frequency monolithic synchronous buck regulator that accepts input voltage from 4.75V to 28V. Two NMOS switches with low on-resistance are integrated on the die. Current mode topology is used for fast transient response and good loop stability.

Shutdown mode reduces the input supply current to less than 1μA. An adjustable soft-start prevents inrush current at turn-on.

This device is available in SOP-8/PP package with exposed pad for low thermal resistance.

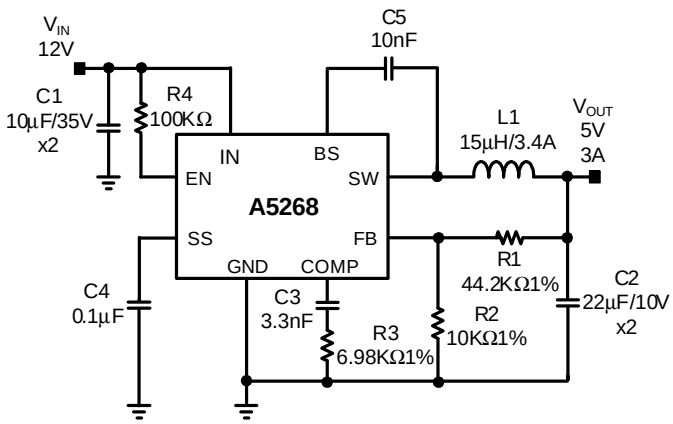
■ Applications

- Distributed Power System
- Networking System
- FPGA, DSP, ASIC Power Supplies
- Notebook Computers

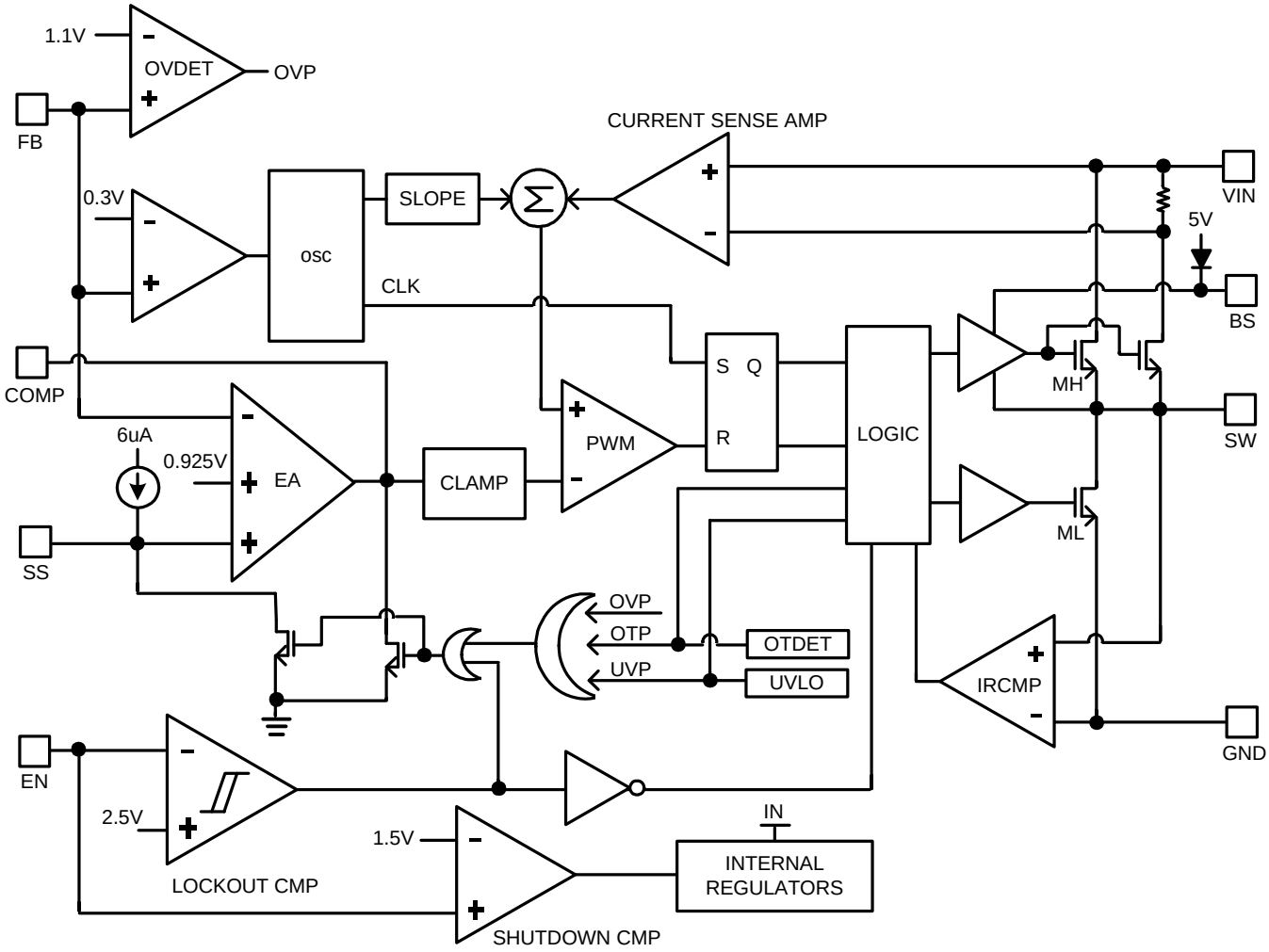
■ Features

- 3A Output Current
- Wide 4.75V to 28V Operating Input Range
- Integrated Power MOSFET Switches
- Output Adjustable from 0.925V to 25V
- Up to 95% Efficiency
- Programmable Soft Start
- Stable with Low ESR Ceramic Output Capacitors
- Cycle-by Cycle Over Current Protection
- Fixed 340KHz Frequency
- Input Under Voltage Lockout
- System Protected by Over-current Limiting, Over-voltage Protection and Thermal Shutdown
- Thermally Enhanced SOP-8/PP Package
- Green Products Meet RoHS Standards

■ Typical Application

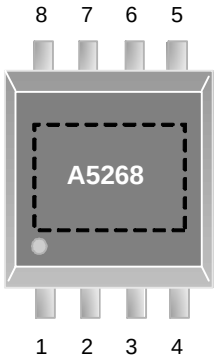


■ Functional Block Diagram



■ Pin Configuration

SOP-8/PP
Top View



A5268

1. BS
2. IN
3. SW
4. GND
5. FB
6. COMP
7. EN
8. SS

Die Attach:
Conductive Epoxy

Note:
The area enclosed by dashed line represents Exposed Pad and connect to GND.

■ Pin Description

Pin Number	Pin Name	Pin Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 10nF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. IN supplies the power to the IC, as well as the step-down converter switches. Drive IN with a 4.75V to 28V power source. Bypass IN to GND with a suitable large capacitor to eliminate noise on the input to the IC.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load. Note that a capacitor is required from SW to BS to power the high-side switch.
4	GND	Ground. Connect the exposed pad to pin 4.
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback reference voltage is 0.925V.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN higher than 2.7V to turn on the regulator, drive it lower than 1.1V to turn it off. Pull up to the IN pin with 100KΩ resister for automatic start up.
8	SS	Soft-start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. Add a 0.1μF capacitor set the soft-start period to 15mS. To disable the soft start feature, leave the SS unconnected.

■ Absolute Maximum Ratings

Parameter	Maximum	Unit
Supply Voltage	-0.3V to +30V	V
Switch Voltage	-1V to V_{IN}+0.3	V
Boost Switch Voltage	-0.3V to V_{SW} + 6	V
All Other Pins	-0.3V to +6	V
EN Voltage	-0.3V to V_{IN}	V
ESD Classification (HBM)	2	kV
ESD Classification (MM)	200	V

■ Recommended Operating Conditions

Parameter	Rating	Unit
Ambient Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	°C
Storage Temperature Range	-65 to +150	°C

■ Thermal Information

Parameter	Package	Die Attach	Symbol	Maximum	Unit
Thermal Resistance* (Junction to Case)	SOP-8/PP	Conductive Epoxy	θ_{JC}	19	°C / W
Thermal Resistance (Junction to Ambient)	SOP-8/PP		θ_{JA}	84	
Internal Power Dissipation	SOP-8/PP		P_D	1450	mW
Maximum Junction Temperature				150	°C
Solder Iron(10 Sec)**				350	

* Measure θ_{JC} on backside center of Exposed Pad.
** MIL-STD-202G 210F

■ Electrical Specifications

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Shutdown Current	I_{SHDN}	V_{EN} = 0V		1	3.0	μA
Supply Current		V_{EN} = 3V, V_{FB} = 1.2V		1.3	1.5	mA
Feedback Voltage	V_{FB}	4.75V <= V_{IN}<=28V	0.90	0.925	0.95	V
OVP Threshold Voltage				1.10		V
Error Amplifier Voltage Gain	A_{EA}			400		V/V
Error Amplifier Transconductance	G_{EA}	ΔIC = ±10μA		800		μA/V
High-side Switch On Resistance	$R_{DS,ON,HI}$			135		mΩ
Low-side Switch On Resistance	$R_{DS,ON,LO}$			105		mΩ
Switch Leakage Current	$I_{SW,LK}$	V_{EN} = 0V, V_{SW} = 0V			10	μA
High-side Switch Current Limit		Minimum Duty Cycle	4	5.8		A
Low-side Switch Current Limit		From Drain to Source		1.25		A
COMP to Current Sense Transconductance	G_{CS}			5.2		A/V
Current Limit Oscillation Frequency	$f_{OSC,CL}$	T_A = 25°C	300	340	380	KHz
		-40°C<=T_A<=+85°C	270		400	KHz
Short Circuit Oscillation Frequency	$f_{OSC,SCR}$	V_{FB} = 0V		116		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} =0.8V		90		%
Minimum On Time	$t_{ON,MIN}$			220		nS
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising, T_A = 25°C	3.8	4.05	4.3	V
		-40°C<=T_A<=+85°C	3.5		4.7	V
Input Undervoltage Lockout Hysteresis	$V_{UVLO,HYST}$			210		mV
Soft-Start Current Source	I_{SS}	V_{SS} = 0V		6		μA
Soft-Start Period	t_{SS}	C_{SS} = 0.1μF		15		mS
EN Lockout Threshold Voltage	V_{EN}	T_A = 25°C	2.2	2.5	2.7	V
		-40°C<=T_A<=+85°C	2.2		2.7	V

■ Electrical Specifications (Contd.)

V_{IN} = 12V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.56	2	V
EN Shutdown Threshold Voltage Hysteresis				210		mV
EN Lockout Hysteresis				210		mV
Thermal Shutdown Temperature	OTP	Shutdown, temperature increasing		160		°C
Thermal Shutdown Hysteresis	OTH	Restore, temperature decreasing		20		°C

■ Detailed Description

Oscillator Frequency

The internal free running oscillator sets the PWM frequency at 340KHz.

Enable and Soft start

The EN Pin provides electrical on/off control of the regulator. Once the EN pin voltage exceeds the lockout threshold voltage, the regulator starts operation and the soft start begins to ramp. If the EN pin voltage is pulled below the lockout threshold voltage, the regulator stops switching and the soft start resets. Connecting the pin to ground or to any voltage less than 1.1V will disable the regulator and activate the shutdown mode. To limit the start-up inrush current, a soft-start circuit is used to ramp up the reference voltage from 0V to its final value, linearly. The soft-start time is 15 ms typically.

Under Voltage Lockout (UVLO)

The A5268 incorporates an under voltage lockout circuit to keep the device disabled when V_{IN} (the input voltage) is below the UVLO start threshold voltage. During power up, internal circuits are held inactive and the soft start is grounded until V_{IN} exceeds the UVLO start threshold voltage. Once the UVLO start threshold voltage is reached, the soft start is released and device start-up begins. The device operates until V_{IN} falls below the UVLO stop threshold voltage. The typical hysteresis in the UVLO comparator is 210mV.

Over-Current Protection

Overcurrent limiting is implemented by monitoring the current through the high side MOSFET. If this current exceeds the over-current threshold limit, the overcurrent indicator is set true. The system will ignore the over-current indicator for the leading edge blanking time at the beginning of each cycle to avoid any turn-on noise glitches.

Once overcurrent indicator is set true. The high-side MOSFET is turned off for the rest of the cycle after a propagation delay. This over-current limiting mode is called cycle-by-cycle current limiting.

Over-voltage Protection

The A5268 has an over-voltage protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions. The OVP circuit include an over-voltage comparator to compare the FB pin voltage and a threshold of 120% x V_{FB}. Once the FB pin voltage is higher than the threshold, the COMP pin and the SS pin are discharged to GND, forcing the high-side MOSFET off. When the FB pin voltage drops lower than the threshold, the high-side MOSFET will be enabled again.

Thermal Shutdown

The A5268 protects itself from overheating with an internal thermal shutdown circuit. If the junction temperature exceeds the thermal shutdown trip point, the voltage reference is grounded and the high-side MOSFET is turned off. The part is restarted under control of the soft start circuit automatically when the junction temperature drops 30°C below the thermal shutdown trip point.

Component Selection

Setting the Output Voltage

The output voltage is using a resistive voltage divider connected from the output voltage to FB. It divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = V_{OUT} \frac{R_2}{R_1 + R_2}$$

the output voltage is:

$$V_{OUT} = 0.925 \times \frac{R_1 + R_2}{R_2}$$

■ Detailed Description (Contd.)

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will have a larger physical size, higher series resistance, and lower saturation current. It will result in less ripple current that will in turn result in lower output ripple voltage. Make sure that the peak inductor current is below the maximum switch current limit. Determine inductance is to allow the peak-to peak ripple current to be approximately 30% of the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where fs is the switching frequency, V_{IN} is the input voltage, V_{OUT} is the output voltage, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current. The choice of which style inductor to use mainly depends on the price vs. size requirements and any EMI constraints.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also be suggested. Choose X5R or X7R dielectrics when using ceramic capacitors.
Since the input capacitor (C1) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

At $V_{IN} = 2V_{OUT}$, where IC1 = $I_{LOAD}/2$ is the worst-case condition occurs. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. When using electrolytic or tantalum capacitors, a high quality, small ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C1 \times f_s} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C1 is the input capacitance value.

Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_s \times C2}\right)$$

Where R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor and C2 is the output capacitance value.
When using ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance which is the main cause for the output voltage ripple. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_s^2 \times L \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

When using tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The A5268 can be optimized for a wide range of capacitance and ESR values.

■ Detailed Description (Contd.)

Compensation Components

A5268 has current mode control for easy compensation and fast transient response. The system stability and transient response are controlled through the C_{OMP} pin. C_{OMP} is the output of the internal transconductance error amplifier. A series capacitor-resistor combination sets a pole-zero combination to govern the characteristics of the control system. The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{OUT}}$$

Where V_{FB} is the feedback voltage (0.925V), A_{VEA} is the error amplifier voltage gain, G_{CS} is the current sense transconductance and R_{LOAD} is the load resistor value. The system has two poles of importance. One is due to the output capacitor and the load resistor, and the other is due to the compensation capacitor (C3) and the output resistor of the error amplifier. These poles are located at:

$$f_{P1} = \frac{G_{EA}}{2p \times C3 \times A_{VEA}}$$

$$f_{P2} = \frac{1}{2p \times C2 \times R_{LOAD}}$$

Where G_{EA} is the error amplifier transconductance.
The system has one zero of importance, due to the compensation capacitor (C3) and the compensation resistor (R3). This zero is located at:

$$f_{Z1} = \frac{1}{2p \times C3 \times R3}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESR} = \frac{1}{2p \times C2 \times R_{ESR}}$$

In this case, a third pole set by the compensation capacitor (C6) and the compensation resistor (R3) is used to compensate the effect of the ESR zero on the loop gain. This pole is located at:

$$f_{P3} = \frac{1}{2p \times C6 \times R3}$$

The goal of compensation design is to shape the converter transfer function to get a desired loop gain. The system crossover frequency where the feedback loop has the unity gain is important. Lower crossover frequencies result in slower line and load transient responses, while higher crossover frequencies could cause system instability. A good standard is to set the crossover frequency below one-tenth of the switching frequency. To optimize the compensation components, the following procedure can be used.

1. Choose the compensation resistor (R3) to set the desired crossover frequency.
Determine R3 by the following equation:

$$R3 = \frac{2p \times C2 \times f_C}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} < \frac{2p \times C2 \times 0.1 \times fs}{G_{EA} \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}}$$

Where f_C is the desired crossover frequency which is typically below one tenth of the switching frequency.

2. Choose the compensation capacitor (C3) to achieve the desired phase margin. For applications with typical inductor values, setting the compensation zero (fZ1) below one-forth of the crossover frequency provides sufficient phase margin.
Determine C3 by the following equation:

$$C3 > \frac{4}{2p \times R3 \times f_C}$$

Where R3 is the compensation resistor.

■ Detailed Description (Contd.)

3. Determine if the second compensation capacitor (C6) is required. It is required if the ESR zero of the output capacitor is located at less than half of the switching frequency, or the following relationship is valid:

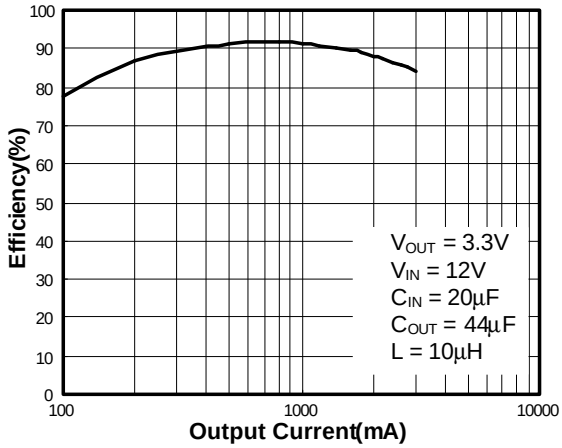
$$\frac{1}{2p \times C2 \times R_{ESR}} < \frac{f_S}{2}$$

If this is the case, then add the second compensation capacitor (C6) to set the pole fP3 at the location of the ESR zero. Determine C6 by the equation:

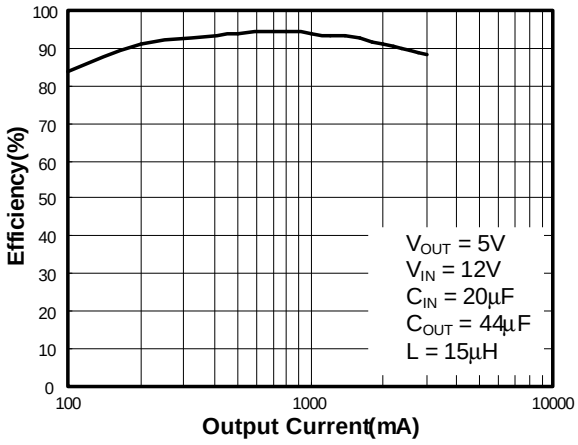
$$C6 = \frac{C2 \times R_{ESR}}{R3}$$

■ Characterization Curve

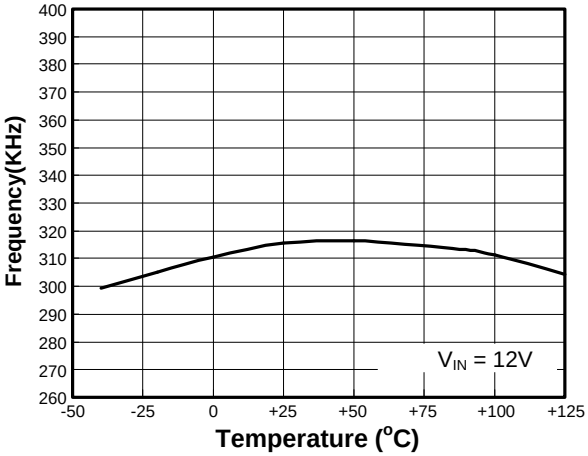
Efficiency vs. Output Current



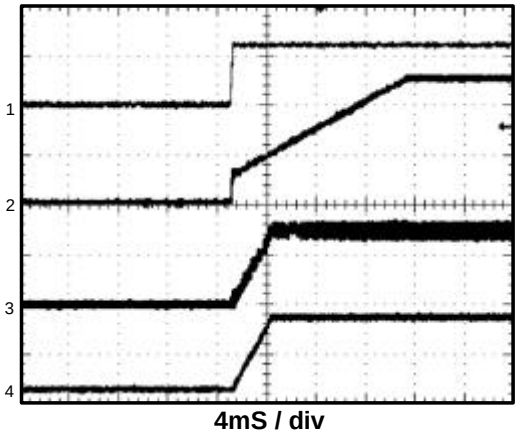
Efficiency vs. Output Current



Frequency vs. Temperature



Start-Up form EN

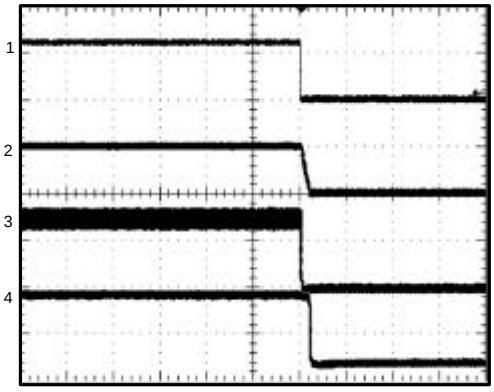


V_{IN} = 12V
V_{OUT} = 5V
I_{OUT} = 3000mA
C_{SS} = 0.1µF

1) EN = 5V/div
2) V_{OUT} = 2V/div
3) I_L = 2A/div
4) I_{OUT} = 2A/div

■ Characterization Curve

Power Off from EN

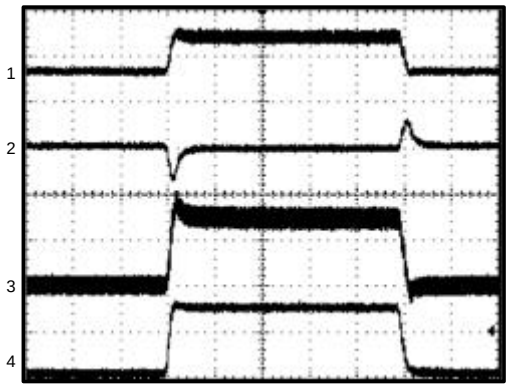


400㎳S / div

V_{IN} = 12V
V_{OUT} = 5V
I_{OUT} = 3000mA
C_{SS} = 0.1µF

1) EN = 5V/div
2) V_{OUT} = 5V/div
3) I_L = 2A/div
4) I_{OUT} = 2A/div

Load Step

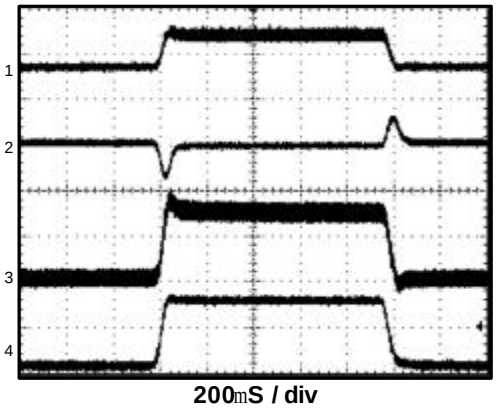


200㎳S / div

V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 0mA to 3000mA
C_{SS} = 470pF, T_A =25°C

1) V_{COMP} = 1V/div
2) V_{OUT} = 500mV/div
3) I_L = 2A/div
4) I_{OUT} = 2A/div

Load Step



200㎳S / div

V_{IN} = 12V
V_{OUT} = 5V
I_{OUT} = 0mA to 3000mA
C_{SS} = 470pF, T_A =25°C

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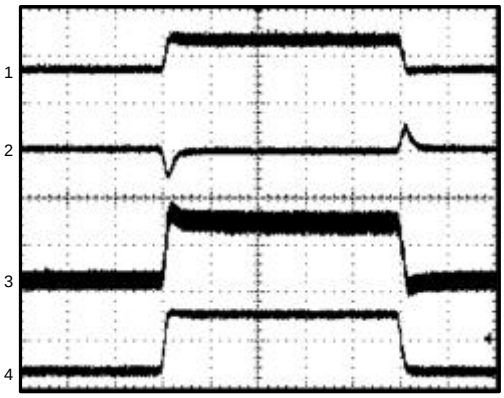
3) I_L = 2A/div
4) I_{OUT} = 2A/div

Load Step



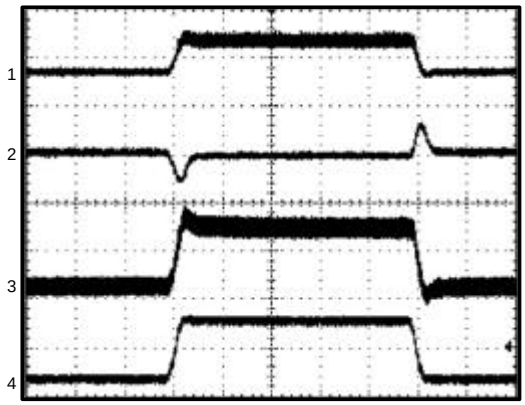
200㎳S / div

V_{IN} = 12V
V_{OUT} = 3.3V
I_{OUT} = 500mA to 3000mA
C_{SS} = 470pF, T_A =25°C

1) V_{COMP} = 1V/div
2) V_{OUT} = 500mV/div
3) I_L = 2A/div
4) I_{OUT} = 2A/div

■ Characterization Curve

Load Step

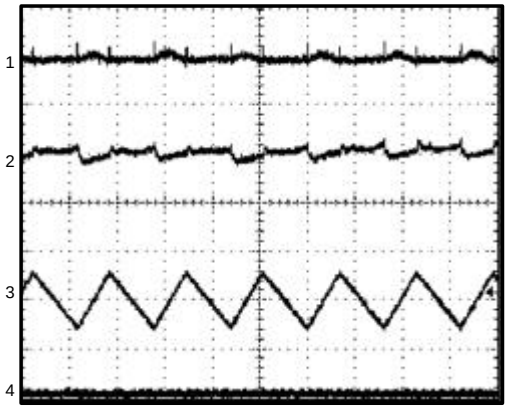


200μS / div

V_{IN} = 12V
V_{OUT} = 5V
I_{OUT} = 500mA to 3000mA
C_{SS} = 470pF, T_A =25°C

1) V_{COMP} = 1V/div
2) V_{OUT} = 500mV/div
3) I_L = 2A/div
4) I_{OUT} = 2A/div

Stead State Test



2μS / div

V_{IN} = 12V
V_{OUT} = 5V
I_{OUT} = 0mA
C_{SS} = 470pF

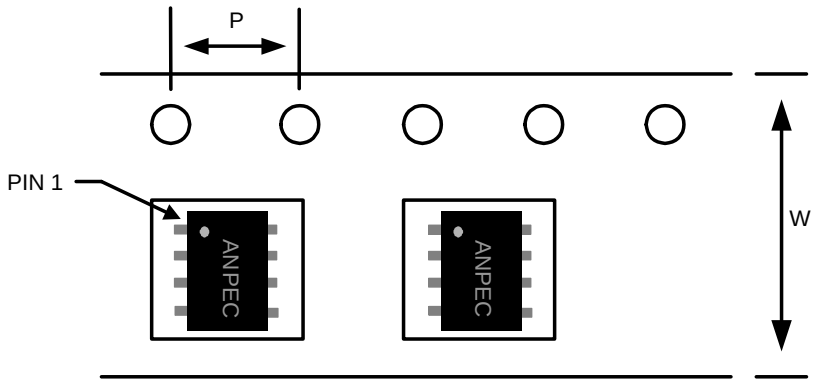
1) V_{IN} = 50V/div
2) V_{COMP} = 20mV/div
3) I_L = 500mA/div
4) I_{OUT} = 500mA/div

■ Date Code Rule

Month Code	
1: January	7: July
2: February	8: August
3: March	9: September
4: April	A: October
5: May	B: November
6: June	C: December

■ Tape and Reel Dimension

SOP-8/PP



Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
SOP-8/PP	12.0±0.1 mm	4.0±0.1 mm	2500pcs	330±1 mm