A5944

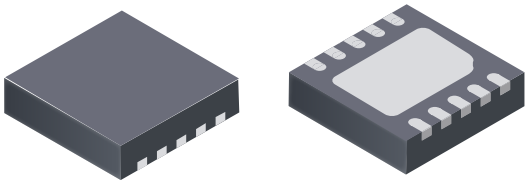
Three-Phase Sensorless Fan Driver

FEATURES AND BENEFITS

- Sinusoidal drive for low audible noise
- Quiet startup adjustment feature
- High efficiency control algorithm
- Sensorless operation
- PWM speed input
- FG speed output
- Lock detection
- Short-circuit protection
- Standby mode

PACKAGE:

10-contact 3 mm × 3 mm DFN package with exposed thermal pad (suffix EJ)



Not to scale

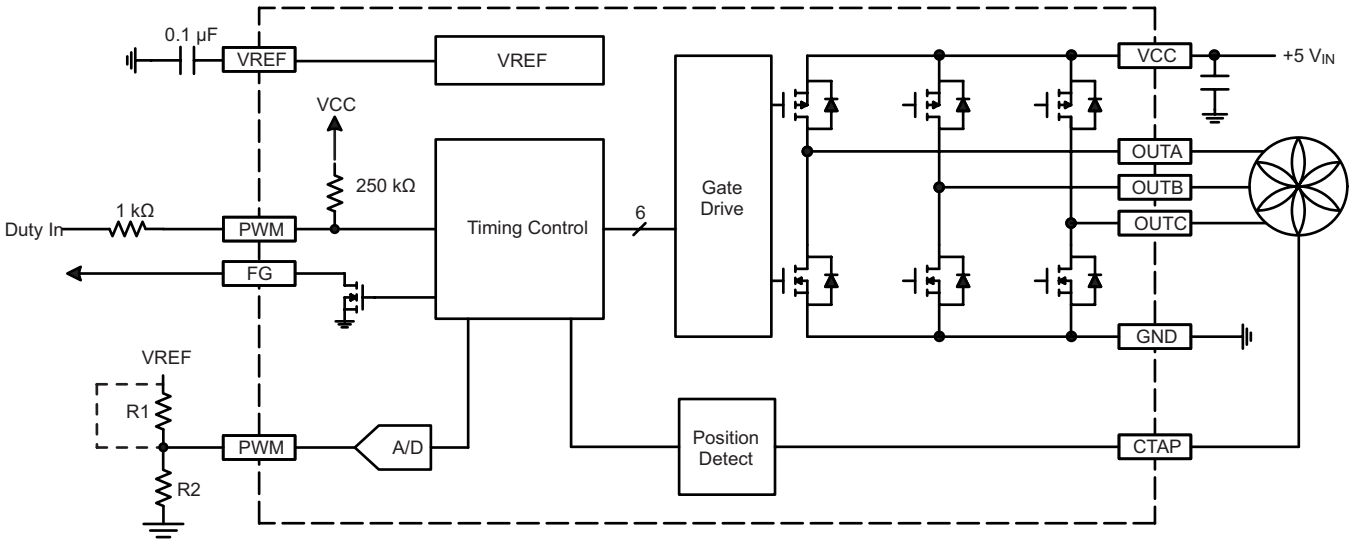
DESCRIPTION

The A5944 three-phase motor drivers incorporate sinusoidal drive to minimize audible noise and vibration for medium power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly start and gradually ramp up the motor to desired speed. The voltage profile is selectable via pin SOFTST to allow proper operation with a wide range of motor characteristics.

The motor speed is controlled by applying a duty cycle command to the PWM input. The PWM input is allowed to operate over a wide frequency range.

The A5944 is supplied in a 10-contact 3 mm × 3 mm DFN package with exposed thermal pad (suffix EJ). The package is lead (Pb) free, with 100% matte-tin leadframe plating.



Typical Application Diagram

SELECTION GUIDE

Part Number	Option	Package	Packing
A5944GEJTR-T	Standard IC	10-contact DFN with exposed thermal pad	1500 pieces per 7-inch reel
A5944GEJTR-1-T	Option 1	10-contact DFN with exposed thermal pad	1500 pieces per 7-inch reel

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS WITH RESPECT TO GND

Characteristic	Symbol	Notes	Rating	Unit
Supply Voltage	V_{CC}		6	V
OUTA, OUTB, OUTC	V_{OUT}		V_{CC} + 1	V
Input Voltage Range	V_{IN}	PWM	–0.3 to 6	V
Logic Output Voltage – FG	V_O	FG	6	V
FG Current	I_{FG}		5	mA
Output Current	I_{OUT}		1	A
Ambient Operating Temperature Range	T_A		–40 to 105	°C
Junction Temperature	T_J		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	On 2-sided PCB with 1 in.^{2} of copper area each side	55	°C/W

*Additional thermal information available on the Allegro website.

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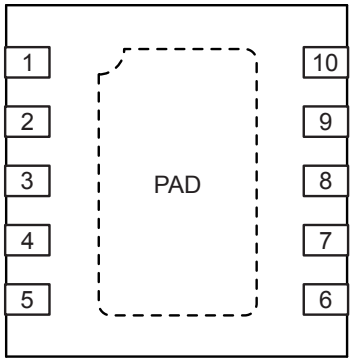
PINOUT DIAGRAM AND TERMINAL LIST TABLE



Package EJ, 10-Contact DFN Pinout Diagram

Terminal List Table

Number	Name	Function
1	FG	Speed Output Signal
2	CTAP	Motor Terminal
3	VCC	Input Supply
4	OUTA	Motor Terminal
5	GND	Ground
6	OUTC	Motor Terminal
7	OUTB	Motor Terminal
8	VREF	Analog Output
9	SOFTST	Analog Input
10	PWM	Logic Input - Speed
–	PAD	Exposed thermal pad, connect to GND

RECOMMENDED OPERATIONAL RANGE

Characteristic	Symbol	Test Conditions*	Value			Unit
			Min.	Typ.	Max.	
VCC Supply Voltage*	V_{CC}		4.5	5	5.5	V
Output Current	I_{OUT}	Rms Phase Current	–	–	450	mA

*A5944 will operate down to 3 V level, 5 V range is recommended for startup condition.

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ELECTRICAL CHARACTERISTICS: Valid at T_A = 25°C, V_{CC} = 3 to 5.5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
SUPPLIES						
VCC Supply Current	I_{CC}		–	5.5	7.5	mA
		Standby Mode, V_{CC} = 5 V	–	25	35	µA
Total Driver R_{DSON} (Sink + Source)	R_{DSON}	I = 500 mA, T_J = 25°C, V_{CC} = 5 V	–	0.74	1	Ω
		Source driver, T_J = 25°C, V_{CC} = 5 V	–	0.48	–	Ω
		Sink driver, T_J = 25°C, V_{CC} = 5 V	–	0.26	–	Ω
VREF	V_{REF}	I_{OUT} = 5 mA	2.7	2.8	2.9	V
Input Current (PWM)	I_{IN}	V_{IN} = 0 V (250 kΩ pullup), V_{CC} = 5 V	14	20	26	µA
Logic Input Low Level	V_{IL}	PWM	–	–	0.8	V
Logic Input High Level	V_{IH}		2	–	–	V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Saturation Voltage	V_{SAT}	I = 5 mA	–	–	0.3	V
FG Output Leakage	I_{FG}	V = 5 V, FG switch OFF	–	–	1	µA
PWM Duty On Threshold	DC_{ON}		–	9	–	%
PWM Duty Off Threshold	DC_{OFF}		–	7.5	–	%
PWM Input Frequency Range	f_{PWM}		0.1	–	100	kHz
Lock Timing	t_{OFF}		4.5	5	5.5	s
SOFTST Input Current	I_{SOFT}		–1	0	1	µA
Motor PWM Frequency	f_{PWM}	A5944GEJTR-T	22.5	25	27.5	kHz
		A5944GEJTR-1-T	45	50	55	kHz
PROTECTION						
VCC UVLO	V_{CCUVLO}	V_{CC} rising	–	2.7	2.95	V
VCC UVLO Hysteresis	V_{CCHYS}		100	150	220	mV
Overcurrent	I_{OCL}		650	850	1050	mA
Thermal Shutdown Threshold	T_{JTSD}	Temperature increasing	150	165	180	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = $T_{JTSD} - \Delta T_J$	–	20	–	°C

*Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

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FUNCTIONAL DESCRIPTION

The A5944 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input.

The PWM input duty is measured and converted to a 9-bit number. This 9-bit "demand" is applied to a PWM generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120-degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

A BEMF detection "window" is opened on phase A modulation profile to measure the rotor position to define the modulation timing. The control system maintains the window to a small level to minimize the disturbance and approximate the ideal sinusoidal current waveform as much as possible.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor, and thermal shutdown.

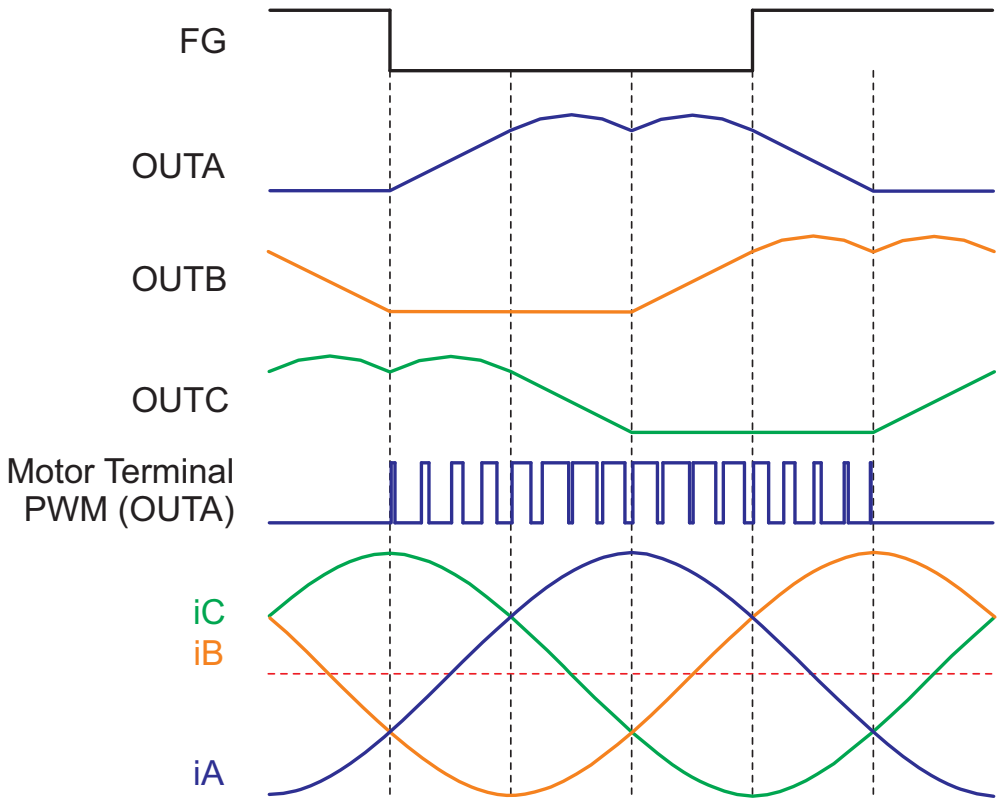

Figure 1: Sinusoidal PWM

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Speed Control

PWM – Duty Cycle Input. A duty cycle measurement circuit converts the applied duty to a demand value (9-bit resolution) to control speed of the fan.

The motor drive will be enabled if duty is larger than DC_ON The PWM input is filtered to prevent spurious noise from turning on or off unexpectedly.

To allow motor to run at 100% with input PWM signal open circuit, connect an external pullup resistor to VCC.

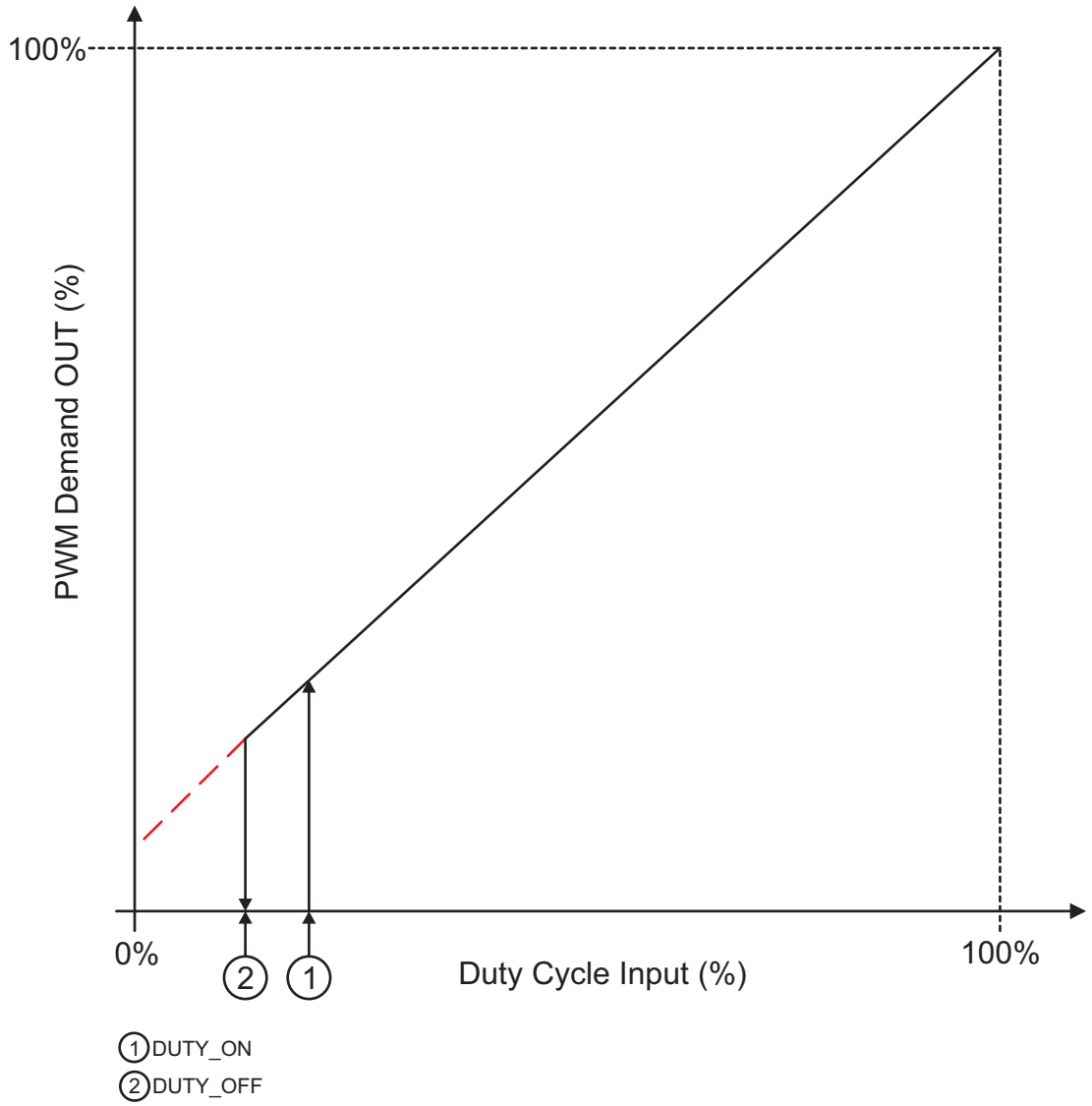

Figure 2: Speed Input Characteristic

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CTAP. Motor common connection. If motor common is not available, the centertap voltage will be generated internally.

Do not add any components to this pin, use direct line to motor common, or leave open circuit.

Lock Detect. Speed is monitored to determine if rotor is locked. If a lock condition is detected, the IC will be disabled for t_{OFF} before an auto-restart is attempted. The first time a lock condition occurs, there is a quick (1 second) delay before restart. Subsequent lock events will result in the full t_{OFF} delay before restart.

Standby Mode. A low-power standby mode achieves minimum power supply consumption for idle state. Standby mode powers down internal circuitry, including VREF, to reduce power dissipation in the idle state. Upon power up, IC is activated and waits for valid PWM duty signal. If PWM is held low for 5 seconds, then the IC enters low-power standby mode.

FG. Open-drain output provides speed information to the system. FG is aligned to the modulation profile as shown in Figure 1.

Maximum Speed Limit. The maximum electrical frequency allowed by A5944 is indicated in Table 1.

Fan maximum speed is related to electrical frequency by:

$$RPM = ElecF \times 60 / (\#polepair)$$

Table 1: Difference Between Part Variants

Part Number	Option	Motor PWM (kHz)	Max. Electrical Frequency	FG
A5944GEJTR-T	Standard IC	25	333 Hz	1 FG period per electrical revolution
A5944GEJTR-1-T	Option 1	50	1.5 kHz	1 FG period per 3 electrical revolutions

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Startup Adjustment

Various permutations of startup parameters are chosen via lookup table with A/D conversion.

16 choices of startup parameters are selected by applying voltage at pin SOFTST.

A resistor divider in range 5 to 20 kΩ is recommended.

The various selections have different choices for open-loop duration, open-loop demand, and initial demand value of soft-start after the open-loop startup period.

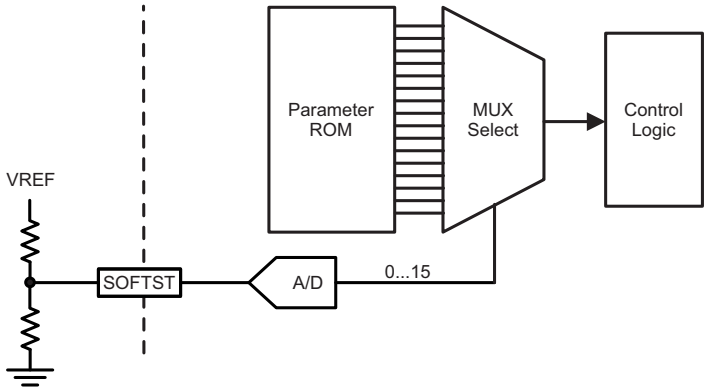

Figure 3: Startup Parameters

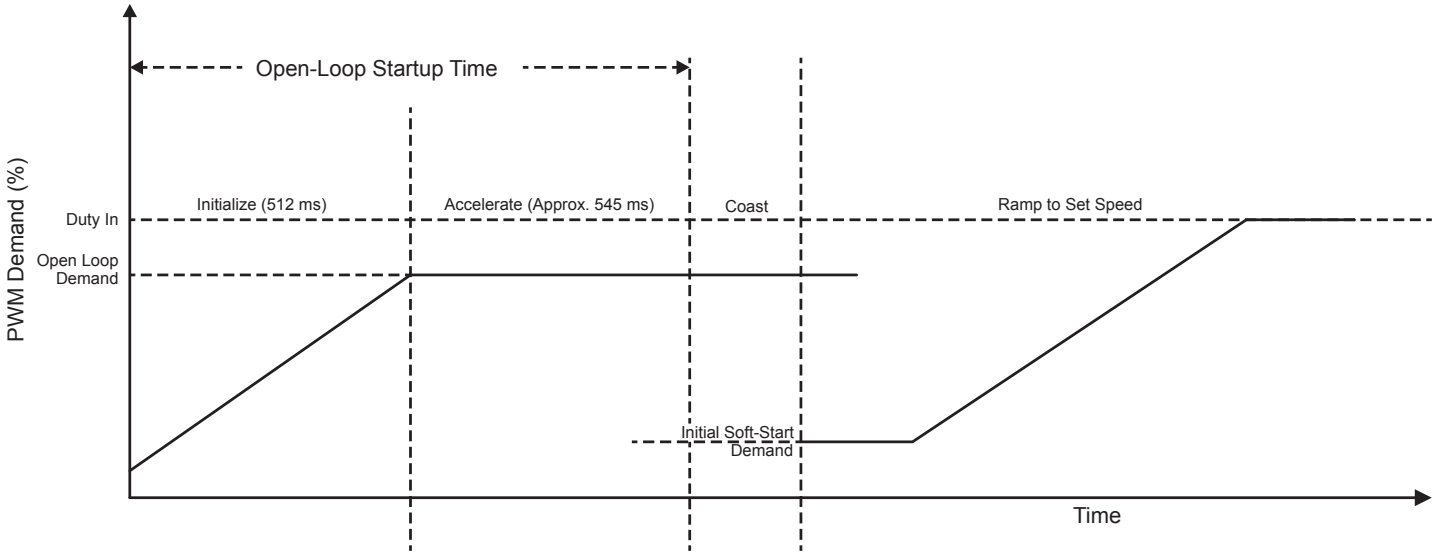

Figure 4: Open-Loop Startup Time

V_{SOFTST}	CODE	Open-Loop Demand (s)	Acceleration Rate (Hz/s)	Initial Demand (%)
GND	0	25%	50	12
0.18	1	25%	20	12
0.37	2	25%	30	12
0.56	3	25%	40	12
0.74	4	25%	60	12
0.93	5	25%	70	12
1.12	6	25%	80	12
1.30	7	25%	90	12

V_{SOFTST}	CODE	Open-Loop Demand (s)	Acceleration Rate (Hz/s)	Initial Demand (%)
1.49	8	50%	20	20
1.68	9	50%	30	20
1.86	10	50%	40	20
2.05	11	50%	50	20
2.24	12	50%	70	20
2.42	13	50%	80	20
2.61	14	50%	90	20
VREF	15	50%	60	20

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APPLICATION INFORMATION

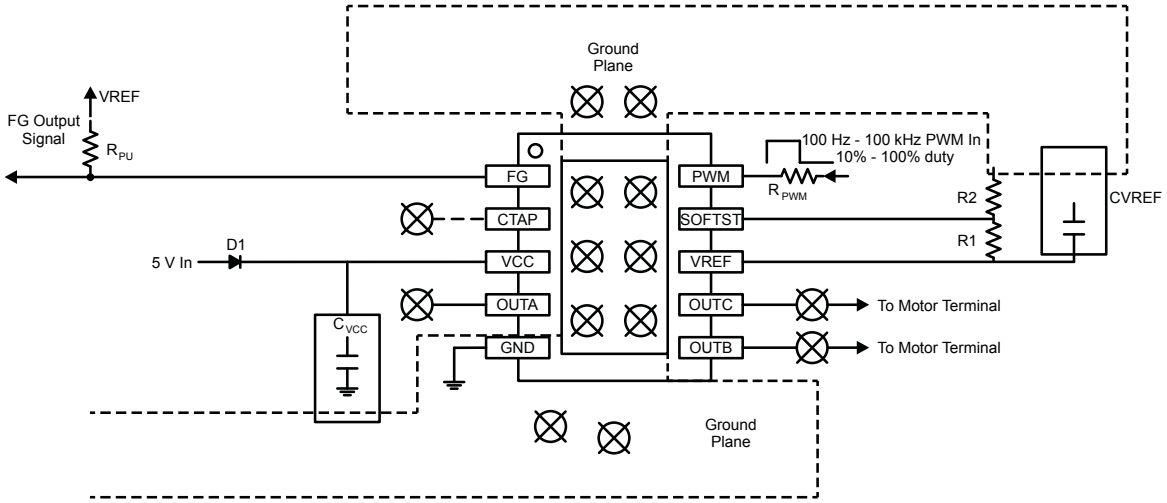

Figure 5: Typical Application Circuit

Name	Suggested Value	Comment
CVREF	0.1 µF/X 5 R/10 V	Ceramic capacitor required.
CVCC	1 µF - 10 µF	Power Supply Stabilization – Electrolytic or ceramic OK.
R_{FG}	10 kΩ	Optional – pull-up resistor for speed feedback.
R1/R2	R1 + R2 = 10 kΩ	Optional – used to set SOFST parameter. Connect to VREF or GND if not used.
D1	Not installed	May be required to isolate motor from system or for reverse polarity protection.
R_{PWM}	1 kΩ	Optional – If PWM wired to connector – RPWM will isolate IC pin from noise or overvoltage transients.

Layout Notes.
Add thermal vias to exposed pad area. Add ground plane on top and bottom of PCB.
Place CVREF & CVCC as close as possible to IC.

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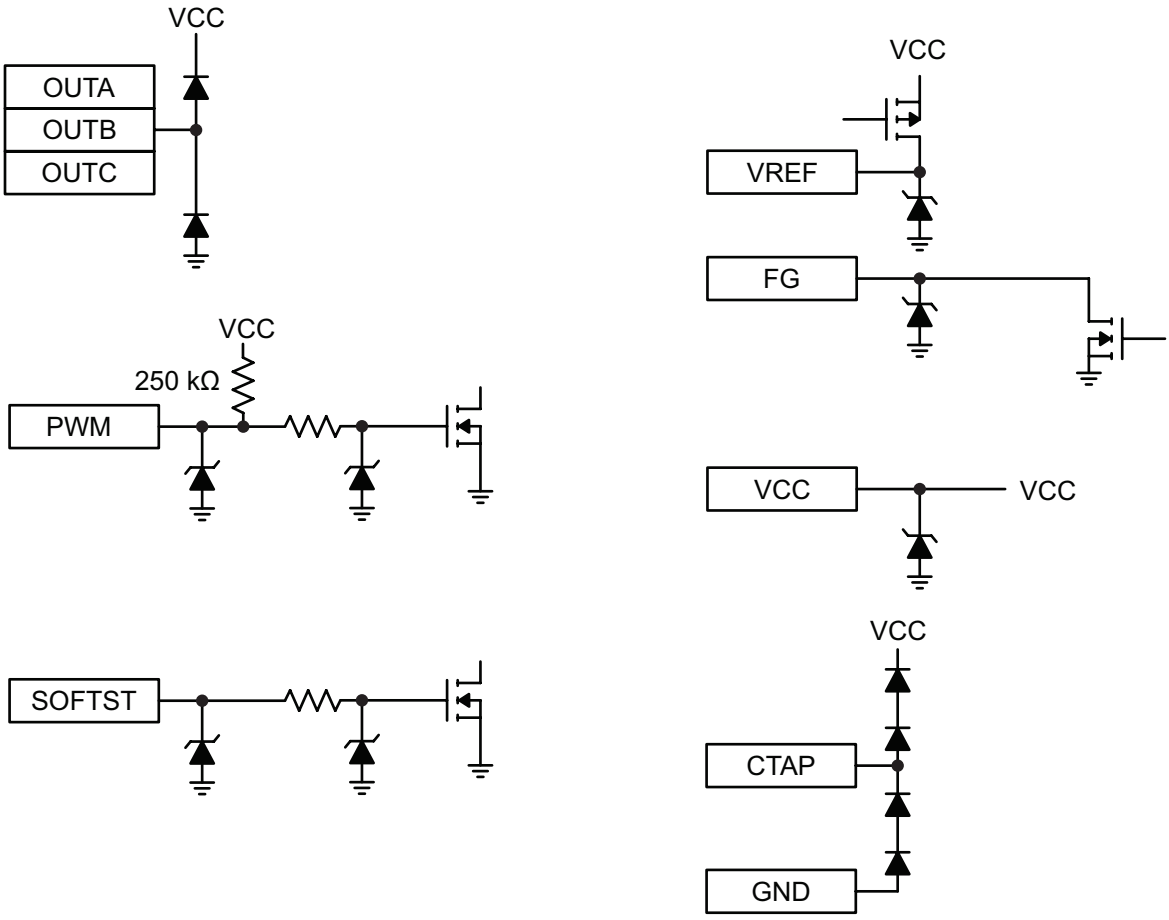
PIN CIRCUIT DIAGRAMS



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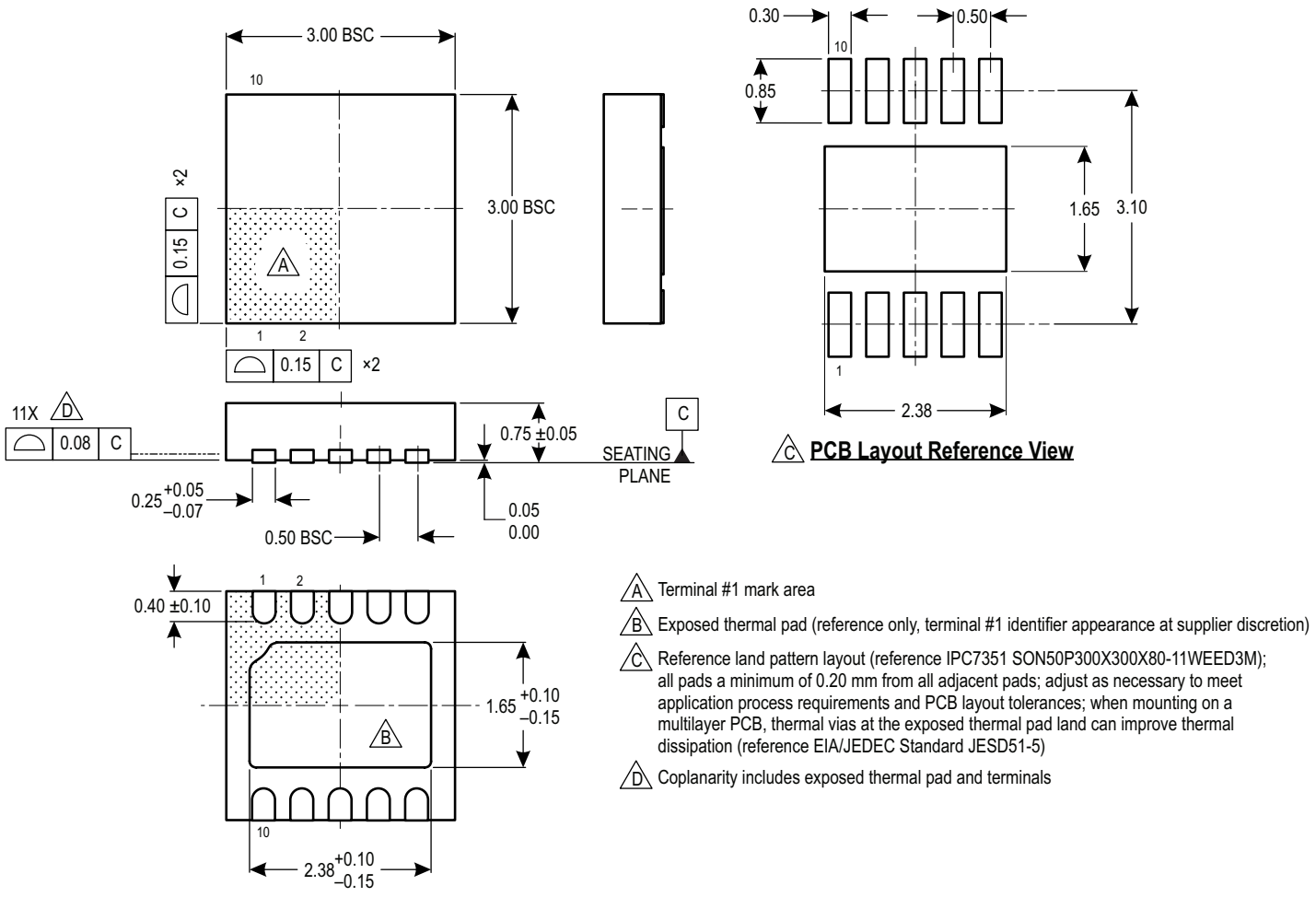
PACKAGE OUTLINE DRAWING

For Reference Only – Not for Tooling Use

(Reference DWG-0000372)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Figuer 6: Package EJ, 10-Pin DFN with Exposed Thermal Pad

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REVISION HISTORY

Number	Date	Description
–	August 15, 2014	Initial Release
1	November 20, 2014	Added V_{OUT} to Absolute Maximum Ratings table
2	November 4, 2016	Changed package offering to EJ
3	February 27, 2017	Updated Table 1, Option 1 Max Electrical Freqency
4	July 29, 2019	Corrected packing count in Selection Guide (page 2) and minor editorial updates
5	July 27, 2021	Updated package drawing (page 11)
6	November 2, 2023	Corrected package drawing (page 11)

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