Three Phase Sinusoidal Fan Controller

FEATURES AND BENEFITS

- AEC-Q100 qualified – K version
- Sinusoidal Drive For Low Audible Noise
- Quiet StartUp
- Proprietary High Efficiency Control Algorithm
- Adjustable Current Source Based Gate Drive
- Speed Input
  - PWM – A5949
  - Analog – A5939
- Windmill Detection
- Hall Element or Hall Latch Compatible
- FG Speed Output
- Lock Detection
- Overcurrent Limit (OCL)
- Short Circuit Protection (OCP)
- Direction Input
- Brake Input

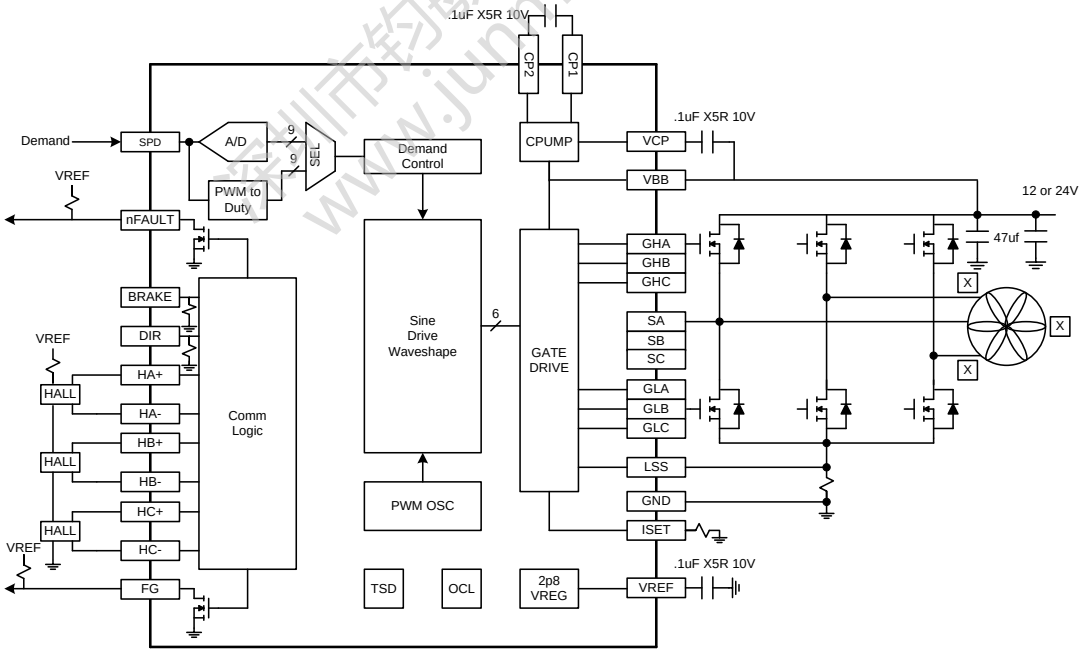
DESCRIPTION

The A5939/A5949 three phase motor controller incorporates sinusoidal drive to minimize audible noise and vibration for high power fans.

A sinusoidal voltage profile is applied to the windings of the motor at startup to quietly startup and gradually ramp up the motor to desired speed.

For A5949, The motor speed is controlled by applying a Duty cycle command to the SPD input The SPD input is allowed to operate over a wide frequency range. For the A5939, speed is controlled with analog voltage in range 250mv to 2.5V.

The A5949 and A5939 are available in a 28L ETSSOP package, suffix “LP”, and a 28Lead QFN, suffix “ET”.



Typical Application

SELECTION GUIDE

Part Number	Ambient Temperature	Package	Packing
A5949GLPTR-T	-40 to 105C		
A5949GETTR-T	-40 to 105C		
A5949KLPTR-T (Note1)	-40 to 125C		
A5939GLPTR-T	-40 to 105C		
A5939GETTR-T	-40 to 105C		
A5939KLPTR-T (Note1)	-40 to 125C		

1. Contact factory for availability

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BB}				50	V
Logic Input Voltage Range (SPD, BRAKE, DIR)	V_{IN}		-.3		6	V
Logic Output – FG, nFAULT	Vo	FG (I<5mA)			6	V
LSS	V_{LSS}		-500		500	mV
		Tw <500ns	-4		4	V
Output Voltage	V_{OUT}	SA,SB,SC	-2		V_{BB}+2	V
ISET			-.3		5.5	V
VCP			V_{BB}-.3		V_{BB}+8	V
CP1			-.3		V_{BB}+.3	V
CP2			V_{BB}-.3		V_{CP}+.3	V
Hall Inputs	V_{HALL}		-.3		6	V
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-55		150	°C
Operating Temperature Range	Ta	"G" version	-40		105	°C
		"K: version	-40		125	°C
Package Thermal Resistance						
LP	Rja	2 sided PCB 1 in^2 Copper		36		°C/W
ES				45		°C/W

TERMINAL LIST

LP	QFN	Pin Name	Pin Description
1	18	VREF	Logic Supply Output
2	19	HA+	Hall Input
3	20	HA-	Hall Input
4	21	HB+	Hall Input
5	22	HB-	Hall Input
6	23	HC+	Hall Input
7	24	HC-	Hall Input
8	25	BRAKE	Logic Input
9	26	DIR	Logic Input
10	27	FG	Speed Output
11	28	nFAULT	Logic Output
12	1	SPD	Speed Input
13	2	ISET	Analog Input
14	3	GND	Ground
15	4	GLA	Gate Drive Output
16	5	GLB	Gate Drive Output
17	6	GLC	Gate Drive Output
18	7	LSS	Low Side Source
19	8	SA	Motor Output
20	9	GHA	Gate Drive Output
21	10	SB	Motor Output
22	11	GHB	Gate Drive Output
23	12	SC	Motor Output
24	13	GHC	Gate Drive Output
25	14	VCP	Charge Pump
26	15	VBB	Power Supply
27	16	CP2	Charge Pump
28	17	CP1	Charge Pump

ELECTRICAL CHARACTERISTICS (unless noted otherwise)
G version: valid for TA = 25°C, V_{BB} = 5.5V to 50V
K version: valid for TA = -40°C to 125°C, V_{BB} = 5.5V to 50V

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
VBB Supply Current	I_{BB}	PWM=LOW, I_{VREF}=0mA		8	10	mA
		Standby Mode		<1	20	µA
VREF	V_{REF}	I_{OUT}=25mA	2.7	2.8	2.9	V
VREF Current Limit	V_{REFOCL}	V_{REF}=0V	80			mA
Charge Pump	V_{CP}	VBB=8V, Relative To V_{BB}	6.5	7	7.5	V
		VBB=5.5V		5		V
I/O						
Input Current	I_{IN}	SPD	-1	<.1	1	µA
		BRAKE, DIR, VIN=5V		50		µA
Logic Input Low Level	V_{IL}				.8	V
Logic Input High Level	V_{IH}		2			V
Logic Input Hysteresis	V_{HYS}		200	300	600	mV
Output Sat Voltage	V_{SAT}	I=5mA, nFAULT, FG			.3	V
Output Leakage	I_{FG}	V=6V, switch OFF			1	µA
Gate Drive						
High Side Gate Drive Output	V_{GH}	VBB=8V	6.5	7		V
Low Side Gate Drive Output	V_{GL}	VBB=8V	6.5	7		V
Gate Drive Source Current	I_{SO}	Relative to target, R_{ISET}=15K to 150K	-20		20	%
Gate Drive Sink Current	I_{SI}	Relative to target, R_{ISET}=15K to 150K	-20		20	%
Dead Time	t_{DT}	unloaded	440	520	600	ns
Motor PWM Frequency	f_{PWM}		23.2	24.4	25.6	Khz

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization

ELECTRICAL CHARACTERISTICS (unless noted otherwise)
G version: valid for TA = 25°C, V_{BB} = 5.5V to 50V
K version: valid for TA = -40°C to 125°C, V_{BB} = 5.5V to 50V

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Hall						
Hall Latch Input Range	V_{HLCM}		0		5.5	V
Hall Element Input Range	V_{HECM}		.2		3.2	V
Hall Element Offset	V_{OFF}	V(Hx+)-V(Hx-)	-5	0	+5	mV
Hysteresis	V_{HYS}	Relative to V_{OFF}	5	13	21	mV
Hall Element Minimum Amplitude	VH		50			mV
SPD Input (PWM mode - A5949)						
PWM Duty On Threshold	DC_{ON}		9.6	10	10.4	%
PWM Duty OFF Threshold	DC_{OFF}		5.6	6	6.4	%
PWM Input Frequency Range	F_{PWM}		.1		100	Khz
SPD Input (Analog mode – A5939)						
SPD On Threshold	VTH_{ON}		210	250	290	mV
SPD Off Threshold	VTH_{OFF}		110	150	190	mV
SPD MAX	VTH_{MAX}			2.5		V
Resolution				4.89		mV
Accuracy				+/- 5LSB		
Protection						
VBB UVLO	VBB_{UVLO}	V_{BB} rising		4.75	4.95	V
VBB UVLO HYS	VBB_{HYS}		200	300	450	mV
VBB Overvoltage Threshold	VBB_{OV}	V_{BB} rising		46.5	47.5	V
VBB Overvoltage Hystersis	VBB_{OVHYS}			2		V
OverCurrent Threshold	V_{OCL}		235	250	265	mV
Lock Timing	t_{OFF}			8		S
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing	150	165	185	°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		20		°C

1. Specified limits are tested at a single temperature and assured over operating temperature range by design and characterization.

Functional Description

The A5949 targets fan applications to meet the objectives of low audible noise, minimal vibration, and high efficiency. Allegro's proprietary control algorithm results in a sinusoidal current waveshape that adapts to a variety of motor characteristics to dynamically optimize efficiency across a wide range of speeds.

The speed of the fan is controlled by variable duty cycle PWM input.

The PWM input duty is measured and converted to a 9bit number. This 9 bit "demand" is applied to a pwm generator block to create the modulation profile. The modulation profile is applied to the three motor outputs, with 120 degree phase relationship, to create the sinusoidal current waveform as shown in Figure 1.

Protection features include lock detection with restart, motor output short circuit, supply undervoltage monitor and thermal shutdown.

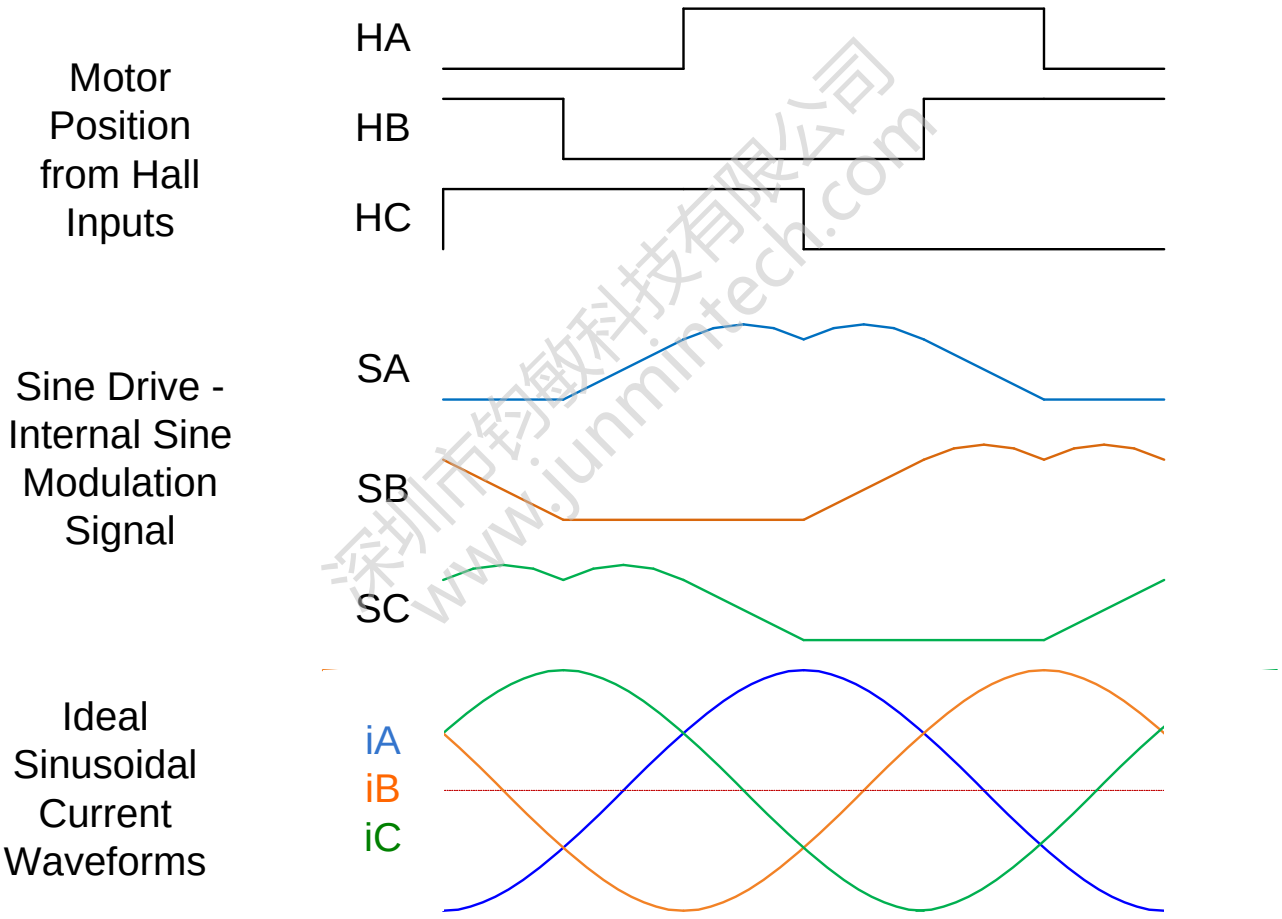
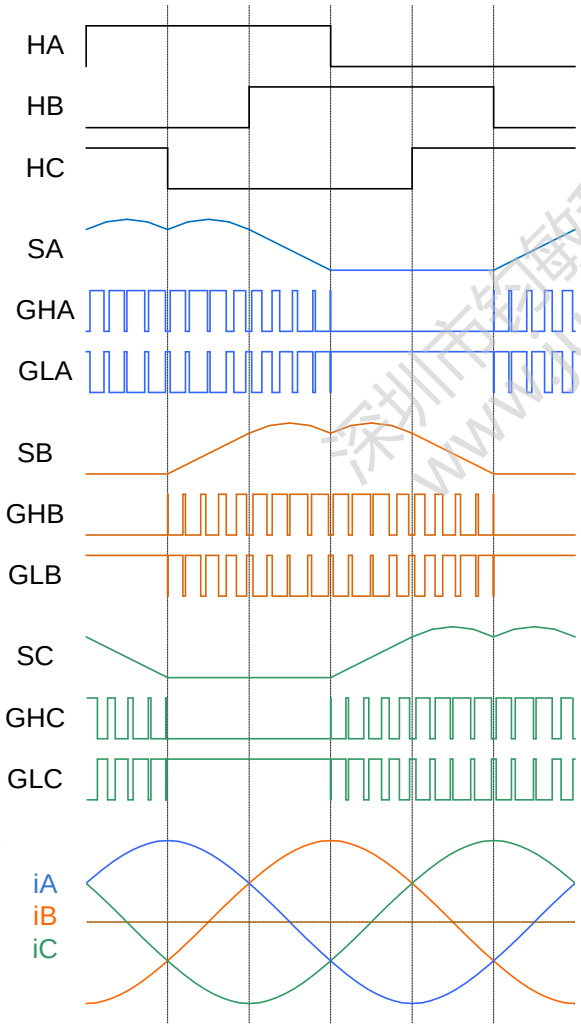


Figure 1: Sinusoidal PWM (DIR=HI)

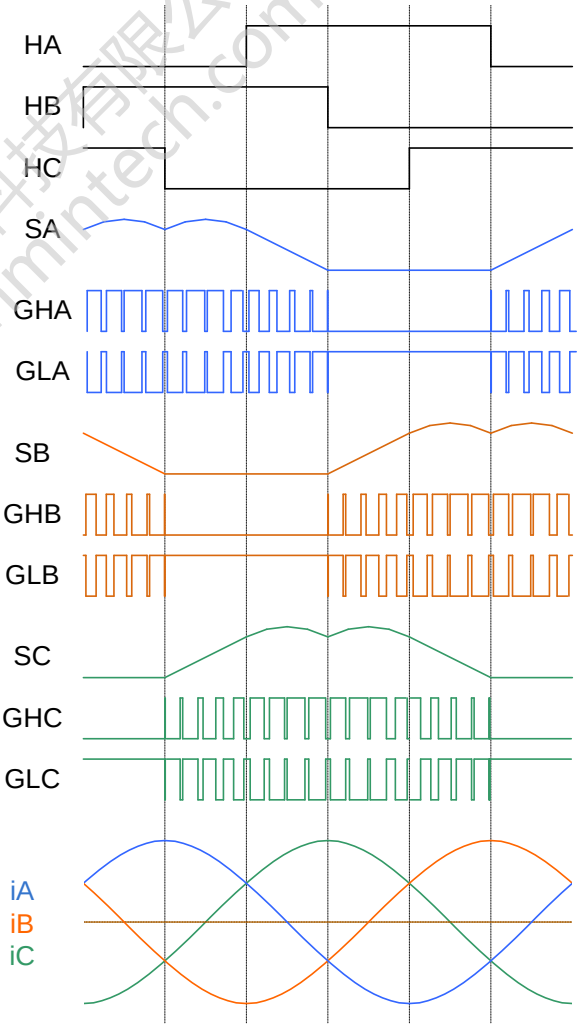
Commutation timing.

HA	HB	HC	DIR	BRK		GHA	GLA	GHB	GLB	GHC	GLC	Mode
H	L	H	H	L		Sine PWM		L	H	Sine	PWM	A→B→C Normal Running
H	L	L	H	L		Sine PWM		Sine PWM		L	H	A→B→C Normal Running
H	H	L	H	L		Sine PWM		Sine PWM		L	H	A→B→C Normal Running
L	H	L	H	L		L	H	Sine PWM		Sine PWM		A→B→C Normal Running
L	H	H	H	L		L	H	Sine PWM		Sine PWM		A→B→C Normal Running
L	L	H	H	L		Sine PWM		L	H	Sine PWM		A→B→C Normal Running
X	X	X	X	H		L	H	L	H	L	H	BRAKE – Low Sides ON
H	H	H	X	X		L	L	L	L	L	L	Fault – All Gate Drive Low
L	L	L	X	X		L	L	L	L	L	L	Fault – All Gate Drive Low
L	H	H	L	L		Sine PWM		Sine PWM		L	H	A→C→B Normal Running
L	H	L	L	L		Sine PWM		L	H	Sine PWM		A→C→B Normal Running
H	H	L	L	L		Sine PWM		L	H	Sine PWM		A→C→B Normal Running
H	L	L	L	L		L	H	Sine PWM		Sine PWM		A→C→B Normal Running
H	L	H	L	L		L	H	Sine PWM		Sine PWM		A→C→B Normal Running
L	L	H	L	L		Sine PWM		Sine PWM		L	H	A→C→B Normal Running

DIR=HI



DIR=LO



Functional Description

VREF. A 2.8V reference output used to power internal digital logic and analog circuitry. V_{REF} can be used to power the Hall elements with up to 25mA bias current if desired. Stabilize with .1uF or greater ceramic capacitor.

FG. Open drain output provides speed information to the system. The system controller can use this information to adjust input command to achieve the desired speed. FG changes state in sync with HA+ hall input, one period per electrical revolution of the motor. The open drain output can be pulled up to V_{REF} or external 3.3 or 5V supply.

BRAKE. Active High signal turns on all low sides for braking function. Brake Function will prevent IC from entering standby mode.

DIR. Logic Input to control motor direction**.** If DIR is changed while motor is running, motor will coast for 8S before braking and then reversing direction.

ISET. A resistor (R_{ISET}) to GND selects the gate current to match the selected MOSFET. The sink and source current ratios are fixed at approximately 2:1. Resistor value R_{ISET} should be in the range 15K to 150K.

The formula for gate drive current is as follows:

I_{GATE_SRC}(mA) = 1.9 + 900/R_{ISET} (Kohms)
I_{GATE_SNK}(mA) = 3.5 + 1700/R_{ISET} (Kohms)

Choice of the gate drive current level and Mosfet pair should consider the fixed 520ns deadtime to prevent a shoothru condition.

External series resistors for Gate lines are not required.

Lock Detect. A logic circuit monitors the hall position sensor outputs to determine if motor is running as expected. If a fault is detected, the motor drive will be disabled for 8S before an auto-restart is attempted. The retry duration is 2S.

The lock detect circuit will be triggered by any of the following:

a) Time between hall transitions more than 84ms. This value is below expected minimum running speed for fan motors.
b) Invalid Hall Code: HA/HB/HC = 000 or 111.

Standby Mode. A low power mode is activated if SPD pin is held low. Standby Mode will turn off all circuitry including charge pump and VREF. Upon power up, A5949 will immediately wake up. If SPD remains low for 8S, standby mode will then be activated.

nFAULT. The following signals will bring output nFAULT low:

1) VBB Undervoltage
2) Thermal Shutdown
3) Charge Pump UVLO
4) VBB Overvoltage
5) Output Vds Fault (OCP)
6) Invalid Hall Code

Phase Advance. A5949 adaptively calculates the proper phase advance across the speed range to allow motor to run at maximum efficiency.

Current Limit. The A5949 signals an overcurrent condition when the voltage sensed at LSS terminal exceeds 250mV. When the overcurrent is indicated the demand to the PWM logic is slowly reduced (.4%/ms) unitl the overcurrent signal no longer occurs. The demand will then increase at the same rate until another overcurrent event is registered. In this manner, the motor will be maintained at an operating speed close to the I_{LIMIT} level.

$$I_{LIMIT} = 250mv/R_{SENSE}$$

SPD. Speed Demand input pin. Choice of analog voltage control or PWM duty control is determined by part number selection

A5939: Analog control. Voltage applied will increase speed demand. An internal 9 bit A/D converter will translate the input to a speed demand. Resolution of the A/D is 4.89mV.

A5949: Duty cycle control. The PWM frequency must be in the range 100Hz to100kHz. Duty cycle resolution is 9Bit.

Speed Control.

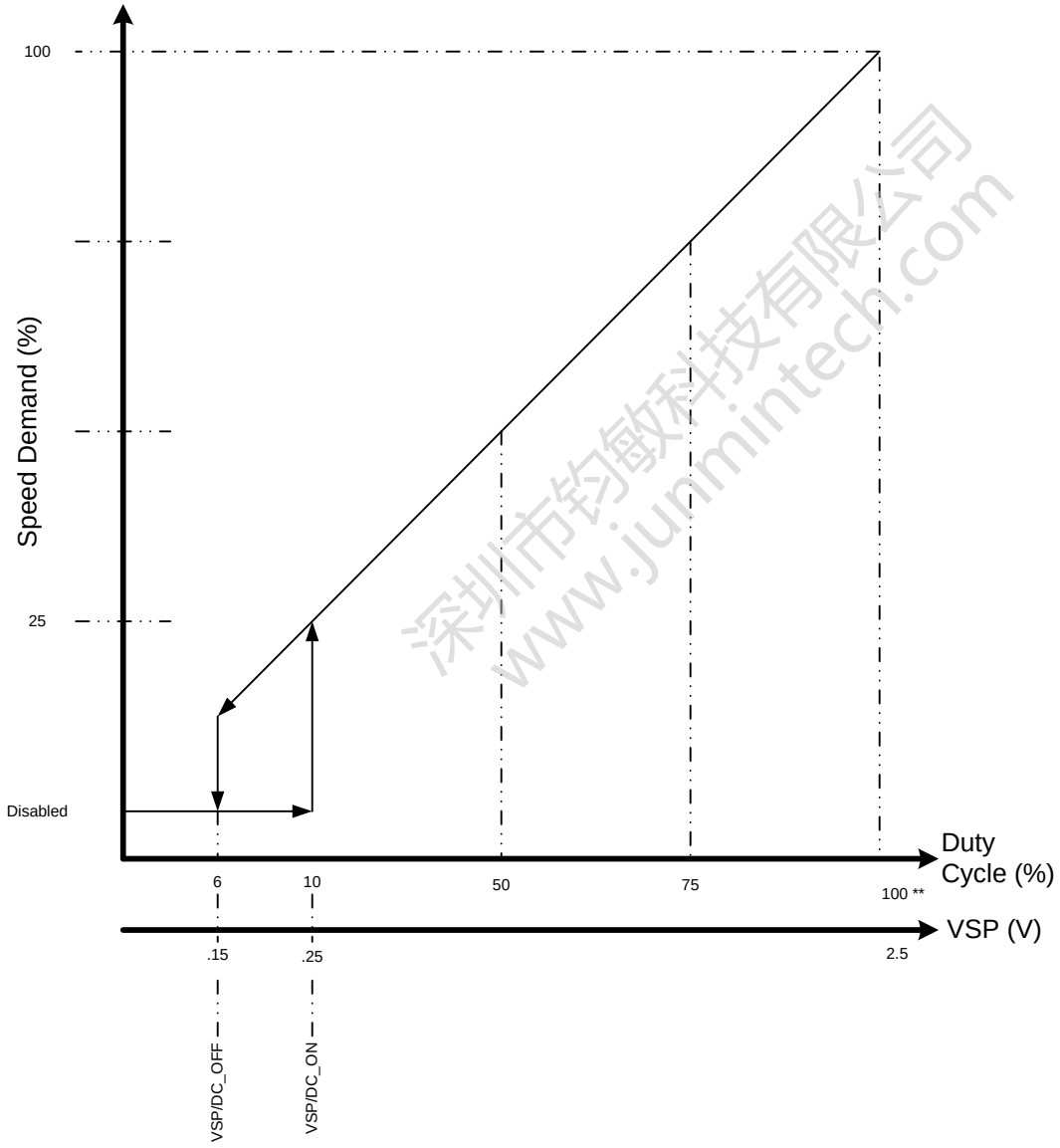
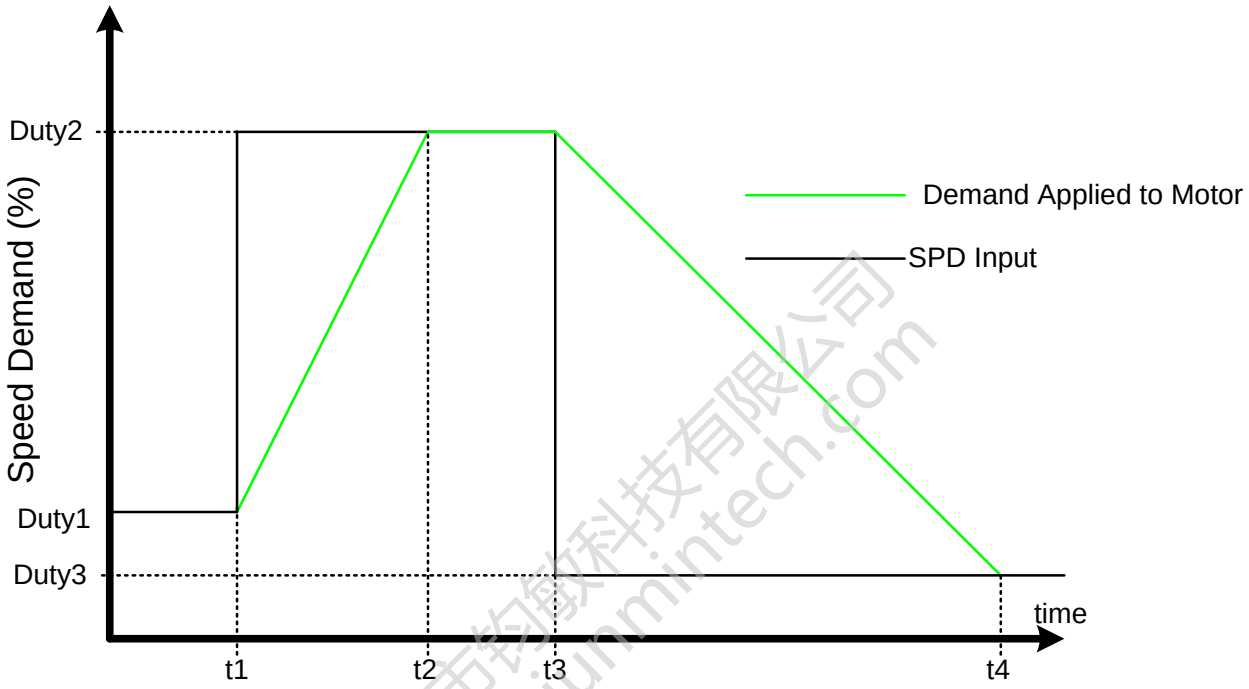


Figure 1) Speed Input Characteristic

Demand Ramp. When the SPD signal (duty or analog Voltage) is changed, an internal circuit ramps from the initial value to final value. This feature will reduce stress on power supply during acceleration, will result in a quieter, gradual speed change for the fan, and will reduce power supply “pump up” which can occur during motor deceleration.



The rate of change is 4ms/bit for acceleration and 8ms/bit for deceleration. The time for duty ramp is calculated as below:

t_{ACCEL} (t1→t2) = (511*(duty2-duty1))*4ms
t_{DECEL} (t3→t4) = (511*(duty2-duty3))*8ms

Application Information:

Typical Application Circuit

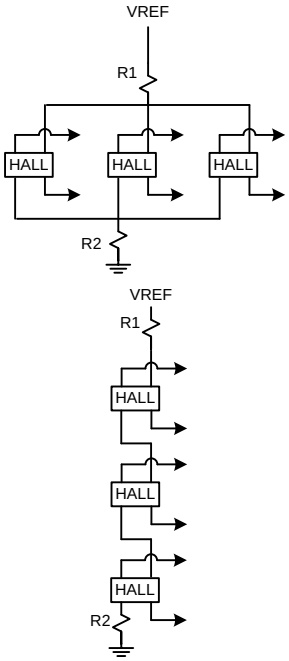
Name	Suggested Value	Comment
CVREF	.1uF/X5R/10V	Ceramic capacitor required
CVBB	47uF -470uF	Power Supply Stabilization – Electrolytic or ceramic OK.
R_{FG}	20K	Optional - pull up resistor for speed feedback
D1	tbd	May be Required to isolate motor from system or for reverse polarity protection
ZD1	tbd	Optional TVS to limit max VBB due to transients due to motor generation or power line. Suggested to clamp below 48V (EX : Fairchild SMBJxxA). Typically required if blocking diode D1 used.
R_{SPD}	1K	Optional – If PWM wired to connector – R_{PWM} will isolate IC pin from noise or overvoltage transients.
C1		
C1		
Rhall		

Layout Notes.

1) Add thermal vias to exposed pad area. Add ground plane on top and bottom of PCB.
2) Place CVREF & CVBB as close as possible to IC.

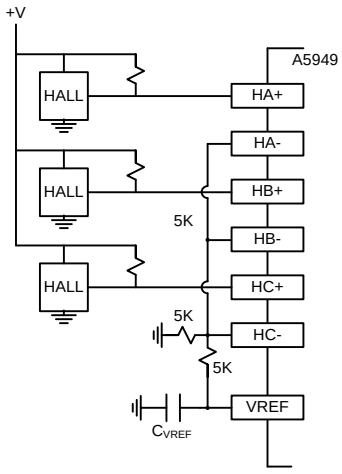
Hall Connection Options

A) Hall Elements

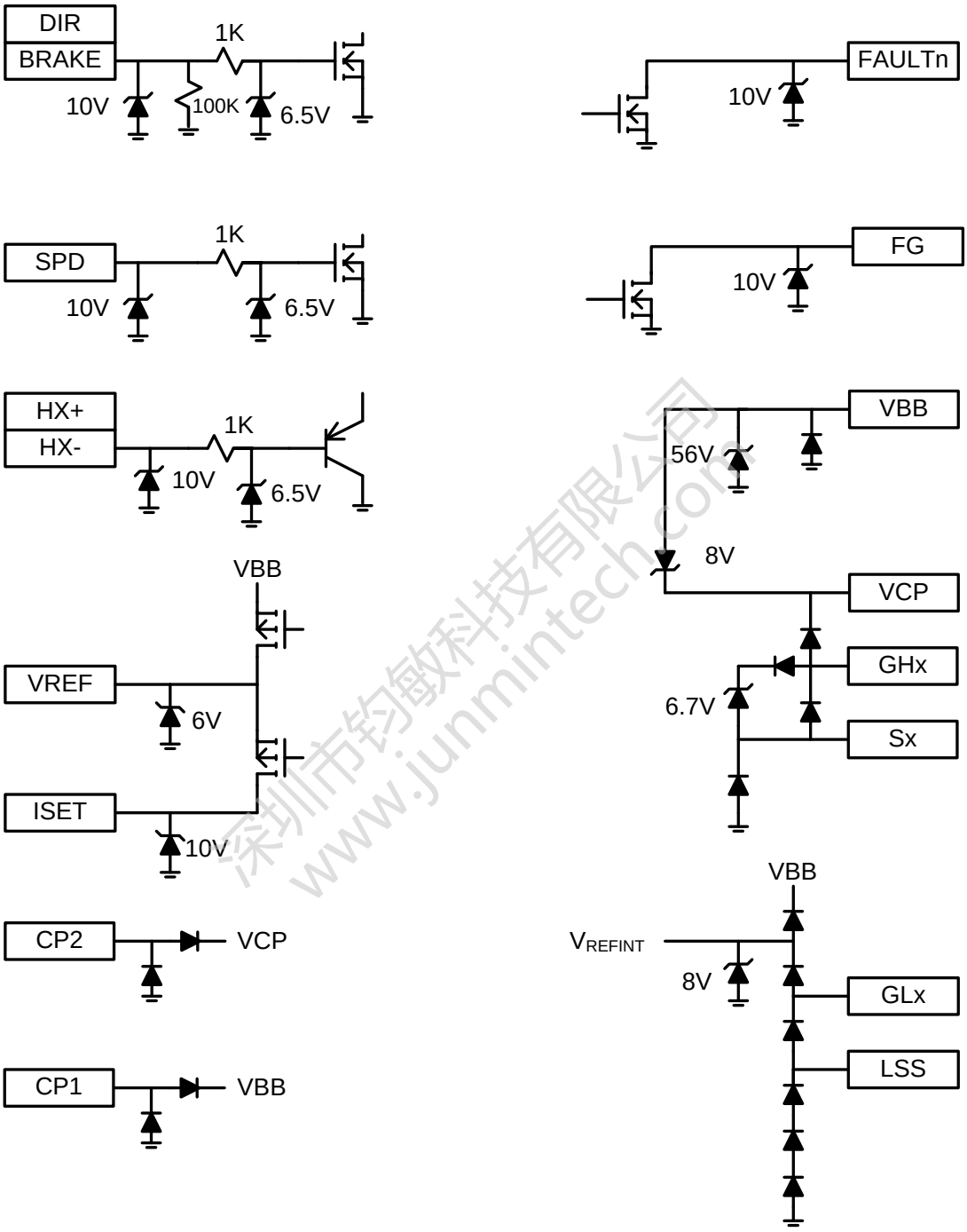


Notes:
1) R2 can be 0ohm if Hall signals > dc level of 200mV
2) Recommended to have Hall bias current >2mA

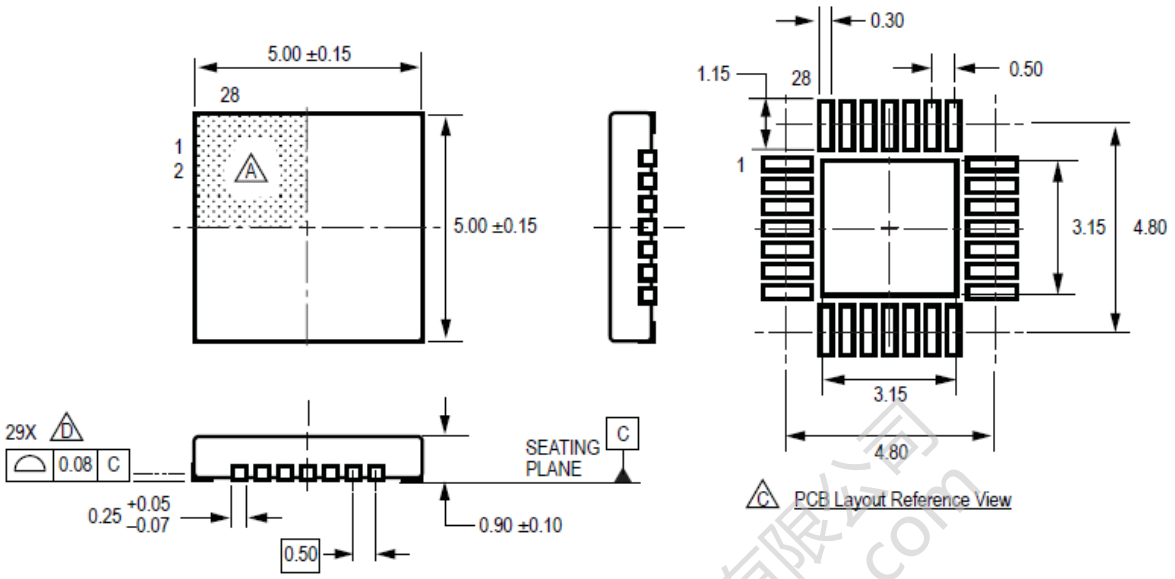
B) Hall Latch

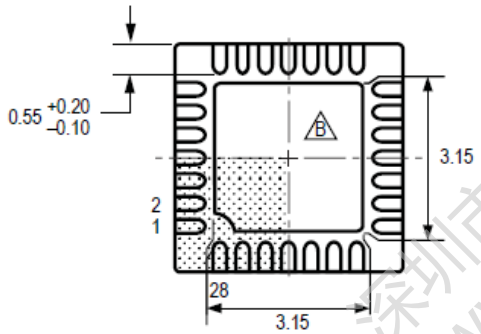


Pin Diagrams



Package ET, 28 pin eQFN





For Reference Only
(reference JEDEC MO-220VHHD-1)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

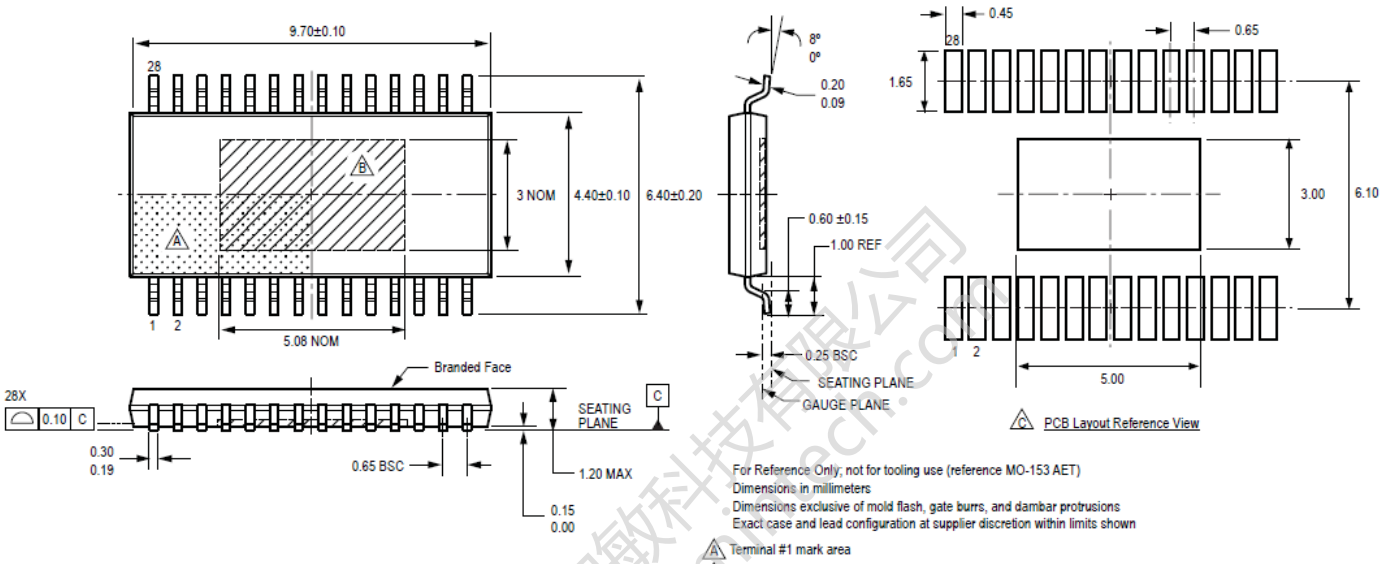
B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P500X500X100-29V1M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Package LP, 28 pin TSSOP

LP Package, 28-Pin TSSOP
with exposed thermal pad



For Reference Only; not for tooling use (reference MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)