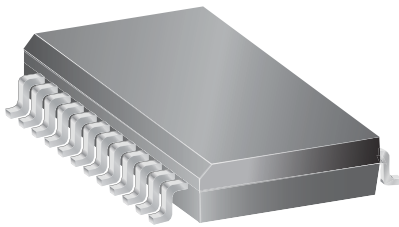# 8-Bit Serial Input Constant-Current Latched LED Driver

Features and Benefits

- Up to 150 mA constant-current outputs
- Undervoltage lockout
- Low-power CMOS logic and latches
- High data input rate
- Similar to Toshiba® TD62715FN
- High/low output current function
- Digital dimming control

## Package: 20-pin SOICW (suffix LW)

Not to scale

Description

The A6277 is specifically designed for LED display applications. Each BiCMOS device includes an 8-bit CMOS shift register, accompanying data latches, and eight NPN constant-current sink drivers.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, typical serial data-input rates are up to 20 MHz. The LED drive current is determined by the user selection of a single resistor. A CMOS serial data output permits cascade connections in applications requiring additional drive lines. For inter-digit blanking, all output drivers can be disabled with an ENABLE input high. In addition, a HIGH/LOW function enables full selected current with the application of a logic low, or 50% selected current with the application of a logic high.

The surface-mount wide SOIC (LW) is lead (Pb) free, with 100% matte-tin leadframe plating.

Functional Block Diagram

Dwg. FP-013-7
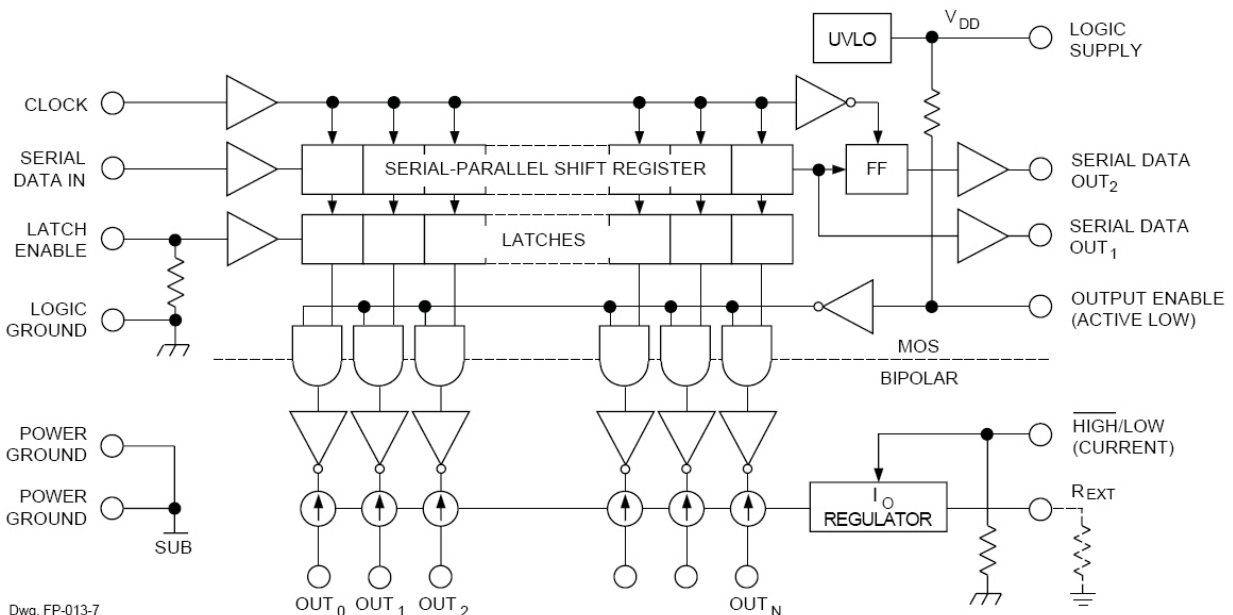
Selection Guide

Part Number	Packing	Package
A6277ELWTR-T	20-pin SOICW	1000 per reel

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		7.0	V
Output Voltage Range	V_O		−0.5 to 24	V
Input Voltage Voltage	V_I		−0.4 to V_{DD} + 0.4	V
Output Current	I_O		150	mA
Operating Ambient Temperature	T_A	Range E	−40 to 85	ºC
Maximum Junction Temperature	T_J(max)		150	ºC
Storage Temperature	T_{stg}		−55 to 150	ºC

* Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

Thermal Characteristics may require derating at maximum conditions, see application information

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Mounted on 1-layer PCB	90	ºC/W

*Additional thermal information available on the Allegro website.

SUFFIX 'LW', $R_{\theta JA}$ = 90°C/W

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2
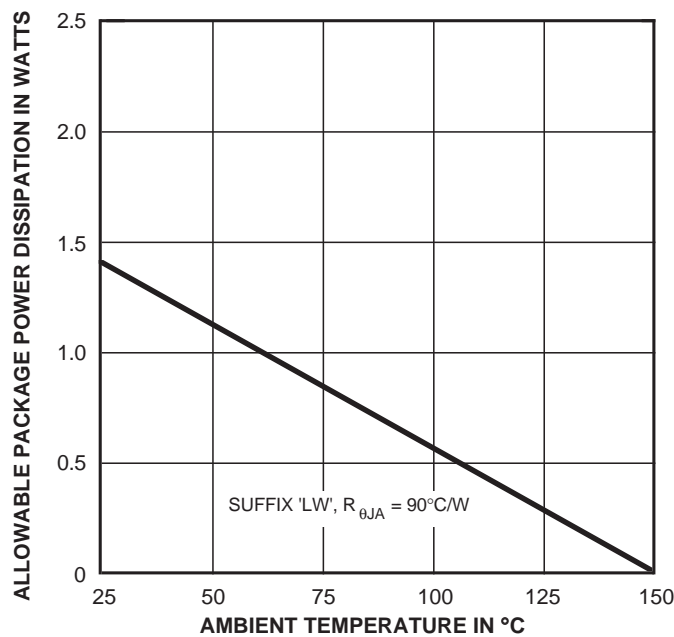
ELECTRICAL CHARACTERISTICS at T_A = +25°C, $V_{H/L}$ = V_{DD} = 5 V (unless otherwise noted).

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
			Limits			
Supply Voltage Range	V_{DD}	Operating	4.5	5.0	5.5	V
Under-Voltage Lockout	$V_{DD(UV)}$	V_{DD} = 0 to 5 V	3.4	–	4.0	V
Output Current (any single output)	I_O	V_{CE} = 1.0 V, R_{EXT} = 160 Ω	100	120	140	mA
		V_{CE} = 0.4 V, R_{EXT} = 470 Ω	34	42	48	mA
Output Current Matching (difference between any two outputs at same V_{CE})	ΔI_O	0.4 V ≤ $V_{CE(A)}$ = $V_{CE(B)}$ ≤ 1.0 V: R_{EXT} = 160 Ω	–	±1.5	±6.0	%
		R_{EXT} = 470 Ω	–	±1.5	±6.0	%
Output Leakage Current	I_{CEX}	V_{OH} = 20 V	–	1.0	5.0	µA
Logic Input Voltage	V_{IH}		$0.7V_{DD}$	–	–	V
	V_{IL}		–	–	$0.3V_{DD}$	V
SERIAL DATA OUT Voltage (SDO$_1$ & SDO$_2$)	V_{OL}	I_{OL} = 1.0 mA	–	–	0.4	V
	V_{OH}	I_{OH} = -1.0 mA	4.6	–	–	V
Input Resistance	R_I	ENABLE input, pull up	150	300	600	kΩ
		LATCH & $\overline{HIGH}$/LOW inputs, pull down	100	270	400	kΩ
Supply Current	$I_{DD(OFF)}$	R_{EXT} = open, V_{OE} = 5 V	–	0.8	1.6	mA
		R_{EXT} = 470 Ω, V_{OE} = 5 V	3.5	6.5	9.5	mA
		R_{EXT} = 160 Ω, V_{OE} = 5 V	14	17	22	mA
	$I_{DD(ON)}$	R_{EXT} = 470 Ω, V_{OE} = 0 V	5.0	10	15	mA
		R_{EXT} = 160 Ω, V_{OE} = 0 V	20	27	40	mA

Typical Data is at V_{DD} = 5 V and is for design information only.

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3

SWITCHING CHARACTERISTICS at T_A = 25°C, V_{DD} = V_{IH} = 5 V, V_{CE} = 0.4 V, V_{IL} = 0 V, R_{EXT} = 470 Ω, I_O = 40 mA, V_L = 3 V, R_L = 65 Ω, C_L = 10.5 pF.

Characteristic	Symbol	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Propagation Delay Time	t_{pHL}	CLOCK-OUT$_n$	–	350	1000	ns
		LATCH-OUT$_n$	–	350	1000	ns
		ENABLE-OUT$_n$	–	350	1000	ns
		CLOCK-SERIAL DATA OUT$_1$	–	40	–	ns
Propagation Delay Time	t_{pLH}	CLOCK-OUT$_n$	–	300	1000	ns
		LATCH-OUT$_n$	–	400	1000	ns
		ENABLE-OUT$_n$	–	380	1000	ns
		CLOCK-SERIAL DATA OUT$_2$	–	40	–	ns
Output Fall Time	t_f	90% to 10% voltage	150	250	1000	ns
Output Rise Time	t_r	10% to 90% voltage	150	250	600	ns

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Output Voltage	V_O		–	1.0	4.0	V
Output Current	I_O	Continuous, any one output	–	–	150	mA
	I_{OH}	SERIAL DATA OUT	–	–	-1.0	mA
	I_{OL}	SERIAL DATA OUT	–	–	1.0	mA
Logic Input Voltage	V_{IH}		0.7V_{DD}	–	–	V
	V_{IL}		–	–	0.3V_{DD}	V
Clock Frequency	f_{CK}	Cascade operation	–	–	10	MHz

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4

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)
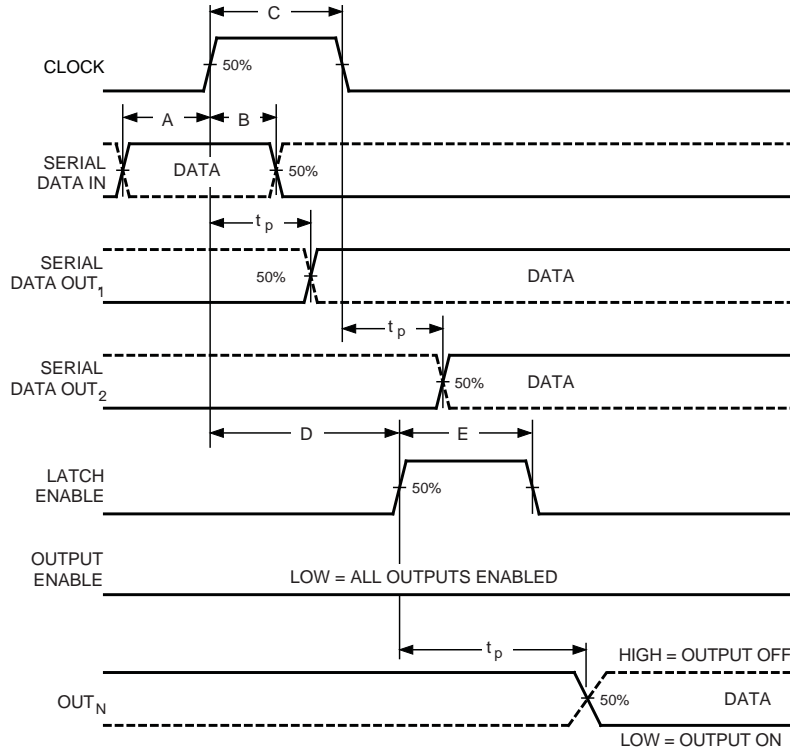
Dwg. WP-029-3
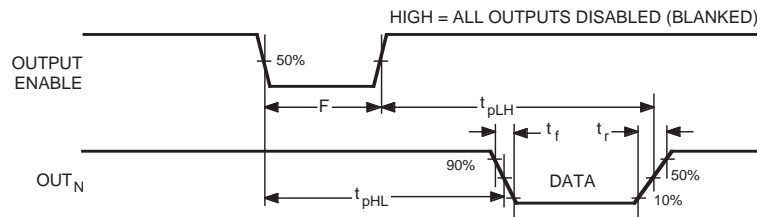
Dwg. WP-030-1A

A. Data Active Time Before Clock Pulse
(Data Set-Up Time), $t_{su(D)}$ .... **60 ns**

B. Data Active Time After Clock Pulse
(Data Hold Time), $t_{h(D)}$ .... **20 ns**

C. Clock Pulse Width, $t_{w(CK)}$ .... **50 ns**

D. Time Between Clock Activation
and Latch Enable, $t_{su(L)}$ .... **100 ns**

E. Latch Enable Pulse Width, $t_{w(L)}$ .... **100 ns**

F. Output Enable Pulse Width, $t_{w(OE)}$ .... **4.5 μs**

NOTE – Timing is representative of a 10 MHz clock.
Significantly higher speeds are attainable.

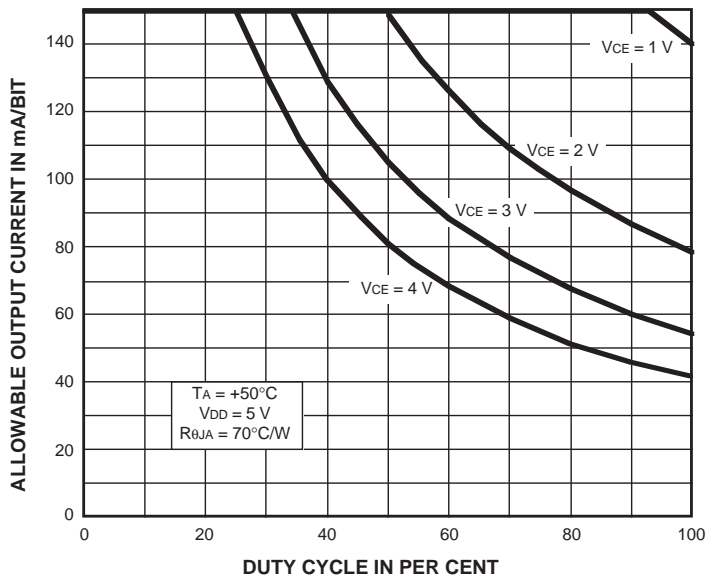— Max. Clock Transition Time, t_r or t_f .... **10 μs**

Information present at any register is transferred to the respective latch when the LATCH ENABLE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the LATCH ENABLE is held high. Applications where the latches are bypassed (LATCH ENABLE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

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5

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE
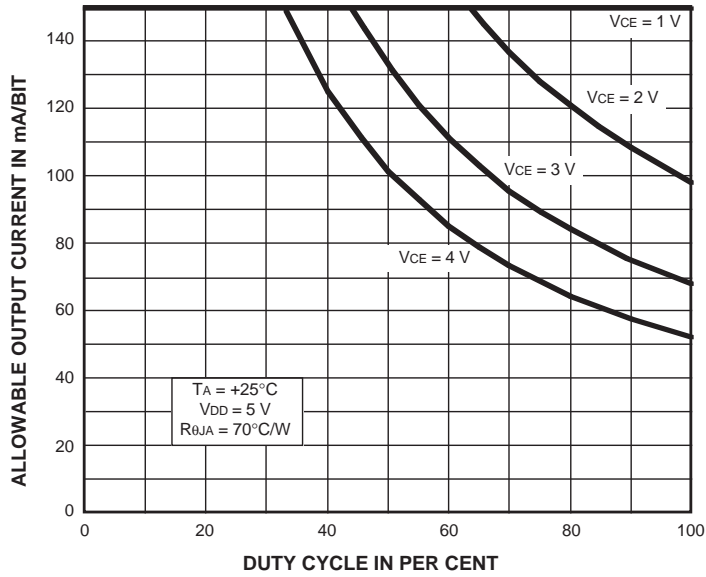
Dwg. GP-062-16

Dwg. GP-062-14
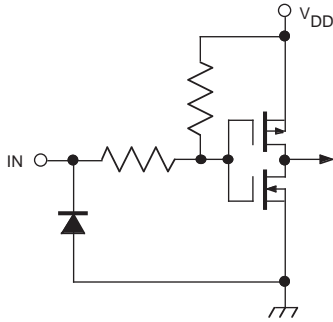
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

Graph: ALLOWABLE OUTPUT CURRENT IN mA/BIT (y-axis, 0 to 140) vs DUTY CYCLE IN PER CENT (x-axis, 0 to 100). Curves labeled $V_{CE} = 0.7$ V, $V_{CE} = 1$ V, $V_{CE} = 2$ V, $V_{CE} = 3$ V, $V_{CE} = 4$ V. Conditions: $T_A = +85°C$, $V_{DD} = 5$ V, $R_{\theta JA} = 70°C/W$.
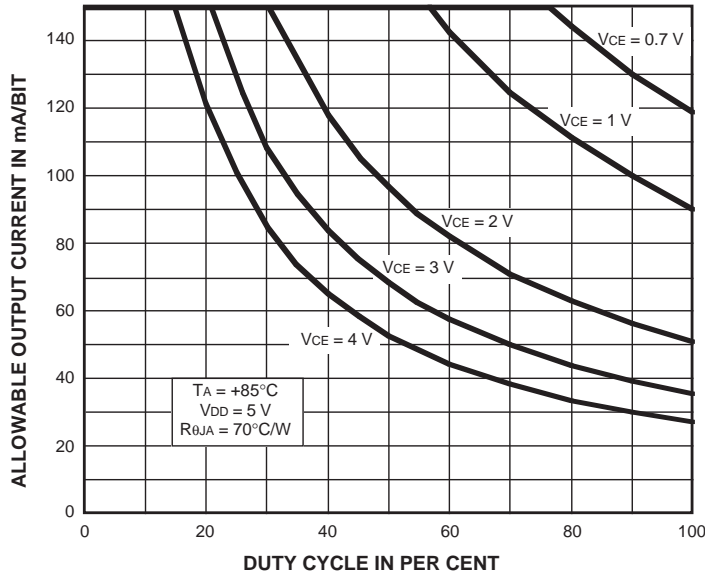
Dwg. GP-062-12

TYPICAL CHARACTERISTICS

Graph: OUTPUT CURRENT IN mA/BIT (y-axis, 0 to 60) vs V_{CE} IN VOLTS (x-axis, 0 to 2.0). Conditions: $T_A = +25°C$, $R_{EXT} = 470 \ \Omega$.
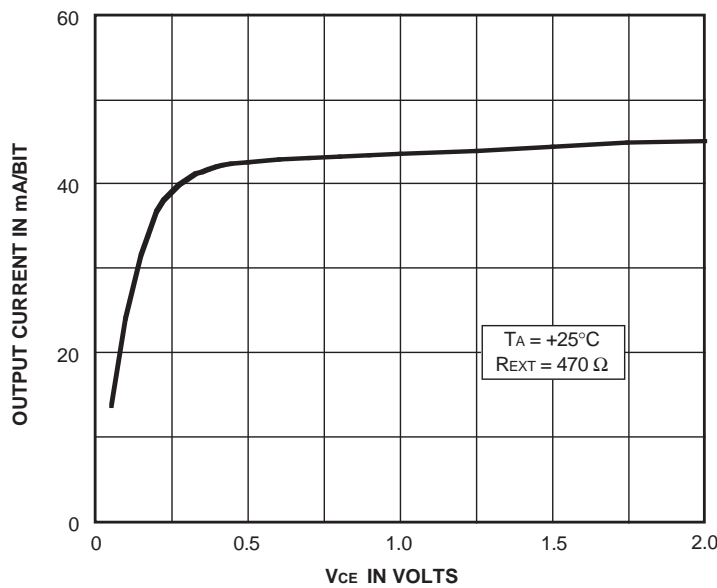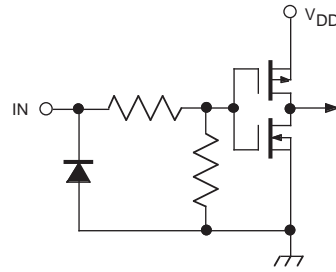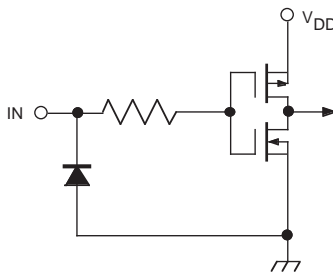
Dwg. GP-063-1

Dwg. EP-010-11

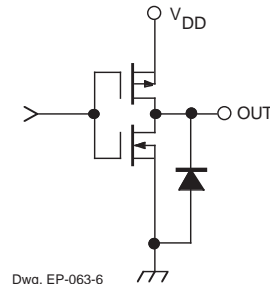OUTPUT ENABLE (active low)

Dwg. EP-010-12

LATCH ENABLE and $\overline{\text{HIGH}}$/LOW

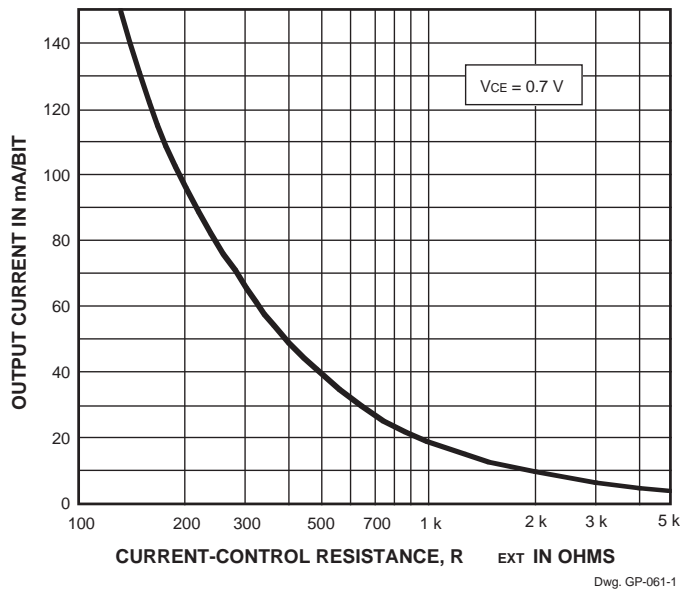Dwg. EP-010-13

CLOCK and SERIAL DATA IN

Dwg. EP-063-6

SERIAL DATA OUT

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents						Serial Data Output	Latch Enable Input	Latch Contents						Output Enable Input	Output Contents					
		I_1	I_2	I_3	...	I_{N-1}	I_N			I_1	I_2	I_3	...	I_{N-1}	I_N		I_1	I_2	I_3	...	I_{N-1}	I_N
H	⌐_	H	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
L	⌐_	L	R_1	R_2	...	R_{N-2}	R_{N-1}	R_{N-1}														
X	‾⌐	R_1	R_2	R_3	...	R_{N-1}	R_N	R_N														
		X	X	X	...	X	X	X	L	R_1	R_2	R_3	...	R_{N-1}	R_N							
		P_1	P_2	P_3	...	P_{N-1}	P_N	P_N	H	P_1	P_2	P_3	...	P_{N-1}	P_N	L	P_1	P_2	P_3	...	P_{N-1}	P_N
										X	X	X	...	X	X	H	H	H	H	...	H	H

L = Low Logic (Voltage) Level   H = High Logic (Voltage) Level   X = Irrelevant   P = Present State   R = Previous State

Applications Information

The load current per bit (I_O) is set by the external resistor (R_{EXT}) as shown in the figure below.

V_{CE} = 0.7 V

OUTPUT CURRENT IN mA/BIT

CURRENT-CONTROL RESISTANCE, R $_{EXT}$ IN OHMS

Dwg. GP-061-1

Package Power Dissipation (P_D). The maximum allowable package power dissipation is determined as
$$P_D(max) = (150 - T_A)/R_{\theta JA}.$$
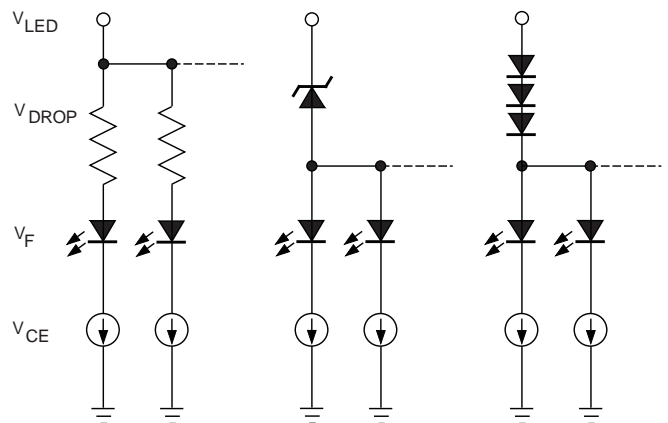The actual package power dissipation is
$$P_D(act) = dc(V_{CE} \bullet I_O \bullet 8) + (V_{DD} \bullet I_{DD}).$$

When the load supply voltage is greater than 3 V to 5 V, considering the package power dissipating limits of these devices, or if $P_D(act) > P_D(max)$, an external voltage reducer (V_{DROP}) should be used.

Load Supply Voltage (V_{LED}). These devices are designed to operate with driver voltage drops (V_{CE}) of 0.4 V to 0.7 V with LED forward voltages (V_F) of 1.2 V to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will be increased significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage or to set any series dropping voltage (V_{DROP}) as
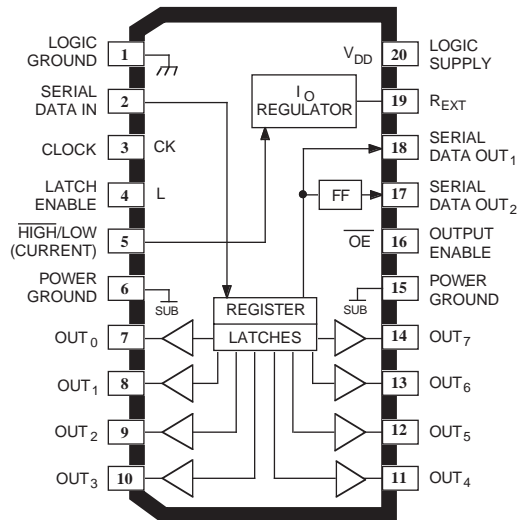$$V_{DROP} = V_{LED} - V_F - V_{CE}$$
with $V_{DROP} = I_o \bullet R_{DROP}$ for a single driver, or a Zener diode (V_Z), or a series string of diodes (approximately
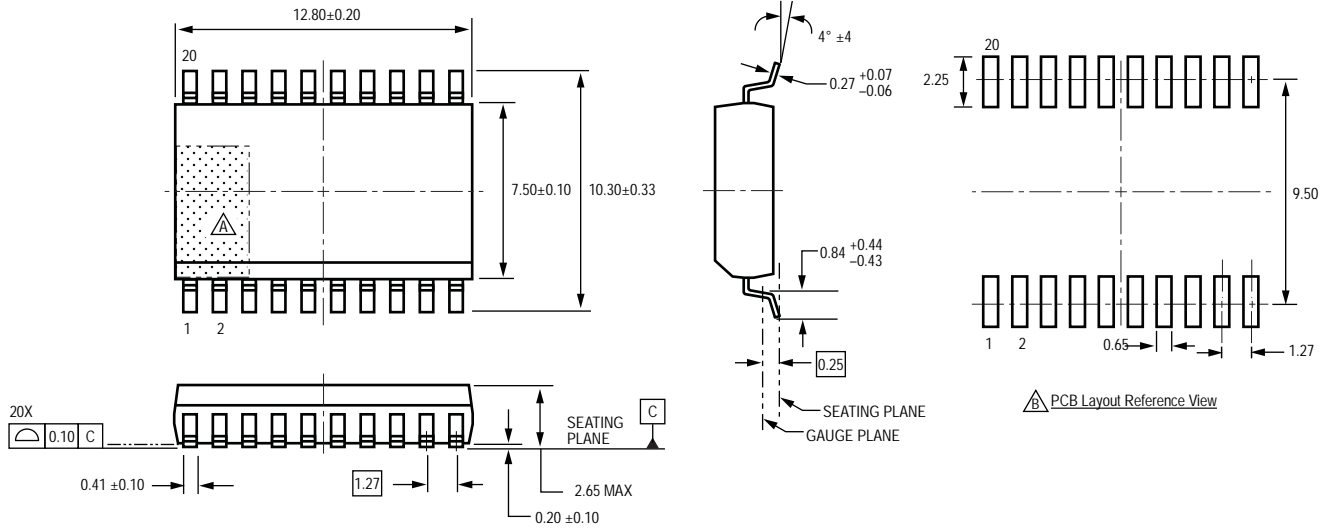
0.7 V per diode) for a group of drivers. If the available voltage source will cause unacceptable dissipation and series resistors or diode(s) are undesirable, a regulator such as the Sanken Series SAI or Series SI can be used to provide supply voltages as low as 3.3 V.

For reference, typical LED forward voltages are:

White	3.5 – 4.0 V
Blue	3.0 – 4.0 V
Green	1.8 – 2.2 V
Yellow	2.0 – 2.1 V
Amber	1.9 – 2.65 V
Red	1.6 – 2.25 V
Infrared	1.2 – 1.5 V

Pattern Layout. This device has separate logic-ground and power-ground terminals. If ground pattern layout contains large common-mode resistance, and the voltage between the system ground and the LATCH ENABLE or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not operate correctly.

V_{LED}

V_{DROP}

V_F

V_{CE}

Dwg. EP-064

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9

Pin-out Diagram

TERMINAL DESCRIPTION

Terminal No.	Terminal Name	Function
1	LOGIC GROUND	Reference terminal for control logic.
2	SERIAL DATA IN	Serial-data input to the shift-register.
3	CLOCK	Clock input terminal for data shift on rising edge.
4	LATCH ENABLE	Data strobe input terminal; serial data is latched with high-level input.
5	HIGH/LOW (CURRENT)	Logic low for 100% of programmed current level; logic high for 50% of programmed current level.
6	POWER GROUND	Ground.
7-14	OUT_{0-7}	The eight current-sinking output terminals.
15	POWER GROUND	Ground.
16	OUTPUT ENABLE	When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
17	SERIAL OUT$_2$	CMOS serial-data output (on clock falling edge).
18	SERIAL OUT$_1$	CMOS serial-data output (on clock rising edge) to the following shift-registers.
19	R_{EXT}	An external resistor at this terminal establishes the output current for all sink drivers.
20	LOGIC SUPPLY	(V_{DD}) The logic supply voltage. Typically 5 V.

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10

Package LW, 20-pin SOICW

12.80±0.20

20

7.50±0.10 10.30±0.33

1 2

20X

⬡ 0.10 C

0.41 ±0.10

1.27

SEATING
PLANE

C

2.65 MAX

0.20 ±0.10

For Reference Only
Dimensions in millimeters
(Reference JEDEC MS-013 AC)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

4° ±4

0.27 +0.07 −0.06

0.84 +0.44 −0.43

0.25

SEATING PLANE
GAUGE PLANE

2.25

20

9.50

1 2

0.65

1.27

Ⓑ PCB Layout Reference View

Ⓐ Terminal #1 mark area

Ⓑ Reference pad layout (reference IPC SOIC127P1030X265-20M)
   All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary
   to meet application process requirements and PCB layout tolerances

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11