

**A64E06161****Preliminary****1M X 16 Bit Low Voltage Super RAM****Document Title****1M X 16 Bit Low Voltage Super RAM****Revision History**

| <u>Rev. No.</u> | <u>History</u> | <u>Issue Date</u> | <u>Remark</u> |
|------------------------|--|--------------------------|----------------------|
| 0.0 | Initial issue | October 12, 2003 | Preliminary |
| 0.1 | Change VCC range and VCCQ range Change page access time from 20ns to 25ns Change operation current (I _{cc1}) from 25mA to 15mA(-70) Change operation current (I _{cc1}) from 20mA to 12mA(-85) Change standby current (I _{sb1}) from 80uA to 100uA Delete reduce memory size 16M, partial array refresh 16M Change operation current (I _{cc2}) form 5mA to 3mA(-70, -85) Change PAR current 12Mb=90uA, 8Mb=80uA, 4Mb=70uA Change TCR current +85°C=100uA +70°C=90uA Change TCR current +45°C=85uA +15°C=75uA | November 30, 2004 | |



Preliminary

1M X 16 Bit Low Voltage Super RAM

Features

- Operating voltage:
VCC: 1.7V to 1.95V
VCCQ: 1.7V to VCC
- Access times: $t_{AA} = 70\text{ns}$ (max.)
- Page Access times: $t_{PAA} = 25\text{ns}$ (max)
- Current:
A64E06161 series:
Operating Current (I_{CC1}) : 15mA (max.)
Standby Current (I_{SB1}) : 100uA (max)
Deep Power Down Standby Current (I_{ZZ}) : 10uA (max.)
- 4-word page length
- Support 4 distinct operation modes for reducing standby power :
Deep Power Down (DPD) mode
Reduce Memory Size (RMS) mode (4M, 8M, 12M)
Partial Array Refresh (PAR) mode (4M,8M,12M)
Temperature Compensated Refresh (TCR) mode
- Industrial operating temperature range: -25°C to $+85^{\circ}\text{C}$ for - I
- Available in 48-ball Mini BGA (6X8) package.

General Description

The A64E06161 is a low operating current 16,777,216-bit super RAM organized as 1,048,576 word by 16bit and operated on low power supply voltage from 1.7V to 1.95V. It is built using AMIC's high performance CMOS DRAM process.

Using hidden refresh technique, the A64E06161 provides a compatible asynchronous interface and data can be read in 4-word page mode for fast access times. The A64E06161 has an internal register named the Configuration Register

(CR) that controls the operation. The A64E06161 is designed for reducing current consumption during hidden self refresh and operating through following mode: Deep Power Down (DPD) mode, Reduce Memory Size (RMS) mode, Partial Array Refresh (PAR) mode and Temperature Compensated refresh (TCR) mode.

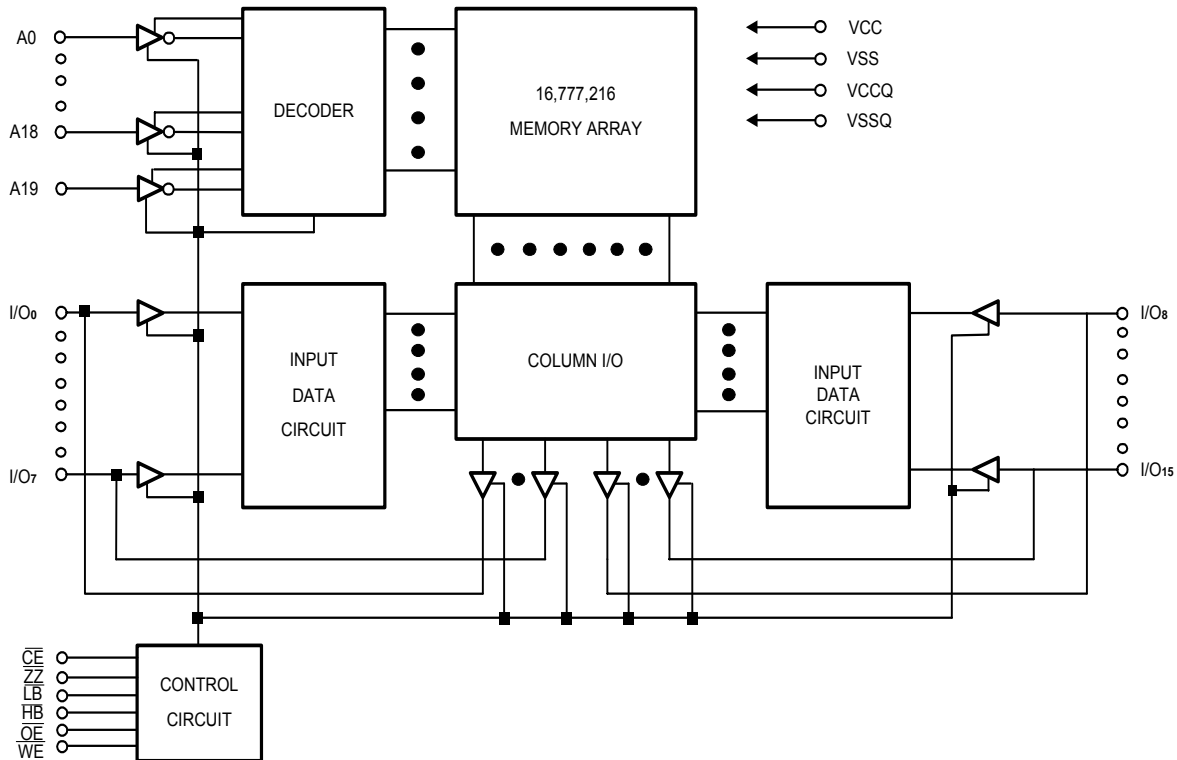
This A64E06161 is suited for low power application such as mobile phone and PDA or other battery-operated handheld device.

Pin Configuration

■ Mini BGA (6X8) Top View

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|------------------------|------------------------|-----|-----|------------------------|------------------------|
| A | $\overline{\text{LB}}$ | $\overline{\text{OE}}$ | A0 | A1 | A2 | $\overline{\text{ZZ}}$ |
| B | I/O ₈ | $\overline{\text{HB}}$ | A3 | A4 | $\overline{\text{CE}}$ | I/O ₀ |
| C | I/O ₉ | I/O ₁₀ | A5 | A6 | I/O ₁ | I/O ₂ |
| D | VSSQ | I/O ₁₁ | A17 | A7 | I/O ₃ | VCC |
| E | VCCQ | I/O ₁₂ | NC | A16 | I/O ₄ | VSS |
| F | I/O ₁₄ | I/O ₁₃ | A14 | A15 | I/O ₅ | I/O ₆ |
| G | I/O ₁₅ | A19 | A12 | A13 | $\overline{\text{WE}}$ | I/O ₇ |
| H | A18 | A8 | A9 | A10 | A11 | NC |

A64E06161G

Block Diagram

Pin Description

| Symbol | Description |
|--------------------------------------|---|
| A0 - A19 | Address Inputs |
| $\overline{\text{CE}}$ | Chip Enable Input |
| $\overline{\text{ZZ}}$ | Sleep Enable Input (When $\overline{\text{ZZ}}$ is low, the CR register can be loaded or the device can enter DPD mode or PAR mode). |
| I/O ₀ - I/O ₁₅ | Data Input/Outputs |
| $\overline{\text{WE}}$ | Write Enable Input |
| $\overline{\text{LB}}$ | Byte Enable Input (I/O ₀ to I/O ₇) |
| $\overline{\text{HB}}$ | Byte Enable Input (I/O ₈ to I/O ₁₅) |
| $\overline{\text{OE}}$ | Output Enable Input |
| VCC | Power |
| VSS | Ground |
| VCCQ | Provide isolated power to I/O for improved noise immunity |
| VSSQ | Provide isolated / Ground to I/O for improved noise immunity |
| NC | No Connection or VSSQ |

Recommended DC Operating Conditions ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -25°C to 85°C)

| Symbol | Parameter | Min. | Max. | Unit |
|-----------------|-------------------------|------|------------|------|
| VCC | Supply Voltage | 1.7 | 1.95 | V |
| VSS | Ground | 0 | 0 | V |
| VCCQ | Supply Voltage I/O only | 1.7 | VCC | V |
| VSSQ | Ground I/O only | 0 | 0 | V |
| V _{IH} | Input High Voltage | 1.4 | VCCQ + 0.2 | V |
| V _{IL} | Input Low Voltage | -0.2 | +0.4 | V |
| C _L | Output Load | - | 30 | pF |

Absolute Maximum Ratings*

VCC to VSS -0.3V to VCC+0.3V
 VCCQ to VSSQ -0.3V to VCCQ+0.3V
 IN, IN/OUT Volt to GND -0.3V to VCCQ + 0.3V
 Storage Temperature, T_{stg} -55°C to +125°C
 Power Dissipation, P_T 0.7W
 Soldering Temp. & Time 260°C, 10 sec

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ or -25°C to 85°C , VCC = 1.7V to 1.95V, VCCQ = 1.7V to VCC GND = 0V)

| Symbol | Parameter | -70 | | -85 | | Unit | Conditions |
|------------------|------------------------------|----------|------|----------|------|------|--|
| | | Min. | Max. | Min. | Max. | | |
| I _{LI} | Input Leakage Current | - | 1 | - | 1 | μA | V _{IN} = GND to VCCQ |
| I _{LO} | Output Leakage Current | - | 1 | - | 1 | μA | $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{ZZ}} = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$ V _{IO} = GND to VCCQ |
| I _{CC1} | Dynamic Operating Current | - | 15 | - | 12 | mA | Min. Cycle, Duty = 100% $\overline{\text{CE}} = V_{IL}$, $\overline{\text{ZZ}} = V_{IH}$ V _{IH} = VCCQ, V _{IL} = 0V, I _{IO} = 0mA |
| I _{CC2} | | - | 3 | - | 3 | mA | $\overline{\text{CE}} = V_{IL}$, $\overline{\text{ZZ}} = V_{IH}$ V _{IH} = VCCQ, V _{IL} = 0V, f = 1MHz, I _{IO} = 0mA |
| I _{SB1} | Standby Power Supply Current | - | 100 | - | 100 | μA | $\overline{\text{CE}} \geq V_{CCQ} - 0.2\text{V}$ $\overline{\text{ZZ}} \geq V_{CCQ} - 0.2\text{V}$ V _{IN} ≥ 0V |
| V _{OL} | Output Low Voltage | - | 0.2 | - | 0.2 | V | I _{OL} = 0.2 mA |
| V _{OH} | Output High Voltage | VCCQ-0.2 | - | VCCQ-0.2 | - | V | I _{OH} = -0.2mA |

Deep Power Down Specifications and Conditions

| Symbol | Description | Conditions | Typ. | Max. | Units |
|-----------------|-----------------|---|------|------|-------|
| I _{ZZ} | Deep Power-Down | V _{IN} = VCCQ or 0V; +25°C ZZ̄ = LOW CR[4] = 0 | | 10 | μA |

Partial Array Refresh Specifications Conditions

| Symbol | Description | Conditions | Density | Array Partition | Typ. | Max. | Units |
|------------------|-------------------------------|--|---------|-----------------|------|------|-------|
| I _{PAR} | Partial Array Refresh Current | V _{IN} = VCCQ or 0V ZZ̄ = LOW CR[4] = 1 | 12Mb | 3/4 | | 90 | μA |
| | | | 8Mb | 1/2 | | 80 | μA |
| | | | 4Mb | 1/4 | | 70 | μA |

Note: I_{PAR} (MAX) values measured with TCR set to 85°C

Temperature Compensated Refresh Specifications Conditions

| Symbol | Description | Conditions | Density | Max Case Temperatures | Typ. | Max. | Units |
|------------------|---|---|---------|-----------------------|------|------|-------|
| I _{TCR} | Temperature Compensated Refresh Standby Current | V _{IN} = VCCQ or 0V Chip Disabled | 16Mb | +85°C | | 100 | μA |
| | | | | +70°C | | 90 | μA |
| | | | | +45°C | | 80 | μA |
| | | | | +15°C | | 70 | μA |

Note: 1. I_{TCR} (MAX) values measured with FULL ARRAY refresh.
2. This device assumes a standby mode if the chip is disabled (\overline{CE} HIGH).

Truth Table

| \overline{CE} | \overline{ZZ} | \overline{OE} | \overline{WE} | \overline{LB} | \overline{HB} | I/O ₀ to I/O ₇ Mode | I/O ₈ to I/O ₁₅ Mode | VCC Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|---|--|-------------------------------------|
| H | H | X | X | X | X | Not selected | Not selected | I _{SB1} |
| H | L | X | X | X | X | Not selected | Not selected | I _{ZZ} ^{*2} |
| H | L | X | X | X | X | Not selected | Not selected | I _{PAR} *2 |
| L | L | X | L | X | X | Not selected | Not selected | Load CR Register |
| L | H | L | H | L | L | Read | Read | I _{CC1} , I _{CC2} |
| | | | | L | H | Read | High - Z | I _{CC1} , I _{CC2} |
| | | | | H | L | High - Z | Read | I _{CC1} , I _{CC2} |
| L | H | X | L | L | L | Write | Write | I _{CC1} , I _{CC2} |
| | | | | L | H | Write | Not Write/Hi - Z | I _{CC1} , I _{CC2} |
| | | | | H | L | Not Write/Hi - Z | Write | I _{CC1} , I _{CC2} |
| L | H | H | H | X | X | High - Z | High - Z | I _{CC1} , I _{CC2} |

Note: 1. X = H or L
2. DPD is enable when CR register A4 is "0"; otherwise, PAR is enable

Capacitance ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

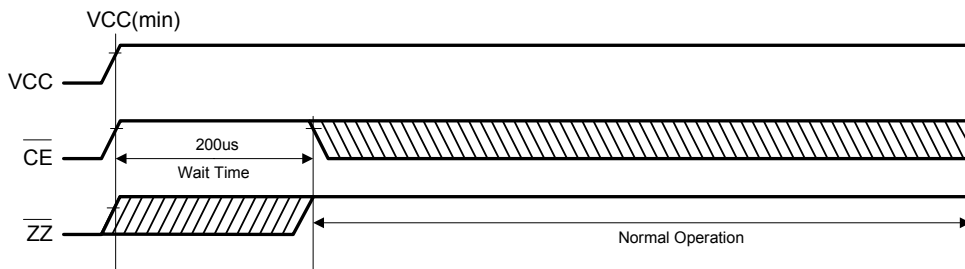
| Symbol | Parameter | Min. | Max. | Unit | Conditions |
|------------|--------------------------|------|------|------|---------------|
| C_{IN}^* | Input Capacitance | - | 6 | pF | $V_{IN} = 0V$ |
| C_{IO}^* | Input/Output Capacitance | - | 6 | pF | $V_{IO} = 0V$ |

* These parameters are sampled and not 100% tested.

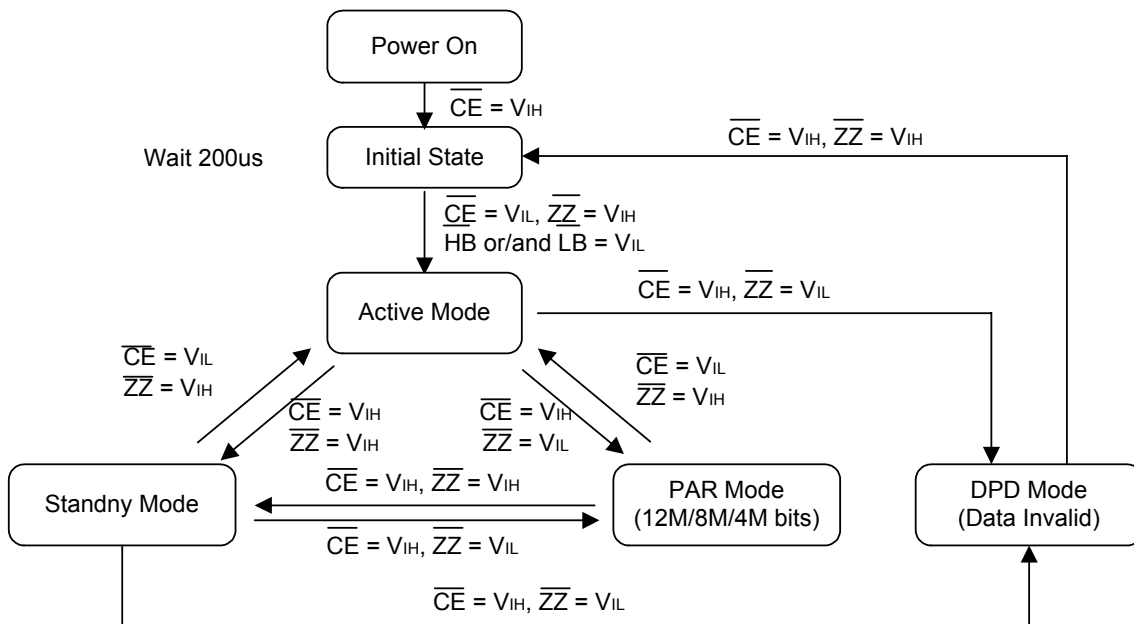
Initialization

The A64E06161 is initialized in the power-on sequence according to the following.

1. To stabilize internal circuits, after turning on the power, a 200 μs or longer wait time must precede any signal toggling.
2. After the wait time, it can be normal operation.

Power on Chart


- Notes: 1. Following power application, make \overline{CE} high level during the wait time 200 μs interval.
 2. After power on sequence, the normal operating \overline{ZZ} must keep at high.

Standby Mode State Machines


Note: DPD is enable when CR register A4 is "0"; otherwise, PAR is enable.

Configuration Register

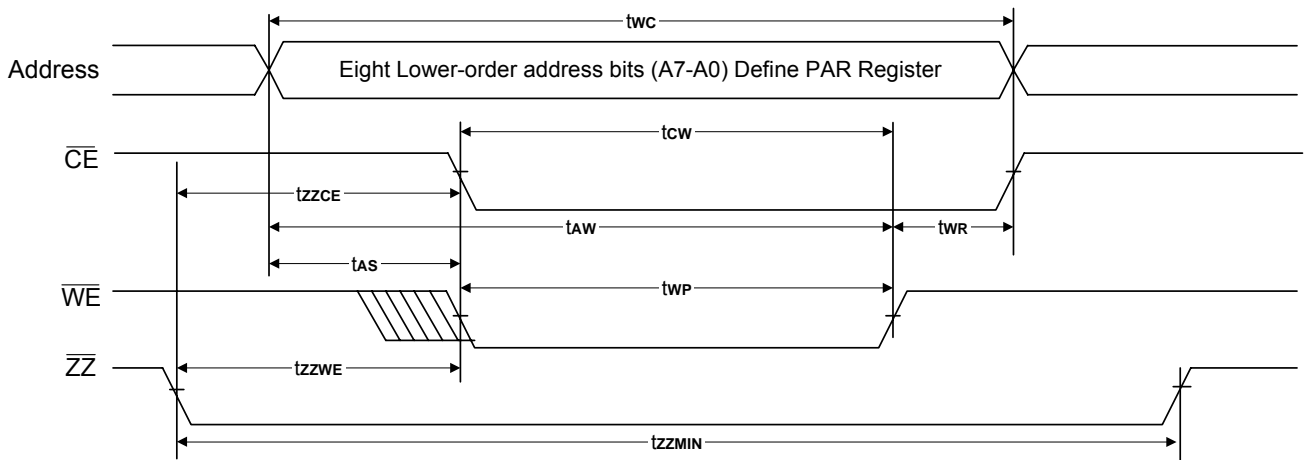
The configuration register (CR) defines how the A64E06161 operates and whether page mode read accesses are permitted. The register is automatically

loaded with default setting during power on and can be updated anytime while the device is operating in a normal state.

CR Register Description

| Reserved | PAGE | TCR | | $\overline{\text{ZZ}}$ Enable Deep Sleep | Array On/Off on $\overline{\text{ZZ}}$ | PAR Top/Bottom Selection | PAR Memory Selection | |
|----------|------|-----|----|--|--|--------------------------|----------------------|----|
| A19 - A8 | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

| Bit(s) | Name | Deserved |
|----------|--|--|
| A19 - A8 | Reserved | Reserved, All must be set to "0" |
| 7 | Page Mode on/off | 0 - Page Mode Disabled (Default) 1 - Page Mode Enabled |
| 6, 5 | Temperature Compensated Register Section | 11 - +85°C (Default) 00 - +70°C 01 - +45°C 10 - +15°C |
| 4 | $\overline{\text{ZZ}}$ Enable Deep Sleep | 0 - DPD Mode Enabled 1 - DPD Mode Disabled (Default) |
| 3 | Array On/Off on $\overline{\text{ZZ}}$ | 0 - PAR Mode (Default) 1 - RMS Mode |
| 2 | PAR Top/Bottom Half Selection | 0 - Bottom (Default) 1 - Top |
| 1 - 0 | PAR Memory Selection | 01 - 3/4 Array (12M) 10 - 1/2 Array (8M) 11 - 1/4 Array (4M) |

CR Register Update – Timing Waveform

Figure 1: CR register update–Timing waveform
Notes:

1. $V_{IH(MAX)} = V_{CCQ} + 0.2V$ for pulse durations less than 20ns.
2. $V_{IL(MIN)} = -1V$ for pulse duration less than 20ns.
3. Overshoot and undershoot specifications are characterized and are not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$ and $T_A = 25^{\circ}C$.
5. The timing values for the CR Register Update are shown in the “Partial Array Mode Timing” table and “AC Characteristics” table.

Page Mode Description

The Page Mode operation takes advantage of the fact that adjacent address can be read in shorter period of time than random addresses. Write operations do not support comparable page mode functionality. The Page Mode operation can be enabled and disabled in the CR register. If the CR register bit A7 is set to a "1", Page Mode operation is enabled.

The A64E06161 provides following operation mode for reducing power:

1. Deep Power Down (DPD) mode
2. Reduce Memory Size (RMS) mode
3. Partial Array Refresh (PAR) mode
4. Temperature Compensated Refresh (TCR) mode

1. Deep Power Down (DPD) mode

In this mode, the internal refresh is turned off and all data integrity of the array is lost. Deep Power Down (DPD) mode is entered by \overline{ZZ} low and keep 10us with A4 register bit set

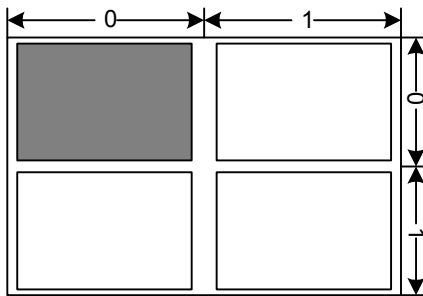
to a "0". The device stays in the Deep Power Down (DPD) mode until \overline{ZZ} is driven High. If the A4 register bit is set equal to "1", Deep Power Down (DPD) mode will not be activated. Once the A64E06161 exits the Deep Power Down (DPD) mode, the content of the CR register is destroyed and the CR register would go into the default state upon normal operation.

2. Reduce Memory Size (RMS) mode

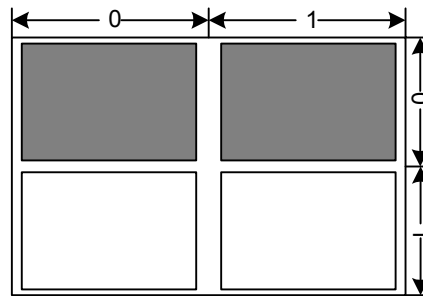
In this mode, the A64E06161 can be operated as a reduced size device. For example, one can operate the 16M A64E06161 as a 4M or 8M memory block. Reduce Memory Size (RMS) mode can be enabled by having the appropriate setting in the CR register. The mode is effective once \overline{ZZ} goes high and remains in the Reduce Memory Size (RMS) mode until full array restored by setting the CR register again. At power on, all four section of the device are activated and the A64E06161 enter into its default state of full memory size and refresh space.

Variable Address Space – Address Patterns

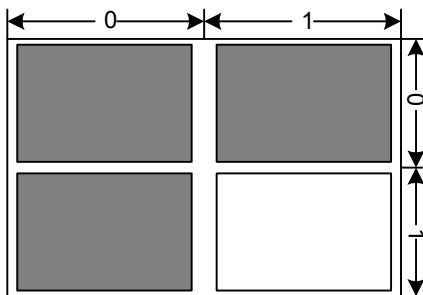
| Partial Array Refresh Mode (A3 = 0, A4 = 1) | | | | | |
|---|--------|--------------------------|----------------------------------|-----------|---------|
| A2 | A1, A0 | Refresh Section | Address | Size | Density |
| 0 | 11 | One-fourth of the Die | 00000h - 3FFFFh (A19 = A18 = 0) | 256K × 16 | 4M |
| 0 | 10 | Half of the Die | 00000h - 7FFFFh (A19 = 0) | 512K × 16 | 8M |
| 0 | 01 | Three-fourths of the Die | 00000h - BFFFFh (A19 : A18 ≠ 11) | 768K × 16 | 12M |
| 1 | 11 | One-fourth of the Die | C0000h - FFFFh (A19 = A18 = 1) | 256K × 16 | 4M |
| 1 | 10 | Half of the Die | 80000h - FFFFh (A19 = 1) | 512K × 16 | 8M |
| 1 | 01 | Three-fourths of the Die | 40000h - FFFFh (A19 : A18 ≠ 00) | 768K × 16 | 12M |
| Reduced Memory Size Mode (A3 = 1, A4 = 1) | | | | | |
| 0 | 11 | One-fourth of the Die | 00000h - 3FFFFh (A19 = A18 = 0) | 256K × 16 | 4M |
| 0 | 10 | Half of the Die | 00000h - 7FFFFh (A19 = 0) | 512K × 16 | 8M |
| 0 | 01 | Three-fourths of the Die | 00000h - BFFFFh (A19 : A18 ≠ 11) | 768K × 16 | 12M |
| 1 | 11 | One-fourth of the Die | C0000h - FFFFh (A19 = A18 = 1) | 256K × 16 | 4M |
| 1 | 10 | Half of the Die | 80000h - FFFFh (A19 = 1) | 512K × 16 | 8M |
| 1 | 01 | Three-fourths of the Die | 40000h - FFFFh (A19 : A18 ≠ 00) | 768K × 16 | 12M |

Memory Block Split
Bottom Address Range


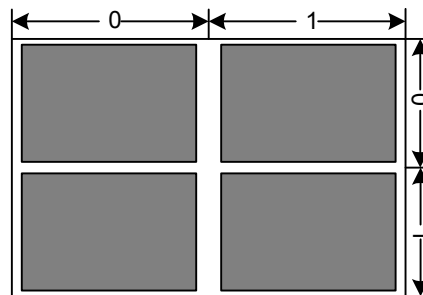
1/4 Address Space Refresh
Active Address Space:
 A0-A17
 A<18,19> = <0,0>



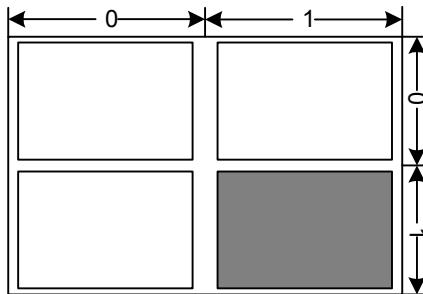
1/2 Address Space Refresh
Active Address Space:
 A0-A18
 A<19> = <0>



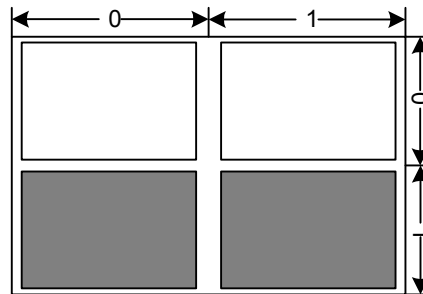
3/4 Address Space Refresh
Active Address Space:
 A0-A19
 A<18,19> = <0,0>, <1,0>, <0,1>



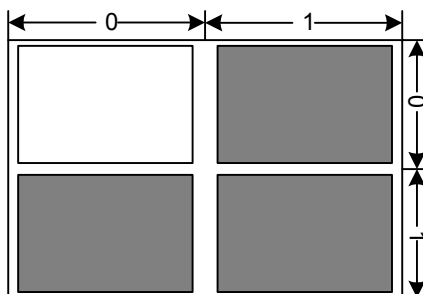
Full Address Space Refresh
Active Address Space:
 A0-A19
 A<18,19> = <X, X>

Top Address Range


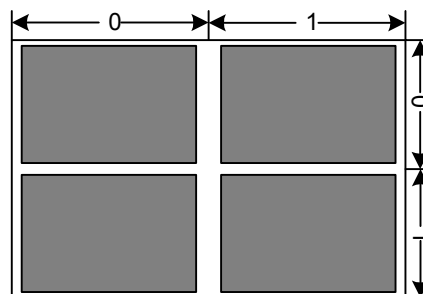
1/4 Address Space Refresh
Active Address Space:
 A0-A17
 A<18,19> = <1,1>



1/2 Address Space Refresh
Active Address Space:
 A0-A18
 A<19> = <1>



3/4 Address Space Refresh
Active Address Space:
 A0-A19
 A<18,19> = <1,0>, <0,1>, <1,1>



Full Address Space Refresh
Active Address Space:
 A0-A19
 A<18,19> = <X, X>

3. Partial Array Refresh (PAR) mode

In this mode, customers can turn off section of A64E06161 in stand-by mode to save standby current. The A64E06161 is divided into four 4M sections allowing certain section to be active. The array partition to be refreshed is determined by the respective bit in the CR register. When \overline{ZZ} is active low, only the portion of the array that is set in the CR register is refreshed and the data is keep at a certain section of memory. The Partial Array Refresh (PAR) mode is only available during standby time (\overline{ZZ} low). Once \overline{ZZ} is turned

high, the A64E06161 goes back to operating in full array refresh. For Partial Array Refresh (PAR) mode to be activated, the register bit, A4 must be set to a "1" value. To change the address space of the Partial Array Refresh (PAR) mode, the CR register must be updated using the CR register description. If the CR register is not updated after power on, the A64E06161 will be in its default state and the whole memory array will be refreshed.

Partial Array Refresh – Entry/Exit

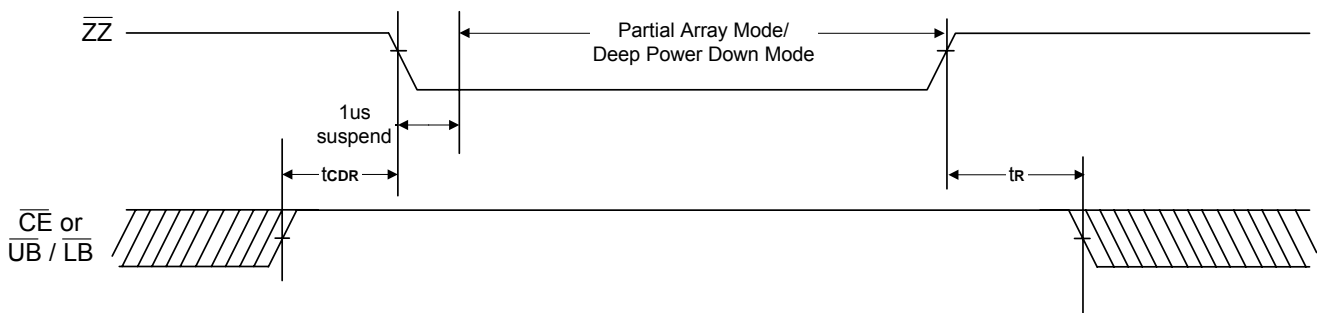


Figure 2: Partial Array refresh – Entry/Exit

Partial Array Mode Timings

| Parameter | Description | Min. | Max. | Unit |
|--------------------|---|------|------|---------|
| t _{ZZWE} | \overline{ZZ} LOW to \overline{WE} LOW | | 1 | μ s |
| t _{CDR} | Chip Deselect to \overline{ZZ} LOW | 0 | | μ s |
| t _r | Operation Recovery Time (Deep Power Down Mode only) | | 200 | μ s |
| t _{ZZMIN} | Deep Power Down Mode Time | 10 | | μ s |
| t _{ZZCE} | \overline{ZZ} LOW to \overline{CE} LOW | 0 | 1 | μ s |
| t _{ZZBE} | \overline{ZZ} LOW to $\overline{UB/LD}$ LOW | 0 | 1 | μ s |

Notes:

1. \overline{OE} and the data pins are in a "don't care" state while the device is in Partial Array Mode.
2. All other timing parameters are as shown in the switching characteristics section.
3. t_r applies only in the Deep Power Down Mode.

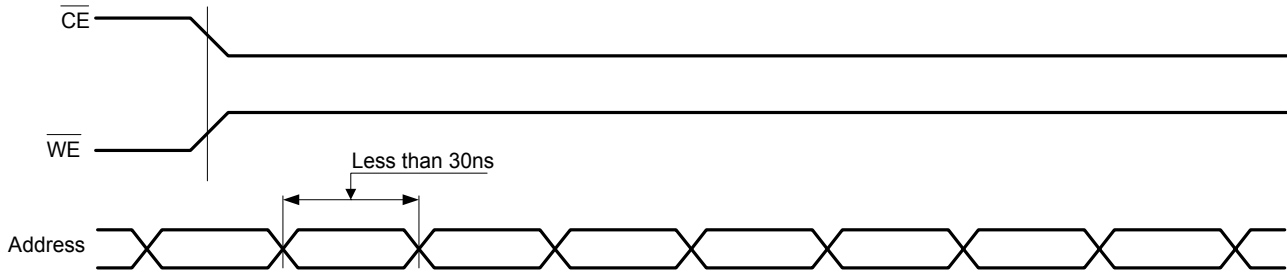
4. Temperature Compensated Refresh (TCR) mode

In this mode, the hidden refresh rate can be optimized for the operating temperature. At higher temperature, the DRAM cell must be refreshed more often than at lower temperature. By setting the temperature of operation in CR register, the refresh rate can be optimized to meet the low standby

current at given operating temperature. There are four selections (+15°C, +45°C, +70°C, +85°C) in the CR register description.

Avoid Timing

Following Figure 3 is show you an abnormal timing which is not supported on Super RAM.

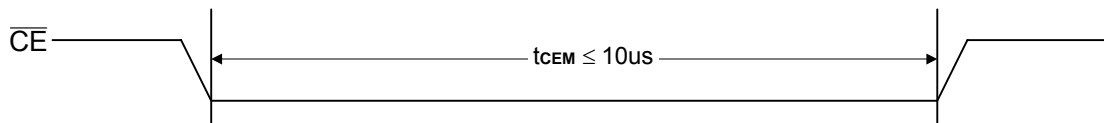


Note: Address = A0 ~ A19 Under CR register A7 = 0
 Address = A2 ~ A19 Under CR register A7 = 1

Figure 3

Operation When Page Mode is Enabled

The maximum \overline{CE} pulse width should not exceed 10 μ s to accommodate orderly scheduling of refresh (Figure 4).



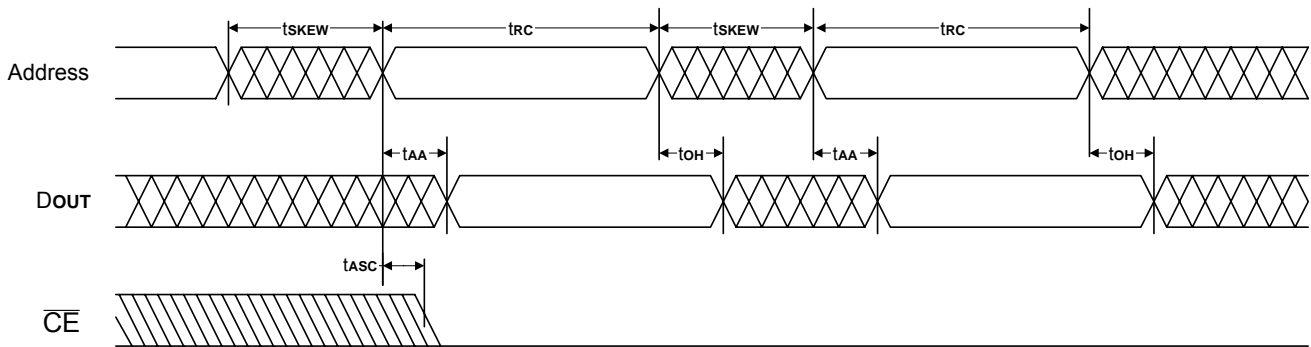
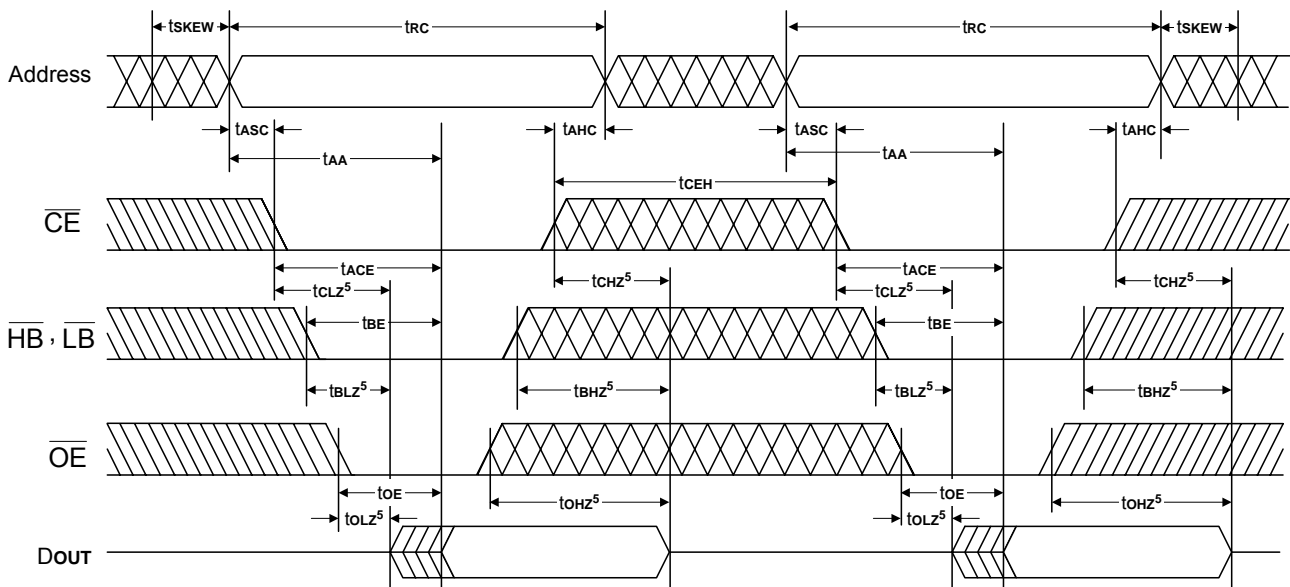
Note: Timing constraints when page mode is enabled.

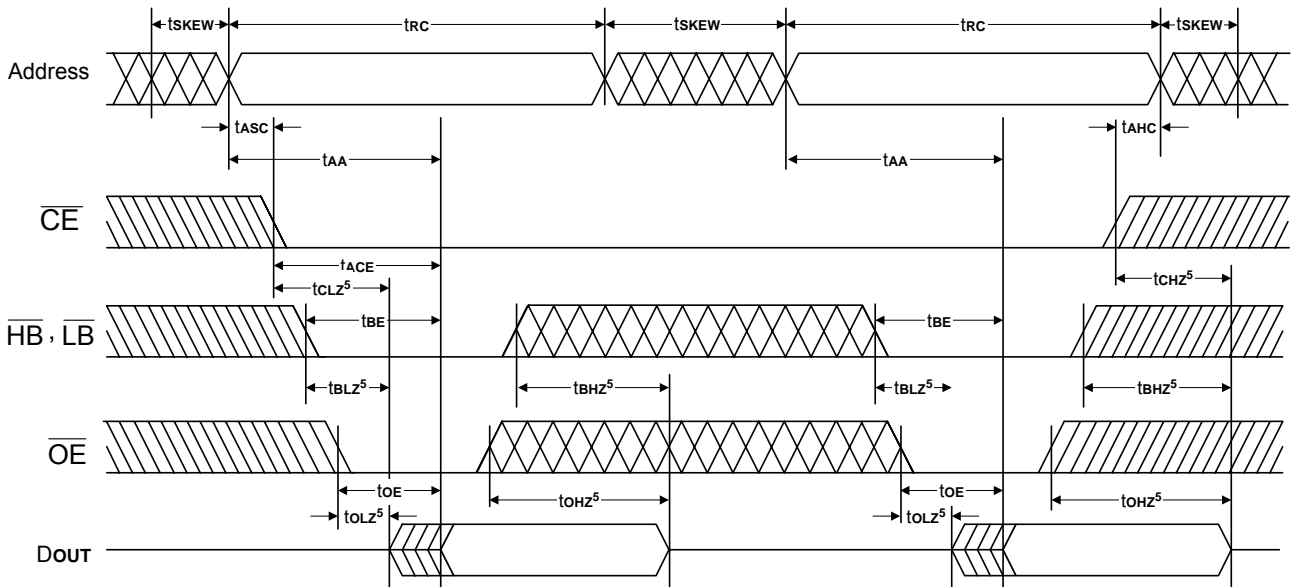
Figure 4: Timing constraint for t_{CEM}

AC Characteristics (TA = 0°C to +70°C or -25°C to 85°C, VCC = 1.7V to 1.95V, VCCQ = 1.7V to VCC GND = 0V)

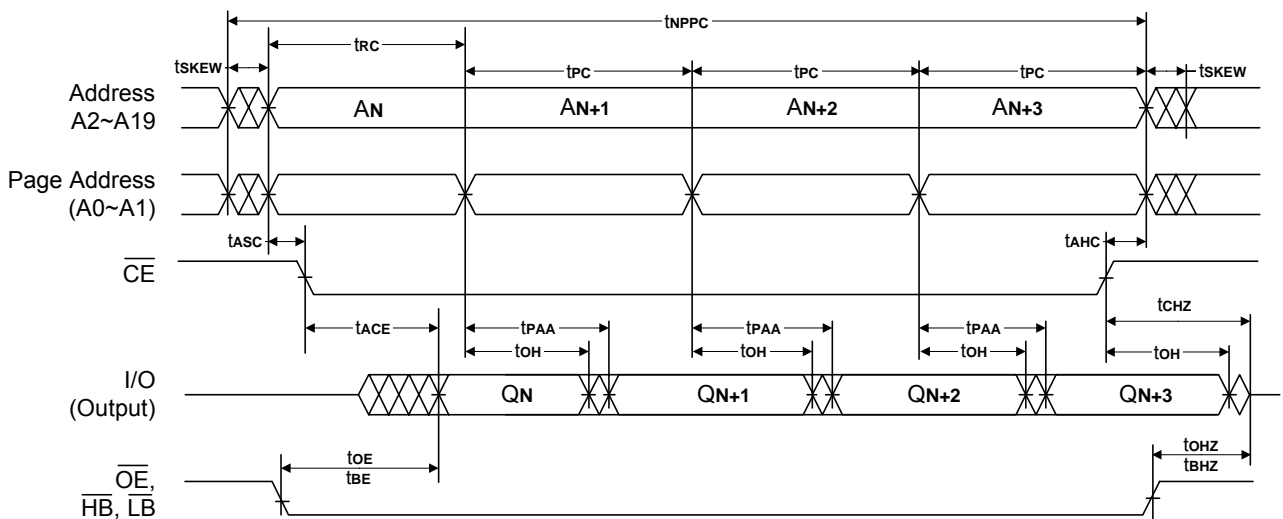
| Symbol | Parameter | -70 | | -85 | | Unit |
|--------------------|---|------|-------|------|-------|------|
| | | Min. | Max. | Min. | Max. | |
| Read Cycle | | | | | | |
| t _{RC} | Read Cycle Time | 70 | 10000 | 85 | 10000 | ns |
| t _{SKEW} | Address Skew | - | 10 | - | 10 | ns |
| t _{AA} | Address Access Time | - | 70 | - | 85 | ns |
| t _{ACE} | Chip Enable Access Time | - | 70 | - | 85 | ns |
| t _{BE} | Byte Enable Access Time | - | 35 | - | 45 | ns |
| t _{OE} | Output Enable to Output Valid | - | 35 | - | 45 | ns |
| t _{CLZ} | Chip Enable to Output in Low Z | 5 | - | 5 | - | ns |
| t _{BLZ} | Byte Enable to Output in Low Z | 5 | - | 5 | - | ns |
| t _{OLZ} | Output Enable to Output in Low Z | 5 | - | 5 | - | ns |
| t _{CHZ} | Chip Disable to Output in High Z | 0 | 14 | 0 | 14 | ns |
| t _{BHZ} | Byte Disable to Output in High Z | 0 | 14 | 0 | 14 | ns |
| t _{OHZ} | Output Disable to Output in High Z | 0 | 14 | 0 | 14 | ns |
| t _{OH} | Output Hold from Address Change | 10 | - | 10 | - | ns |
| t _{ASC} | Address Setup to \overline{CE} Low | 0 | - | 0 | - | ns |
| t _{AHC} | Address Hold Time from \overline{CE} High | 0 | - | 0 | - | ns |
| t _{CEH} | \overline{CE} High Pulse Width | 10 | - | 10 | - | ns |
| t _{PC} | Page Read Cycle Time | 25 | - | 25 | - | ns |
| t _{PAA} | Page access Time | - | 25 | - | 25 | ns |
| t _{NPPC} | Normal to Page Read Cycle Time | - | 10 | - | 10 | μs |
| Write Cycle | | | | | | |
| t _{WC} | Write Cycle Time | 70 | 10000 | 85 | 10000 | ns |
| t _{SKEW} | Address Skew | - | 10 | - | 10 | ns |
| t _{CW} | Chip Enable to End of Write | 70 | - | 85 | - | ns |
| t _{BW} | Byte Enable to End of Write | 60 | - | 70 | - | ns |
| t _{AS} | Address Setup Time | 0 | - | 0 | - | ns |
| t _{AW} | Address Valid to End of Write | 70 | - | 85 | - | ns |
| t _{WP} | Write Pulse Width | 50 | - | 60 | - | ns |
| t _{WR} | Write Recovery Time | 0 | - | 0 | - | ns |
| t _{WHZ} | Write to Output in High Z | - | 14 | - | 14 | ns |
| t _{DW} | Data to Write Time Overlap | 30 | - | 35 | - | ns |
| t _{DH} | Data Hold from Write Time | 0 | - | 0 | - | ns |
| t _{OW} | Output Active from End of Write | 5 | - | 5 | - | ns |
| t _{ASC} | Address Setup to \overline{CE} Low | 0 | - | 0 | - | ns |
| t _{AHC} | Address Hold Time from \overline{CE} High | 0 | - | 0 | - | ns |
| t _{CEH} | \overline{CE} High Pulse Width | 10 | - | 10 | - | ns |
| t _{WEH} | \overline{WE} High Pulse Width | 10 | - | 10 | - | ns |
| t _{CEM} | Maximum \overline{CE} Pulse width | - | 10 | - | 10 | μs |

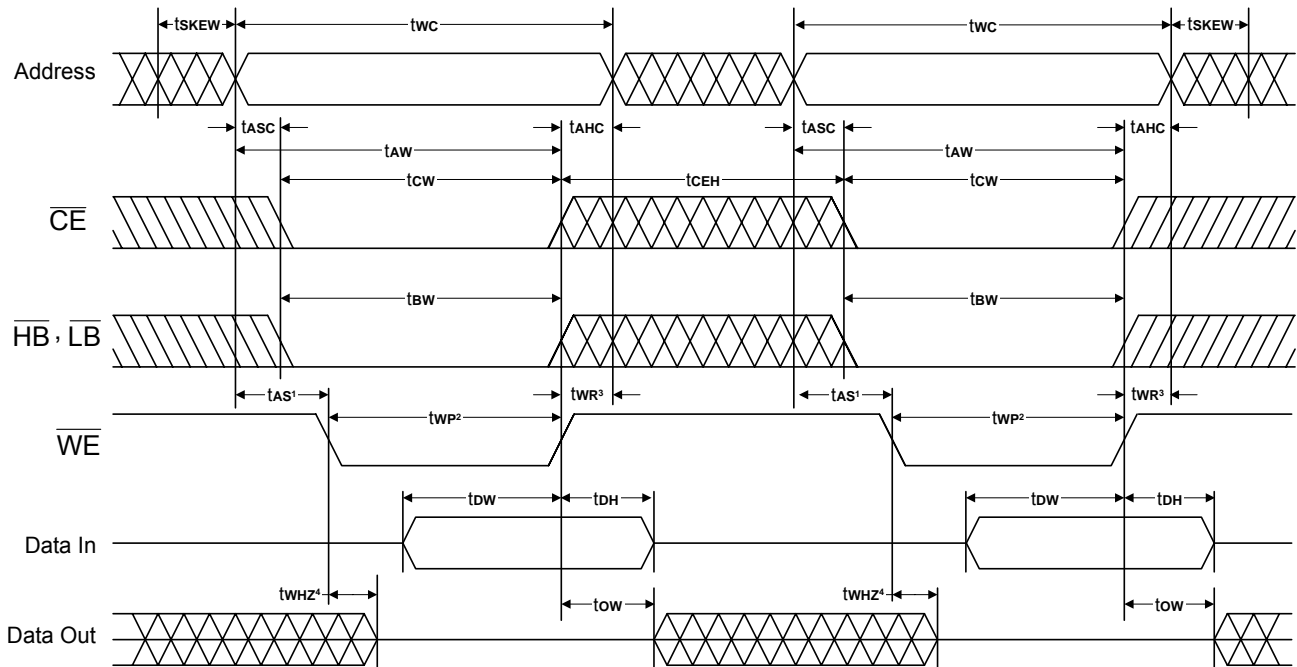
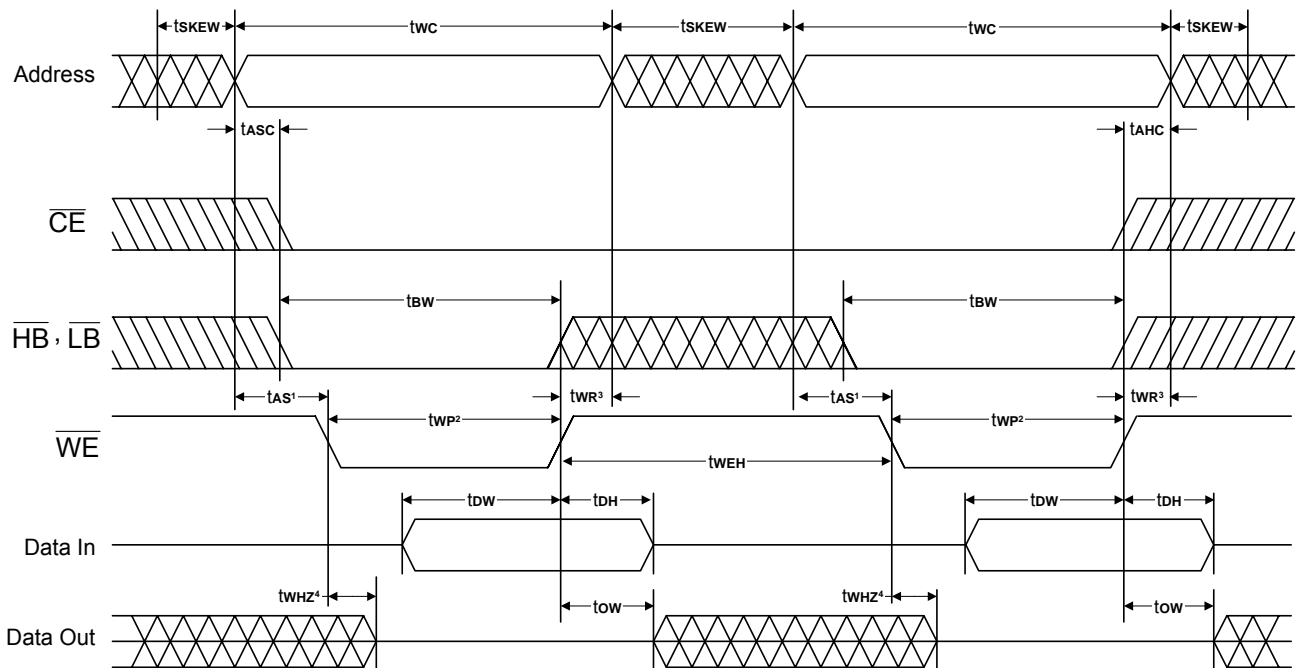
Note: t_{CHZ}, t_{BHZ} and t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

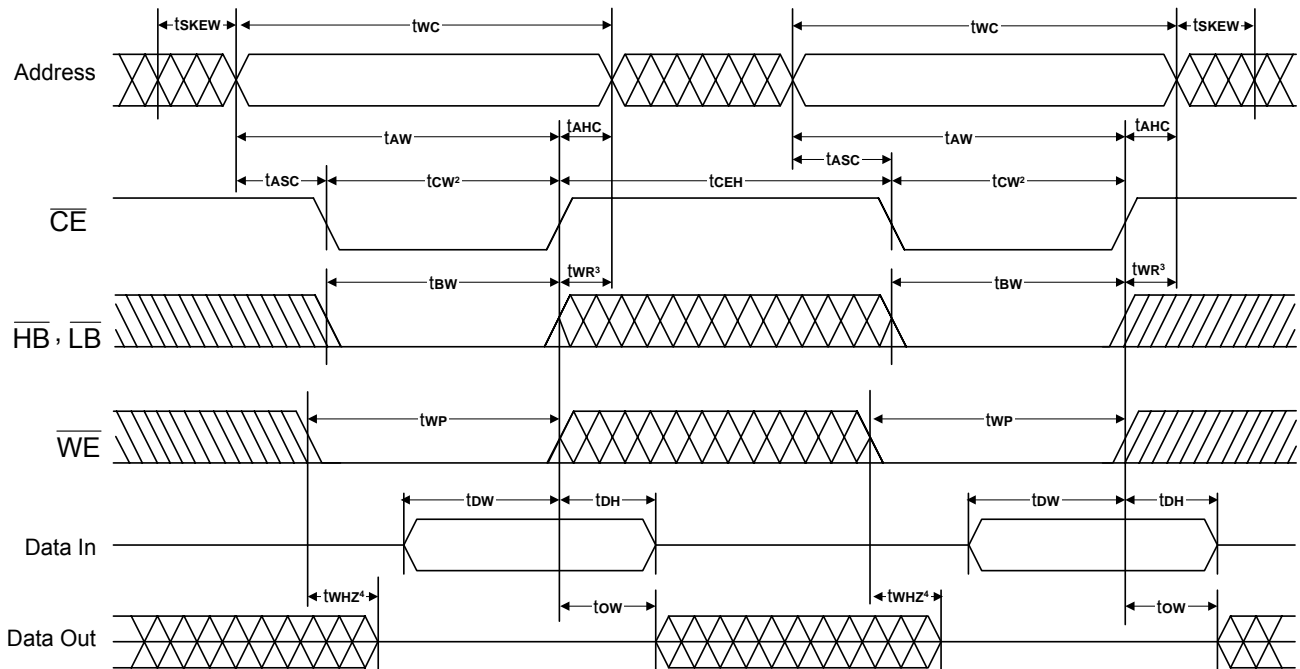
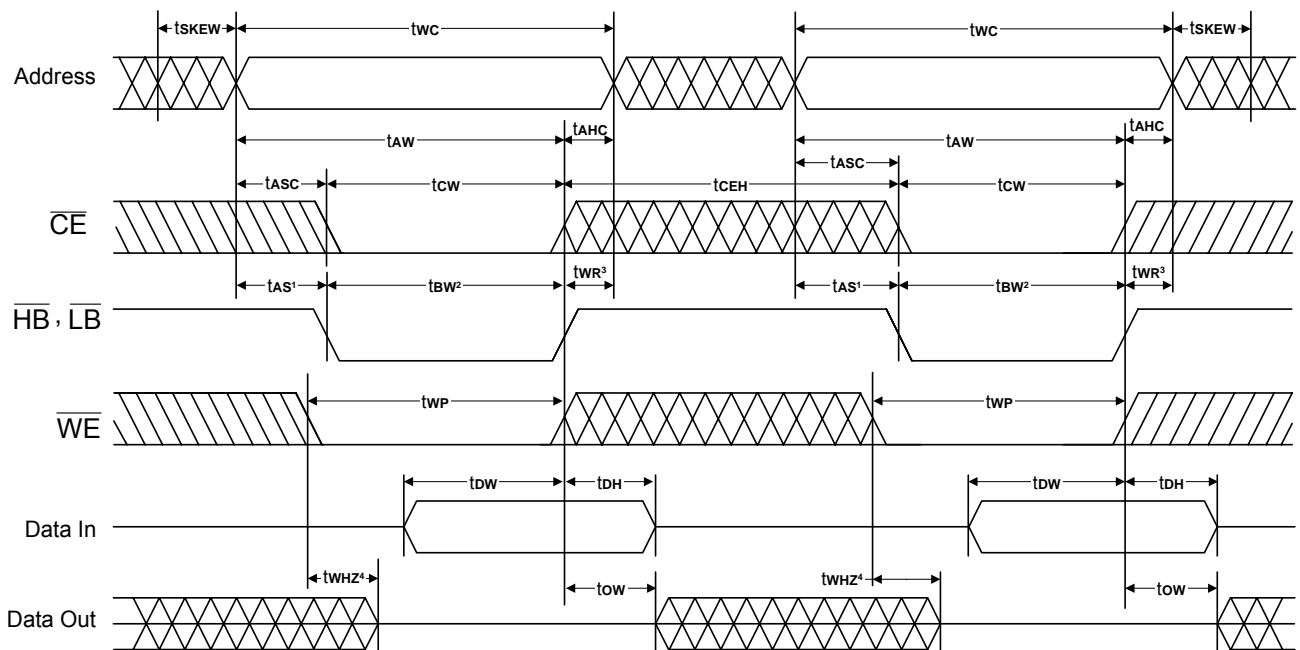
Timing Waveforms
Read Cycle 1^(1, 2, 4, 6)

Read Cycle 2-1^(1, 3, 6)


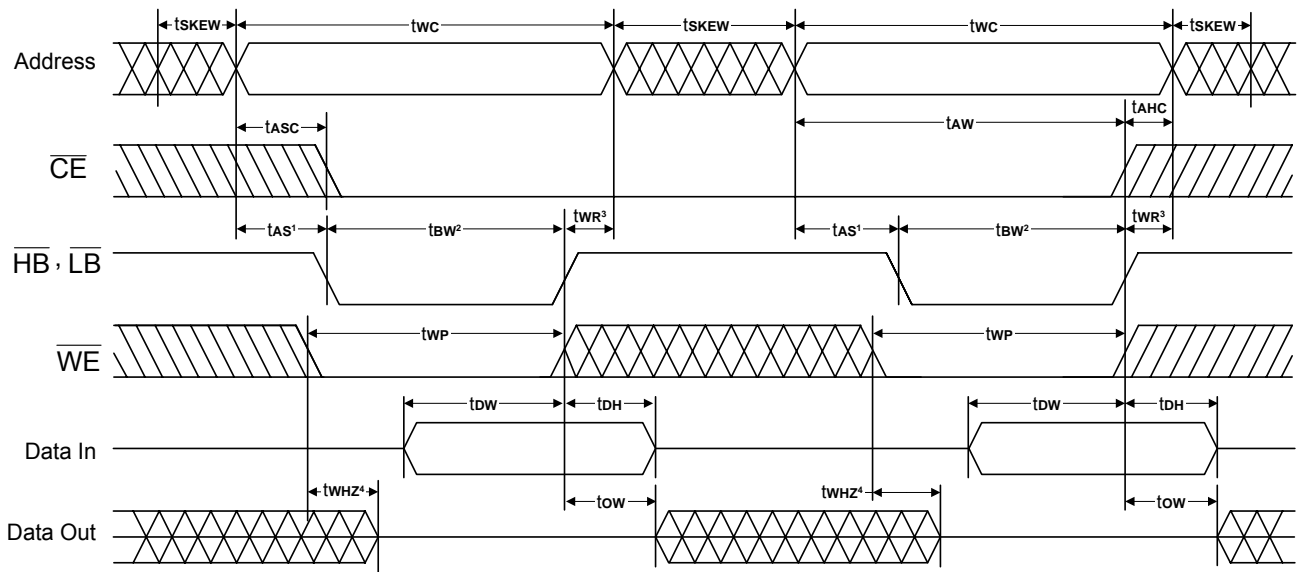
Read Cycle 2-2^(1, 3, 6)


- Notes:
1. \overline{WE} is high for Read Cycle.
 2. Device is continuously enabled $\overline{CE} = V_{IL}$, $\overline{HB} = V_{IL}$ and, or $\overline{LB} = V_{IL}$.
 3. Address valid prior to or coincident with \overline{CE} and (\overline{HB} and, or \overline{LB}) transition low.
 4. $\overline{OE} = V_{IL}$.
 5. Transition is measured $\pm 500mV$ from steady state. This parameter is sampled and not 100% tested.
 6. \overline{ZZ} is high for Read Cycle.

Timing Waveforms
Words Page Read Cycle Timing Chart


Timing Waveforms (continued)
**Write Cycle 1-1⁽⁶⁾
(Write Enable Controlled)**

**Write Cycle 1-2⁽⁶⁾
(Write Enable Controlled)**


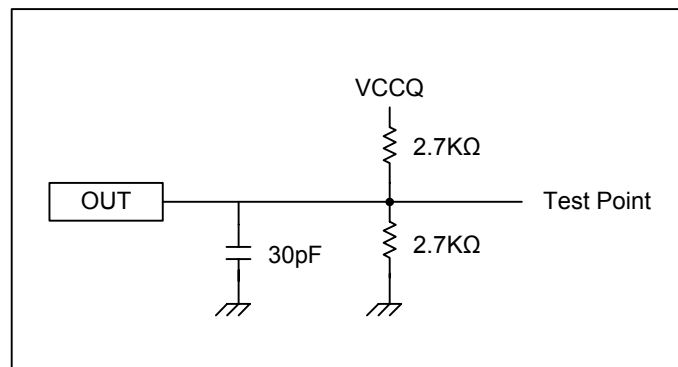
Timing Waveforms (continued)
**Write Cycle 2-1⁽⁶⁾
(Chip Enable Controlled)**

Timing Waveforms
**Write Cycle 3-1⁽⁶⁾
(Byte Enable Controlled)**


Write Cycle 3-2⁽⁶⁾
(Byte Enable Controlled)


- Notes:
1. t_{AS} is measured from the address valid to the beginning of Write.
 2. A Write occurs during the overlap (t_{WP} , t_{BW}) of a low \overline{CE} , \overline{WE} and (\overline{HB} and, or \overline{LB}).
 3. t_{WR} is measured from the earliest of \overline{CE} or \overline{WE} or (\overline{HB} and, or \overline{LB}) going high to the end of the Write cycle.
 4. OE level is high or low.
 5. Transition is measured $\pm 500\text{mV}$ from steady state. This parameter is sampled and not 100% tested.
 6. ZZ is high for Write Cycle.

AC Test Conditions

| | |
|--|------------------------------------|
| Input Pulse Levels | $V_{CCQ} * 0.2$ to $V_{CCQ} * 0.8$ |
| Input Rise And Fall Time | 2 ns (10% to 90%) |
| Input and Output Timing Reference Levels | $0.5 * V_{CCQ}$ |
| Output Load | See Figures 5 |


Figure 5. Output Load Circuit

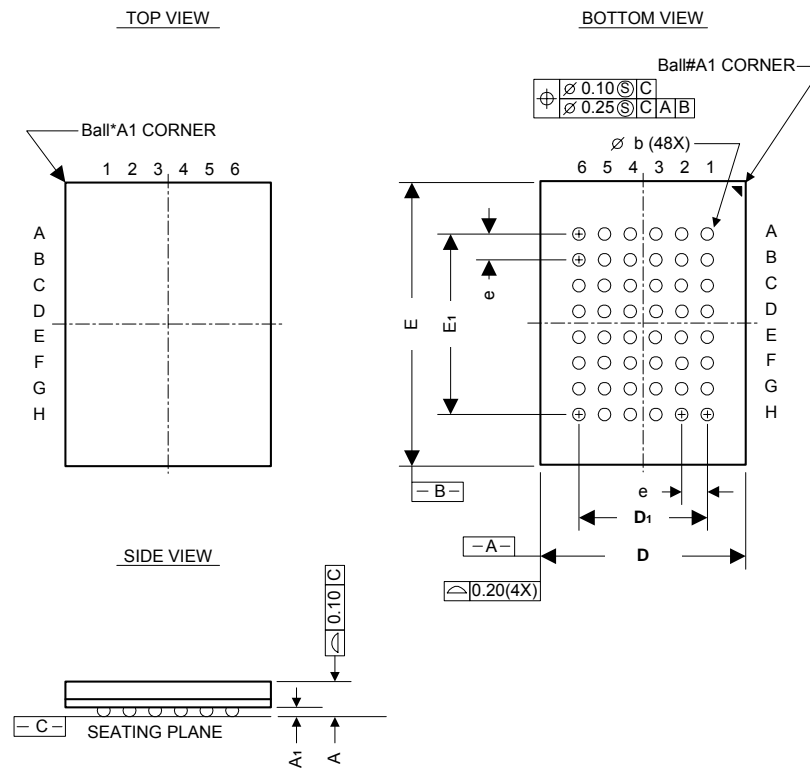
Ordering Information

| Part No. | Access Time (ns) | Operating Current Max. (mA) | Deep Power Down Mode Standby Current Max. (μA) | Package |
|-----------------|-------------------------|--|--|----------------|
| A64E06161G-70 | 70 | 15 | 10 | 48B Mini BGA |
| A64E06161G-85 | 85 | 12 | 10 | 48B Mini BGA |
| A64E06161G-70I | 70 | 15 | 10 | 48B Mini BGA |
| A64E06161G-85I | 85 | 12 | 10 | 48B Mini BGA |

Note: -I is for industrial operating temperature range

Package Information
**48LD CSP (6 x 8 mm) Outline Dimensions
(48TFBGA)**

unit: mm



| Symbol | Dimensions in mm | | |
|----------------|------------------|------|------|
| | MIN. | NOM. | MAX. |
| A | --- | --- | 1.20 |
| A ₁ | 0.20 | 0.25 | 0.30 |
| D | 5.90 | 6.00 | 6.10 |
| E | 7.90 | 8.00 | 8.10 |
| D ₁ | --- | 3.75 | --- |
| E ₁ | --- | 5.25 | --- |
| e | --- | 0.75 | --- |
| b | 0.30 | 0.35 | 0.40 |

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS ϕ 0.3mm (SMD)
SUGGEST TO DESIGN THE PCB LAND SIZE AS ϕ 0.3mm (NSMD)