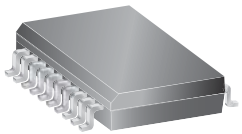
10-Bit Serial Input Latched Source Driver

Features and Benefits

- Controlled output slew rate
- High-speed data storage
- 60 V minimum output breakdown
- High data-input rate
- PNP active pull-downs
- Low output-saturation voltages
- Low-power CMOS logic and latches
- Improved replacements for TL4810x, UCN5810x, and UCQ5810x

Packages:

18-pin DIP
(A package)



20-pin SOICW
(LW package)

Not to scale

Description

The A6810 combines 10-bit CMOS shift registers, accompanying data latches, and control circuitry with bipolar sourcing outputs and PNP active pull-downs. Designed primarily to drive vacuum-fluorescent (VF) displays, the 60 V and –40 mA output ratings also allow this device to be used in many other peripheral power driver applications. The A6810 features an increased data input rate (compared with the older UCN/UCQ5810-F) and a controlled output slew rate.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 3.3 or 5 V logic supply, serial data-input rates of at least 10 MHz can be attained

A CMOS serial data output permits cascaded connections in applications requiring additional drive lines. Similar devices are available as the A6812 (20-bit) and A6818 (32-bit).

The A6810 output source drivers are NPN Darlingtons, capable of sourcing up to 40 mA. The controlled output slew rate reduces electromagnetic noise, which is an important consideration in systems that include telecommunications and microprocessors, and to meet government emissions regulations. For inter-digit

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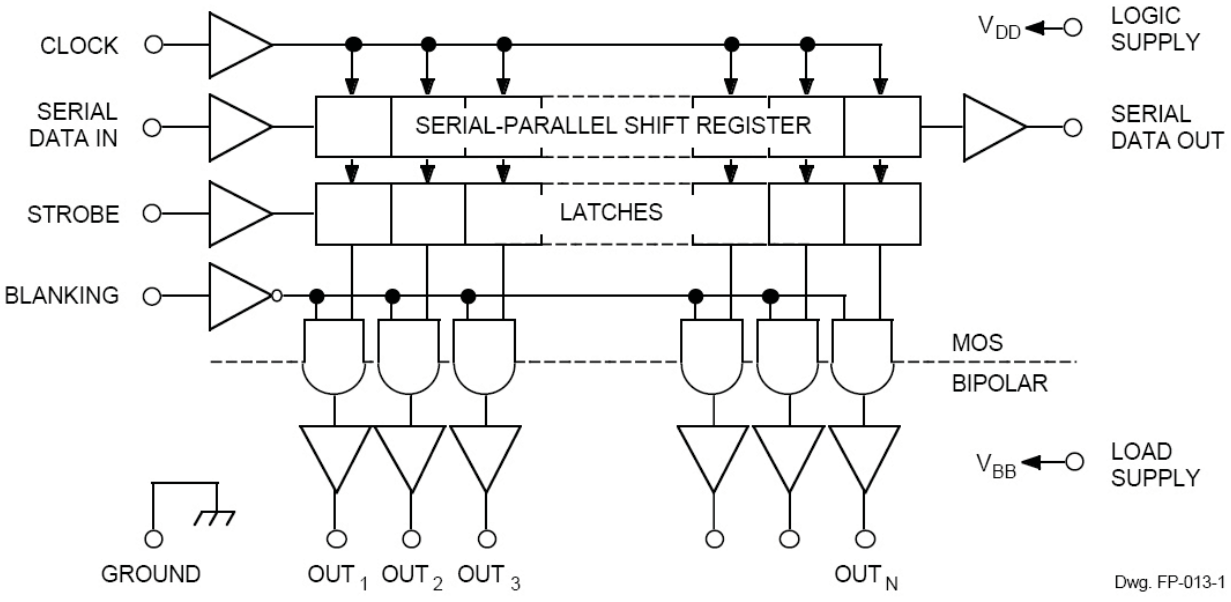
Functional Block Diagram



Description (continued)

blanking, all output drivers can be disabled and all sink drivers turned on with a BLANKING input high. The PNP active pull-downs can sink at least 2.5 mA.

The A6810 is available in three temperature ranges for optimum performance in commercial (S), industrial (E), and automotive (K) applications. It is provided in two package styles, through-hole DIP (package A) and surface-mount SOIC (package LW). Copper leadframes, low logic-power dissipation, and low output-saturation voltages allow all devices to source 25 mA from all outputs continuously over the full operating temperature range.

The lead (Pb) free versions have 100% matte tin leadframe plating.

Selection Guide

Part Number	Pb-free	Packing	Ambient Temperature, T_A (°C)	Package
~~A6810EA-T~~	Yes	21 pieces/tube	–40 to 85	18-pin DIP
~~A6810SA-T~~	Yes	21 pieces/tube	–20 to 85	
~~A6810ELWTR-T~~	Yes	1000 pieces/13-in. reel	–40 to 85	20-pin SOIC-W
~~A6810KLWTR-T~~	Yes	1000 pieces/13-in. reel	–40 to 125	
~~A6810SLWTR-T~~	Yes	1000 pieces/13-in. reel	–20 to 85	

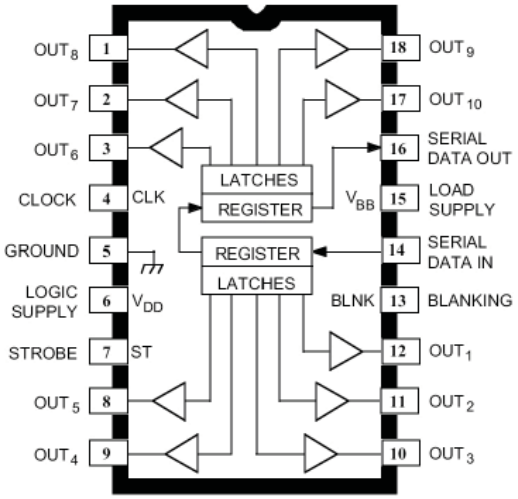
*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change May 3, 2010. Deadline for receipt of LAST TIME BUY orders is October 29, 2010.

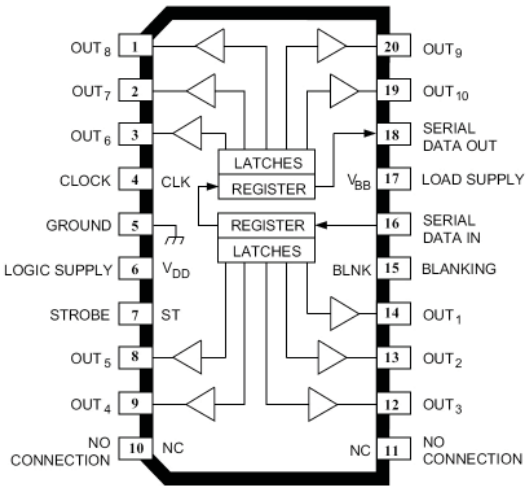
Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
Logic Supply Voltage	V_{DD}		7.0	V
Driver Supply Voltage	V_{BB}		60	V
Input Voltage Range	V_{IN}		–0.3 to V_{DD} + 0.3	V
Continuous Output Current Range	I_{OUT}		–40 to 15	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	°C
		Range K	–40 to 125	°C
		Range S	–20 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 125	°C

*Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

Pin-out Diagrams

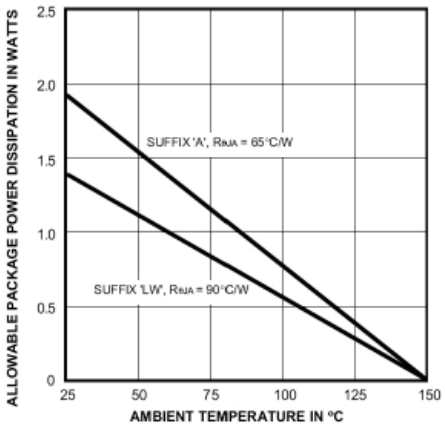




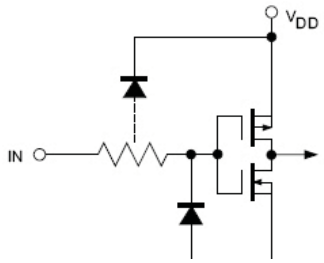
Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	Package A, 1-layer PCB with copper limited to solder pads	65	°C/W
		Package LW, 1-layer PCB with copper limited to solder pads	90	°C/W

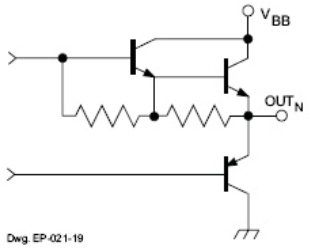
*Additional thermal information available on the Allegro website.



TYPICAL INPUT CIRCUIT



TYPICAL OUTPUT DRIVER



ELECTRICAL CHARACTERISTICS at T_A = +25°C (A6810S-) or over operating temperature range (A6810E-), V_{BB} = 60 V, logic supply operating voltage V_{DD} = 3.0 to 5.5 V; unless otherwise noted

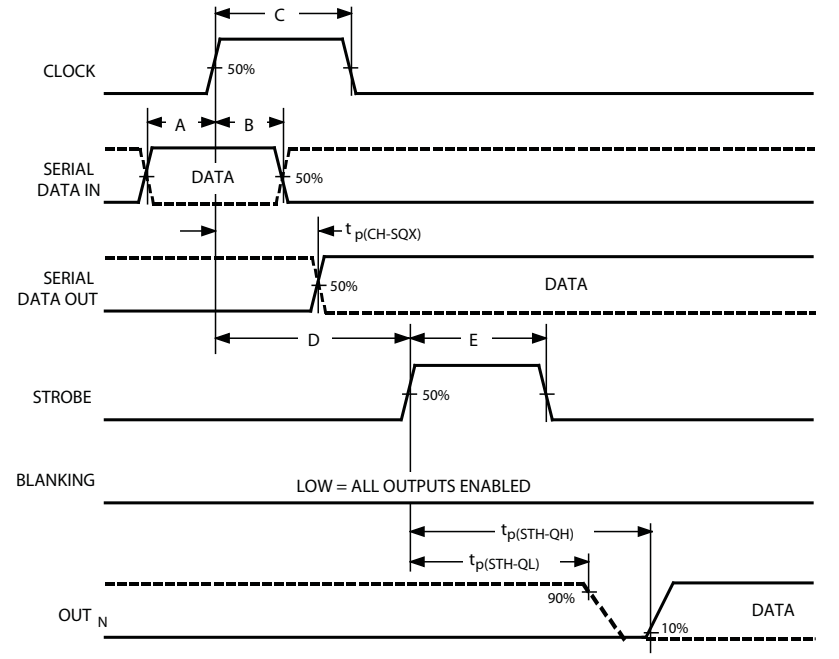
Characteristic	Symbol	Test Conditions	Limits @ V_{DD} = 3.3 V			Limits @ V_{DD} = 5 V			Units
			Mln.	Typ.	Max.	Min.	Typ.	Max.	
Output Leakage Current	I_{CEX}	V_{OUT} = 0 V	—	<-0.1	-15	—	<-0.1	-15	µA
Output Voltage	$V_{OUT(1)}$	I_{OUT} = -25 mA	57.5	58.3	—	57.5	58.3	—	V
	$V_{OUT(0)}$	I_{OUT} = 1 mA	—	1.0	1.5	—	1.0	1.5	V
Output Pull-Down Current	$I_{OUT(0)}$	V_{OUT} = 5 V to V_{BB}	2.5	5.0	—	2.5	5.0	—	mA
Input Voltage	$V_{IN(1)}$		2.2	—	—	3.3	—	—	V
	$V_{IN(0)}$		—	—	1.1	—	—	1.7	V
Input Current	$I_{IN(1)}$	V_{IN} = V_{DD}	—	<0.01	1.0	—	<0.01	1.0	µA
	$I_{IN(0)}$	V_{IN} = 0 V	—	<-0.01	-1.0	—	<-0.01	-1.0	µA
Input Clamp Voltage	V_{IK}	I_{IN} = -200 µA	—	-0.8	-1.5	—	-0.8	-1.5	V
Serial Data Output Voltage	$V_{OUT(1)}$	I_{OUT} = -200 µA	2.8	3.05	—	4.5	4.75	—	V
	$V_{OUT(0)}$	I_{OUT} = 200 µA	—	0.15	0.3	—	0.15	0.3	V
Maximum Clock Frequency	f_c		10*	—	—	10*	—	—	MHz
Logic Supply Current	$I_{DD(1)}$	All Outputs High	—	0.25	0.75	—	0.3	1.0	mA
	$I_{DD(0)}$	All Outputs Low	—	0.25	0.75	—	0.3	1.0	mA
Load Supply Current	$I_{BB(1)}$	All Outputs High, No Load	—	1.5	3.0	—	1.5	3.0	mA
	$I_{BB(0)}$	All Outputs Low	—	0.2	20	—	0.2	20	µA
Blanking-to-Output Delay	$t_{dis(BQ)}$	C_L = 30 pF, 50% to 50%	—	0.7	2.0	—	0.7	2.0	µs
	$t_{en(BQ)}$	C_L = 30 pF, 50% to 50%	—	1.8	3.0	—	1.8	3.0	µs
Strobe-to-Output Delay	$t_{p(STH-QL)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	0.7	2.0	—	0.7	2.0	µs
	$t_{p(STH-QH)}$	R_L = 2.3 kΩ, C_L ≤ 30 pF	—	1.8	3.0	—	1.8	3.0	µs
Output Fall Time	t_f	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Rise Time	t_r	R_L = 2.3 kΩ, C_L ≤ 30 pF	2.4	—	12	2.4	—	12	µs
Output Slew Rate	dV/dt	R_L = 2.3 kΩ, C_L ≤ 30 pF	4.0	—	20	4.0	—	20	V/µs
Clock-to-Serial Data Out Delay	$t_{p(CH-SQX)}$	I_{OUT} = ±200 µA	—	50	—	—	50	—	ns

Negative current is defined as coming out of (sourcing) the specified device terminal.

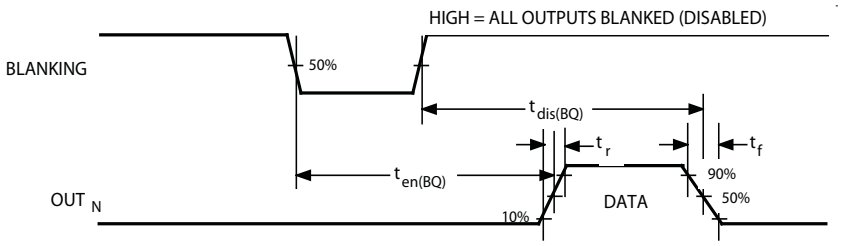
Typical data is is for design information only and is at T_A = +25°C.

*Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)



Dwg. WP-029



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A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ ..... **25 ns**
B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ ..... **25 ns**
C. Clock Pulse Width, $t_{w(CH)}$ ..... **50 ns**
D. Time Between Clock Activation and Strobe, $t_{su(C)}$ ..... **100 ns**
E. Strobe Pulse Width, $t_{w(STH)}$ ..... **50 ns**

NOTE – Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Serial Data present at the input is transferred to the shift register on the logic "0" to logic "1" transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the BLANKING input be high during serial data entry.

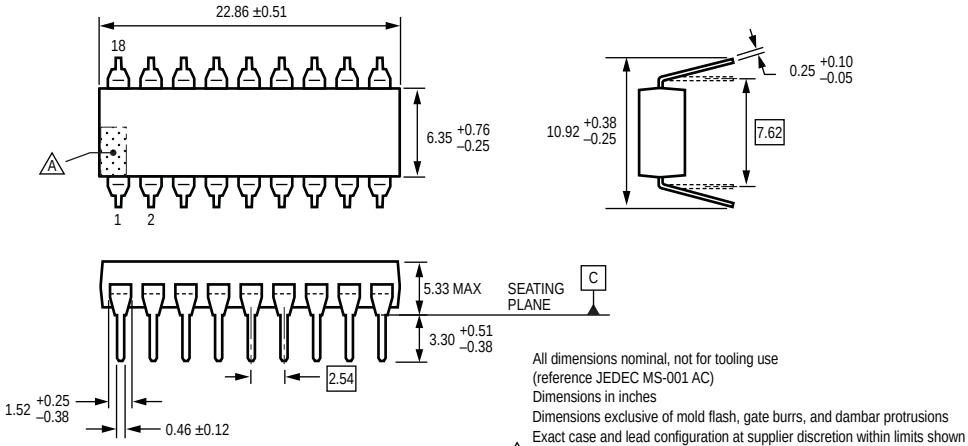
When the BLANKING input is high, the output source drivers are disabled (OFF); the PNP active pull-down sink drivers are ON. The information stored in the latches is not affected by the BLANKING input. With the BLANKING input low, the outputs are controlled by the state of their respective latches.

TRUTH TABLE

Serial Data Input	Clock Input	Shift Register Contents	Serial Data Output	Strobe Input	Latch Contents	Output Blanking	Output Contents
		I_1 I_2 I_3 ... I_{N-1} I_N			I_1 I_2 I_3 ... I_{N-1} I_N		I_1 I_2 I_3 ... I_{N-1} I_N
H		H R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
L		L R_1 R_2 ... R_{N-2} R_{N-1}	R_{N-1}				
X		R_1 R_2 R_3 ... R_{N-1} R_N	R_N				
		X X X ... X X	X	L	R_1 R_2 R_3 ... R_{N-1} R_N		
		P_1 P_2 P_3 ... P_{N-1} P_N	P_N	H	P_1 P_2 P_3 ... P_{N-1} P_N	L	P_1 P_2 P_3 ... P_{N-1} P_N
					X X X ... X X	H	L L L ... L L

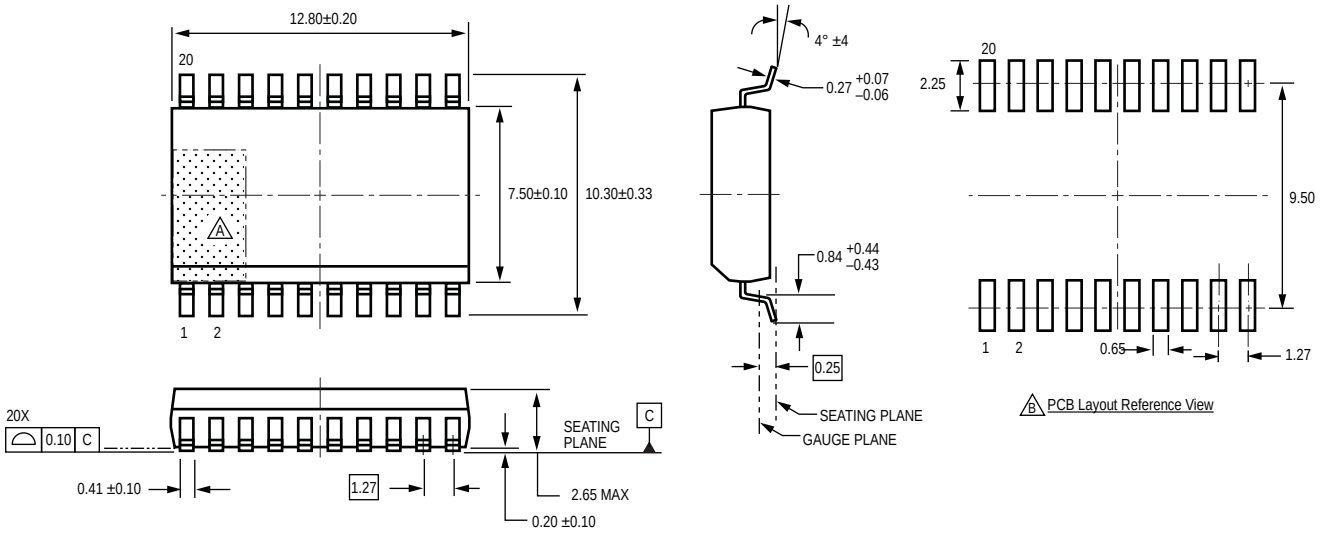
L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

Package A 18-Pin DIP



All dimensions nominal, not for tooling use
(reference JEDEC MS-001 AC)
Dimensions in inches
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown
A Terminal #1 mark area

Package LW 20-Pin SOICW



For Reference Only
Dimensions in millimeters
(Reference JEDEC MS-013 AC)
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area
B Reference pad layout (reference IPC SOIC127P1030X265-20M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

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