A6841

DABiC-5 8-Bit Serial Input Latched Sink Drivers

Package A 18-pin DIP



Package LW 18-pin Wide Body SOIC



Package LW-20 20-pin Wide Body SOIC



ABSOLUTE MAXIMUM RATINGS

Output voitage
V _{CE} 50 V
$V_{CE(SUS)}$ (for inductiove load applications)35 V
Logic Supply Voltage, V _{DD} 7 V
Emitter Supply Voltage, V_{EE} 20 V
Input Voltage Range, V_{IN} 0.3 V to V_{DD} +0.3 V
Continuous Output Current (each output), $I_{\mbox{\scriptsize OUT}} \dots 500~\mbox{\scriptsize mA}$
Package Power Dissipation, P _D , see chart, page 6
Operating Temperature Range
Ambient Temperature, T _△ –20°C to +85°C

Caution: CMOS devices have input-static protection, but are susceptible to damage when exposed to extremely high static-electrical charges.

Storage Temperature, T_S -55°C to +150°C

The merging of low-power CMOS logic and bipolar output power drivers permit the A6841 integrated circuits to be used in a wide variety of peripheral power driver applications. Each device has an eight-bit CMOS shift register and CMOS control circuitry, eight CMOS data latches, and eight bipolar current-sinking Darlington output drivers. The 500 mA NPN Darlington outputs, with integral transient-suppression diodes, are suitable for use with relays, solenoids, and other inductive loads.

All package variations of the A6841 offer premium performance with a minimum output-breakdown voltage rating of 50 V (35 V sustaining). All drivers can be operated with a split supply where the negative supply is up to -20 V.

The CMOS inputs are compatible with standard CMOS logic levels. TTL circuits may require the use of appropriate pull-up resistors. By using the serial data output, drivers can be cascaded for interface applications requiring additional drive lines.

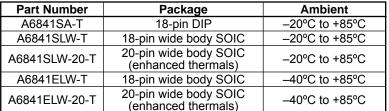
The A6841SA devices are furnished in a standard 18-pin plastic DIP. The A6841SLW device is available in an 18-lead SOIC package. A 20-pin SOIC version, A6841SLW-20 has improved thermal characteristics. The SOIC drivers are also available for operation to a temperature of -40°C (part number suffix *ELW*). These devices are lead (Pb) free, with 100% matte tin plated leadframes.

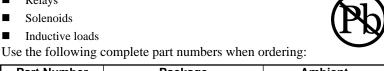
FEATURES

- 3.3 V to 5 V logic supply range
- Power on reset (POR)
- To 10 MHz data input rate
- CMOS, TTL compatible inputs
- -40°C operation available
- Low-power CMOS logic and latches
- Schmitt trigger inputs for improved noise immunity
- High-voltage current-sink outputs
- Internal pull-up/pull down resistors
- Output transient-protection diodes
- Single or split supply operation

APPLICATIONS

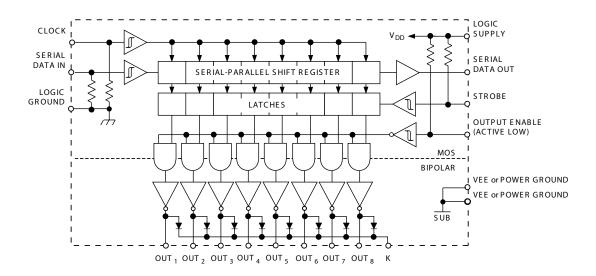
- Relays
- Solenoids
- Inductive loads



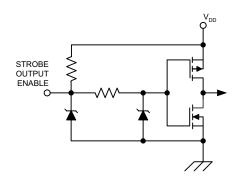


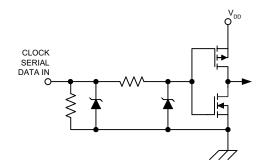


Functional Block Diagram

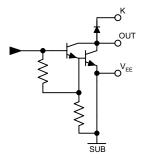


Typical Input Circuits





Typical Output Driver





ELECTRICAL CHARACTERISTICS¹ Unless otherwise noted: $T_A = 25^{\circ}C$, $V_{ee} = 0$ V, logic supply operating voltage $V_{dd} = 3.0 \, \text{V}$ to $5.5 \, \text{V}$

			V _{dd} = 3.3 V		\				
Characteristic	Symbol	Test Conditions	Min.	Тур.	Max.	Min.	Тур.	Max.	Units
Output Leakage Current	I _{CEX}	V _{OUT} = 50 V	-	_	10	-	-	10	μΑ
Output Sustaining Voltage	V _{CE(SUS)}	I _{OUT} = 350 mA, L = 3 mH	35	_	-	35	_	-	V
Oallantan Freittan Oatsmatian	V _{CE(SAT)}	I _{OUT} = 100 mA	_	_	1.1	_	_	1.1	V
Collector–Emitter Saturation Voltage		I _{OUT} = 200 mA	_	_	1.3	_	_	1.3	V
ronage		I _{OUT} = 350 mA	-	_	1.6	_	_	1.6	V
Input Voltage	V _{IN(1)}		2.2	_	-	3.3	_	-	V
Imput voltage	V _{IN(0)}		-	_	1.1	-	_	1.7	V
Input Resistance	R _{IN}		50	_	_	50	-	_	kΩ
Serial Data Output Voltage	V _{OUT(1)}	I _{OUT} = -200 μA	2.8	3.05	_	4.5	4.75	-	V
Serial Data Output Voltage	V _{OUT(0)}	I _{OUT} = 200 μA	_	0.15	0.3	_	0.15	0.3	V
Maximum Clock Frequency ²	f _c		10	_	_	10	_	_	MHz
	I _{DD(1)}	One output on, OE = L, ST = H	_	_	2.0	_	_	2.0	mA
Logic Supply Current	I _{DD(0)}	All outputs off, OE = H, ST = H, P1 through P8 = L	-	_	100	_	_	100	μΑ
Clamp Diode Leakage Current	I _r	V _r = 50 V	-	_	50	-	_	50	μΑ
Clamp Diode Forward Voltage	V _f	I _f = 350 mA	-	_	2	-	_	2	V
Output Enable-to-Output Delay	t _{dis(BQ)}	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	-	_	1.0	-	_	1.0	μs
Output Enable-to-Output Delay	t _{en(BQ)}	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	_	_	1.0	_	_	1.0	μs
Strobe-to-Output Delay	t _{p(STH-QL)}	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	_	_	1.0	_	_	1.0	μs
Strobe-to-Output Delay	t _{p(STH-QH)}	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	-	_	1.0	_	_	1.0	μs
Output Fall Time	t _f	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	-	_	1.0	_	_	1.0	μs
Output Rise Time	t _r	V _{CC} = 50 V, R1 = 500 Ω, C1≤30 pF	-	_	1.0	-	_	1.0	μs
Clock-to-Serial Data Out Delay	t _{p(CH-SQX)}	I _{OUT} = ±200 μA	-	50	-	-	50	-	ns

¹Positive (negative) current is defined as conventional current going into (coming out of) the specified device pin.

Truth Table

Serial		Shift Register Contents	Serial		Latch Contents	Output	Output Contents
Data	Clock		Data	Strobe		Enable	
Input	Input	l ₁ l ₂ l ₃ l ₈	Output	Input	l ₁ l ₂ l ₃ l ₈	Input	l ₁ l ₂ l ₃ l ₈
Н		H R ₁ R ₂ R ₇	R ₇				
L	」」	L R ₁ R ₂ R ₇	R ₇				
Х	"	$R_1 R_2 R_3 R_8$	R ₈				
		X X X X	Χ	┙	R ₁ R ₂ R ₃ R ₈		
		P ₁ P ₂ P ₃ P ₈	P ₈	Н	P ₁ P ₂ P ₃ P ₈	L	P ₁ P ₂ P ₃ P ₈
					X X X X	Н	ннн н

L = Low Logic Level H = High Logic Level R = Previous State OE = Output Enable

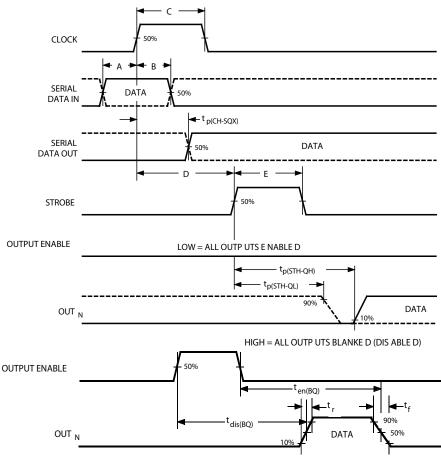
X = Irrelevant P = Present State ST = Strobe



²Operation at a clock frequency greater than the specified minimum value is possible but not warranteed.

Timing Requirements and Specifications

(Logic Levels are V_{DD} and Ground)



Key	Description	Symbol	Time (ns)
Α	Data Active Time Before Clock Pulse (Data Set-Up Time)	t _{su(D)}	25
В	Data Active Time After Clock Pulse (Data Hold Time)	t _{h(D)}	25
С	Clock Pulse Width	t _{w(CH)}	50
D	Time Between Clock Activation and Strobe	t _{su(C)}	100
E	Strobe Pulse Width	t _{w(STH)}	50

NOTE: Timing is representative of a 10 MHz clock. Higher speeds may be attainable; operation at high temperatures will reduce the specified maximum clock frequency.

Powering-on with the inputs in the low state ensures that the registers and latches power-on in the low state (POR).

Serial Data present at the input is transferred to the shift register on the logical 0 to logical 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUT-PUT. The SERIAL DATA must appear at the input prior to the rising edge of the CLOCK input waveform.

Information present at any register is transferred to the respective latch when the STROBE is high (serial-to-parallel conversion). The latches will continue to accept new data as long as the STROBE is held high. Applications where the latches are bypassed (STROBE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

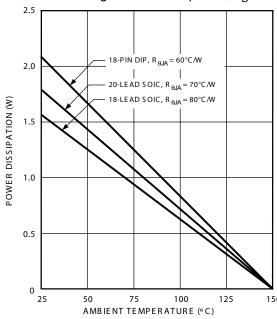
When the OUTPUT ENABLE input is high, all of the output buffers are disabled (OFF). The information stored in the latches or shift register is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.



Terminal List Table

Name	Description	Pin			
Name	Description	18-pin	20-pin		
VEE	Power Ground to substrate	1, 9	1, 9		
CLK	Clock	2	2		
DATA IN	Serial Data In	3	3		
GND	Logic Ground	4	4		
V _{DD}	Logic Supply	5	5		
DATA OUT	Serial Data Out, for cascading devices	6	6		
ST	Strobe	7	7		
ŌĒ	Output Enable (active low)	8	8		
К	Common to +V _L , for inductive loads	10	12		
NC	Not connected	_	10, 11		
OUT ₈	Sink Output 8	11	13		
OUT ₇	Sink Output 7	12	14		
OUT ₆	Sink Output 6	13	15		
OUT ₅	Sink Output 5	14	16		
OUT ₄	Sink Output 4	15	17		
OUT ₃	Sink Output 3	16	18		
OUT ₂	Sink Output 2	17	19		
OUT ₁	Sink Output 1	18	20		

Allowable Package Power Dissipation, PD

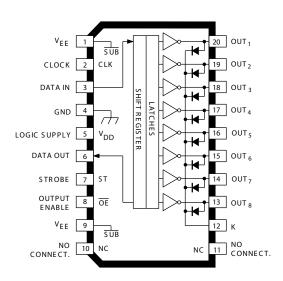




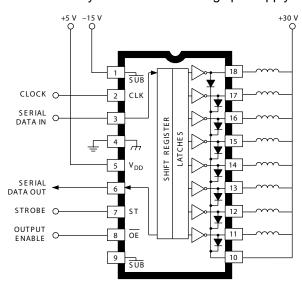
Package LW (18-pin Wide Body SOIC) Package A (18-pin DIP) 18 OUT 1 CLK SERIAL 16 OUT₃ REGISTER LATCHES LOGIC GROUND LOGIC SUPPLY SHIFT SERIAL 13 OUT₆ DATA OUT 12 OUT₇ STROBE 7 OUTPUT ENABLE 11 OUT₈ 10 V_{EE} [

Note the 18-pin DIP package and the SOIC packages are electrically identical and share common terminal number assignments.

Package LW[TBD] (20-pin Wide Body SOIC)

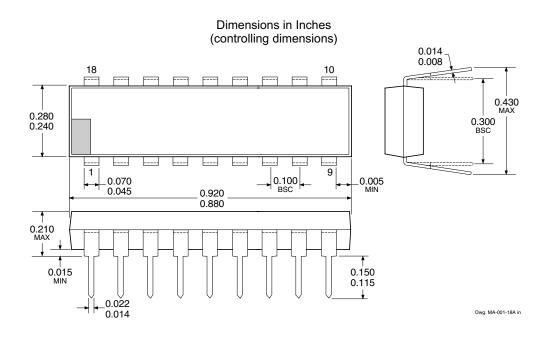


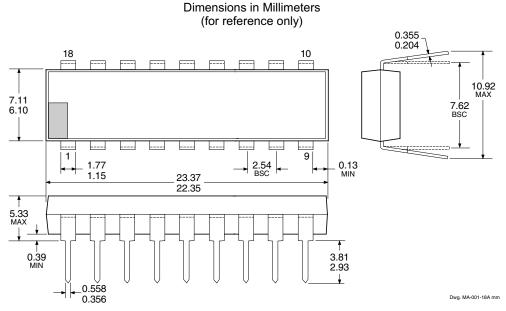
Typical Application Relay/solenoid driver using split supply





Package A 18-pin DIP



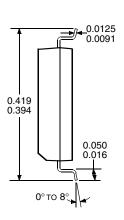


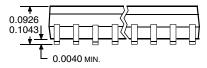
- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 - 2. Lead spacing tolerance is non-cumulative.
 - 3. Lead thickness is measured at seating plane or below.



Package LW 18-pin Wide Body SOIC

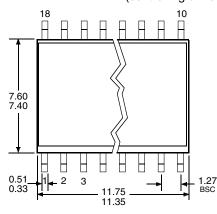
Dimensions in Inches (for reference only) 18 10 0.2992 0.2914 0.020 0.013 0.4625 0.4469 0.050 0.050 0.0469

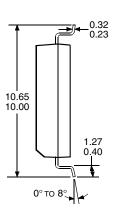


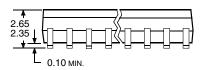


Dwg. MA-008-18A in

Dimensions in Millimeters (controlling dimensions)







Dwg. MA-008-18A mm

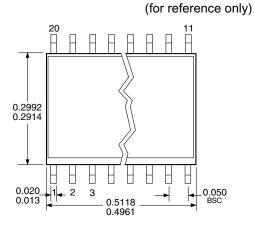
NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.

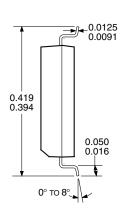
2. Lead spacing tolerance is non-cumulative.

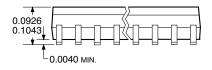


Package LW-20 20-pin Wide Body SOIC

Dimensions in Inches

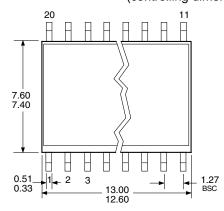


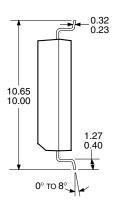


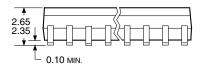


Dwg. MA-008-20 in

Dimensions in Millimeters (controlling dimensions)







- NOTES: 1. Exact body and lead configuration at vendor's option within limits shown.
 - 2. Lead spacing tolerance is non-cumulative.



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