## DESCRIPTION

The A7122 is a high efficiency synchronous, buck DC/DC converter. Its input voltage range is from 2.6V to 6V and provides an adjustable regulated output voltage from 0.6V to $V_{IN}$ while delivering up to 2A of output current.

The internal synchronous switches increase efficiency and eliminate the need for an external Schottky diode. It runs at a fixed 3MHz frequency, which allows the use of small inductor with L<1uH while maintaining a high efficiency and small output voltage ripple.

When Mode pin is connected to GND, the A7122 is operating in PFM/PWM auto-switch mode which enhance the efficiency at light-load.

The A7122 is available in DFN8(2x2) and SOT-25 packages.

## FEATURES

- Adjustable Output Voltage, $V_{FB}$=0.6V
- Maximum output current is 2A
- Range of operation input voltage: Max 6V
- Standby current: 30uA (typ.)
- Line regulation: 0.1%/V (typ.)
- Load regulation: 10mV (typ.)
- High efficiency, up to 96%
- Environment Temperature: -20°C~85°C
- Available in DFN8(2x2) and SOT-25 Packages

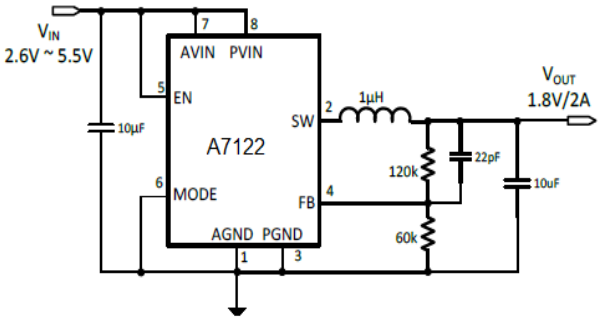
## APPLICATION

- Power Management for 3G modem
- Smart Phone
- Tablet PC
- Set Top Box
- Other Battery Powered Device

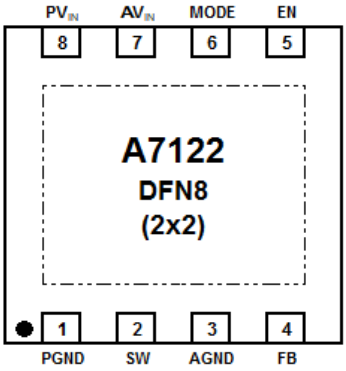
## ORDERING INFORMATION

| Package Type | Part Number | |
|---|---|---|
| DFN8(2x2) | J8 | A7122J8R |
| | | A7122J8VR |
| SOT-25 | E5 | A7122E5R |
| | | A7122E5VR |
| Note | R: Tape & Reel<br>V: Halogen free Package | |
| AiT provides all RoHS products<br>Suffix " V " means Halogen free Package | | |

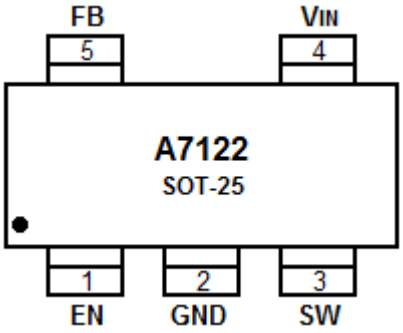
## TYPICAL APPLICATION



## PIN DESCRIPTION




Top View




Top View

| Pin # | | Symbol | Function |
|---|---|---|---|
| DFN8(2X2) | SOT-25 | | |
| 1 | - | PGND | Power Ground. Bypass with a 10μF ceramic capacitor to $PV_{IN}$ |
| 2 | 3 | SW | Inductor Connection. Connect an inductor Between SW and the regulator output. |
| 3 | - | AGND | Analog Ground, Connect to PGND |
| 4 | 5 | FB | Feedback Input. Connect an external resistor divider from the output to FB and GND to set the output to a voltage between 0.6V and $V_{IN}$ |
| 5 | 1 | EN | Enable pin for the IC. Drive this pin to high to enable the part, low to disable. |
| 6 | - | MODE | When forced high, the device operates in fixed frequency PWM mode. When forced low, it enables the Power Save Mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated. |
| 7 | - | $AV_{IN}$ | Analog Power. Short externally to $PV_{IN}$ |
| 8 | - | $PV_{IN}$ | Supply Voltage. Bypass with a 10μF ceramic capacitor to PGND |
| - | 2 | GND | GND |
| - | 4 | $V_{IN}$ | $V_{IN}$ |

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Max Input Voltage | | 6V |
| $T_J$, Max Operating Junction Temperature | | 125°C |
| $T_A$, Ambient Temperature | | -20°C to 85°C |
| $\theta_{JC}$, Package Thermal Resistance | DFN8(2X2) | 25°C/W |
| Power Dissipation | SOT-25 | 250mW |
| $T_S$, Storage Temperature | | -40°C to 150°C |
| Lead Temperature & Time | | 260°C, 10S |
| HBM, ESD | | >2000V |

Stress beyond above listed “Absolute Maximum Ratings” may lead permanent damage to the device. These are stress ratings only and operations of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Input Voltage Range | Max. 6V |
| $T_J$, Operating Junction Temperature | -20°C to 125°C |

## ELECTRICAL CHARACTERISTICS

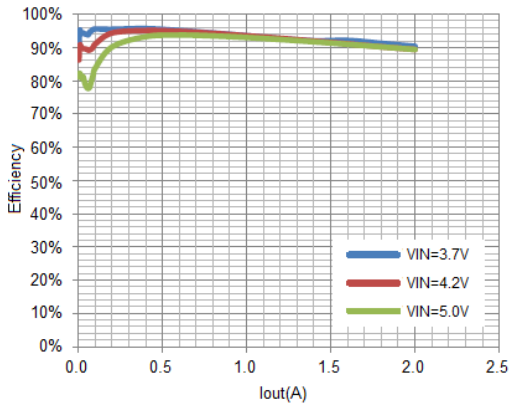
$V_{IN}$=5V, $T_A$=25°C

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{DD}$ | | 2.6 | | 6.0 | V |
| Input Under Voltage Lockout | UVLO | Increase $V_{IN}$ | 2.1 | 2.2 | | V |
| Feedback Voltage | $V_{REF}$ | $V_{IN}$=5V, $V_{EN}$=5V | 0.588 | 0.6 | 0.612 | V |
| Feedback Leakage current | $I_{FBLK}$ | | | 0.01 | 0.1 | uA |
| Quiescent Current | $I_Q$ | Active, $V_{FB}$=0.65V, No Switching | | 30 | | uA |
| | | Shutdown | | 0.1 | 1 | uA |
| Line Regulation | LnReg | $V_{IN}$=2.7V to 5.5V | | 0.04 | | %/V |
| Load Regulation | LdReg | $I_{OUT}$=0.1 to 2A | | 0.15 | | %/A |
| Switching Frequency | $F_{SOC}$ | | 2.4 | 3 | 3.6 | MHz |
| PMOS Rdson | $R_{DSON}P$ | $I_{SW}$=200mA | | 100 | 120 | mΩ |
| NMOS Rdson | $R_{DSON}N$ | $I_{SW}$=200mA | | 80 | 100 | mΩ |
| Peak Current Limit | $I_{LIMIT}$ | | 2.5 | 3 | | A |
| SW Leakage Current | $I_{SWLK}$ | $V_{OUT}$=5.5V, EN=GND | | | 10 | uA |
| EN/MODE High Threshold | $V_{ENH}$, $V_{MDH}$ | | | | 1.5 | V |
| EN/MODE Low Threshold | $V_{ENL}$, $V_{MDL}$ | | 0.4 | | | V |
| EN/MODE Leakage Current | $I_{ENLK}$, $I_{MDLK}$ | EN=MODE=GND | | | 1 | uA |
| Discharge Resistance | $R_{DISCHARGE}$ | EN=GND | 180 | 300 | 450 | Ω |

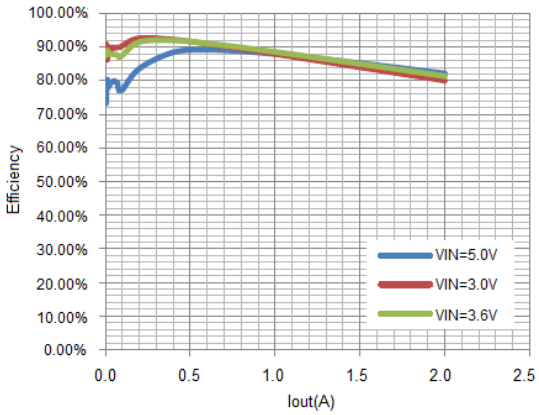
## TYPICAL PERFORMANCE CHARACTERISTICS

($V_{IN}$=3.6V, L=1uH, $C_{IN}$=10uF, $C_{OUT}$=10uF, $T_A$=25°C, unless otherwise stated)

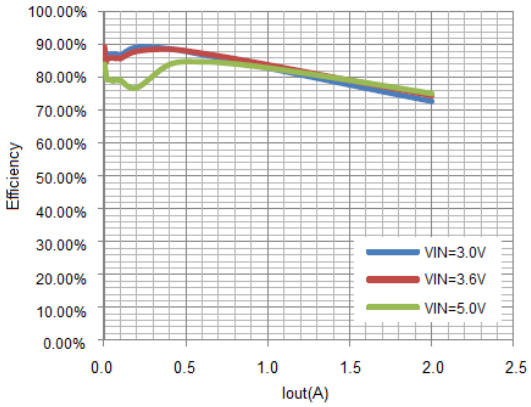
1. Efficiency at $V_{OUT}$=3.3V



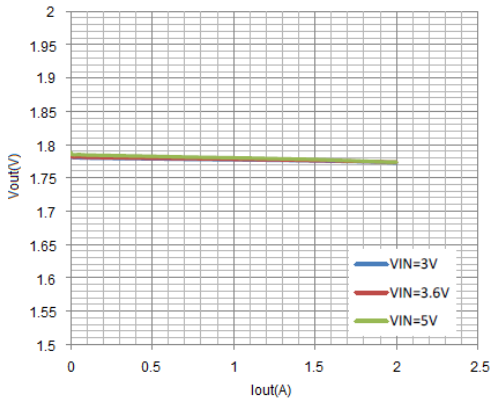

2. Efficiency at $V_{OUT}$=1.8V




3. Efficiency at $V_{OUT}$=1.2V

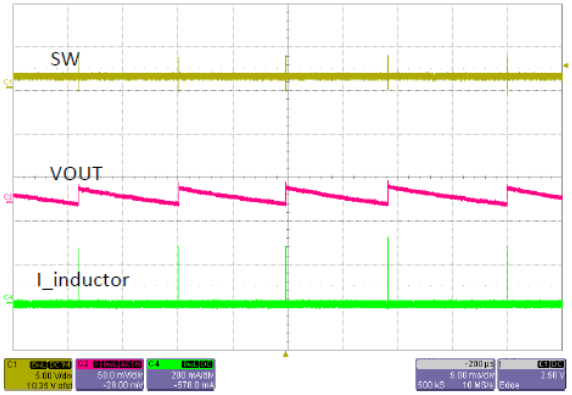



4. Load Regulation at $V_{OUT}$=1.8V



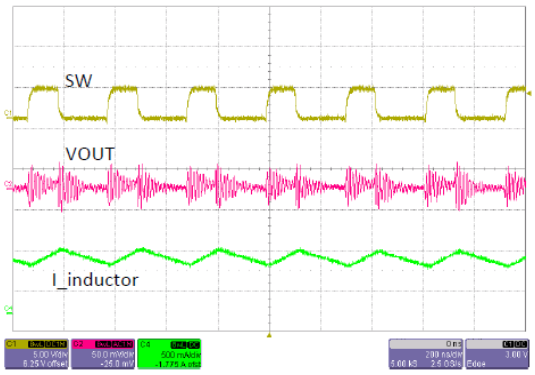

5. Switching waveform

$V_{IN}$=3.6V, $V_{OUT}$=1.2V $I_{OUT}$=0A



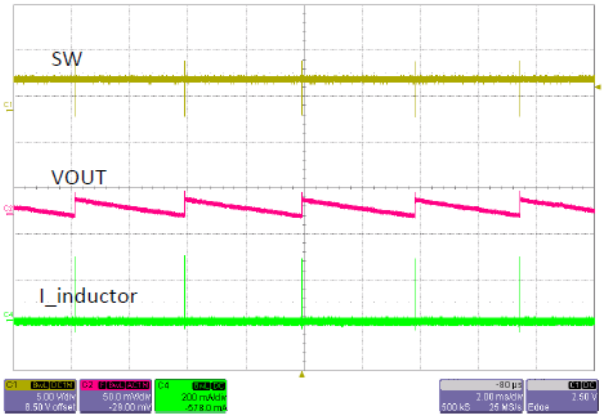

6. Switching waveform

$V_{IN}$=3.6V, $V_{OUT}$=1.2V $I_{OUT}$=0.7A



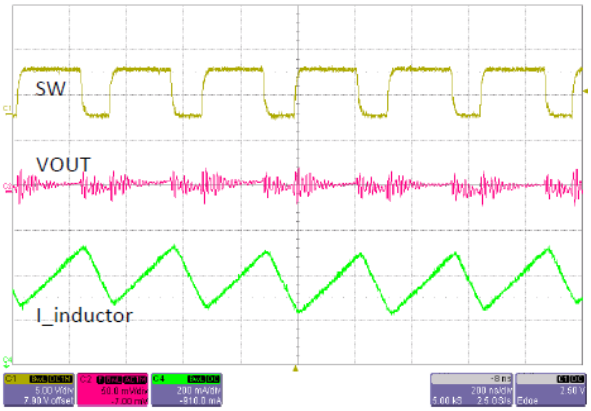
7. Switching waveform

$V_{IN}$=5V, $V_{OUT}$=3.3V, $I_{OUT}$=0A



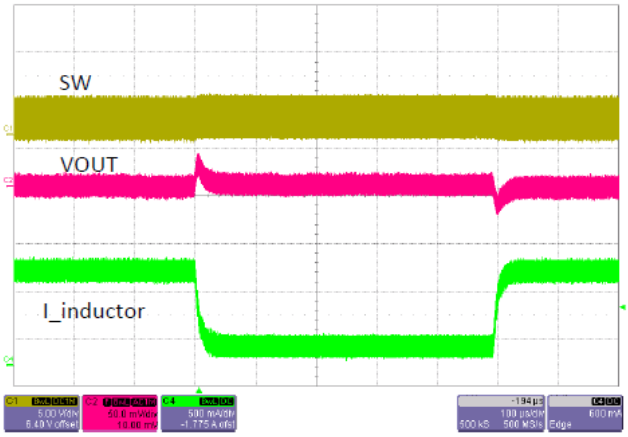

8. Switching waveform

$V_{IN}$=5V, $V_{OUT}$=3.3V, $I_{OUT}$=0.5A



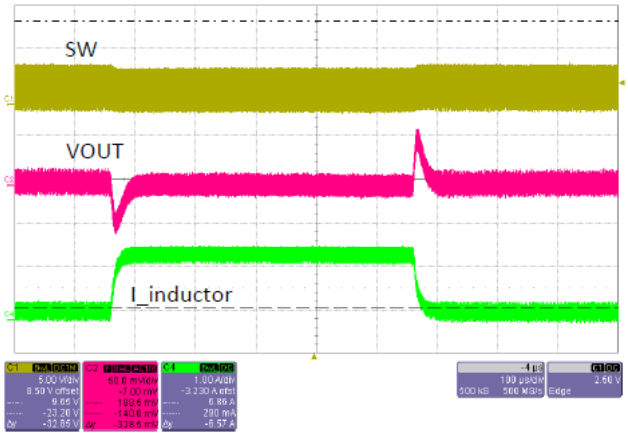

9. Load Transient

$V_{IN}$=3.6V, $V_{OUT}$=1.2V, $I_{OUT}$=0.2A/1A

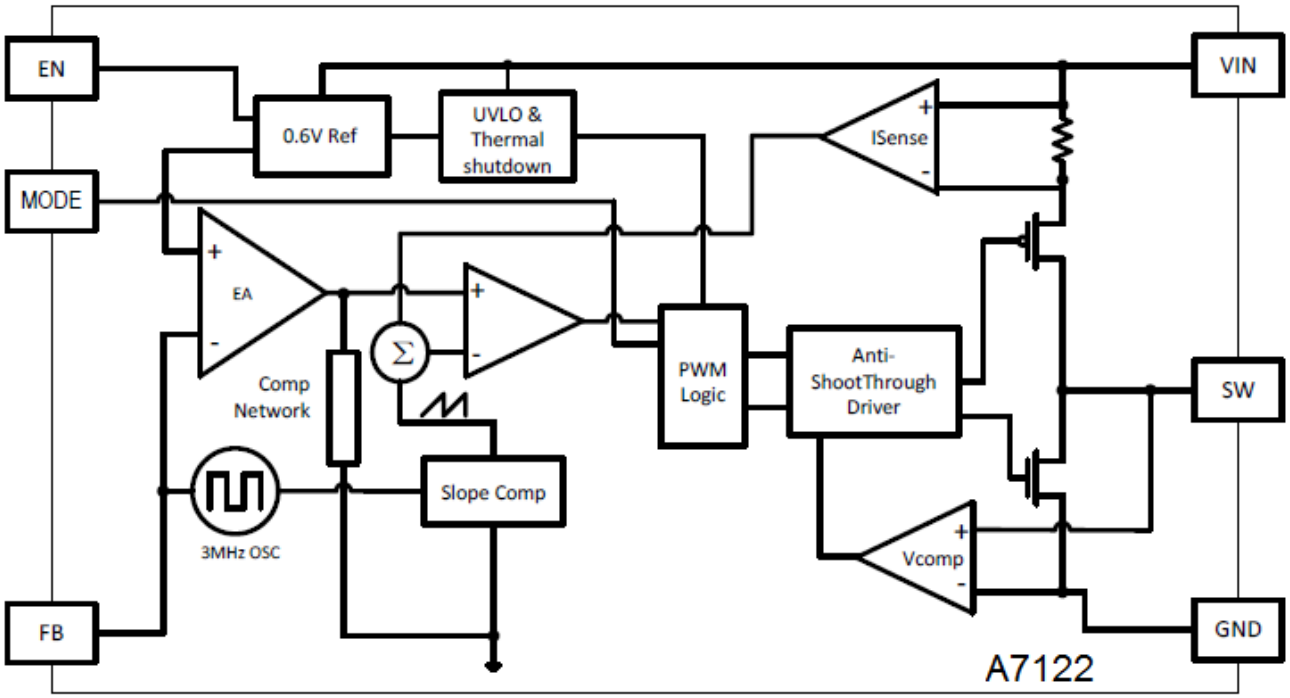



10. Load Transient

$V_{IN}$=3.6V, $V_{OUT}$=1.8V, $I_{OUT}$=0.2A/1.5A



## BLOCK DIAGRAM



## DETAILED INFORMATION

### Functional Descriptions

The A7122 high efficiency switching regulator is a small, simple, DC-to-DC step-down converter capable of delivering up to 2A of output current. The device operates in pulse-width modulation (PWM) at 3MHz from a 2.6V to 5.5V input voltage and provides an output voltage from 0.6V to $V_{IN}$, making the A7122 ideal for on-board post-regulation applications. An internal synchronous rectifier improves efficiency and eliminates the typical Schottky free-wheeling diode. Using the on resistance of the internal high-side MOSFET to sense switching currents eliminates current-sense resistors, further improving efficiency and cost.

### Loop Operation

A7122 uses a PWM current-mode control scheme. An open-loop comparator compares the integrated voltage-feedback signal against the sum of the amplified current-sense signal and the slope compensation ramp. At each rising edge of the internal clock, the internal high-side MOSFET turns on until the PWM comparator terminates the on cycle. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in the inductor. The current mode feedback system regulates the peak inductor current as a function of the output voltage error signal. During the off cycle, the internal high-side P-channel MOSFET turns off, and the internal low-side N-channel MOSFET turns on. The inductor releases the stored energy as its current ramps down while still providing current to the output.

### Current Sense

An internal current-sense amplifier senses the current through the high-side MOSFET during on time and produces a proportional current signal, which is used to sum with the slope compensation signal. The summed signal then is compared with the error amplifier output by the PWM comparator to terminate the on cycle.

### Current Limit

There is a cycle-by-cycle current limit on the high-side MOSFET. When the current flowing out of SW exceeds this limit, the high-side MOSFET turns off and the synchronous rectifier turns on. A7122 utilizes a frequency fold-back mode to prevent overheating during short-circuit output conditions. The device enters frequency fold-back mode when the FB voltage drops below 200mV, limiting the current to $I_{PEAK}$ and reducing power dissipation. Normal operation resumes upon removal of the short-circuit condition.

### Soft Start

A7122 has a internal soft-start circuitry to reduce supply inrush current during startup conditions. When the device exits under-voltage lockout (UVLO), shutdown mode, or restarts following a thermal-overload event, the l soft-start circuitry slowly ramps up current available at SW.

### UVLO and Thermal Shutdown

If $V_{IN}$ drops below 2V, the UVLO circuit inhibits switching. Once $V_{IN}$ rises above 2.1V, the UVLO clears, and the soft-start sequence activates. Thermal-overload protection limits total power dissipation in the device. When the junction temperature exceeds $T_J$= +160°C, a thermal sensor forces the device into shutdown, allowing the die to cool. The thermal sensor turns the device on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous overload conditions. Following a thermal-shutdown condition, the soft-start sequence begins.

## DESIGN PROCEDURE

### Inductor Selection

The peak-to-peak ripple is limited to 30% of the maximum output current. This places the peak current far enough from the minimum overcurrent trip level to ensure reliable operation while providing enough current ripples for the current mode converter to operate stably. In this case, for 2A maximum output current, the maximum inductor ripple current is 667 mA. The inductor size is estimated as following equation:

$$L_{IDEAL}=(V_{IN(MAX)}-V_{OUT})/I_{RIPPLE}*D_{MIN}*(1/F_{OSC})$$

Therefore,

for $V_{OUT}$=1.8V, the inductor values is calculated to be L = 0.60μH. Choose 1μH

And for $V_{OUT}$ =1.2V, the inductor values is calculated to be L = 0.469μH. Choose 0.47μH

The resulting ripple is

$$I_{RIPPLE}=(V_{IN(MAX)}-V_{OUT})/L_{ACTUAL}*D_{MIN}*(1/F_{OSC})$$

When,

$V_{OUT}$=1.8V, $I_{RIPPLE}$=403mA

$V_{OUT}$=1.2V, $I_{RIPPLE}$=665mA

### Output Capacitor Selection

For most applications a nominal 10μF or 22μF capacitor is suitable. The A7122 internal compensation is designed for a fixed corner frequency that is equal to

$$FC=\frac{1}{2*\pi\sqrt{C_{OUT}*L}} = 50Khz$$

For example, for $V_{OUT}$=1.8V, L=1μH, $C_{OUT}$=10μF, for $V_{OUT}$ =1.2V, L=0.47μH, $C_{OUT}$=22μF

### Setting Output Voltage

Output voltages are set by external resistors. The FB_ threshold is 0.6V.

$$R_{TOP} = R_{BOTTOM} \times [(V_{OUT} / 0.6) - 1]$$

### Guidelines for Input Capacitor and Output Capacitor

The input capacitor in a DC-to-DC converter reduces current peaks drawn from the battery or other input power source and reduces switching noise in the controller. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source. The output capacitor keeps output ripple small and ensures control-loop stability. The output capacitor must also have low impedance at the switching frequency. Ceramic, polymer, and tantalum capacitors are suitable, with ceramic exhibiting the lowest ESR and high-frequency impedance. Output ripple with a ceramic output capacitor is approximately as follows:

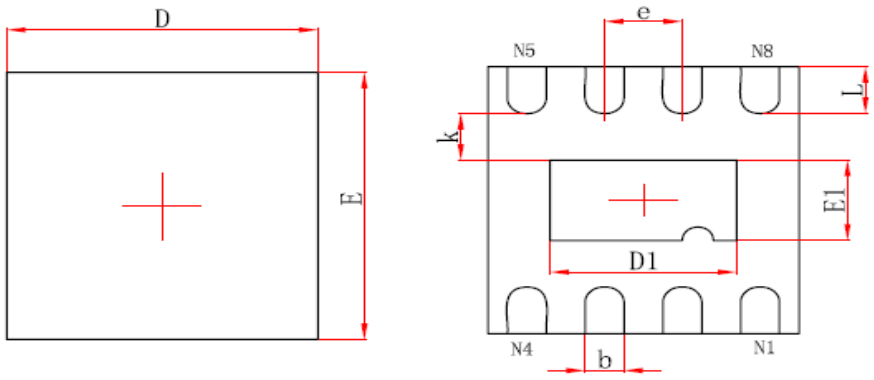
$$V_{RIPPLE} = I_{L(PEAK)}[1 / (2\pi \times f_{OSC} \times C_{OUT})]$$

If the capacitor has significant ESR, the output ripple component due to capacitor ESR is as follows:

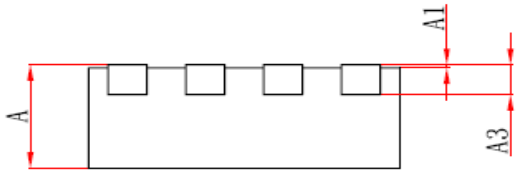
$$V_{RIPPLE(ESR)} = I_{L(PEAK)} \times ESR$$

## PACKAGE INFORMATION

Dimension in DFN8(2x2) (Unit: mm)



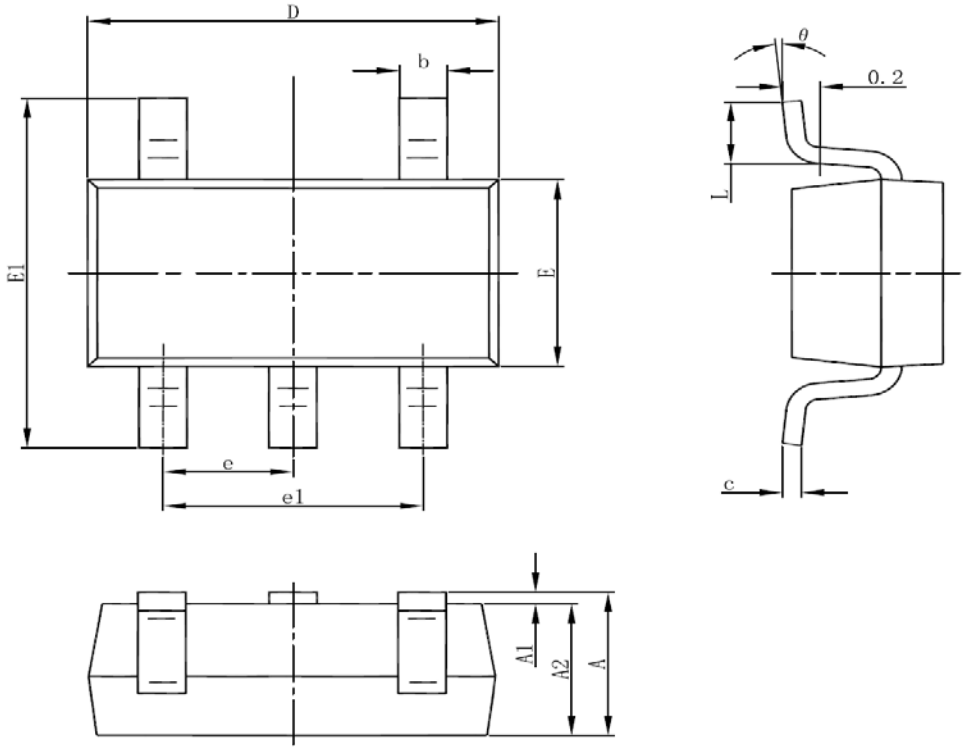

**Top View** **Bottom View**




**Side View**

| Symbol | Min | Max |
|---|---|---|
| A | 0.700 | 0.800 |
| A1 | 0.000 | 0.050 |
| A3 | 0.180 | 0.250 |
| D | 1.900 | 2.100 |
| E | 1.900 | 2.100 |
| D1 | 1.500 | 1.700 |
| E1 | 1.000 | 1.200 |
| k | 0.200MIN. | |
| b | 0.180 | 0.300 |
| e | 0.500(BSC) | |
| L | 0.200 | 0.300 |

Dimension in SOT-25 (Unit: mm)




| Symbol | Min | Max |
|---|---|---|
| A | 1.000 | 1.300 |
| A1 | 0.000 | 0.400 |
| A2 | 0.700 | 0.900 |
| b | 0.300 | 0.500 |
| c | 0.100 | 0.250 |
| D | 2.700 | 3.100 |
| E | 1.500 | 1.800 |
| E1 | 2.500 | 3.100 |
| e | 0.950(BSC) | |
| e1 | 1.700 | 2.100 |
| L | 0.200MIN. | |
| θ | 0° | 8° |

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