Document Title

Mini Power 315/433/480/510/868/915MHz FSK/GFSK Transceiver with 2K ~ 250Kbps

Revision History

Rev. No.	History	Issue Date	Remark
0.0	Initial issue	Sep., 2011	Objective
0.1	Modify description of Ch 12 and Ch 13.	Feb., 2012	Preliminary
0.2	Update specification and A50 application circuit	April, 2012	Preliminary
0.3	Update Figure 13.1, PLLII (02h) and Fdev (06h, page0) formula.	June, 2012	Preliminary

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1. Typical Applications

- ISM Band Data Communication
- Wireless Remote Controller
- RKE (Remote Keyless Entry)
- Building Automation
- Home Security
- Wireless Sensor Networking
- Energy Control and Management
- RKE (Remote Keyless Entry)
- AMR (Auto Metering Reading)

2. General Description

A7129 is a monolithic low-IF architecture CMOS FSK/GFSK TRX for wireless applications in the 315/433/470/510/868/915MHz ISM bands. This device is especially suitable for battery-powered application and the 470MHz ~ 510MHz wireless AMR (Auto Meter Reading) in China and 868.3MHz wireless M-bus in Europe.

A7129 is one of AMICCOM's **Mini Power Family** in sub 1GHz ISM band product line. A7129 is optimized for very low power consumption (i.e. 434MHz band, 3.8mA @ RX mode and 24 mA @ TX mode,10.5dBm). In addition, A7129 can offer a very good link budget with a high efficient class-E power amplifier up to 12 dBm and a low phase noise receiver (-110 dBm RX sensitivity @ 100Kbps / FSK / 433.92MHz). Therefore, A7129 is very suitable for battery powered application with a nice LOS (line-of-sight) wireless range.

A7129 incorporates a baseband modem with the programmable data rate divider from 2K to 250Kbps. For a battery powered system, A7129 supports fast PLL settling time (120 us), Xtal settling time (1100 us) and on-chip Regulator settling time (850 us) to reduce average power consumption. The RF synthesizer contains a VCO and a low noise fractional-N PLL with an output channel frequency resolution of 366 Hz. The VCO frequency operates at to the wanted radio frequency to cover all RF band. Since A7129 is a low-IF architecture TRX with programmable IFBW (IF Filter Bandwidth, 50KHz/100KHz/150KHz/250KHz), the RXLO shall be configured to offset an intermediate frequency (IF) to TXRF regarding to the IFBW setting.

A7129's **control registers** are accessed via 3-wire or 4-wire SPI interface including TX/RF FIFO, VCO frequency, to chip calibration procedures. Another one, via SPI as well, is the unique **Strobe command**, A7129 can be controlled from power saving mode (deep sleep, sleep, idle, standby), PLL mode, TX mode and RX mode. In addition to SPI, the digital connections between A7129 and MCU are GIO1 and GIO2 (multi-function GPIO) to indicate A7129's status so that MCU could use either polling or interrupt for radio control.

For packet handling, A7129 supports direct mode and FIFO mode. In direct mode, MCU or Encoder shall deliver the defined packet (preamble + sync word + payload) to GIO1 or GIO2/TXD pin. Then, in RX mode, MCU or Decoder can receive the coming packet (preamble + sync word + payload) in bit sequence from GIO1 or GIO2/RXD pin.

In FIFO mode, preamble is self-generated by A7129. User just needs to assign the sync word to this device by ID R/W command via SPI. For payload, the built-in separated 64-bytes TX/RX FIFO are used to be this purpose to let user R/W the wanted payload. User can also enable additional packet features like CRC for error detection, FEC (hamming 7 by 4) for 1-bit data correction per code word, Manchester coding, as well as data whitening for data encryption / decryption.

Additional device features such as on-chip regulator, RSSI for clear channel assessment, a thermal sensor, low battery detector, carrier detect, preamble detect, frame sync in FIFO mode, auto-ack and auto-resend, AIF (Auto IF function), AFC (Auto Frequency compensation), Auto calibration (VCO, IF Filter), PLL/CLK Generator, on-chip compensated capacitors of Xtal loading, and WOR (Wake on RX) to support the ability to periodically wake up from sleep mode to RX mode and listen for incoming packets without MCU interaction, can be used to simplify system development and cost. Overall, A7129's highly integrated features and low current consumption offer a reduced BOM cost for a high performance ISM bands product. All features are integrated in a small QFN 4X4 24 pins package.

3. Features

- Small size (QFN 4X4, 24 pins).
- Frequency band: 315/433/470/510/868/915 MHz.
- FSK and GFSK modulation.
- Programmable data rate from 2Kbps to 250Kbps.
- Programmable TX power level from – 40 dBm to 12 dBm.
- On chip regulator, supports input voltage 1.8 ~ 3.6 V.
- Deep sleep current (0.5uA).
- Sleep current (1.5 uA).

- Ultra Low Current Consumption
  - RX Current consumption (AGC Off) 434MHz: 3.8mA.
  - RX Current consumption (AGC Off) 868MHz: 4.4mA.
  - TX Current consumption 433MHz: 24mA @ 10.5dBm.
  - TX Current consumption 868MHz: 24mA @ 10dBm.
- Fast PLL settling time (120 us).
- Supports low cost crystal (12.8 / 16 / 19.2 MHz).
- AGC (Auto Gain Control) for the wide RSSI dynamic range.
- Programmable IF filter bandwidth (50KHz / 100KHz / 150KHz / 250KHz).
- High RX sensitivity, i.e. 433.92MHz.
  - -117dBm at 2Kbps on-air data rate.
  - -112dBm at 50Kbps on-air data rate.
  - -110dBm at 100Kbps on-air data rate.
- Easy to use
  - Support 3-wire or 4-wire SPI.
  - Unique Strobe command via SPI.
  - AGC ON with 9-bits RSSI.
  - AGC OFF with 8-bits RSSI.
  - Auto Calibrations (VCO, IF Filter, RSSI).
  - Auto IF function.
  - Auto Frequency Compensation.
  - Auto CRC Filtering.
  - Auto FEC by (7, 4) Hamming code (1 bit error correction / code word).
  - Auto-resend (max 15 cycles).
  - Auto-acknowledgement.
  - Manchester encoding.
  - Programmable carrier sense indicator.
  - Data Whitening for payload encryption and decryption.
  - Separated 64 bytes RX and TX FIFO.
  - Easy FIFO / Segment FIFO / FIFO Extension (up to 16K bytes).
  - Support FIFO mode with frame sync to MCU.
  - Support direct mode with recovery clock output to MCU.
- On chip 8-bits ADC.
- Low Battery indication.
- On-chip low power RC oscillator for WOR (Wake on RX) function.

4. Pin Configurations

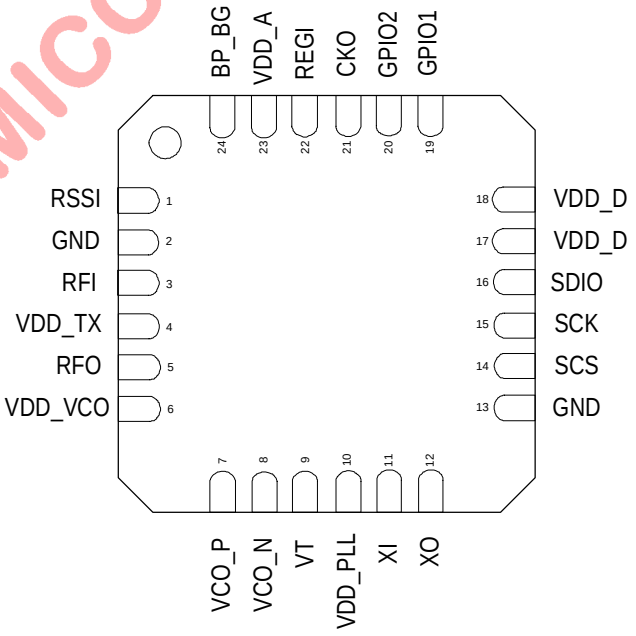


Figure 4.1 QFN4x4 Package Top View

5. RF Chip Block Diagram

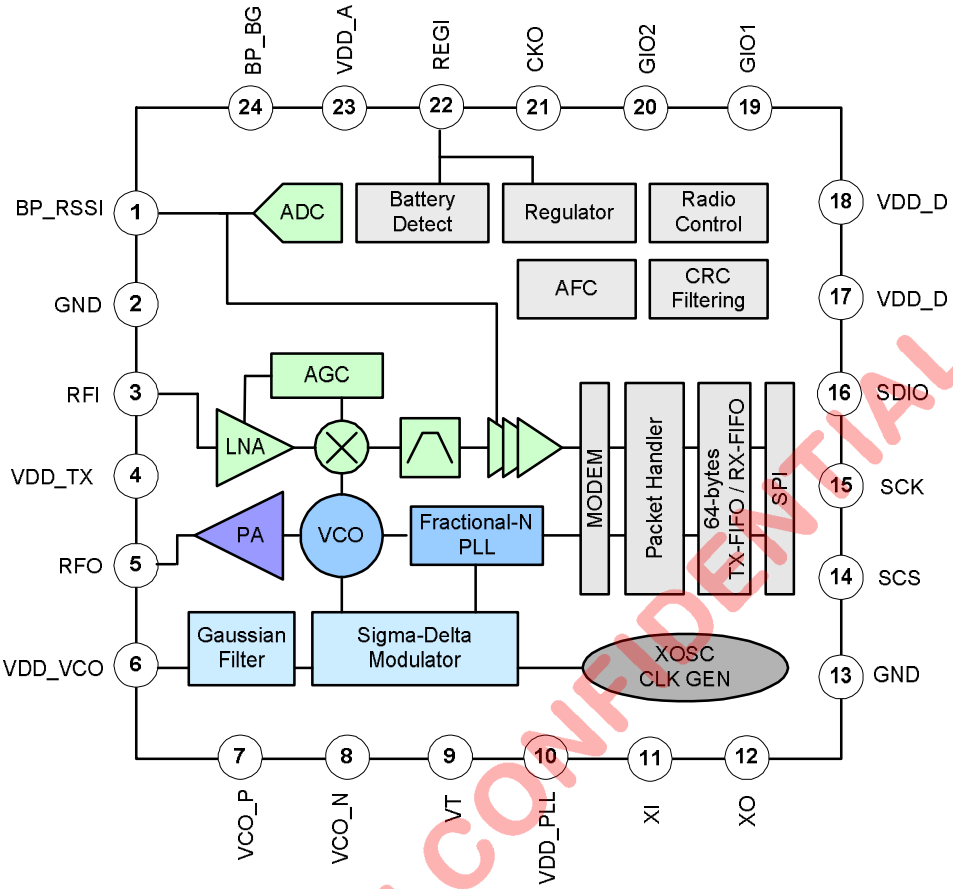


Figure 5.1 System Block Diagram

6. Pin Descriptions

Note: I (input), O(output), G(Ground).

Pin No.	Symbol	I/O	Function Description
1	BP_RSSI	I/O	I: ADC input. O: RSSI bypass. Connect to bypass capacitor.
2	GND	G	Ground.
3	RFI	I	RF input. Connect to matching circuit.
4	VDD_TX	O	TX supply voltage input.
5	RFO	O	RF output. Connect to matching circuit. (recommend powered by VDD directly).
6	VDD_VCO	I	VCO supply voltage input.
7	VCO_P	I	VCO positive pin, connected to external inductor.
8	VCO_N	I	VCO negative pin, connected to external inductor.
9	VT	O	Charge-pump output. Connect to loop filter.
10	VDD_PLL	O	PLL supply voltage input.
11	XI	I	Crystal oscillator input. Connect to tank capacitor.
12	XO	O	Crystal oscillator output. Connect to tank capacitor.
13	GND	O	Digital ground pin.
14	SCS	DI	SPI chip select input.
15	SCK	DI	SPI clock input.
16	SDIO	DI/O	SPI data IO.
17	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.
18	VDD_D	O	Digital supply voltage output. Connect to bypass capacitor.

19	GIO1	DI/O	Multi-function IO 1 / SPI data output.
20	GIO2	DI/O	Multi-function IO 2 / SPI data output.
21	CKO	DO	Multi-function clock output.
22	REGI	I	Regulator input. Connect to VDD supply.
23	VDD_A	O	Analog supply voltage output. Connect to bypass capacitor.
24	BP_BG	O	Band-gap bypass. Connect to bypass capacitor.
	Back side plate	**G**	**Ground. Back side plate shall be well-solder to ground; otherwise, it will impact RF performance.**

7. Absolute Maximum Ratings

Parameter	With respect to	Rating	Unit
Supply voltage range (VDD)	GND	-0.3 ~ 3.6	V
Digital IO pins range	GND	-0.3 ~ VDD+0.3	V
Voltage on the analog pins range	GND	-0.3 ~ 2.1	V
Max. Input RF level		10	dBm
Storage Temperature range		-55 ~ 125	°C
ESD Rating	HBM	± 2K	V
	MM*	± 100	V

*Stresses above those listed under “Absolute Maximum Rating” may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

*Device is ESD sensitive. Use appropriate ESD precautions. HBM (Human Body Mode) is tested under MIL-STD-883F Method 3015.7. MM (Machine Mode) is tested under JEDEC EIA/JESD22-A115-A.
*Device is Moisture Sensitivity Level III (MSL 3).

8. Specification

(Ta=25℃, **VDD=3.3V**, F_{XTAL} =12.8MHz, FSK modulation with Matching circuit and low pass filter)

Parameter	Description	Min.	Typ.	Max.	Unit
General					
Operating Temperature		-40		85	°C
Supply Voltage		1.8	3.3	3.6	V
Current Consumption	Deep Sleep Mode (no register retention) [1]		0.5		uA
	Sleep Mode (WOR Off) [1]		1.5		uA
	Sleep Mode (WOR On) [1]		2.5		uA
	Idle Mode(Xtal off)		0.08		mA
	Standby Mode(Xtal on)		0.45		mA
Current Consumption 434MHz band	PLL mode		2		mA
	RX mode (AGC Off)		3.8		mA
	TX -40dBm (TBG=0, TDC=0, PAC=0)		TBD		mA
	TX 9dBm (TBG=x, TDC=x, PAC=x)		TBD		mA
	TX 10.5dBm (TBG=7, TDC=0, PAC=1)		24		mA
	TX 12dBm (TBG=7, TDC=3, PAC=3)		TBD		mA
Current Consumption 470MHz ~ 510MHz band (without LPF)	PLL mode		2		mA
	RX mode (AGC Off)		3.9		mA
	TX -40dBm (TBG=0, TDC=0, PAC=0)		TBD		mA
	TX 9dBm (TBG=x, TDC=x, PAC=x)		TBD		mA
	TX 11dBm (TBG=5, TDC=1, PAC=1)		24		mA
	TX 13 dBm (TBG=7, TDC=3, PAC=3)		TBD		mA
Current Consumption 868MHz band	PLL mode		2.5		mA
	RX mode (AGC Off)		4.4		mA
	TX -40dBm (TBG=0, TDC=0, PAC=0)		TBD		mA
	TX 10dBm (TBG=7, TDC=1, PAC=1)		24		mA
	TX 11.5dBm (TBG=7, TDC=3, PAC=3)		TBD		mA
Phase Locked Loop					
X'TAL Settling Time	Couple=0, low current		1.1		ms
X'TAL frequency	Data rate (2K/10K/50K/100K/150Kbps)		**12.8**/16/19.2		MHz
	Data rate (250Kbps)		16		MHz
	Data rate (32.768Kbps / 16.384Kbps)		12.582912		MHz
	Data rate (38.4Kbps / 19.2Kbps / 9.6Kbps)		19.6608		MHz
X'TAL ESR				100	Ohm
X'TAL Capacitor Load (Cload)	Recommend		20		pF
434MHz PLL Phase noise (loop component: R1=8.2K,C1=22nF,C2=150pF)	PN @100KHz offset		85		dBc/Hz
	PN @500KHz offset		105		dBc/Hz
	PN @1MHz offset		110		dBc/Hz
480MHz PLL Phase noise (loop component: R1=8.2K,C1=22nF,C2=150pF)	PN @100KHz offset		85		dBc/Hz
	PN @500KHz offset		105		dBc/Hz
	PN @1MHz offset		110		dBc/Hz
868MHz PLL Phase noise (loop component: R1=8.2K,C1=22nF,C2=150pF)	PN @100KHz offset		83		dBc/Hz
	PN @500KHz offset		101		dBc/Hz
	PN @1MHz offset		108		dBc/Hz
PLL Settling Time	Standby to PLL		120		μs

@settle to ± 7.5kHz					
Transmitter					
TX Power Range	480MHz	-40	10	13	dB
TX Power Range	868MHz	-40	10	11	dB
TX Settling Time	PLL to TX		70		μs
TX Spurious Emission 1. Pout = 10 dBm 2. with LPF	f < 1GHz (RBW =100kHz)			-36	dBm
	47MHz< f <74MHz 87.5MHz< f <118MHz 174MHz< f <230MHz 470MHz< f <862MHz (RBW =100kHz)			-54	dBm
	Above 1GHz (RBW = 1MHz)			-30	dBm
	2nd Harmonic			-30	dBm
	3rd Harmonic			-30	dBm
Receiver					
IF Frequency	50K Mode		100		KHz
	100K Mode		200		
	150K Mode		300		
	250K Mode		500		
IF Filter Bandwidth	50K Mode		50		KHz
	100K Mode		100		
	150K Mode		150		
	250K Mode		250		
434MHz RX Sensitivity [2] @BER=0.1% high gain mode	10kbps (IFBW = 50KHz, Fdev = 18.75KHz)		-117		dBm
	50kbps		-112		dBm
	100kbps		-110		
	150kbps		TBD		
	250kbps		TBD		
480MHz RX Sensitivity [2] @BER=0.1% high gain mode (without LPF)	2kbps (IFBW = 50KHz, Fdev = 8KHz)		-120		dBm
	2kbps (IFBW = 100KHz, Fdev = 8KHz)		-118		dBm
	10kbps (IFBW = 50KHz, Fdev = 18.75KHz)		-118		dBm
	10kbps (IFBW = 100KHz, Fdev = 37.5KHz)		-117		dBm
	50kbps (Fdev = 18.75KHz)		-112		dBm
	100kbps (Fdev = 37.5KHz)		-110		
	150kbps (Fdev = 56.25KHz)		-106		
	250kbps (Fdev = 93.75KHz, Xtal = 16MHz)		-102		
868MHz RX Sensitivity [2] @BER=0.1% high gain mode	2kbps (IFBW = 50KHz, Fdev = 8KHz)		-115		dBm
	2kbps (IFBW = 100KHz, Fdev = 8KHz)		-112		dBm
	10kbps (IFBW = 50KHz, Fdev = 18.75KHz)		-110		dBm
	10kbps (IFBW = 100KHz, Fdev = 37.5KHz)		-111		dBm
	50kbps (Fdev = 18.75KHz)		-107		dBm
	100kbps (Fdev = 37.5KHz)		-105		
	150kbps (Fdev = 56.25KHz)		TBD		
	250kbps (Fdev = 93.75KHz)		TBD		
915MHz RX Sensitivity [2] @BER=0.1% high gain mode	50kbps		-106		dBm
	100kbps		-103		
	150kbps		-102		
	250kbps		-100		
Interference (470MHz, 100Kbps)	Co-channel		-6		dB
	ACR1 (C/I_{ch1})		27		dB
	ACR2 (C/I_{ch2})		41		dB

	Offset ± 10MHz		50		dB
	Image (C/I_{IM})		26		dB
RX Spurious	25MHz ~ 1GHz			-57	dBm
	Above 1GHz			-47	dBm
Max Operation Input Power	@ RF input (BER = 0.1%)			10	dBm
RX Settling Time	PLL to RX		150		µs
	Standby to RX		350		µs
Regulator					
Regulator settling time	Pin 19 connected to 1nF		1		ms
Band-gap reference voltage			0.6		V
Analog Regulator output voltage		1.2	**1.2**	1.5	V
TX regulator output voltage		1.8	**1.8**	2.1	V
Digital Regulator output voltage		1.2	**1.8**	1.8	V
Digital IO DC characteristics					
High Level Input Voltage (V_{IH})		0.8*VDD		VDD	V
Low Level Input Voltage (V_{IL})		0		0.2*VDD	V
High Level Output Voltage (V_{OH})	@I_{OH}= -0.5mA	VDD-0.4		VDD	V
Low Level Output Voltage (V_{OL})	@I_{OL}= 0.5mA	0		0.4	V

Note 1: When digital I/O pins are configured as input, those pins shall NOT be floating but pull either high or low (SCS shall be pulled high only); otherwise, leakage current will be induced.
Note 2: Max Data rate= 50kbps @50K Mode, Max Data rate= 150kbps @150K Mode.

9. Control Register

A7129 chip contains 31 x 16-bit control registers, and can read or write data via simple 3-wire serial interface（SCS, SCK, SDIO）. All control registers are listed below.

9.1 Control Register Table

A d d / N a m e	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h Systemclock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
01h PLL I	W	-	CHI2F	CHI2I	CHF1	CHF0	CHIS	CHFS	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
04h PLL IV	W	TXDBG	EDIVS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	ADCR	VCI	CPS	ISDIV	SDPW2	SDPW1	NSDO	EDI
05h PLLV	W	VICMP	IA14	IA13	IA12	IA11	IA10	IA9	IA8	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
06h PLLVI	W	RFC3	RFC2	RFC1	RFC0	RIC11	RIC10	RIC9	RIC8	RIC7	RIC6	RIC5	RIC4	RIC3	RIC2	RIC1	RIC0
07h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCDNP	CRCINV	PGBS2	PGBS1	PGBS0	RBS	--	XCC	XCP1	XCP0	CGS	XS
08h PA0(TX I)	W	RCDLY2	RCDLY1	RCDLY0	TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
08h PA1(WORI)	W	WAC5	WAC4	WAC3	WAC2	WAC1	WAC0	WSL9	WSL8	WSL7	WSL6	WSL5	WSL4	WSL3	WSL2	WSL1	WSL0
	R	--	--	--	--	--	--	--	--	VBD	-	RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
08h PA2(WOR2)	W	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0	WOR_CD	WN3	WN2	WN1	WN0	WOR_S	RCOSC_E	TSEL	TWSOE	RCOT1	RCOT0
	R	--	--	--	--	--	--	--	--	--	--	--		--	--	--	--
08h PA3(RFI)	W	QCLIM	CDSEL1	CDSEL0	PRRC1	PRRC0	RSM1	RSM0	RAMP1	RAMP0	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RHM7	RHM6	RHM5	RHM4	RHM3	RHM2	RHM1	RHM0	RLM7	RLM6	RLM5	RLM4	RLM3	RLM2	RLM1	RLM0
08h PA4(PM)	W	CST	POWRS	CELS	STS	LVR	--	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
08h PA5(RTH)	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
08h PA6(AGC)	W	EXTL	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0	HDM	AGCE	ERSSM	EXRSI	LGM1	LGM	MGM1	MGM0
	R	--	--	--	--	--	--	--	--	--	--	--	--	LGC1	LGC	MGC1	MGC0
08h PA7(AGC2)	W	RGVA1	RGVA0	RGVT1	RGVT0	LHM1	LHM0	MHM1	MHM0	IGM1	IGM0	CA1	CA0	TXIB1	TXIB0	RSA1	RSA0
	R	--	--	--	--	LHC1	LHC0	MHC1	MHC0	IGC1	IGC0	--	--	--	--	--	--
08h PA8(GPIO)	W	WRCKS	MCNT1	MCNT0	DDPC	G2S3	G2S2	G2S1	G2S0	G2I	G2OE	G1S3	G1S2	G1S1	G1S0	G1I	G1OE
08h PA9(CKO)	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKS3	CKS2	CKS1	CKS0	CKOI	CKOE	SCT
08h PA10(VCB)	W	CDTM1	CDTM0	FEP13	FEP12	FEP11	FEP10	FEP9	FEP8	PKT1	PKT0	PKS	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
	R	--	--	--	--	--	--	--	--	--	--	--	VCCF	VCB3	VCB2	VCB1	VCB0
08h PA11(CHG1)	W	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
	R	--	--	--	--	FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
08h PA12(CHG2)	W	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
	R	--	--	--	--	FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
08h PA13 FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
08h PA14 Code	W	PML2	IDL1	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL0	PML1	PML0
08h PA15 WCAL	W	--	--	--	--	--	MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0	MVS1	MVS0	MCALS	MAN	ENCAL
	R	--	--	--	--	--	--	NUMH8	NUMH7	NUMH6	NUMH5	NUMH4	NUMH3	NUMH2	NUMH1	NUMH0	ENCAL
09h PB0 TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
09h PB1 IF1	W	AIF	IFOA14	IFOA13	IFOA12	IFOA11	IFOA10	IFOA9	IFOA8	IFOA7	IFOA6	IFOA5	IFOA4	IFOA3	IFOA2	IFOA1	IFOA0
09h PB2 IF2	W	FPA15	FPA14	FPA13	FPA12	FPA11	FPA10	FPA9	FPA8	FPA7	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0
09h PB3 ACK	W	MRCKS	RNUM3	RNUM2	RNUM1	RNUM0	CDRS1	CDRS0	SYNCS	VKM	VKP	ARTMS	ARC3	ARC2	ARC1	ARC0	EARKS
	R	--	--	--	--	--	--	--	--	--	ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EARKS
09h PB3 PB4 ART	W	RND7	RND6	RND5	RND4	RND3	RND2	RND1	RND0	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
0Ah RX I	W	ETH2	DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	BW1	BW0	ULS	RXDI
0Bh RX II	W	PMD2	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
	R	--	--	--	--	--	--	--	ADCO8	ADCO7	ADCO6	ADCO5	ADCO4	ADCO3	ADCO2	ADCO1	ADCO0
0Ch	W	ARSSI	RADC	AVSEL1	AVSEL0	MVSEL1	MVSEL0	XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0

ADC	R	PWR	XEM	PLLEM	TRSM	TREM	--	VBD1	VBD0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	WMODE	INFS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MFBS	MFB3	MFB2	MFB1	MFB0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
0Fh Modecontrol	W	DFCD	VBS	SWT	RSSC	VCC	CCE	WWSE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
	R	--	WWSE	CCER	RSSC	VCC	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM

Legend: -- = unimplemented

9.2 Control Register Description

9.2.1 System clock (Address: 00h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h System clock	W	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
	R	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0	GRS	GRC4	GRC3	GRC2	GRC1	GRC0	CSC2	CSC1	CSC0
Reset		0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

SDR[6:0]: Data Rate Divider.

$$Data\ rate = \frac{1}{128} \cdot \frac{f_{system}}{SDR[6:0]+1}$$ where Fsystem is system clock.

If DMOS (0Ah) = 0, $$Data\ rate = \frac{1}{128} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$$ (recommended).

If DMOS (0Ah) = 1, $$Data\ rate = \frac{1}{64} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$$

GRS: Reference Clock Selection for the internal CLK Generator.
[0]: PLL CLK Gen. = F_{CGRF} x 48, where F_{CGRF} is from below GRC divider
[1]: PLL CLK Gen. = F_{CGRF} x 32

GRC[4:0]: Generation Reference Clock Divider.
GRC [4:0] is the clock divider to generate a PFD clock for the internal CLK Generator.

$$f_{CGRF} = \frac{f_{xtal}}{GRC[4:0]+1}$$

CSC[2:0]: System Clock Divider setting.
CSC is the clock divider of F_{MSCK} to generate the wanted data clock and IF calibration clock where F_{MSCK} is either from Xtal itself (CGS = 0) or from the internal CLK Generator (CGS = 1).

$$f_{CSCK} = \frac{f_{MSCK}}{CSC[2:0]+1}$$

F_{CSCK} shall be set appropriately, otherwise, IF Filter calibration will be failure.

Please refer to chapter 12 for details.

9.2.2 PLL I (Address: 01h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01h PLL I	W		CHI1	CHI0	CHF1	CHF0	CHIS	CHFS	IP8	IP7	IP6	IP5	IP4	IP3	IP2	IP1	IP0
Reset										1	0	0	0	0	0	0	0

CHI[1:0]: Reserved. CHI shall be [00].

CHF[1:0]: charge-pump current setting for fractional-N synthesizer. Recommend CHF = [01].
[00]: 48uA
[01]: 96uA
[10]: 192uA
[11]: 384uA

CHIS: Reserved. CHIS shall be [0].

CHFS: Fractional-N Charge Pump Current Scale. Recommend CHFS = [1].
[0]: normal fractional-N synthesizer Charge-pump current
[1]: fractional-N synthesizer charge-pump current scale(x2)

IP[8:0]: LO frequency Integer Part setting.

Pease refer to Chapter 13 for detail.

9.2.3 PLL II (Address: 02h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
02h PLL II	W	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FP[15:0]: LO Frequency Fractional Part setting.

$$f_{\mathrm{LO\_BASE}} = f_{PFD} \cdot (IP[8:0] + \frac{FP[15:0]}{2^{16}}) \quad \text{(unit: Hz)}$$

where $f_{\mathrm{LO\_BASE}}$, the base frequency of VCO

where $f_{\mathrm{PFD}} = f_{Xtal} \div (RFC[3:0]+1)$, the comparison frequency of RF_PLL.

A7129's RF frequency is implemented by an offset scheme regarding to the below formula.

The wanted RF frequency is equal to VCO frequency, $F_{RF} = F_{VCO} = F_{LO\_BASE} + F_{OFFSET}$.

where f_{OFFSET}, the offset frequency of VCO is set by FPA [15:0] (09h, page 2) $f_{\mathrm{OFFSET}} = f_{PFD} \cdot (\frac{FPA[15:0] \cdot 2^6}{2^{16}})$

Please refer to Chapter 13 for details.

9.2.4 PLL III (Address: 03h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
03h PLL III	W	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
	R	AFC	MC14	MC13	MC12	MC11	MC10	MC9	MC8	MC7	MC6	MC5	MC4	MC3	MC2	MC1	MC0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AFC: Auto Frequency Compensation selection.
[0]: manual
[1]: auto

MC[14:0]: PLL Fractional Part Compensation value.
[Write]：Manual setting to LO fractional part compensation value when AFC = [0].
[Read]：Frequency offset value when AFC = [1].

9.2.5 PLL IV (Address: 04h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
04h PLL IV	W	TXDBG	EDIVS	CKX2	MD1	PDL2	PDL1	PDL0	MD0	ADCR	VCI	CPS	ISDIV	SDPW1	SDPW	NSDO	EDI
Reset				0	0	0	1	1	0	0	0	1	0	0	0	0	0

TXDBG: TX Debug mode. TXDBG shall be [0].
[0]: Disable
[1]: Enable

EDIVS: Synthesizer Selection. EDIVS shall be [0].
[0]: Fractional-N PLL
[1]: Reserved

MD1: RF Band select.
[0]: Low band (310MHz ~ 510MHz)
[1]: High band (860MHz ~ 930MHz)

CKX2: Reserved. CKX2 shall be [0].

MD0: LO Buffer current select.
[0]: Low current
[1]: High current

PDL[2:0]: PLL Settling Delay Time setting.

PDL [2:0]	PLL Delay Timer	Note
000	20 us	
001	40 us	
010	60 us	
011	80 us	Recommend
100	100 us	
101	120 us	
110	140 us	
111	160 us	

ADCR: Reserved. ADCR should be= [0].

VCI: VCO current calibration test bit. Reserved. VCI shall be [0].

CPS: Charge Pump tri-state setting. Recommend CPS = [1].
[0]: Tri-state.
[1]: Normal operation.

ISDIV: Divider current test bit. Recommend ISDIV = [0].
[0]: low current.
[1]: high current.

SDPW[1:0]: Pulse Width of sigma-delta modulator. SDPW shall be [00].

NSDO: Mash sigma delta order setting. Recommend NSDO = [0].
[0]: order 2. **[1]:** order 3.

EDI: Dither Noise setting. Recommend EDI = [0].
[0]: Disable. **[1]:** Enable.

9.2.6 PLL V (Address: 05h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
05h PLL V	W	VICMP	IA14	IA13	IA12	IA11	IA10	IA9	IA8	IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VICMP: Reserved. VICMP shall be [0].

IA[14:0]: Reserved. IA shall be [0x0000].

9.2.7 PLL VI (Address: 06h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
06h PLL VI	W	RFC3	RFC2	RFC1	RFC0	RIC11	RIC10	RIC9	RIC8	RIC7	RIC6	RIC5	RIC4	RIC3	RIC2	RIC1	RIC0
Reset		0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1

RFC[3:0]: R-Counter for Fractional-N PLL
RFC is used to divide crystal frequency for the comparison frequency of the Franc-N PLL by
F_{PFD} = Fxtal / (RFC[3:0]+1)

RIC[11:0]: Reserved. RIC shall be [0x000]

9.2.8Crystal (Address: 07h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCDNP	CRCINV	PGBS2	PGBS1	PGBS0	-	-	XCC	XCP1	XCP0	CGS	XS
Reset		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

PGAS[3:0]: Page selector for the 08h register.

CRCDNP: CRC Mode Select.
[0]: CRC-CCITT ($X^{16}+X^{12}+X^5+1$).
[1]: CRC-DNP ($X^{16}+X^{13}+X^{12}+X^{11}+X^{10}+X^8+X^6+X^5+X^2+1$).

CRCINV: CRC Inverted Select.
[0]: disable. **[1]:** enable

PGBS[2:0]: Page selector for the 09h register.

XCC: Crystal Current setting.
[0]: Low current. **[1]:** High current.

XCP[1:0]: Crystal Regulating Couple setting. Recommend XCP =[00].

CGS: Clock Generation Selection.
[0]: Disable, F_{MSCK} = Xtal freq.
[1]: Enable, F_{MSCK} = CLK Generator. Please refer to chapter 12 for details.

XS: Crystal Oscillator Selection. Recommend XS = [1].
[0]: Disable **[1]:** Enable

9.2.9 TX I (Address: 08h) Page 0

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h TX I	W	RC_DLY2	RC_DLY1	RC_DLY0	TME	GS	FDP2	FDP1	FDP0	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
Reset		0	0	0	1	0	1	0	1	0	1	0	0	0	0	0	0

RC_DLY[2:0]: RSSI calibration RL Delay setting. Recommend RC_DLY= [000]
[000]: 100us. **[001]:** 300us. **[010]:** 500us. **[011]:** 700us.
[100]: 900us. **[101]:** 1.1ms. **[110]:** 1.3ms. **[111]:** 1.5ms.

TME: TX Modulation Enable.
[0]: Disable.
[1]: Enable.

GS: Gaussian Filter Selection.
[0]: Disable.
[1]: Enable.

FDP[2:0]: Frequency Deviation Exponential Coefficient setting.

FD[7:0]: TX Frequency Deviation setting.

For both Gaussian filter is enabled (GS =1) or disabled（GS = 0）：

$$f_{dev} = 2 \cdot f_{PFD} \cdot FD[7:0] \cdot \frac{2^{FDP[2:0]}}{2^{19}} \quad \text{(unit: Hz)}$$

where $f_{PFD} = f_{Xtal} \div (RFC[3:0]+1)$, is the comparison frequency of RF_PLL.

Note2: please refer to Chapter 13 for details.

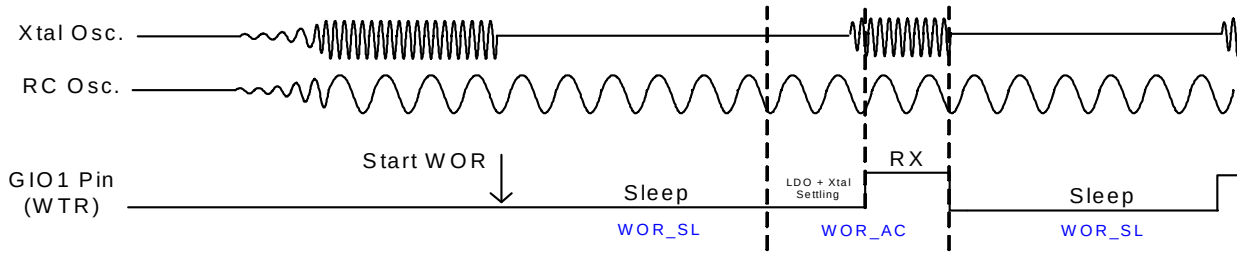
9.2.9.1 WOR I (Address: 08h) Page1

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h TX I	W	WAC5	WAC4	WAC3	WAC2	WAC1	WAC0	WSL9	WSL8	WSL7	WSL6	WSL5	WSL4	WSL3	WSL2	WSL1	WSL0
	R									VBD		RCOC5	RCOC4	RCOC3	RCOC2	RCOC1	RCOC0
Reset		0	0	0	0	0	0	0	0	0		0	0	0	0	0	0

WOR_AC [5:0]: 6-bits WOR Active Period.
WOR Active Period = (WOR_AC[5:0]+1) x (1/4092), (244us ~ 15.6ms).

WOR_SL [9:0]: 10-bits WOR Sleep Period.

WOR Sleep Period = (WOR_SL[9:0]+1) x (1/4092), (7.8ms ~ 7.99s).



VBD: Battery Detection flag (Read Only).
[0]: Battery Low.
[1]: Battery High.

RCOC[5:0]: RC Oscillator Calibration value (Read Only).

9.2.9.2 WOR II (Address: 08h) Page 2

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h WOR II	W	RSSC_D1	RSSC_D0	RS_DLY2	RS_DLY1	RS_DLY0	WOR_CD	WN3	WN2	WN1	WN0	WOR_S	RCOSC_E	TSEL	TWSOE	RCOT1	RCOT0
Reset		0	0	0	0	1	0	0	0	0	0	0	1	0	1	0	0

RSSC_D [1:0]: RSSI calibration Delay setting. Recommend RSSC_D = [00].
[00]: 10us. **[01]:** 20us. **[10]:** 30us. **[11]:** 40us.

RS_DLY [2:0]: RSSI Measurement Delay while in RX mode. Recommend RS_DLY = [000].
[000]: 10us. **[001]:** 20us. **[010]:** 30us. **[011]:** 40us. **[100]:** 50us. **[101]:** 60us. **[110]:** 70us. **[111]:** 80us.

WOR_CD: Wake up MCU select.

WN[3:0]: The number of RX wake up times.
Wake up times = (WN[3:0] + 1).

WOR_S: Wake up MCU select.

[WOR_CD, WOR_S]	Wake up MCU select.
[00]	By Frame Sync OK
[01]	By preamble Detect OK.
[1x]	By carrier detect OK.

RCOSC_E: RC Oscillator for WOR or TWOR.
[0]: Disable. **[1]:** Enable.

TSEL: TWOR Duty select.
[0]: Use WOR_AC [5:0]. (where WOR_AC is located in 08h, page 1)
[1]: Use WOR_SL [9:0]. (where WOR_SL is located in 08h, page 1)

TWSOE: Wake up MCU Mode select.
[0]: By WOR mode. Wake up MCU while receiving a packet.
[1]: By TWOR mode. Wake up MCU by TWOR timer.

RCOT [1:0]: RC Oscillator current setting. Recommend RCOT = [00].

9.2.9.3 RF Current (Address: 08h) Page 3

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h RFI	W	QCLIM	CD SEL1	CD SEL0	PRRC1	PRRC0	RSM1	RSM0	RMP1	RMP0	TRT2	TRT1	TRT0	ASMV2	ASMV1	ASMV0	AMVS
	R	RHM7	RHM6	RHM5	RHM4	RHM3	RHM2	RHM1	RHM0	RLM7	RLM6	RLM5	RLM4	RLM3	RLM2	RLM1	RLM0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

QCLIM: Reserved. Shall be [0].

CDSEL [1:0]: Carrier Detect select by GIO1S.
If GIO1S is set to be [0010], Carrier Detect scheme has below tree options.
[0X]: RSSI Carrier Detect.
[10]: In-band Carrier Detect.
[11]: RSSI Carrier Detect plus In-band Carrier Detect.

PRRC [1:0]: Reserved. PRRC shall be [10].

RSM [1:0]: RSSI Margin. Recommend RSM = [01].
RSM = (RTH – RTL).
[00]: 5. **[01]:** 10. **[10]:** 15. **[11]:** 20.

RMP [1:0]: PA Ramp up/down Timing Scale setting.
[00]: 1. **[01]:** 2. **[10]:** 4. **[11]:** 8.

TRT [2:0]: TX Ramp down discharge current select. Recommend TRT =[111].

ASMV [2:0]: TX Ramp up Timing Select. Recommend ASMV =[111].
[000]: 2us, **[001]:** 4us. **[010]:** 6us. **[011]:** 8us. **[100]:** 10us, **[101]:** 12us. **[110]:** 14us. **[111]:** 16us.

Actual TX ramp up time = ASMV [2:0] x RMP[1:0]

AMVS : PA Ramp Up Enable. Recommend AMVS = [1].
[0]: Disable. **[1]:** Enable.

RHM [7:0]: RSSI calibration high threshold level (Read Only).

RLM [7:0]: RSSI calibration low threshold (Read Only).

9.2.9.4 Power Manage (Address: 08h) Page 4

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h PM	W	CST	POWRS	CELS	STS	LVR	--	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
Reset		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CST: DC average length selection. CST shall be [0].
[0]: DC average length unchanged. **[1]:** DC average length halves.

POWRS: Reserved. Shall be [0].

CELS: Reserved. Shall be [0].

STS: Reserved. Shall be [0].

LVR: Reserved. Shall be [0].

RGC[1:0]: Reserved. Recommend RGC = [01].

SPSS: Mode Back select if WOR is enabled. Recommend SPSS = [0].
[0]: Standby mode. **[1]:** PLL mode.

RGV [1:0]: Digital Regulator Voltage select. Recommend RGV = [11].
[00]: 1.2V
[01]: 1.4V
[10]: 1.6V
[11]: 1.8V

QDS: VDD_A Quick Discharge select. Recommend QDS = [1].
[0]: Normal. **[1]:** Quick discharge.

BVT [2:0]: Battery Voltage Threshold select.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BDS: Battery Detection selection.
[0]: Disable. **[1]:** Enable.

9.2.9.5 AGC RSSI Threshold (Address: 08h) Page 5

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h RTH	W	IRTH7	IRTH6	IRTH5	IRTH4	IRTH3	IRTH2	IRTH1	IRTH0	IRTL7	IRTL6	IRTL5	IRTL4	IRTL3	IRTL2	IRTL1	IRTL0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IRTH[7:0]: AGC high Threshold. Recommend IRTH = [0x07].

IRTL[7:0]: AGC low Threshold. Recommend IRTL = [0x04].

If ADC ≤ IRTL. DVT[1:0] (0Eh) = 11.

If ADC ≥ IRTH. DVT[1:0] (0Eh) = 00.
If IRTL ≤ ADC ≤ IRTH. DVT[1:0] (0Eh) = 01.

9.2.9.6 AGC Control(Address: 08h) Page 6

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h AGC	W	EXTL	VRSEL	MS	MSCL4	MSCL3	MSCL2	MSCL1	MSCL0	HDM	AGCE	ERSSM	EXRSI	LGM1	LGM0	MGM1	MGM0
	R	--	--	--	--	--	--	--	--	--	--	--	--	LGC1	LGC0	MGC1	MGC0
Reset		--	--	0	0	0	0	0	0	0	0	0	0	1	1	1	1

EXTL: VCO Calibration test bit. EXTL shall be [0].

VRSEL: AGC Function select.
[0]: RSSI AGC. **[1]:** wideband AGC.

MS: AGC Manual Scale select. Recommend MS = [0].
[0]: Auto (RL−RH).
[1]: Manual by MSCL[4:0].

MSCL[4:0]: AGC Manual Scale setting.

HDM: AGC HOLD select.
[0]: No hold.
[1]: Hold Gain Switching when ID is sync.

AGCE: Auto Gain Control Enable.
[0]: Disable. **[1]:** Enable.

ERSSM : Ending mode for RSSI measurement. Recommend ERSSM = [0].
[0]: RSSI value frozen before leaving RX.
[1]: RSSI value frozen when valid frame sync (ID and header check ok).

EXRSI: Reserved. EXRSI shall be [0].

LGM [1:0]: LNA Gain Attenuation select. Recommend LGM = [00].
[00]: -12dB. **[01]:** -6dB. **[10]:** Max. **[11]:** Reserved.

MGM [1:0]: Mixer Gain Attenuation select. Recommend MGM = [00].
[00]: -18dB. **[01]:** -12dB. **[10]:** -6dB. **[11]:** Max.

LGC[1:0]: LNA Gain Check (Read Only).

MGC[1:0]: Mixer Gain Check (Read Only).

9.2.9.7 AGC Control II(Address: 08h) Page 7

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h AGC2	W	RGVA1	RGVA0	RGVT1	RGVT0	LHM1	LHM0	MHM1	MHM0	IGM1	IGM0	CA1	CA0	TXIB1	TXIB0	RSAGC1	RSAGC0
	R	--	--	--	--	LHC1	LHC0	MHC1	MHC0	IGC1	IGC0	--	--	--	--	--	--
Reset		--	--	--	--	--	--	--	--	--	--	--	--	0	0	0	0

RGVA[1:0]: Analog Regulator Voltage Select. Recommend RGVA = [11].
[00]: 0.9V
[01]: 1.0V
[10]: 1.1V
[11]: 1.2V

RGVT[1:0]: PA Regulator Voltage Select. Recommend RGVT = [10].
[00]: 1.6V
[01]: 1.8V
[10]: 2.0V
[11]: 2.2V

LHM[1:0]: LNA Current Select. Recommend LHM = [10].
[00]: min.
[01]: mid.
[10]: high
[11]: max

LHC[1:0]: LNA Current Check. (Read only)

MHM[1:0]: Mixer Current Select. Recommend MHM = [10].
[00]: min.

[01]: mid.
[10]: high
[11]: max

MHC[1:0]: Mixer Current Check. (Read only)

IGM[1:0]: BPF Gain Select. Recommend IGM = [11].
[00]: -18dB. **[01]:** -12dB. **[10]:** -6dB. **[11]:** Max.

IGC[1:0]: BPF Gain Check. (Read only)

CA[1:0]: AGC peak detect test bit. CA shall be [00].

TXIB[1:0]: Reserved. TXIB shall be [00].

RSAGC[1:0]: Reserved. RSAGC shall be [00].

9.2.9.8 GPIO (Address: 08h) Page 8

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h GPIO	W	WRCKS	MCNT1	MCNT0	DDPC	GIO2S3	GIO2S2	GIO2S1	GIO2S0	G2I	G2OE	GIO1S3	GIO1S2	GIO1S1	GIO1S0	G1I	G1OE
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

WRCKS: WOR Reference clock select.
[0]: WOR Ref clock when PF8M is equal or close to 6.4MHz.
[1]: WOR Ref clock when PF8M is equal or close to 8MHz.

MCNT[1:0]: Main Clock Divider.

[00]: $f_{MCNT} = f_{MSCK}$

[01]: $f_{MCNT} = f_{MSCK} / 2$

[10]: $f_{MCNT} = f_{MSCK} / 3$

[11]: $f_{MCNT} = f_{MSCK} / 4$

Please refer to Chapter 12 for details.

DDPC (Direct mode data pin control): Direct mode modem data can be accessed via SDIO pin.
[0]: Disable. **[1]:** Enable.

GIO2S [3:0]: GIO2 pin function select.

GIO2S [3:0]	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	External sync input(for direct mode)(only in SCT=0) Preamble Detect Output (PMDO)(only in SCT=1)	
[0100]	TWOR	
[0101]	In phase demodulator input(DMIQ) or DVT[1](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_RX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	VPOAK (Valid Packet or Auto ACK OK Output)	
[1101]	FPF	
[1110]	PDN_TX	
[1111]	FMTDO (FIFO mode TX Data Output testing)	

If GIO2S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A7129 supports to accept an external frame sync signal from MCU to feed to GIO2 pin to determine the timing of fixing DC estimation voltage of demodulator.

G2I: GIO2 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G2OE: GIO2 pin output enable.
[0]: High Z. **[1]:** Enable.

GIO1S [3:0]: GIO1 pin function select.

GIO1S [3:0]	TX state	RX state
[0000]	ARCWTR (Wait until TX or RX finished)	
[0001]	EOAC (end of access code)	FSYNC(frame sync)
[0010]	TMEO(TX modulation enable)	CD(carrier detect)
[0011]	External sync input(for direct mode) Preamble Detect Output (PMDO)	
[0100]	MCU wakeup signal (TWWS) or WTR	
[0101]	Quadrature phase demodulator input (DMII).or DVT[0](AGC)	
[0110]	SDO (4 wires SPI data out)	
[0111]	TRXD In/Out (Direct mode)	
[1000]	RXD (Direct mode)	
[1001]	TXD (Direct mode)	
[1010]	PDN_TX	
[1011]	External FSYNC input in RX direct mode *	
[1100]	VPOAK (Valid Packet or Auto ACK OK Output)	
[1101]	FPF	
[1110]	Battery Detect flag.(BDF)	
[1111]	FMRDI. (FIFO mode RX input for testing)(for internal testing)	

If GIO1S = [1011] and direct mode is selected, the internal frame sync function will be disabled. In such case, A7129 supports to accept an external frame sync signal from MCU to feed to GIO1 pin to determine the timing of fixing DC estimation voltage of demodulator.

G1I: GIO1 pin output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

G1OE: GIO1pin output enable.
[0]: High Z. **[1]:** Enable.

9.2.9.9 CKO (Address: 08h) Page 9

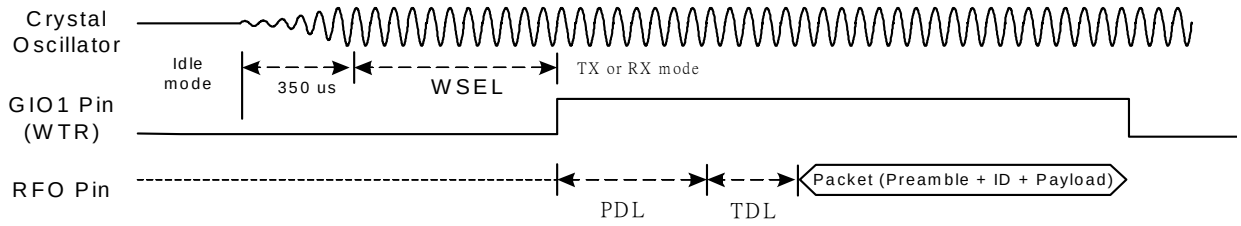
Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h CKO	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKS3	CKS2	CKS1	CKS0	CKOI	CKOE	SCT
Reset		0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

INTXC: Internal Crystal Load selection. Recommend INTXC = [1].
[0]: Use external capacitors. **[1]:** Use on-chip capacitors.

XCL[4:0]: On-chip Crystal Capacitor Load setting.
Set XCL = [10000] as the first value to fine tune the carrier frequency and minimize the frequency drift if Xtal Cload = 20pF.
XCL is active when INTXC=1 and Each XCL step is typical 1.68 pF.
XCL is the on-chip capacitor for Xtal oscillator to fine tune offset frequency of the wanted RF carrier.
Please refer to chapter 11 or contact AMICCOM's FAE.

XCL[4:0]	Xtal C-load (pF)
00000	0
00001	1.68
00010	3.36
…	
11110	50.4
11111	52.08

WSEL[2:0]: Crystal Settling Delay setting (200us ~ 2.5ms). Recommend WSEL = [011].
[000]: 200us. **[001]:** 400us. **[010]:** 600us. **[011]:** 800us.
[100]: 1ms. **[101]:** 1.5ms. **[110]:** 2ms. **[111]:** 2.5ms.



CKOS [3:0]: CKO pin output select.
[0000]: DCK (TX data clock).
[0001]: RCK (RX recovery clock).
[0010]: FPF (FIFO pointer flag for FIFO extension).
[0011]: Logic OR gate by EOP, EOVBC, EOFBC, EOVCC, EOVDC and RSSC_OK. (Internal usage only).
[0100]: BBCK.
[0101]: BBCK.
[0110]: BBCK.
[0111]: RTCIN (RTC timer input).
[1000]: WCK.
[1001]: PF8M (F_{SYCK}).
[1010]: ROSC.
[1011]: EOADC.
[1100]: OKADCN.
[1101]: 0.
[1110]: RTCO (RTC timer output).
[1101]: EOCAL.
[1110]: VPOAK
[1111]: Reserved

CKOI: CKO pin Output signal invert.
[0]: Non-inverted output. **[1]:** Inverted output.

CKOE: CKO pin Output Enable.
[0]: High Z. **[1]:** Enable.

SCT: Reserved. SCT shall be [1].

9.2.9.10 VCO current (Address: 08h) Page 10

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h VCB	CDTM 1	CDTM 0	FEP 13	FEP 12	FEP 11	FEP 10	FEP9	FEP8	CDTM 1	PKT1	PKT0	PKS	VCOC3	VCOC2	VCOC1	VCOC0	MVCS
	-	-	-	-	-	-	-	-	-	-	-	-	VCCF	VCB3	VCB2	VCB1	VCB0
Reset	0	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0

CDTM[1:0]: Carrier detect number of times setting.
[00]: 16. **[01]:** 32 **[10]:** 64. **[11]:**128

PKT[1:0]: VCO Peak Detect threshold test bit. PKT shall be [00].

PKS: VCO Current Calibration Mode Select. Recommend PKS = [0].
[0]: Normal.
[1]: VCO current calibration by peak detection.

VCOC [3:0]: VCO Current Bank Calibration result. Recommend VCOC = [0010].
If SWT = [0] @ 0Fh, then VCOC= [1000].
If SWT = [1] @ 0Fh, then VCOC[3:0] = Manual setting.

MVCS: VCO current calibration select. Recommend MVCS = [0].
[0]: Auto. **[1]:** Manual.

VCCF : VCO Current Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

VCB [3:0]: VCO Current Bank Calibration Value (Read Only).
MVCS= 0: Auto calibration value.
MVCS= 1: Manual calibration value.

9.2.9.11 Channel Group (I) (Address: 08h) Page 11

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h CHG1	W					FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
	R					FPL3	FPL2	FPL1	FPL0	IPL7	IPL6	IPL5	IPL4	IPL3	IPL2	IPL1	IPL0
Reset						0	0	0	0	0	0	0	0	0	0	0	0

FPL [3:0]: VCO Calibration Fractional Part Setting for Low Boundary Channel Group.
Please refer to A7129's reference code for the wanted RF band.

IPL [7:0]: VCO Calibration Integer Part Setting for Low Boundary Channel Group.
Please refer to A7129's reference code for the wanted RF band.

9.2.9.12 Channel Group (II) (Address: 08h) Page 12

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h CHG2	W					FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
	R					FPH3	FPH2	FPH1	FPH0	IPH7	IPH6	IPH5	IPH4	IPH3	IPH2	IPH1	IPH0
Reset						0	0	0	0	0	0	0	0	0	0	0	0

FPH [3:0]: VCO Calibration Fractional Part Setting for High Boundary Channel Group.
Please refer to A7129's reference code for the wanted RF band.

IPH [7:0]: VCO Calibration Integer Part Setting for High Boundary Channel Group.
Please refer to A7129's reference code for the wanted RF band.

9.2.9.13 FIFO (Address: 08h) Page 13

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h FIFO	W	FPM1	FPM0	PSA5	PSA4	PSA3	PSA2	PSA1	PSA0	FEP7	FEP6	FEP5	FEP4	FEP3	FEP2	FEP1	FEP0
Reset		0	1	0	0	0	0	0	0	0	0	1	1	0	1	1	1

FPM [1:0]: FIFO Pointer Margin.
FPM is used in FIFO extension mode for an indicator.

FPM[1:0]	Bytes in TX FIFO	Bytes in RX FIFO
[00]	4	60
[01]	8	56
[10]	12	52
[11]	16	48

PSA [5:0]: Used for Segment FIFO.
Used in FIFO segment mode.

FEP [13:0]: FIFO End Pointer for TX FIFO and Rx FIFO.
Where FEP[13:0] are located at here and FEP[13:8] are located at 08h page 10.
FIFO Length Setting = (FEP [13:0] +1).
For example, if FEP = 0x3F, it means FIFO length is 64 bytes.
For FIFO extension mode, FEP's value shall be set larger than 0x3F.
Please refer to section 16.4.2 for details.

9.2.9.14 Code (Address: 0Ch) Page 14

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h Code	W	PML2	IDL1	WS6	WS5	WS4	WS3	WS2	WS1	WS0	MCS	WHTS	FECS	CRCS	IDL0	PML1	PML0
Reset		0	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1

PML [2:0] (bit 15 / 1 / 0): Preamble Length Select. Recommend PML= [011].
[000]: 1 byte. **[001]:** 2 bytes. **[010]:** 3 bytes. **[011]:** 4 bytes.
[100]: 16 byte. **[101]:** 32 bytes. **[110]:** 48 bytes. **[111]:** 64 bytes.

IDL[1:0] (bit 14 / 2): ID code length setting. Recommend IDL=[01].
IDL [1:0] = [Bit14, Bit2].
[00]: 2 bytes. **[01]:** 4 bytes. **[10]:** 6 bytes. **[11]:** 8 bytes.

WS [6:0]: Data Whitening Seed (data encryption key, only for FIFO mode).

MCS: Manchester Code Enable. (only for FIFO mode)
[0]: Disable. **[1]:** Enable.

WHTS: Data Whitening. (Data Encryption, only for FIFO mode)
[0]: Disable. **[1]:** Enable (The data is whitened by multiplying with PN7).

FECS: FEC Select. (only for FIFO mode)
[0]: Disable. **[1]:** Enable (The FEC is (7, 4) Hamming code).

CRCS: CRC Select. (only for FIFO mode)
[0]: Disable. **[1]:** Enable.

9.2.9.15 WCAL (Address: 08h) Page 15

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h WCAL	W						MRCT5	MRCT4	MRCT3	MRCT2	MRCT1	MRCT0	MVS1	MVS0	MCALS	MAN	ENCAL
	R							NUMH8	NUMH7	NUMH6	NUMH5	NUMH4	NUMH3	NUMH2	NUMH1	NUMH0	ENCAL
Reset							0	0	0	0	0	0	0	0	0	0	0

MRCT[5:0]: Manual setting of RC Timer for WOR mode.

MVS[1:0]: WOR Calibration sample clock select based on CKOT.
[00]: 1/2. **[01]:** 1/4. **[10]:** 1/8. **[11]:** 1/16.

MCALS: WOR Calibration select.
[0]: Continuous mode. **[1]:** Single mode.

MAN: WOR Calibration Manual select.
[0]: Auto
[1]: Manual

ENCAL: WOR Calibration Enable. ENCAL shall be [0] when WOR calibration is finished.
[0]: Disable. **[1]:** Enable.

ENCAL: WOR Calibration Flag (read only).

NUMLH[8:0]: WOR Calibration result. (Read only.)

9.2.10.0 TX II (Address: 09h) Page 0

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
Reset		0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

MCNTR: Divided by 2 select.
[0]: $PF8M = f_{\mathrm{MCNT}} \div 2$ where PF8M is one of baseband clock sources.
[1]: $PF8M = f_{\mathrm{MCNT}}$
where $f_{\mathrm{MCNT}} = f_{MSCK} \div (MCNT[1:0])$, located in 0x08 page 8.
Please refer to Chapter 12 for details.

DPR [2:0]: Scaling of PDL and TDL. Recommend DPR = [000].

BT [1:0]: Moving average for Gaussian filter select.
If GS = [0],
Gaussian filter is disabled, **BT = [00]:** not average. **[01]:** 2 bit average. **[10]:** 4 bit average. **[11]:** 8 bit average
That means BT is used to smooth TX data transition.
If GS = [1],
Gaussian filter is enabled, **BT = [00]:** 2.0. **[01]:** 1.0. **[10]:** 0.5. **[11]:** 0.5
That means BT is used to configure shape of Gaussian filter.

TDL[1:0]:TX Settling Delay select.

TDL [1:0]	TX Delay Timer	Note
00	20 us	Recommend
01	40 us	
10	60 us	
11	80 us	

TXDI: TX data inverted. Recommend TXDI = [0].
[0]: normal. **[1]:** invert

PAC[1:0]: PA current setting.

Please refer to Chapter 8 and A7129 App. Note for programmable TX output power.

TDC[1:0]: TX Driver current setting.

Please refer to Chapter 8 and A7129 App. Note for programmable TX output power.

TBG[2:0]: TX Buffer Gain setting.

Please refer to Chapter 8 and A7129 App. Note for programmable TX output power.

DID [15:0]: Device ID data. (Read Only).

9.2.10.1 IFI (Address: 09h) Page1

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h IFI	W	AIF	IFOA14	IFOA13	IFOA12	IFOA11	IFOA10	IFOA9	IFOA8	IFOA7	IFOA6	IFOA5	IFOA4	IFOA3	IFOA2	IFOA1	IFOA0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

AIF: Auto IF enable.
[0]: disable. **[1]:** enable.

IFOA[14:0]: Auto IF offset frequency setting.
When AIF=1, ULS=0(Up side band): $F_{RXLO} = F_{LO} - IFOA[14:0]$
When AIF=1, ULS=1(Low side band): $F_{RXLO} = F_{LO} + IFOA[14:0]$

9.2.10.2 IFII (Address: 09h) Page2

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h IF II	W	FPA15	FPA14	FPA13	FPA12	FPA11	FPA10	FPA9	FPA8	FPA7	FPA6	FPA5	FPA4	FPA3	FPA2	FPA1	FPA0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FPA[15:0]: LO setting for frequency offset.

$$f_{OFFSET} = f_{PFD} \cdot \left(\frac{FPA[15:0] \cdot 2^6}{2^{16}}\right) \quad \text{(unit: Hz)}$$

Where F_{PFD} = Fxtal / (RFC[3:0]+1)

From PLL II (02h), $f_{LO\_BASE} = f_{PFD} \cdot \left(IP[8:0] + \frac{FP[15:0]}{2^{16}}\right)$ (unit: Hz)

Therefore, VLO frequency $F_{LO} = F_{RF} = F_{LO\_BASE} + F_{OFFSET}$.

Please refer to Ch13 for details.

9.2.10.3 ACK (Address: 09h) Page3

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h TX II	W	MRCKS	RNUM3	RNUM2	RNUM1	RNUM0	CDRS1	CDRS0	SYNCS	VKM	VPM	ARTMS	ARC3	ARC2	ARC1	ARC0	EARKS
	R										ARTEF	VPOAK	RCR3	RCR2	RCR1	RCR0	EARKS
Reset		0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0

MRCKS: Reserved for internal usage only. Shall be set to [0].

RNUM[3:0]:Reserved for internal usage only. Shall be set to [011]..

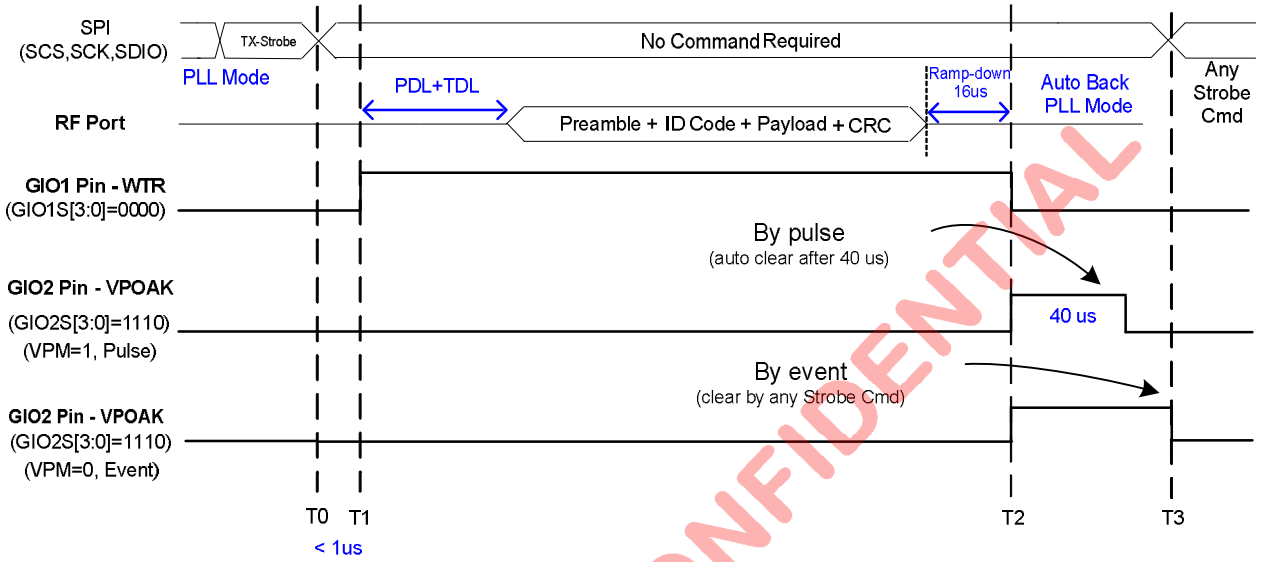
SYNCS: RX demodulation sync word detect type select.
[0]: Sync word detect by re-preamble.
[1]: Sync word detect by using 64bytes buffer.

CDRS[1:0]: Carrier detect range select. Recommend CDRS = [01].
[00]: 8. **[01]:** 16. **[10]:** 24. **[11]:**32 .

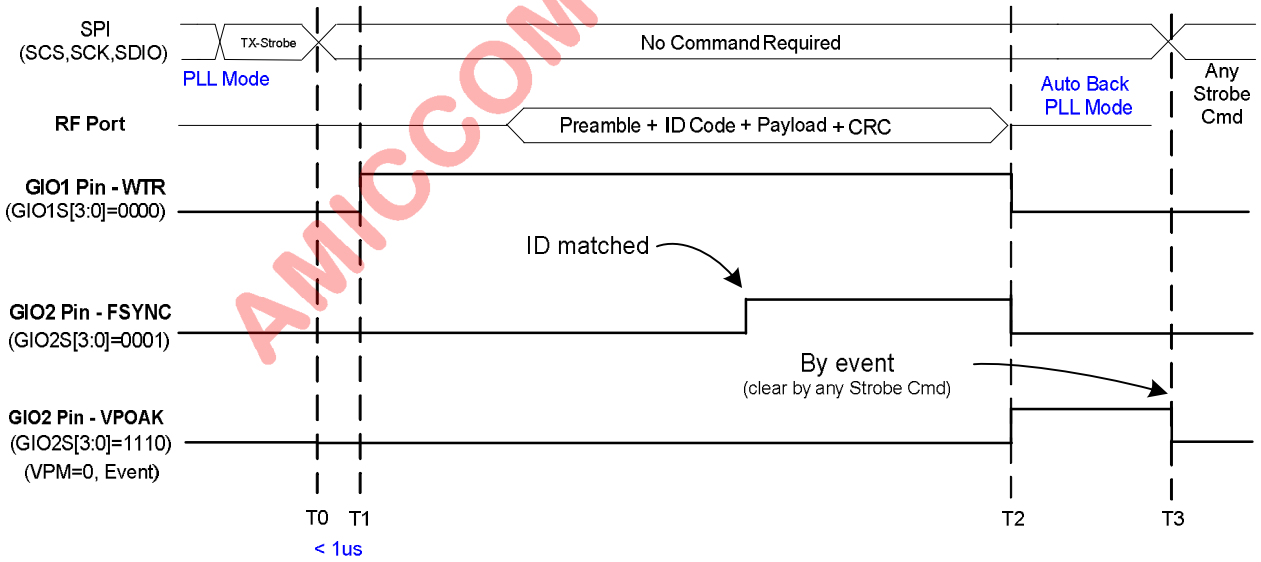
VKM: Valid Packet mode select.
[0]: by event. **[1]:** by pulse.

VPM: Valid Pulse width select.
[0]: 10u. **[1]:** 30u.

TX Mode (**disable** auto-resend, EARKS=0).



RX Mode (**disable** Auto-ack, EAKKS =0).



Note1, If auto-resend is enabled (EAR = 1), WTR behavior is different while it is output to GIO1 and GIO2.
Note2, If auto-ack is enabled (EAK = 1), WTR behavior is different while it is output to GIO1 and GIO2.
Note3, VPOAK's behavior is controlled by VPM (0Bh) and VPW (0Bh).
Refer to chapter 19 for details

ARTMS: Auto-resend Interval select.
[0]: random interval. **[1]:** fixed interval.

ARC [3:0] : Auto-resend Cycle Setting.
[0000]: resend disable.

[0001]: 1 **[0010]:** 2 **[0011]:** 3 **[0100]:** 4 **[0101]:** 5 **[0110]:** 6 **[0111]:** 7
[1000]: 8 **[1001]:** 9 **[1010]:** 10 **[1011]:** 11 **[1100]:** 12 **[1101]:** 13 **[1110]:** 14 **[1111]:** 15

EARKS: Auto-ack or auto-resend enable.
[0]: disable. **[1]:** enable auto-resend (TX) or enable auto-ack (RX)

ARTEF: Auto-resend ending flag (read only).
[0]: Resend on going. **[1]:** Finish resending.

VPOAK: Valid Packet or ACK OK Flag (ready only).
This flag is clear by Strobe Command.
[0]: Neither valid packet nor ACK OK.
[1]: Valid packet or ACK OK.

RCR [3:0]: Auto Resend Cycle Decremented Count (read only).
Decremented of ARC[3:0] during auto-resend.

9.2.10.4 ART (Address: 09h) Page4

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h TX II	W	RND07	RND6	RND5	RND4	RND3	RND2	RND1	RND0	ARD7	ARD6	ARD5	ARD4	ARD3	ARD2	ARD1	ARD0
	R																
Reset		0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1

RND [7:0]: Random seed for auto-resend interval.

ARD[7:0] : Auto Resend Delay
ARD Delay = 200 us * (ARD+1) → (200us ~ 51.2 ms)
Each step is 200 us.
[0000-0000]: 200 us.
[0000-0001]: 400 us.
[0000-0010]: 600 us.
…
…
[1111-1111]: 51.2 ms.

9.2.11 RX I (Address: 0Ah)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ah RX I	W	ETH2	DMT	MPL1	MPL0	SLF2	SLF1	SLF0	ETH1	ETH0	DMOS	DMG1	DMG0	IFBW1	IFBW0	ULS	RXDI
Reset		0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	0

ETH [2:0] (bit 15/8/7): ID code error bit tolerance. Recommend ETH = [001].
ETH [2:0] is located in [Bit15, Bit8, Bit7]
[000]: 0 bit. **[001]:** 1bit. **[010]:** 2 bits. **[011]:** 3 bits. **[100]:** 4 bits. **[101]:** 5 bits. **[110]:** 6 bits. **[111]:** 7 bits.

DMT : Demodulator test bit. DMT shall be [0].
[0]: Normal.
[1]: Test mode.

MPL [1:0]: Symbol recovery loop filter setting after ID SYNC. MPL shall be [01].

SLF [2:0]: Symbol recovery loop filter setting. SLF shall be [100].

DMOS: Demodulator over-sample select. Recommend DMOS = [1].
[0]: x16.
[1]: x32.

DMG [1:0]: Demodulator Gain select. Recommend DMG = [01].
[00]: x1. **[01]:** x3. **[1x]:** x5.

IFBW [1:0]: IF Band Pass Filter select.
[00]: 50KHz. data rate ≦50Kbps. (Xtal shall be chosen ± 10 ppm stability in case of RX sensitivity degradation.)
[01]: 100KHz. 50K < data rate ≦100Kbps.
[10]: 150KHz. 100K < data rate ≦150Kbps.
[11]: 250KHz. 150K < data rate ≦250Kbps.

Since A7129 is a low-IF TRX, on-chip IFBW is implemented with 4 optional Filter Bandwidth.
The IF Filter shall be calibrated after power on reset. In performance point of view, the narrower IFBW results the better RX sensitivity. To make a successful IFBW calibration, an appreciated setting of calibration clock is necessary.

Please refer to Chapter 12 and A7129's reference code for details.

ULS: RX Up/Low side band select. Recommend ULS = [0].
[0]: Up side band, TX A-terminal frequency – IF = RX B-terminal frequency
[1]: Low side band, TX A-terminal frequency + IF = RX B-terminal frequency

RXDI: RX Data Invert. Recommend RXDI = [0].
[0]: normal. **[1]:** inverted.

9.2.12 RX II (Address: 0Bh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Bh RX II	W	PMD2	PMD1	PMD0	DCV7	DCV6	DCV5	DCV4	DCV3	DCV2	DCV1	DCV0	DCL2	DCL1	DCL0	DCM1	DCM0
	R								ADCO 8	ADCO 7	ADCO 6	ADCO 5	ADCO 4	ADCO 3	ADCO 2	ADCO 1	ADCO 0
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PMD[2:0]: Preamble pattern detection. Recommend PMD = [100].
When DCM[1:0] = 01, 10, 11, chip will execute preamble length detection automatically.
[000]: 0 bit
[001]: 4 bits
[010]: 8 bits (Default value)
[011]: 16 bits
[100]: 24 bits.
[101] and [11x]: 32bits.
Remark: detection length setting should be smaller than the setting value of PML[1:0](Code register(0x0C)).

DCV[7:0]: Data DC average value setting. Recommend DCV = [10010].
This setting is only active when DCM (09h) = [00].

DCL[2:0]: Data Length of Peak Detect average setting. Recommend DCL = [010].
DCL[2:0] is used to let A7129 detects n times "0" or n times "1" to result DC estimation voltage of demodulator.

DCL[2:0]	DC average	
	Before ID Sync	After ID Sync
000	4	32
001	8	32
010	16	32
011	32	32
100	4	64
101	8	64
110	16	64
111	32	64

For example,
If DCL[2:0] = 000,
Before ID sync, by peak detect method to update a new DC value for every 4 times 1" and 4 times "0" .
After ID sync, by peak detect method, to update a new DC value for every 32 times "1" and 32 times "0" .

DCM [1:0]: Demodulator DC estimation mode. Recommend DCM = [01].
[00]: By DC average value, DCV[7:0],(0Bh).
[01]: DC holds after preamble detected.
[10]: DC holds after ID detected.
[11]: DC value when chip receive specific data length (set by DCL[:2:0])..

ADCO[8:0]: RSSI value if AGC =1 (Read Only).

9.2.13 ADC (Address: 0Ch)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Ch ADC	W	ARSSI	RADC	AVSEL1	AVSEL0	MVSEL1	MVSEL0	XADS	CDM	RTH7	RTH6	RTH5	RTH4	RTH3	RTH2	RTH1	RTH0
	R	PWR	XEM	PLLEM	TRSM	TREM		VBD1	VBD0	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1	ADC0
Reset		0	0	0	0	0	0	0	0	0	0	01	0	0	0	0	0

ARSSI: Auto RSSI measurement enable.
[0]: Disable. **[1]:** Enable.

ARSSI shall be [1] for auto RSSI measurement before MCU issues RX strobe command.

RADC: ADC Read Out Average Mode.
[0]: 1, 2, 4, 8 average mode. If RADC = 0, ADC average is set by AVSEL[1:0] (0Ch).
[1]: 8, 16, 32, 64 average mode. If RADC = 1, ADC average is set by MVSEL[1:0] (0Ch).

AVSEL [1:0]: ADC average mode. Recommend AVSEL = [10].
[00]: No average. **[01]:** 2. **[10]:** 4. **[11]:** 8.

MVSEL [1:0]: ADC average mode for VCO calibration and RSSI. Recommend MVSEL = [10].
[00]: 8. **[01]:** 16. **[10]:** 32. **[11]:** 64.

XADS: ADC input signal source select.
[0]: Internal temperature sensor or RSSI signal.
[1]: External signal source.

CDM: Carrier Detect enable
[0]: RSSI/Temperature measurement.
[1]: Carrier detect

RTH[7:0]: Threshold value of Carrier Detect (Active in RX mode only).
CD (Carrier Detect) =1 when RSSI ≧ RTH.
CD (Carrier Detect) =0 when RSSI < RTL.

PWR: Power Status (Read Only).
[0]: Power off. **[1]:** Power on.

XEM: Crystal Status (Read Only).
[0]: Disable. **[1]:** Enable.

PLLER: PLL Status (Read Only).
[0]: Disable. **[1]:** Enable.

TRSM: TRX Mode Status (Read Only).
[0]: RX mode. **[1]:** TX mode.

TREM: TRX Status (Read Only).
[0]: Disable. **[1]:** Enable.

VBD[1:0]: VCO bias detect (Read Only).

ADC[7:0]: ADC value (Read Only).

9.2.14 Pin Control (Address: 0Dh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Dh Pin control	W	RFT2	RFT1	RFT0	PRS	SCMDS	WMODE	INFS	IRQI	IRQ1	IRQ0	IRQE	CKOI	CKO1	CKO0	CKOE	SCKI
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

RFT [2:0]: RF Analog Pin Configuration. Recommend RFT= [000].

{XADS, RFT[2:0]}	BP_BG (Pin 30)	RSSI (Pin 1)
[0000]	Band-gap voltage	RSSI voltage
[0001]	Analog temperature voltage	RSSI voltage
[0010]	Band-gap voltage	No connection
[0011]	Analog temperature voltage	No connection
[0100]	BPF positive in phase output	BPF negative in phase output
[0101]	BPF positive quadrature phase output	BPF negative quadrature phase output
[0110]	RSSI voltage	No connection
[0111]	RSSI voltage	No connection
[1000]	Band-gap voltage	External ADC input source
[1001]	Analog temperature voltage	External ADC input source
[1010]	Band-gap voltage	External ADC input source
[1011]	Analog temperature voltage	External ADC input source
[1100]	No connection	External ADC input source
[1101]	No connection	External ADC input source
[1110]	No connection	External ADC input source
[1111]	No connection	External ADC input source

PRS: Read frequency mode for AFC=1. Recommend PRS= [0].
[0]: no frequency compensation.
[1]: frequency offset in AFC mode

SCMDS: Strobe Command select. Recommend SCMDS= [1].
[0]: register control. **[1]:** strobe control.

WMODE: WOT or WOR select for WORE=1.
[1]: WOT (Wake-on-TX).
[0]: WOR (Wake-on-RX).

INFS: Infinite FIFO length select.
[0]: fixed length. **[1]:** infinite length

IRQI: Reserved. IRQI shall be [0].

IRQ[1:0]: Reserved. Use GIO1S/ GIO2S instead. Shall be [00].

IRQE: Reserved. Use G1OE/ G2OE instead. Shall be [0].

CKOI: Reserved. Use 08h page 9 instead. Shall be [0].

CKO[1:0]: Reserved. Use 08h page 9 CKOS instead. Shall be [00].

CKOE: Reserved. Use 08h page 9 instead. Shall be [0].

SCKI: SPI Clock Inverted. Recommend SCKI= [0].
[0]: Normal. **[1]:** Inverted.

9.2.15 Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
Reset		0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

MSCRC: CRC Filtering Enable. Recommend MSCRC = [1].
[0]: Disable. **[1]:** Enable.

VTL[2:0]: VT low threshold setting for VCO calibration. Recommend VTL = [100].
[000]: VTL=0.1V. **[001]:** VTL=0.2V. **[010]:** VTL=0.3V. **[011]:** VTL=0.4V. **[100]:** VTL=0.5V. **[101]:** VTL=0.6V.
[110]: VTL=0.7V. **[111]:** VTL=0.8V.

VTH[2:0]: VT high threshold setting for VCO calibration. Recommend VTH = [111].
[000]: VTH=Vdd-0.1V. **[001]:** VTH=Vdd-0.2V. **[010]:** VTH=Vdd-0.3V. **[011]:** VTH=Vdd-0.4V. **[100]:** VTH=Vdd-0.5V.
[101]: VTH=Vdd-0.6V. **[110]:** VTH=Vdd-0.7V. **[111]:** VTH=Vdd-0.8V.

MVBS: VCO band calibration select.
[0]: Auto. **[1]:** Manual.

MVB[2:0]: VCO bank manual setting. VCO frequency increases when MVB decreases.

MIFS: IF Filter Calibration Select.
[0]: Auto. **[1]:** Manual.

MIF[3:0]: IF filter Manual Setting.

FCD [4:0]: IF Filter Auto Calibration Deviation from Goal (read only).

DVT[1:0]: VT output (Read Only).
[00]: VT< VTL< VTH.
[01]: VTL< VT< VTH.
[10]: No used.
[11]: VTL< VTH< VT.

VBCF: VCO Band Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

VB[2:0]: VCO Bank Auto Calibration Result (Read Only).

FBCF: IF Filter Auto Calibration Flag (Read Only).
[0]: Pass. **[1]:** Fail.

FB[3:0]: IF Filter Auto Calibration Result (Read Only).

9.2.16 Mode control (Address: 0Fh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Fh Mode control	W	DFCD	VBS	SWT	RSSC	VCC	CCE	WORE	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
	R	--	--	WORE	RSSC	CCER	FECF	CRCF	FMT	FMS	CER	PLLE	TRSR	TRER	VBC	FBC	ADCM
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DFCD: Packet Filtering by Carrier Detect.

The received packet is filtered if the input power level is below RTH (0Ah).
[0]: Disable. **[1]:** Enable.

VBS: Reserved. Should set to [0].

SWT: VCO Current and ADC clock and System clock select. Recommend SWT = [0].
[0]: Original
[1]: Update

RSSC: RSSI Calibration.
[0]: Disable. **[1]:** Enable.

VCC: VCO current calibration
[0]: Disable
[1]: Enable

CCE: Chip enable by register.
[0]: chip turn-off. **[1]:** chip turn-on.

WORE: WOR or WOT function enable.
[0]: Disable. **[1]:** Enable.

FMT: Reserved for internal usage only. Shall be set to [0].

FMS: Direct/FIFO mode select.
[0]: Direct mode. **[1]:** FIFO mode.

CER: Crystal enable by register.
[0]: crystal turn-off. **[1]:** crystal turn-on.

PLLE: PLL enable by register.
[0]: PLL off. **[1]:** PLL on.

TRSR: TRX Mode select by register.
[0]: RX mode. **[1]:** TX mode.
When bit TRER=1, the chip will enter TX or RX mode by TRSR register.

TRER: TRX mode enable by register. Shall be set to [1].
[0]: Reserved.
[1]: By register control (CER and TRSR). In FIFO mode, this bit will be cleared after end of packet encountered.

VBC: VCO Bank calibration enable (Auto clear when done).
[0]: Disable. **[1]:** Enable.

FBC: IF Filter Bank calibration enable (Auto clear when done).
[0]: Disable . **[1]:** Enable.

ADCM: ADC measurement (Auto clear when done).
[0]: Disable. **[1]:** Enable.

	Non-Rx mode	RX mode
[0]	None	None
[1]	Temperature measurement (XADS=0) or external analog signal conversion from pin 1 (XADS=1)	RSSI, carrier detect

FECF: FEC flag. (Bit 10, FECF is read clear.)
[0]: FEC pass. **[1]:** FEC error.

CRCF: CRC flag. (Bit 9, CRCF is read clear.)
[0]: CRC pass. **[1]:** CRC error.

10. SPI (3-wire)

The A7129 communicates with a host MCU via 3-wire SPI interface (SCS, SCK, SDIO) or 4-wire SPI (SDO from GIO1 or GIO2) with a max data rate 10Mbps. A SPI transition is a 24-bits sequence which consists of an 8-bits address and a 16-bits data word. The MCU should set SCS (SPI chip select) pin low in order to access A7129. Via the SPI interface, user can access the **control registers** and issue **Strobe commands**. The SPI data will be latched into the registers at the rising edge of SCK. When reading registers from the RF chip, after input the wanted register address, the bit data will be transferred from the falling edge of SCK.

10.1 SPI Format

Address Byte(8 bits)								Data words(16 bits)															
R/W	Command			Address				Data															
A7	A6	A5	A4	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SPI format

Address Byte (8 bits):

Bit A7: R/W bit
[0]: Write.
[1]: Read.

Bit A6~A4: Command
[00x]: read/write control register.
[01x]: read/write ID code.
[10x]: read/write FIFO register.
[110]: reset TX/RX FIFO pointer.
[111]: RF chip Reset (soft reset and all registers will be clean to initial value).

Bit A3~A0: Address of control register

Strobe Command table:

Address Byte (8 bits)								description
A7	A6	A5	A4	A3	A2	A1	A0	
0	0	0	0	A3	A2	A1	A0	Write control register
1	0	0	x	A3	A2	A1	A0	Read control register
0	0	1	x	x	X	x	x	Write ID code command
1	0	1	x	x	X	x	x	Read ID code command
0	1	0	x	x	X	x	x	TX FIFO write command
1	1	0	x	x	X	x	x	RX FIFO read command
X	1	1	1	x	X	x	x	Software Reset command
0	1	1	0	x	X	x	x	TX FIFO address pointer reset command
1	1	1	0	x	X	x	x	RX FIFO address pointer reset command
0	0	0	1	0	0	0	0	Sleep mode
0	0	0	1	0	0	1	0	Idle mode
0	0	0	1	0	1	0	0	Standby mode
0	0	0	1	0	1	1	0	PLL mode
0	0	0	1	1	0	0	0	RX mode
0	0	0	1	1	0	1	0	TX mode
0	0	0	1	1	1	0	0	Deep sleep mode (tri-state)
0	0	0	1	1	1	1	1	Deep sleep mode (pull-high)

Remark: X (Don't care).

Data Words (16-bits) : On-chip registers in sequence of D15~D0.

10.2 SPI Timing Chart

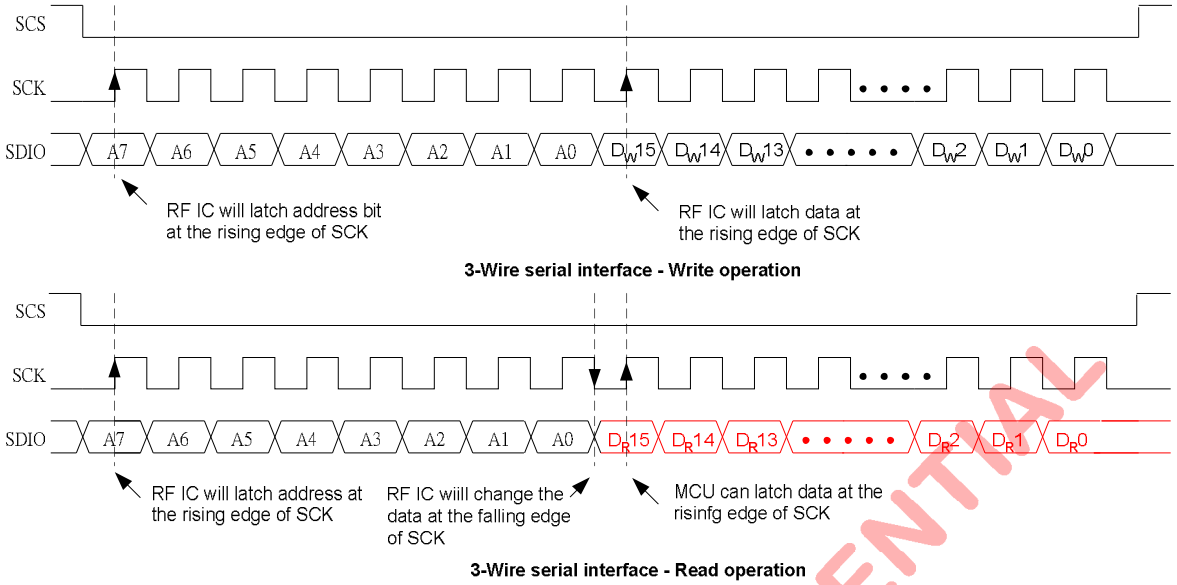


Figure 10.1. SPI read/write sequence

10.3 Control register access

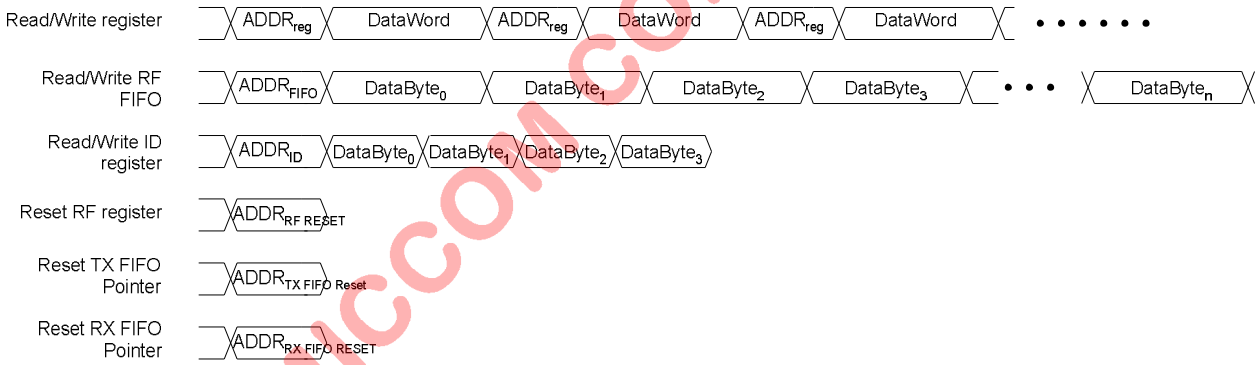


Figure 10.2. Access type of control register

10.4 SPI Timing Specification

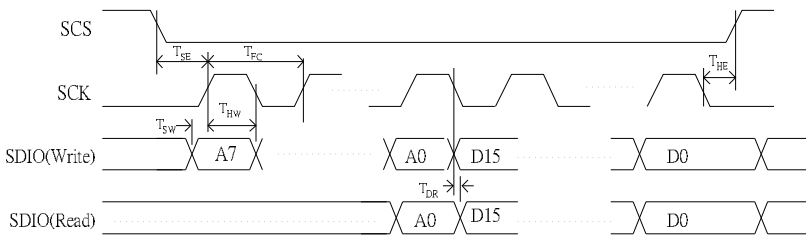


Figure 10.3 SPI timing sequence

Parameter	Description	Min.	Max.	Unit
T_{FC}	Clock frequency.		10	MHz
T_{SE}	SCS setup time.	50		ns

T_{HE}	SCS hold time.	50		ns
T_{SW}	SDIO setup time.	50		ns
T_{HW}	SDIO hold time.	50		ns
T_{DR}	SDIO delay time.	0	100	ns
T_{HR}	SDIO hold time.	0		ns

10.5 Reset Command

The MCU could issue a software reset command to A7129 by sending a Reset Command through the SPI interface as shown below. After a reset command, A7129 is in standby mode.

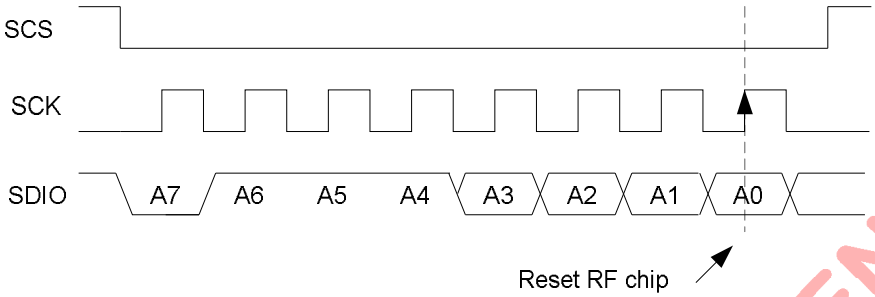


Figure 10.5 Reset Command

10.6 Reset TX FIFO Pointer

The SPI timing sequences for resetting TX FIFO Pointer is shown below. The address pointer of TX FIFO is reset to 0x00 at the rising edge of SCK at bit A0.

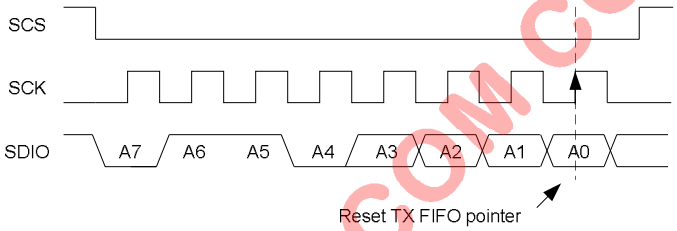


Figure 10.6 TX FIFO Pointer Reset

10.7 Reset Rx FIFO Pointer

The SPI timing sequences for resetting RX FIFO Pointer is shown below. The address pointer of RX FIFO is reset to 0x00 at the rising edge of SCK at bit A0.

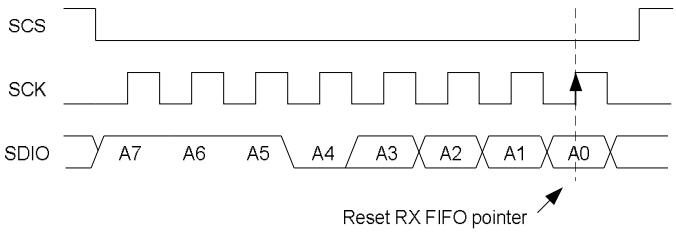


Figure 10.7 RX FIFO Pointer Reset

10.8 ID Read/Write Command

A7129 has built-in 32-bits ID Registers for customized identification code. It is accessed via SPI interface. ID length is recommended to be 32 bits by setting IDL. The timing sequences are shown below. First execute the ID Red/write command in address byte, and then write data bytes with length of the 4 bytes.

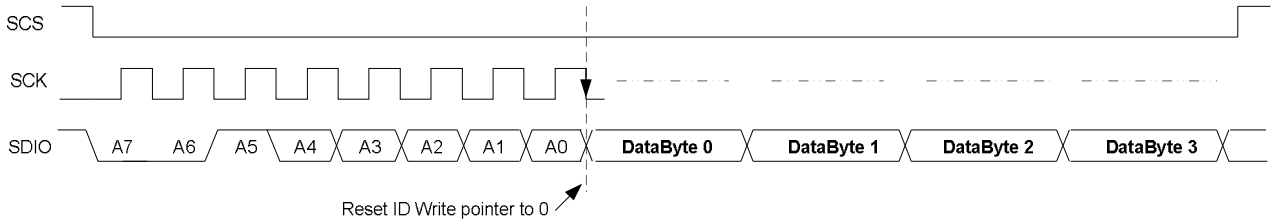


Figure 10.8 ID Write Command

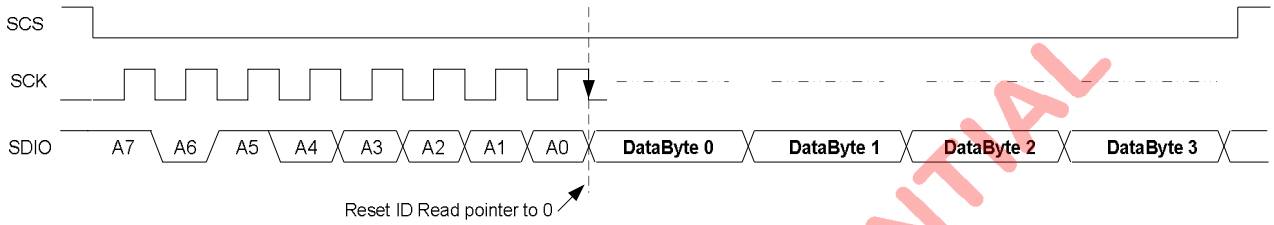


Figure 10.9 ID Read Command

10.9 FIFO R/W Command

TX FIFO Write Command

To execute the TX FIFO write procedure, according to the command table, user should write the corresponding command into Address Byte, and then write data into the Data Bytes. After completing the writing action, toggle SCS=1 to end the TX FIFO writing procedure.

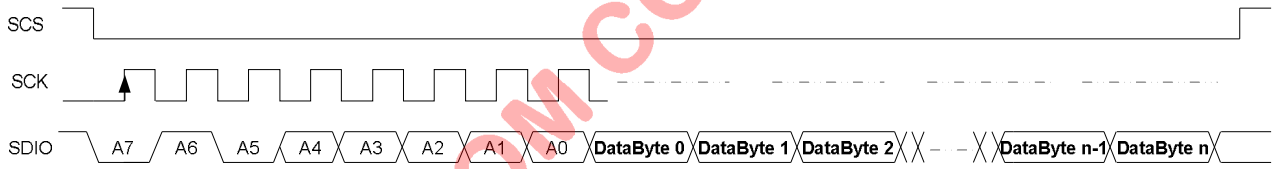


Figure 10.10 TX FIFO Write Command

RX FIFO Write Command

To execute the RX FIFO read procedure, according to the command table, user should write the corresponding command into Address Byte, and then read out RX FIFO. After completing the reading action, toggle SCS=1 to end the RX FIFO writing procedure.

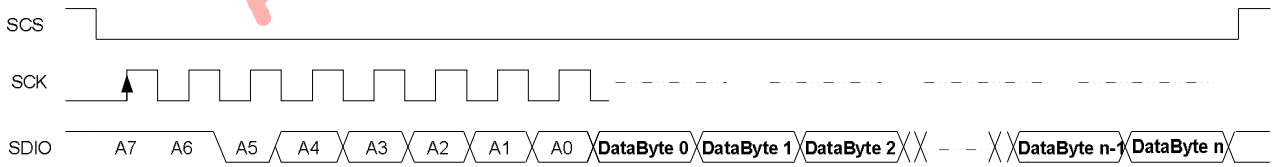


Figure 10.11 RX FIFO Read Command

11 Crystal Oscillator

A7129 needs external crystal or external clock to generate internal wanted clock.

Relative Control Register / Crystal (Address: 07h)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
07h Crystal	W	PGAS3	PGAS2	PGAS1	PGAS0	CRCDNP	CRCINV	PGBS2	PGBS1	PGBS0	-	-	XCC	XCP1	XCP0	CGS	XS
Reset		0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

11.1 Use External Crystal

Figure 12.1 shows the connection of crystal network between XI and XO pins. C1 and C2 capacitance built inside A7129 are used to adjust different crystal loading. User can set INTXC [4:0] (08h, page 9) to meet crystal loading requirement. A7129 supports low cost crystal within ± 30 ppm accuracy. Be aware that crystal accuracy requirement includes initial tolerance, temperature drift, aging and crystal loading.

CKO (Address: 08h) Page 9

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h CKO	W	INTXC	XCL4	XCL3	XCL2	XCL1	XCL0	WSEL2	WSEL1	WSEL0	CKS3	CKS2	CKS1	CKS0	CKOI	CKOE	SCT
Reset		0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0

Note: set XS= 1 (07h) and INTXC(08h, page 9) to enable external crystal oscillator and on-chip crystal compensated capacitors.

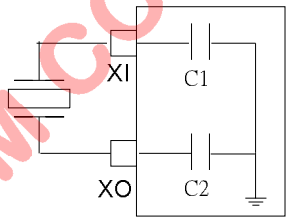
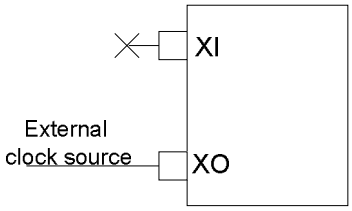


Figure11.1 Crystal network connection for using external crystal

11.2 Use External Clock

A7129 has built-in AC couple capacitor to support external clock input. Figure 11.2 shows how to connect. In such case, XI pin is left opened.

Note: set XS = 0 (07h) to select external clock (AC couple capacitor active.). And the frequency accuracy of external clock shall be controlled within ± 30 ppm and the clock swing (peak-to-peak) shall be larger than 1.0V.



External clock is controlled within ± 30ppm and Vpp is above 1.0V.

Figure 12.2 Connect to external clock source

12. System Clock

A7129's main system clock, F_{MSCK}, can be either come from Xtal oscillator itself or from the internal PLL clock generator. The purpose of the internal clock generator is used to support multi Xtal frequency and/or special requirements of the wanted data rate.

12.1 Clock Domain

Since F_{MSCK} is the root of the data rate clock, IF Filter calibration clock, as well as baseband clock, therefore, there are several clock dividers implemented by configurable registers such as CSC, SDR, DMOS, MCNT and MCNTR. Table 12.1 lists the most important constraints how to configure those registers successfully and figure 12.1 illustrates the detailed clock domain.

Signal	Constraints	Note
F_{MSCK} (main system clk)	If CGS = 0, F_{MSCK} = Xtal freq. If CGS = 1, F_{MSCK} = Clk Gen	If using Clk Gen, F_{MSCK} range can be from 20M ~ 50MHz that depends on GRC and GRS.
DCK (data rate clock)	$DCK = \frac{1}{64} \cdot \frac{f_{CSCK}}{SDR[6:0]+1}$	DCK = the wanted data rate
Demodulator Oversample	F_{MSCK} = F_{IFREF} x (32)	Use 32 oversample by set DMOS = 1
IFBW calibration	F_{IFREF} = IF Filter BW x (2)	F_{IFREF} is derived from F_{MSCK}
PF8M	equal or close to 6.4MHz	Set WRCKS = 0 for successful WOR calibration
	equal or close to 8MHz	Set WRCKS = 1 for successful WOR calibration

Table 12.1 Constraints of the key signals and its usage.

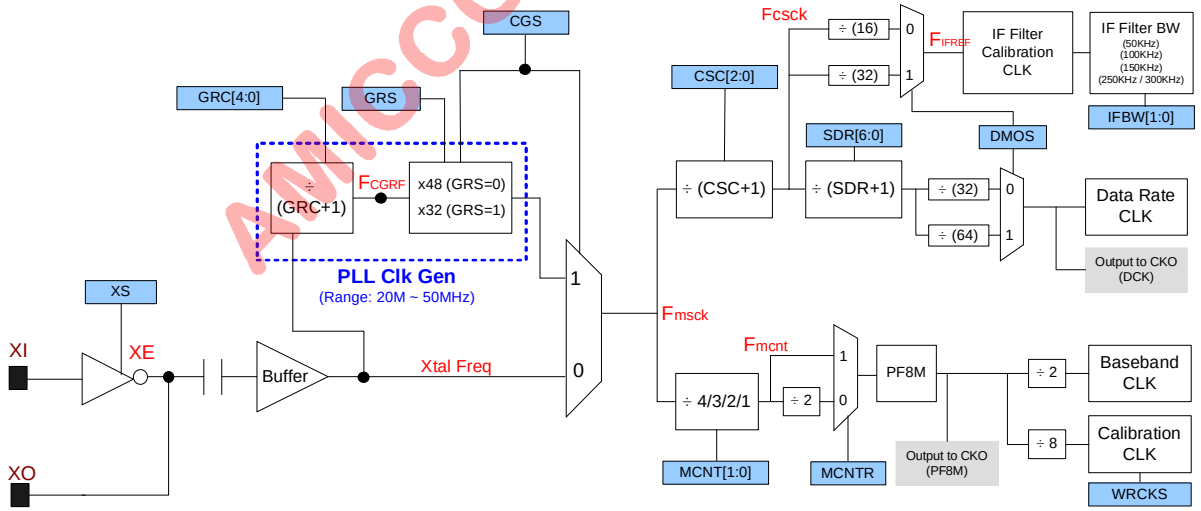


Figure 12.1 Illustrations from Xtal oscillator to main system clock and its clock domain.

12.2 System Clock and IF Filter

In general, data rate is almost the first consideration to start a new design. While choosing a wanted data rate, A7129 offers 4 optional IFBW (50KHz / 100KHz / 150KHz / 250KHz) to trade off RX sensitivity and frequency tolerance.

Table 12.2 lists the recommended IFBW vs data rate. For example, 10Kbps data rate is mapping to 50KHz IFBW. In this case, using ± 10 ppm Xtal is necessary this is because the narrower IFBW the poorer frequency tolerance, but, the better RX sensitivity. However, user can also choose 100KHz IFBW to handle a larger frequency tolerance in a RF system. That means using a larger Xtal tolerance is ok, i.e. ±20 ppm. But, its disadvantage is to suffer RX sensitivity.

Data rate	IFBW	F_{IFREF}	Constraints
2K ~ 50kbps	~ 50kHz	~ 50kHz x 2	The actual F_{IFREF} ,which is derived from system clock, is double of IFBW
≦100kbps	~ 100kHz	~ 100kHz x2	
≦150kbps	~ 150kHz	~ 150kHz x2	
≦250kbps	~ 250kHz	~ 250kHz x2	

Table 12.2 General case of IFBW mapping to Data Rate.

12.3 Example of 10Kbps data rate by 12.8MHz Xtal

Since IFBW is so important to impact RX sensitivity, A7129 has an IFBW calibration procedure to overcome the process deviation of semiconductor. To make a successful IFBW calibration, the relationships among F_{MSCK}, F_{IFREF} and DCK must be satisfied. Figure 12.2 illustrates the detailed configurations to clock dividers.

1. Data rate = 10Kbps
2. Xtal = 12.8MHz
3. Clk Gen = disable
4. IFBW[1:0] = [00], targeted BW = 50KHz

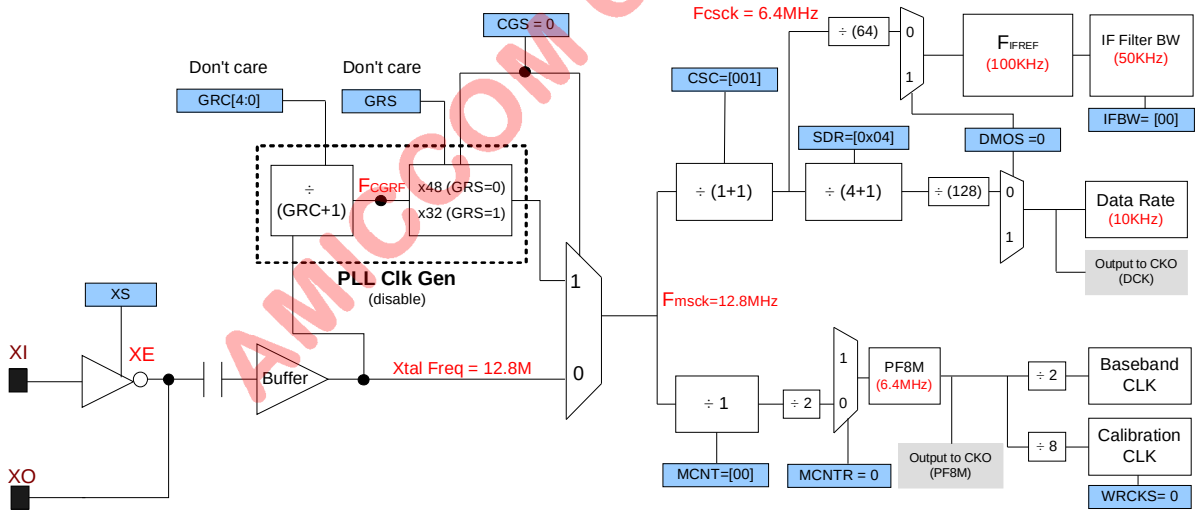


Figure 12.2 Configurations of 10Kbps when IFBW = 50KHz

5. If choosing IFBW = 100KHz, figure 12.3 illustrates the different results of CSC and F_{CSCK}.
6. Data rate = 10Kbps
7. Xtal = 12.8MHz
8. Clk Gen = disable
9. IFBW[1:0] = [01], targeted BW = 100KHz

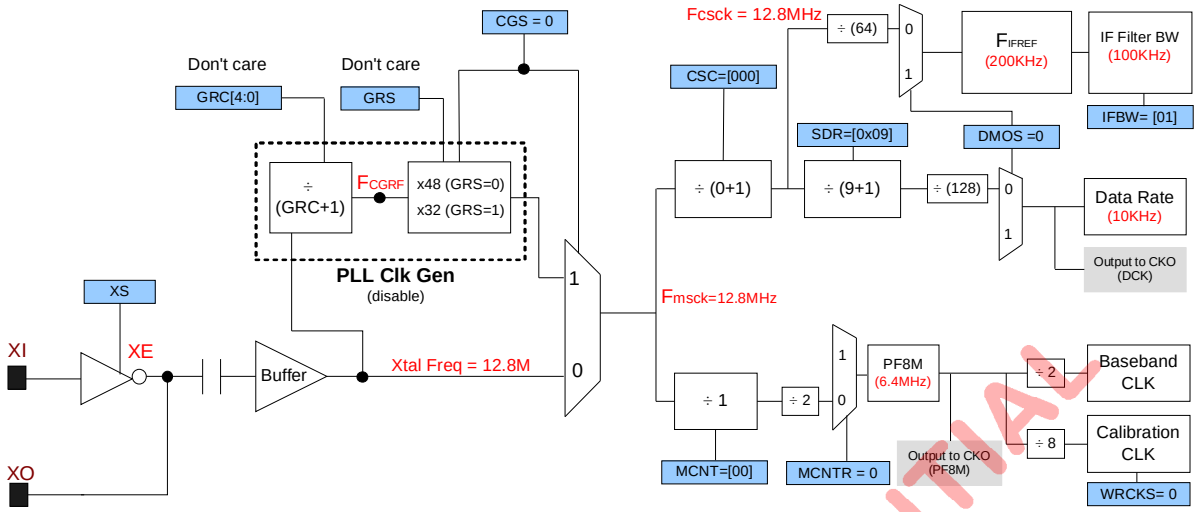


Figure 12.3 Configurations of 10Kbps when IFBW = 100KHz

12.4 Example of special data rate by 19.6608MHz Xtal.

A7129 can support most general data rate such as 10K, 50K, 100K, 150K, 250Kbps. For special data rate such as 38.4Kbps, the internal Clk Gen can be enabled with a special Xtal frequency to get the wanted DCK and IFBW. Figure 12.4 illustrates the detailed configurations to clock dividers.

1. Data rate = 38.4Kbps
2. Xtal = 19.6608MHz
3. Clk Gen = disable
4. IFBW[1:0]= [10] , targeted BW = 150KHz

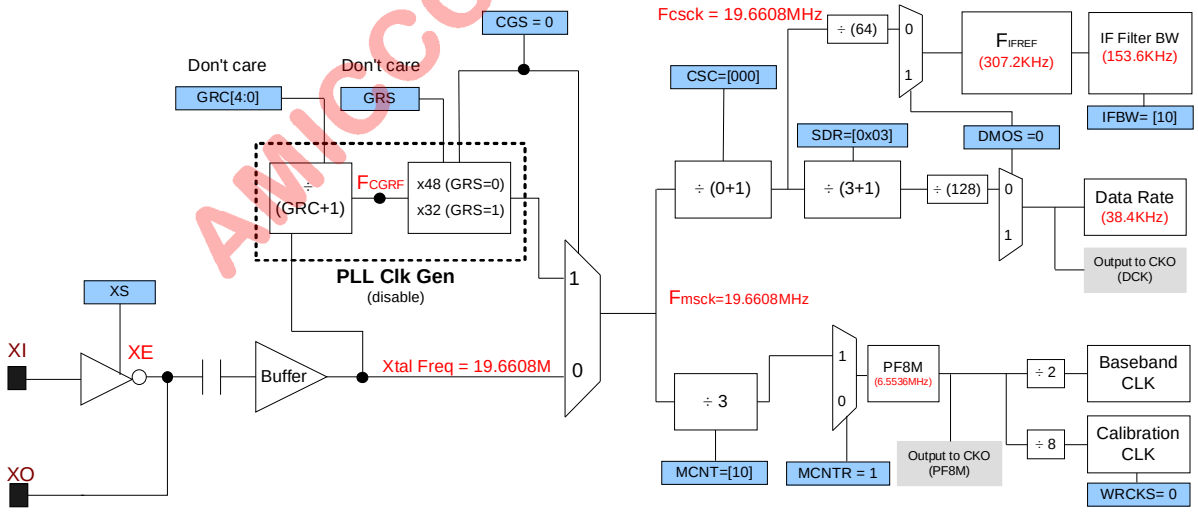


Figure 12.4 Configurations of 38.4Kbps when IFBW = 153.6KHz

5. If choosing IFBW = [11]. IFBW will become 307.2KHz instead of the expected 250KHz because of F_{IFREF} (higher F_{IFREF} results larger IF bandwidth if IF Filter Calibration is successful.). Figure 12.5 illustrates the different results of CSC and FCSCK.
6. Data rate = 38.4Kbps
7. Xtal = 19.6608MHz
8. Clk Gen = enable
9. IFBW = 307.2KHz

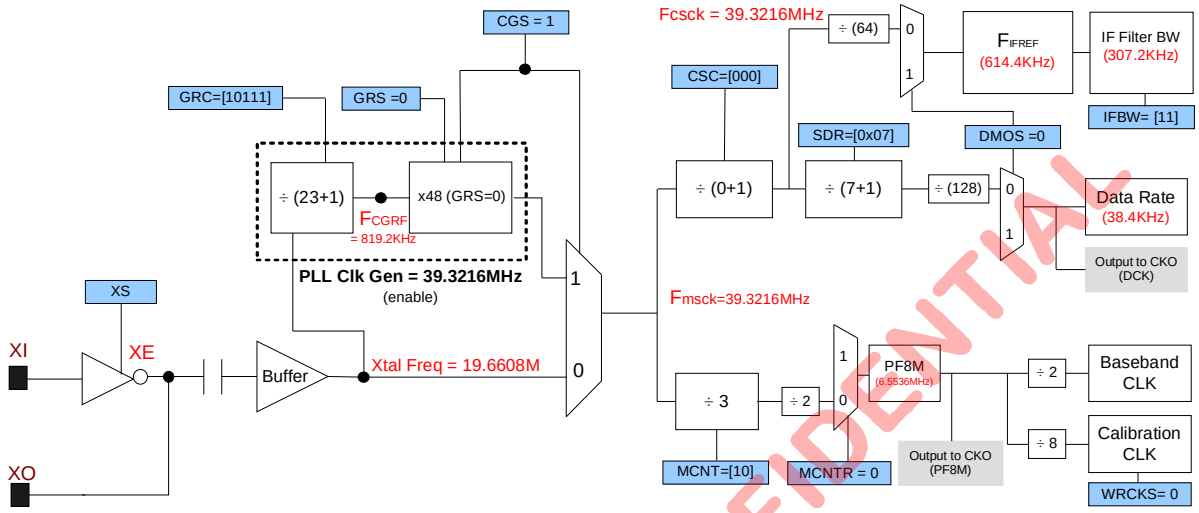


Figure 12.5Configurations of 38.4Kbps when IFBW = 307.2KHz

13. Tranceiver Frequency

A7129 is a half-duplex transceiver with embedded PA and LNA. For TX or RX frequency setting, user just needs to set up LO (Local Oscillator) frequency for two ways radio transmission.

To target full range of Sub 1GHz ISM band (315/433/470/868/915MHz band), A7129 applies offset concept by LO frequency $F_{LO} = F_{LO\_BASE} + F_{OFFSET}$. Therefore, this device is easy to implement single channel operation or frequency hopping (multi-channels) by setting, IF Register II (FPA [15:0]).

Below is the frequency synthesizer block diagram which shows that VCO frequency (F_{VCO}) is operated at the wanted RF frequency (F_{RF}).

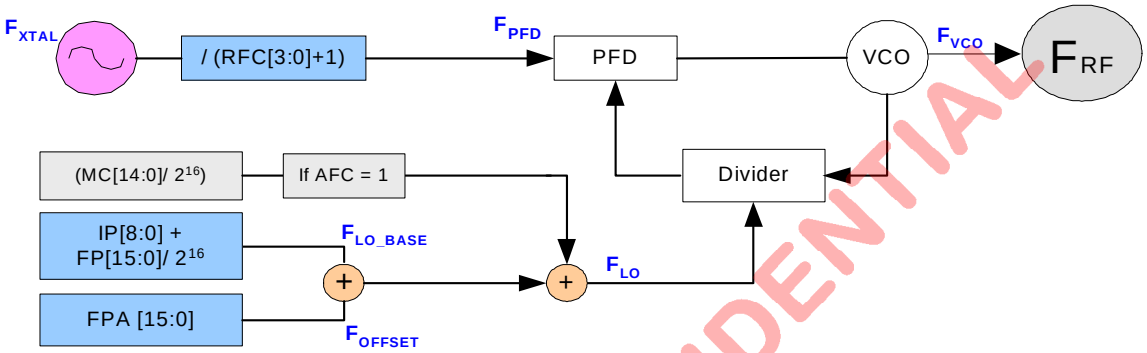


Figure 13.1 Frequency synthesizer block diagram

$F_{RF} = F_{VCO} = F_{LO\_BASE} + F_{OFFSET}$ (unit: Hz)

where f_{RF}, the wanted RF frequency, is equal to VCO frequency.

where f_{LO_BASE}, the base frequency of LO frequency.

where f_{OFFSET}, the offset frequency of LO frequency.

Example:
How to get (F_{RF}) = 433.921MHz by a 12.8MHz Xtal.

1. Set AFC = 0 to disable AFC function.
2. Set RFC (06h) = [000], (F_{PFD}) = Xtal frequency = 12.8MHz.
3. Set MD1 (04h) = [0] for 433MHz band.
4. Set IP [7:0] (01h) for integer part. Set IP[8:0] = 33 = 0x021
5. Set FP [15:0] (02h) for fractional part. Set FP[15:0] = 58987 = 0xE66B
6. $$f_{LO\_BASE} = f_{PFD} \cdot (IP[8:0] + \frac{FP[15:0]}{2^{16}}) = 12.8 \times (33 + \frac{58987}{2^{16}}) = 433.921 \text{ (MHz)}$$
7. Set FPA [15:0] (09h, page 2) for offset part. Set FPA = 0x0000 for zero offset.
8. $$f_{OFFSET} = f_{PFD} \cdot (\frac{FPA[15:0] \cdot 2^6}{2^{16}}) = 12.8 \times \frac{0}{2^{10}} = 0 \text{ (MHz)}$$
9. For TX radio frequency (F_{TXRF}) is equal to $F_{RF} = F_{VCO} = F_{LO\_BASE} + F_{OFFSET} = 433.921 + 0 = 433.921$ *(MHz)*.
10. RX LO frequency (F_{RXLO}) is shall be set to ONE F_{IF} offset because low-IF architecture.

.

RX LO frequency $F_{RXLO} = F_{TXRF} - F_{IFREF}$; when ULS (0Ah) = 0 for up side band.

14. State machine

A7129 has seven major operation modes from current consumption point of view as shown in Table 14.1. From accessing data point of view, if FMS=1 (0Fh), FIFO mode is enabled, otherwise, A7129 is in direct mode.

14.1 Key Strobe Commands

A7129 has below 7 operation modes in current consumption point of view. Those are,
(1) Deep Sleep mode
(2) Sleep mode
(3) Idle mode
(4) Standby mode
(5) PLL mode
(6) TX mode
(7) RX mode

After power on reset or software reset or deep sleep mode, user has to do calibration process because all control registers are in initial values. The calibration process of A7129 is very easy, user only needs to issue Strobe commands and enable calibration registers. If so, the calibrations are automatically completed by A7129's internal state machine. Table 14.1 shows a summary of key circuitry among those strobe commands.

Mode	Register retention	Regulator	Xtal Osc.	VCO	PLL	RX	TX	Strobe Command
Deep Sleep (Tri-state)	No	OFF	OFF	OFF	OFF	OFF	OFF	(1101-0000)b
Deep Sleep (pull-high)	No	OFF	OFF	OFF	OFF	OFF	OFF	(1111-0011)b
Sleep	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0000-xxxx)b
Idle	Yes	ON	OFF	OFF	OFF	OFF	OFF	(0001-xxxx)b
Standby	Yes	ON	ON	OFF	OFF	OFF	OFF	(0010-xxxx)b
PLL	Yes	ON	ON	ON	ON	OFF	OFF	(0011-xxxx)b
TX	Yes	ON	ON	ON	ON	OFF	ON	(0101-xxxx)b
RX	Yes	ON	ON	ON	ON	ON	OFF	(0100-xxxx)b
SW RST								(x111-xxxx)b

Remark: x means "don't care"

Table 14.1. Operation mode and strobe command

14.2 FIFO mode

This mode is suitable for the requirements of general purpose applications and can be chosen by setting FMS = 1. After calibration, user can issue Strobe command to enter standby mode where write TX FIFO or read RX FIFO. From standby mode to packet data transmission, only one Strobe command is needed. Once transmission is done, A7129 is auto back to standby mode. Figure 14.1 and Figure 14.2 are TX and RX timing diagram respectively. Figure 14.3 illustrates state diagram of FIFO mode.

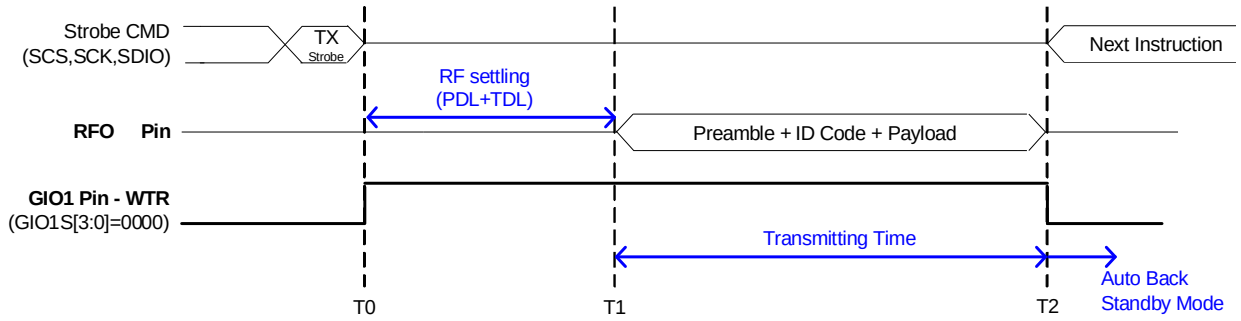


Figure 14.1 TX timing of FIFO Mode

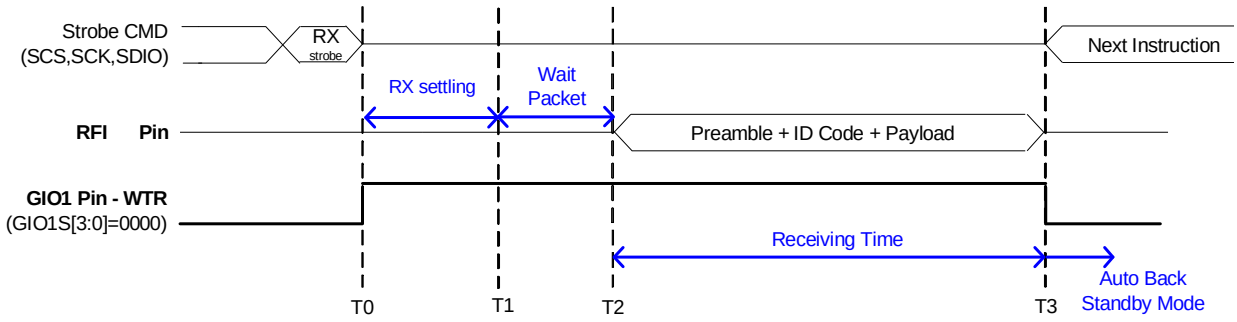


Figure 14.2 RX timing of FIFO Mode

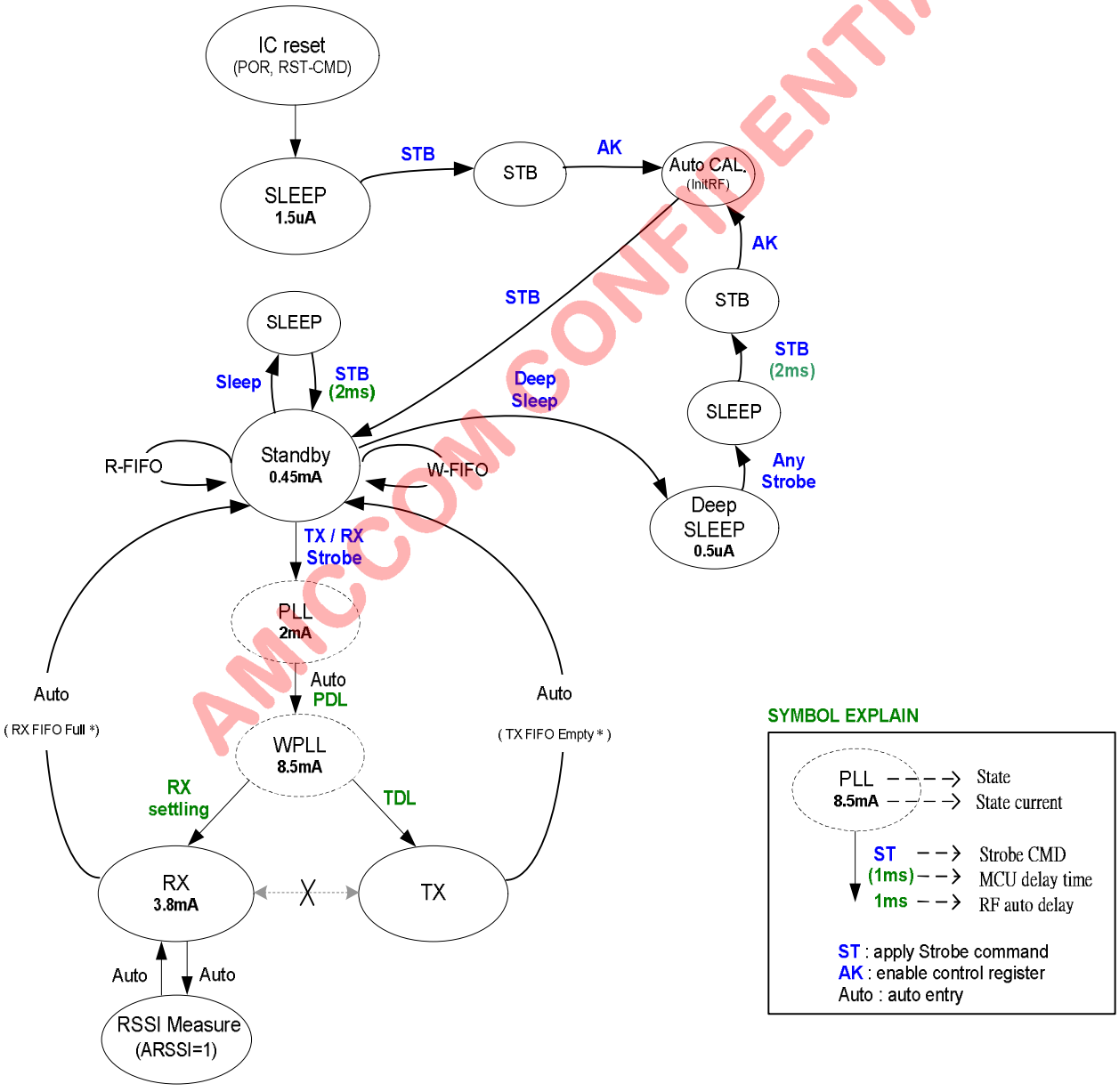


Figure 14.3 State diagram of FIFO Mode

14.3 Direct mode

This mode is suitable to let MCU to drive customized packet to A7129 directly by setting FMS = 0. In TX mode, MCU shall send customized packet in bit sequence (simply called raw TXD) to GIO1 or GIO2 pin. In RX mode, the receiving raw bit streams (simply called RXD) can be configured output to GIO1 or GIO2 pin. Be aware that a customized packet shall be preceded by a 32 bits preamble to let A7129 get a suitable DC estimation voltage. After calibration flow, for every state transition, user has to issue Strobe command to A7129 for fully control. This mode is also suitable for the requirement of versatile packet format.

Figure 14.4 and Figure 14.5 are TX and RX timing diagram in direct mode respectively. Figure 14.3 illustrates state diagram of direct mode.

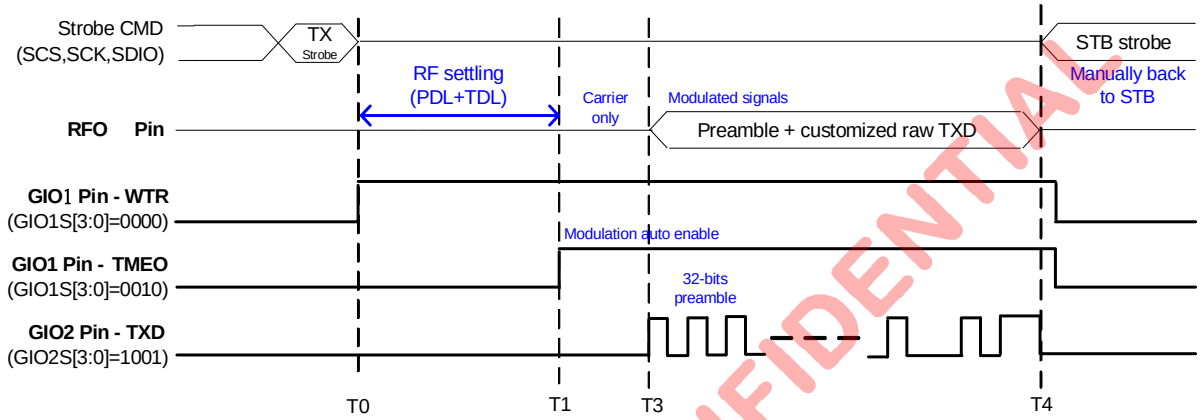


Figure 14.4 TX timing of Direct Mode

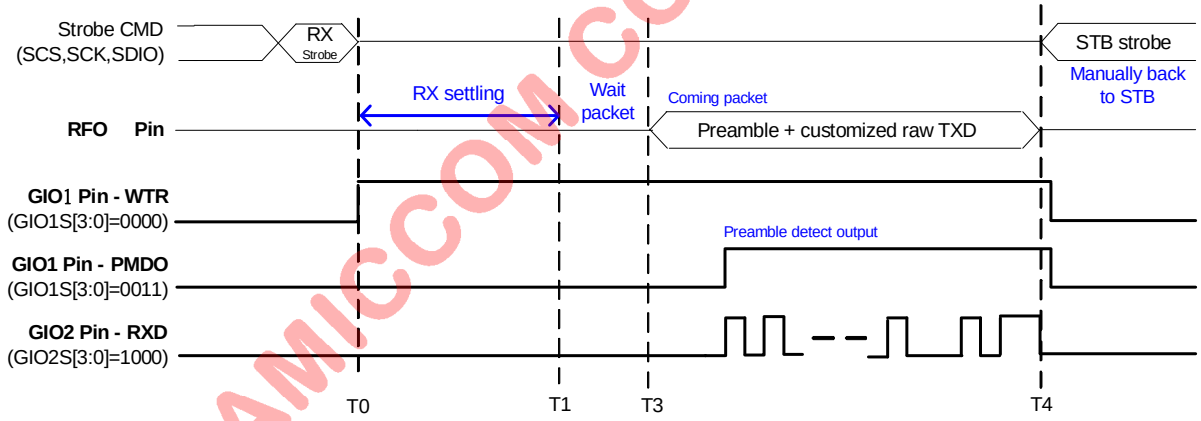


Figure 14.5 RX timing of Direct Mode

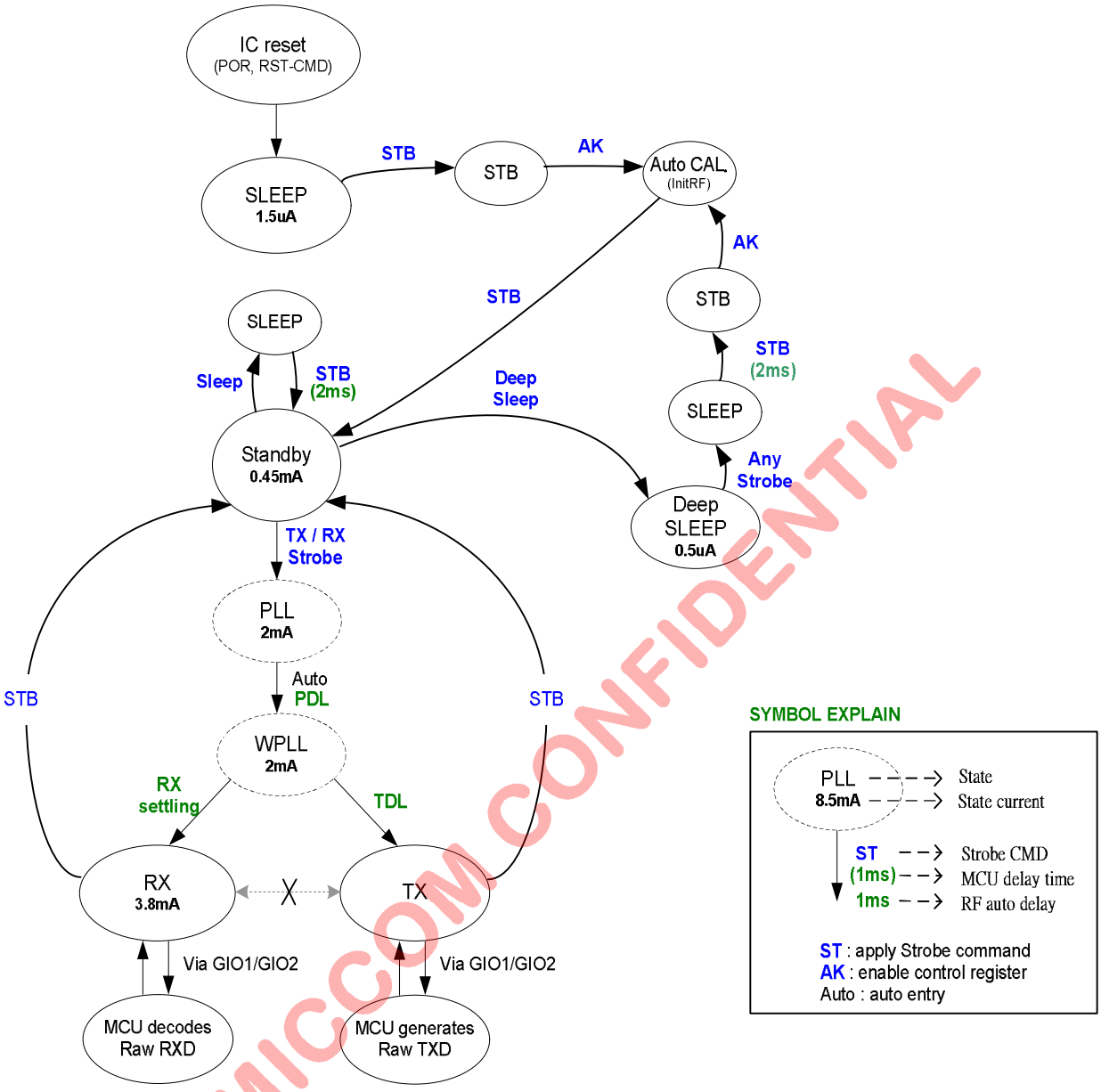


Figure 14.6 State diagram of Direct Mode

15. Calibration

A7129 needs calibration process during initialization with 2 calibration items, they are IF CAL (IF Filter calibration) and VCO band CAL (VCO band calibration).

1. VCO Bank Calibration is to select best VCO frequency bank for the calibrated frequency.
2. VCO Current Calibration.
3. IF Filter Bank Calibration is to calibrate IF filter bandwidth and center frequency.

Please notice that VCO Current, Bank and Deviation should be calibrated in PLL mode by sequence. IF Filter Bank and RSSI could be calibrated in either standby or PLL mode.

15.1 IF Calibration Process

Under the Stand by state (XOSC is on), set bit MIFS=0(auto calibration) or bit MIFS=1(Manual calibration) to execute the IF calibration. When the mode control register bit FBC=1, the chip will enter CAL state, and starts the calibration process.

If RF chip is not in the STB state when bit FBC is set to 1, RF chip will not start the calibration process until it enters the STB state. Once the calibration is completed, bit FBC will be cleared to 0 automatically, and RF chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7129 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock).

15.2. VCO band Calibration Process

Before the VCO band calibration, user should first set operating frequency in PLL I and PLL II registers, meanwhile, the range of VT (VTH[2:0], VTL[2:0]) and VCO also needs to be set properly.

Under the Stand by state (XOSC is on), set bit MVBS=0(auto calibration) or bit MVBS=1(manual calibration) to execute the VCO band calibration. After setting the mode control register bit VBC=1, the chip will enter CAL state, and starts the calibration process. If RF chip is not in the STB state when bit VBC is set to 1, RF chip will not start the calibration process until it entering STB state. When the calibration is completed, bit VBC will be cleared to 0 automatically, and chip will leave from CAL state and back to STB state.

If the mode control register bit TRER=1, FBC=1 or VBC=1are set simultaneously, RF chip will enter the CAL state first, and after completion of IF filter calibration or VCO band calibration process, RF chip can then enter into TX/RX state. The maximum time required for A7129 RF chip to perform IF Calibration process is about 16 * 256 * (1 / system clock). The maximum time required for A7129 RF chip to perform VCO band Calibration process is about 4 * PLL settling time.

Calibration (Address: 0Eh)

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0Eh Calibration	W	MSCRC	VTL2	VTL1	VTL0	VTH2	VTH1	VTH0	MVBS	MVB2	MVB1	MVB0	MIFS	MIF3	MIF2	MIF1	MIF0
	R	FCD4	FCD3	FCD2	FCD1	FCD0	DVT1	DVT0	VBCF	VB2	VB1	VB0	FBCF	FB3	FB2	FB1	FB0
Reset		0	0	0	0	0	0	0	0	1	0	0	0	0	1	1	0

16. FIFO (First In First Out)

A7129 supports separated 64-bytes TX and RX FIFO by enabling FMS =1 (0Fh). TX FIFO represents transmitted payload. On the other hand, once RX circuitry synchronizes ID Code, received payload is stored into RX FIFO.

16.1 Packet Format

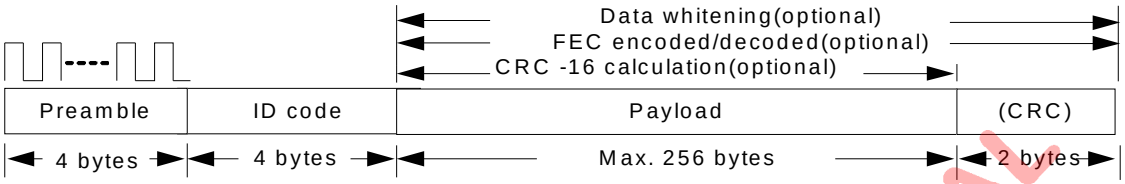


Figure 16.1 Packet Format of FIFO mode

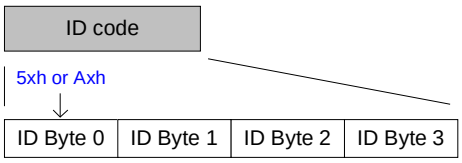


Figure 16.2 ID Code Format

Preamble:
The packet is led by preamble composed of alternate 0 and 1. If the first bit of ID code is 0, preamble shall be 0101…0101. In the contrast, if the first bit of ID code is 1, preamble shall be 1010…1010.
Preamble length is recommended to set 4 bytes by PML [1:0] (08h, page 14).

ID code:
ID code is recommended to set 4 bytes by IDL=1 (08h, page 14). ID Code is sequenced by Byte 2, 4, 6 and 8 (Recommend to set ID Byte 0 = 5xh or Axh). If RX circuitry checks the ID code correct, received payload will be stored into RX FIFO. In special case, ID code could be set error tolerance (0~ 3bit error) by ETH [1:0] (0Ah) for ID synchronization check.

Payload:
Payload length is programmable by FEP [13:0] (08h, page 10, 13) to define the FIFO length. The physical FIFO length is 64 bytes. A7129 also supports logical FIFO extension up to 16K bytes. See section 16.4.3 for details.

CRC (option):
In FIFO mode, if CRC is enabled (CRCS=1, 08h, page 14), 2-bytes of CRC value is transmitted automatically after payload. In the same way, RX circuitry will check CRC value and show the result to CRC Flag (0Fh).

16.2 Bit Stream Process

A7129 supports 3 optional bit stream processes for payload, they are,

(1) CCITT-16 CRC ($x^{16} + x^{15} + x^2 + 1$).
(2) (7, 4) Hamming FEC
(3) Data Whitening by XOR PN7 (7-bits Pseudo Random Sequence).

CRC (Cyclic Redundancy Check):

1. CRC is enabled by CRCS= 1 (08h, page 14). TX circuitry calculates the CRC value of payload (preamble, ID code excluded) and transmits 2-bytes CRC value after payload.
2. RX circuitry checks CRC value and shows the result to CRC Flag (0Fh). If CRCF=0, received payload is correct, else error occurred. (CRCF is read only, it is revised internally while receiving every packet.)

FEC (Forward Error Correction):

1. FEC is enabled by FECS= 1 (08h, page 14). Payload and CRC value (if CRCS=1) are encoded by (7, 4) Hamming code.
2. Each 4-bits (nibble) of payload is encoded into 7-bits code word as well as delivered out automatically. **(ex. 64 bytes payload will be encoded to 128 code words, each code word is 7 bits.)**
3. RX circuitry decodes received code words automatically. FEC supports 1-bit error correction each code word. Once 1-bit error occurred, FEC flag=1 (0Fh). (FECF is read only, it is revised internally while receiving every packet.)

Data Whitening:

1. Data whitening is enabled by WHTS= 1 (08h, page 14). The initial seed of PN7 is WS [6:0] (08h, page 14). Payload is always encrypted by bit XOR operation with PN7. CRC and/or FEC are also encrypted if CRCS=1 and/or if FECS=1.
2. RX circuitry decrypts received payload and 2-bytes CRC (if CRCS=1) automatically. Please notice that user shall set the same WS [6:0] to TX and RX.

16.3 Transmission Time

Based on CRC and FEC options, the transmission time differs depending on the chosen of CRC and FEC options. See table 16.1 for details.

Data Rate = 250 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 4 us = 2.304 ms
32	32	512	16 bits	Disable	592 bit X 4 us = 2.368 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 4 us = 3.840 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 4 us = 3.952 ms

Data Rate = 125 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 8 us = 4.608 ms
32	32	512	16 bits	Disable	592 bit X 8 us = 4.736 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 8 us = 7.580 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 8 us = 7.904 ms

Data Rate = 50 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 20 us = 11.52 ms
32	32	512	16 bits	Disable	592 bit X 20 us = 11.84 ms
32	32	512	Disable	512 x 7 / 4	960 bit X 20 us = 19.20 ms
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 20 us = 19.76 ms

Data Rate = 2 Kbps

Preamble (bits)	ID Code (bits)	Payload (bits)	CRC (bits)	FEC	Transmission Time / Packet
32	32	512	Disable	Disable	576 bit X 0.5 ms = 0.288 s
32	32	512	16 bits	Disable	592 bit X 0.5 ms = 0.296 s
32	32	512	Disable	512 x 7 / 4	960 bit X 0.5 ms = 0.480 s
32	32	512	16 x 7 / 4	512 x 7 / 4	988 bit X 0.5 ms = 0.494 s

Table 16.1 Transmission time

16.4 Usage of TX and RX FIFO

In application points of view, A7129 supports 3 options of FIFO arrangement.
(1) Easy FIFO
(2) Segment FIFO
(3) FIFO Extension

16.4.1 Easy FIFO Mode

In Easy FIFO mode, max FIFO length is 64 bytes. FIFO length is equal to **(FEP [13:0] +1)**. User just needs to control FEP [13:0] and disable PSA and FPM as shown below.

Register setting

TX	RX	Control Registers		
TX-FIFO (byte)	RX-FIFO (byte)	FEP[13:0]	PSA [5:0]	FPM [1:0]
1	1	0x000	0	0
8	8	0x007	0	0
16	16	0x00F	0	0
32	32	0x01F	0	0
64	64	0x03F	0	0

Table 16.2 Control registers of Easy FIFO

Procedure of TX FIFO Transmitting

1. Initialize all control registers (refer to A7129 reference code).
2. Set FEP [13:0] = 0x3F for 64-bytes FIFO.
3. Issue TX FIFO write pointer reset.
4. MCU writes 64-bytes data to TX FIFO.
5. Issue TX mode.
6. Done.

Procedure of RX FIFO Reading

1. When RX FIFO is full, WTR (or FSYNC) can be used to trigger MCU for RX FIFO reading.
2. Issue RX FIFO read pointer reset.
3. MCU read 64-bytes from RX FIFO.
4. Done

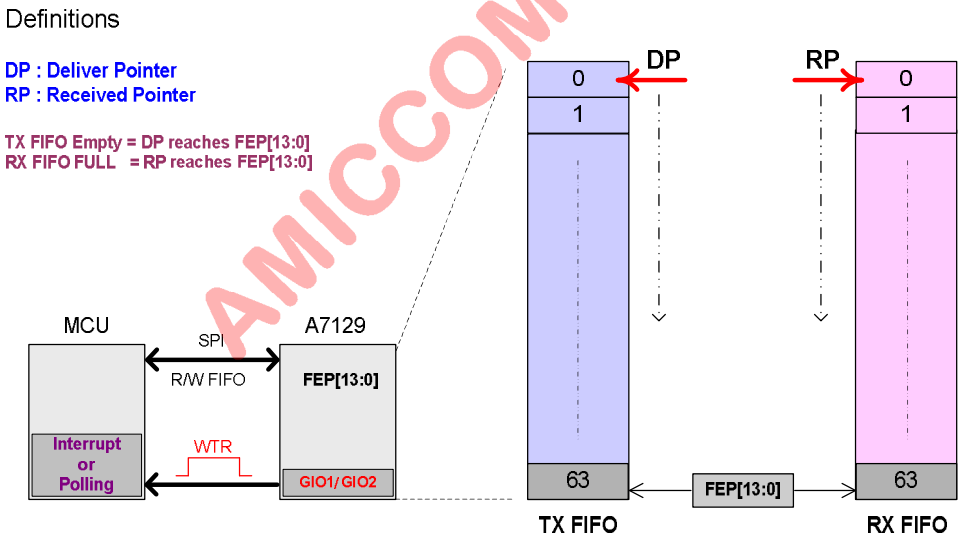


Figure 16.3 Easy FIFO mode

16.4.2 Segment FIFO

In Segment FIFO, TX FIFO length is equal to (FEP [13:0] − PSA [5:0]+1). FPM [1:0] should be zero. This function is very useful for button applications. In such case, each button is used to transmit fixed code (data) every time. During initialization, each fixed code is written into corresponding segment FIFO once and for all. Then, if button is triggered, MCU just assigns corresponding segment FIFO (PSA [5:0] and FEP [13:0]) and issues TX strobe command.

For example, if TX FIFO is arranged into 8 segments, each TX segment and RX FIFO length is divided into 8 bytes

TX				Control Registers		
Segment	**PSA**	**FEP**	**FIFO Length**	**PSA[5:0]**	**FEP[13:0]**	**FPM[1:0]**
1	PSA1	FEP1	8 bytes	0x00	0x007	0
2	PSA2	FEP2	8 bytes	0x08	0x00F	0
3	PSA3	FEP3	8 bytes	0x10	0x017	0
4	PSA4	FEP4	8 bytes	0x18	0x01F	0
5	PSA5	FEP5	8 bytes	0x20	0x027	0
6	PSA6	FEP6	8 bytes	0x28	0x02F	0
7	PSA7	FEP7	8 bytes	0x30	0x037	0
8	PSA8	FEP8	8 bytes	0x38	0x03F	0

RX	Control Registers		
FIFO Length	**PSA[5:0]**	**FEP[13:0]**	**FPM[1:0]**
8 bytes	0	0x007	0

Table 16.3 Segment FIFO is arranged into 8 segments

Procedures of TX FIFO Transmitting

1. Initialize all control registers (refer to A7129 reference code).
2. Strobe command – TX FIFO write pointer reset.
3. Input the wanted code to the corresponding segment FIFO once and for all.
4. To transmit segment 1, set PSA = 0x00 and FEP= 0x007
   Else, to transmit segment 2, set PSA = 0x08 and FEP= 0x00F
   Else, to transmit segment 3, set PSA = 0x10 and FEP= 0x017
   Else, to transmit segment 4, set PSA = 0x18 and FEP= 0x01F
   Else, to transmit segment 5, set PSA = 0x20 and FEP= 0x027
   Else, to transmit segment 6, set PSA = 0x28 and FEP= 0x02F
   Else, to transmit segment 7, set PSA = 0x30 and FEP= 0x037
   Else, to transmit segment 8, set PSA = 0x38 and FEP= 0x03F
5. Send TX Strobe Command.
6. Done.

Procedures of RX FIFO Reading

1. Set FEP [13:0] = 0x007.
2. If RX FIFO is full, WTR (or FSYNC) is used to trigger MCU for RX FIFO reading.
3. Strobe command – RX FIFO read pointer reset.
4. MCU read 8-bytes from RX FIFO.
5. Done.

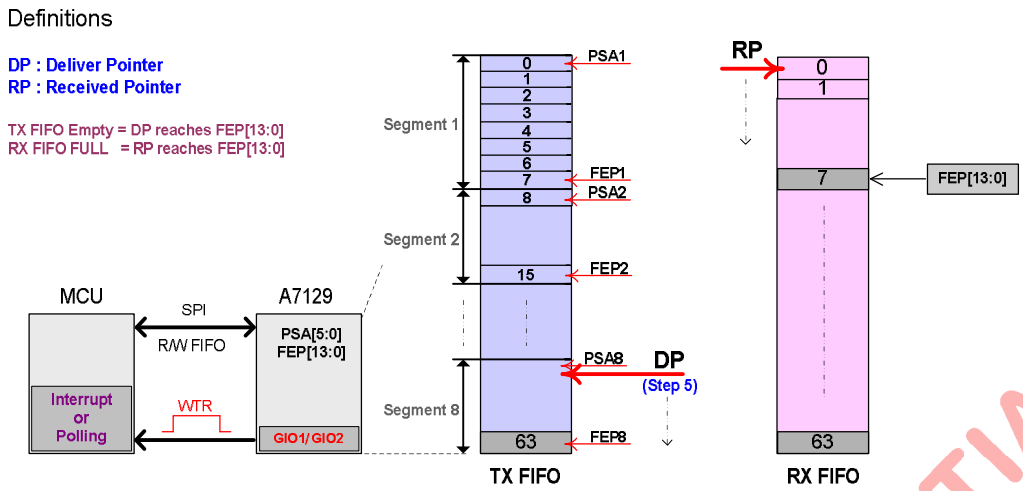


Figure 16.4 Segment FIFO Mode

16.4.3 FIFO Extension

In FIFO Extension, MCU can deliver a packet more than 64 bytes by monitoring FPF signal (from CKO or GIO1 or GIO2 pin). FIFO length is equal to **(FEP [13:0] +1)**. PSA [5:0] shall be zero, and FPM [1:0] is used to set FPF threshold (FIFO Pointer Flag). FIFO extension is max. 16K bytes by setting FEP [13:0].

Be notice, SPI speed is important to prevent error operation (over-write) in FIFO extension mode. We recommend the min. SPI speed shall be equal or greater than **(A7129 on-air data rate + 100Kbps)**.Please refer to AMICCOM's reference code (FIFO extension) for details.

Procedures of TX FIFO Extension

1. Initialize all control registers (refer to A7129 reference code).
2. Set FEP [13:0] = 0x0FF for 256-bytes FIFO extension.
3. Set FPM [1:0] = [11] for FPF trigger condition.
4. Set CKOS = [0010] to output FPF signal.
5. Strobe command – TX FIFO write pointer reset.
6. MCU writes 1st 64-bytes TX FIFO.
7. TX Strobe command.
8. MCU monitors FPF from A7129's CKO pin.
9. FPF triggers MCU to write 2nd 48-bytes TX FIFO.
10. Monitor FPF.
11. FPF triggers MCU to write 3rd 48-bytes TX FIFO.
12. Monitor FPF.
13. FPF triggers MCU to write 4th 48-bytes TX FIFO.
14. Monitor FPF.
15. FPF triggers MCU to write 5th 48-bytes TX FIFO.
16. Done.

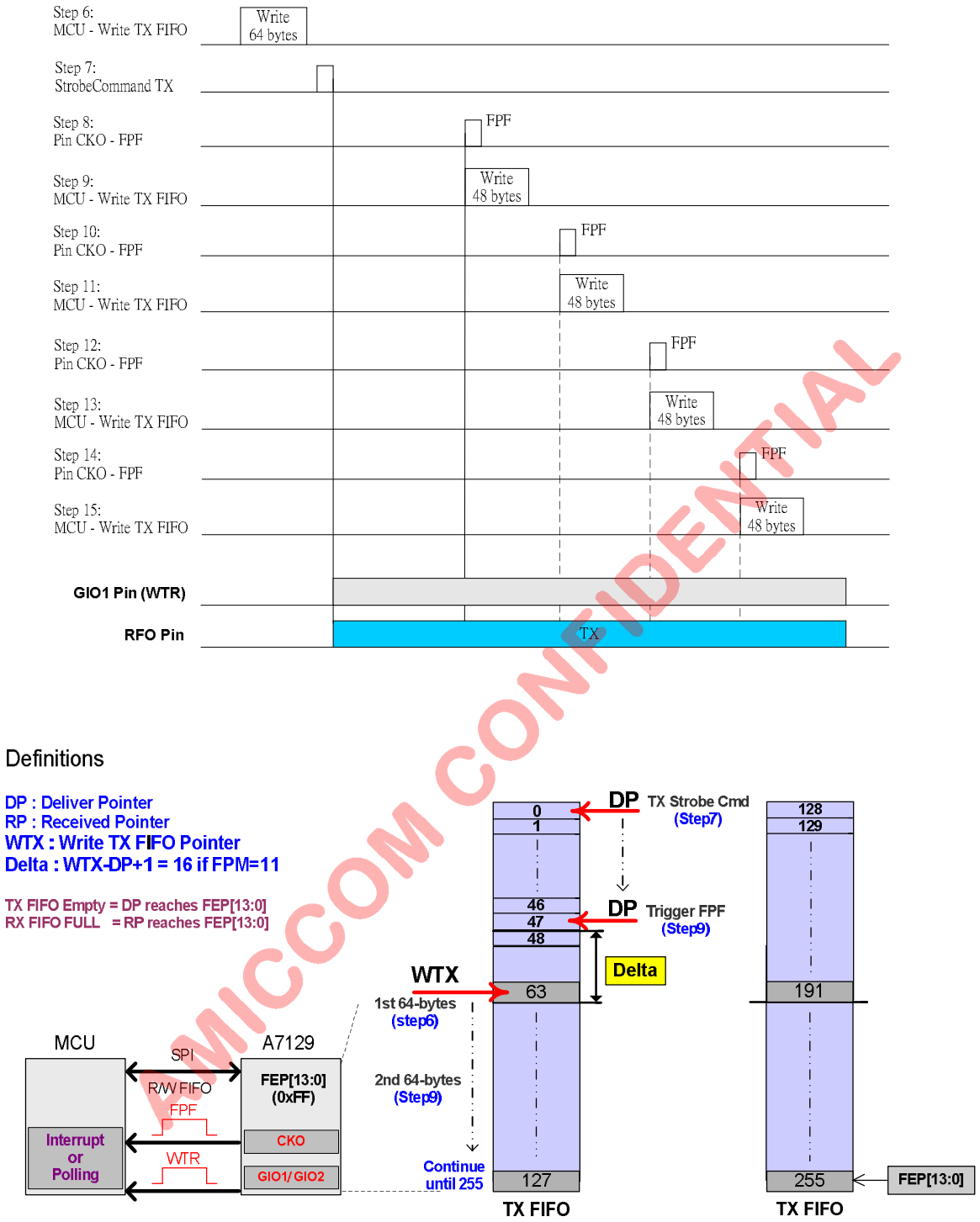
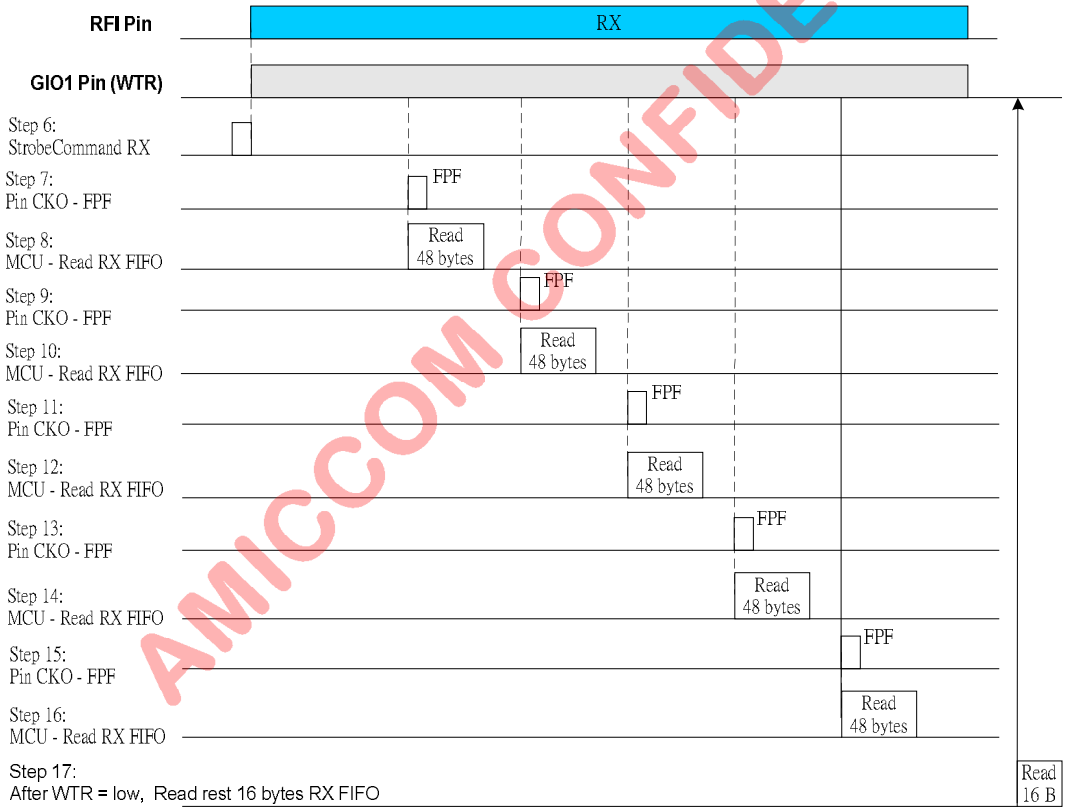


Figure 16.5 TX FIFO Extension

Procedures of RX FIFO Reading

1. Initialize all control registers (refer A7129 reference code).
2. Set FEP [13:0] = 0x0FF for 256-bytes FIFO extension.
3. Set FPM [1:0] = 11b for FPF trigger condition.
4. Set CKOS = [0010] to output FPF signal.
5. Send Strobe command – RX FIFO read pointer reset.
6. Send RX Strobe command.
7. MCU monitors FPF from A7129's CKO pin.
8. FPF triggers MCU to read 1st 48-bytes RX FIFO.
9. Monitor FPF.
10. FPF triggers MCU to read 2nd 48-bytes RX FIFO.
11. Monitor FPF.
12. FPF triggers MCU to read 3rd 48-bytes RX FIFO.
13. Monitor FPF.
14. FPF triggers MCU to read 4th 48-bytes RX FIFO.
15. Monitor FPF.
16. FPF triggers MCU to read 5th 48-bytes RX FIFO.
17. Monitor WTR falling edge or WTR = low, read the rest 16-bytes RX FIFO
18. Done.



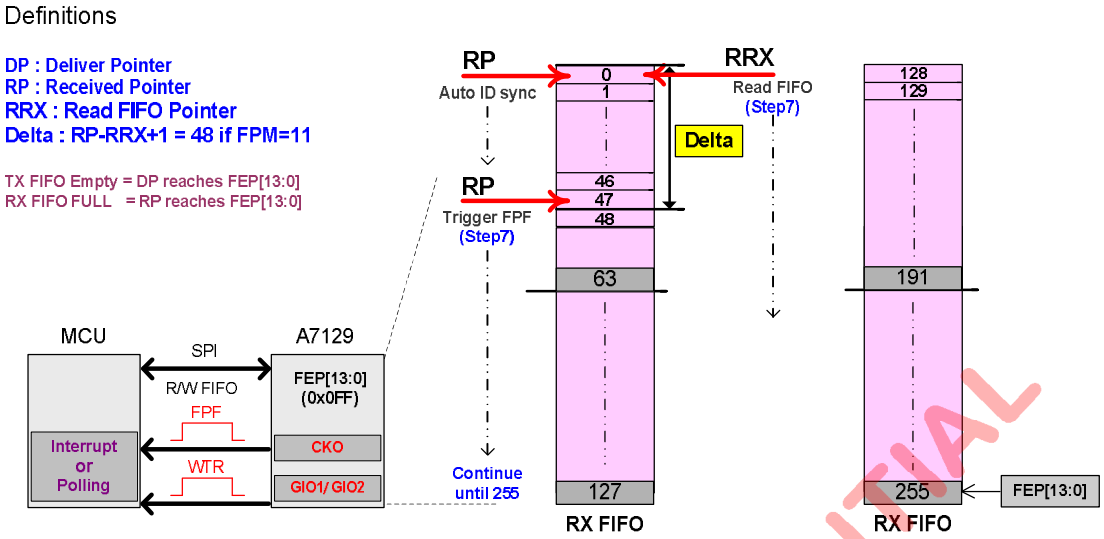


Figure 16.6 RX FIFO Extension Mode

17. Analog Digital Converter

A7129 contains a built-in 8-bit ADC for internal temperature measurement, RSSI measurement.

XADS	CDM	None Rx state	RX state
0	0	Temperature measurement	RSSI measurement
0	1	N/A	Carrier detector

The conversion time of 8-bit ADC is depends on the clock input to ADC. It takes 20 cycles to complete the conversion. The clock source of ADC comes from Crystal oscillator, and according to the setting of bit GRC[4:0] in system clock register, user can select the ADC clock source to be 800KHz or 1.2MHz.

17.1 Temperature Measurement

A7129 has a simple on-chip temperature sensor. Set bit CDM=0 in ADC register first, then enable bit ADCM=1 in the mode control register to start the measurement of temperature. When the measurement is completed, the bit ADCM will be cleared to 0. User can then read the ADC[7:0] values from the ADC register.

17.2 RSSI Measurement

A7129 has a built-in RSSI (received signal strength indicator) read from ADC to measure the received RF signal strength. When the measurement procedure is completed, the RSSI value can be read form ADC register, the range of RSSI is 0~511. Larger signal strength is corresponding to smaller RSSI value, and vice versa. In RX state, set bit CDM=0 in ADC register, and then set bit ADCM=1 in mode control register to start the RSSI measurement. Once the measurement is completed, the bit ADCM will be cleared to 0. User can read the RSSI value from ADCO[8:0] (0x0B).

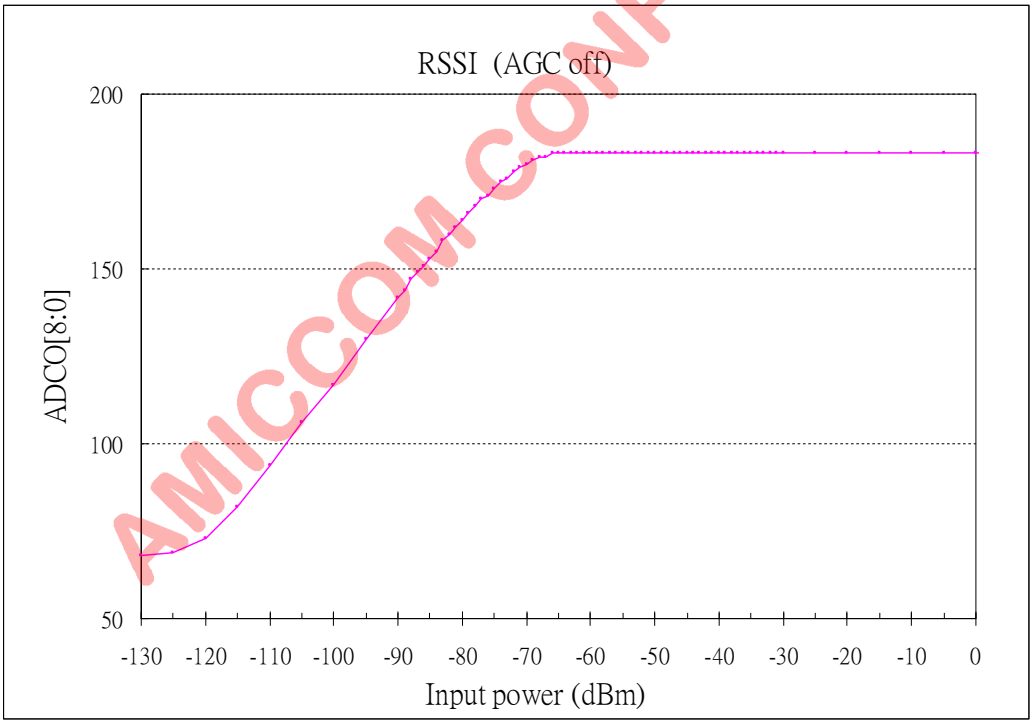


Figure 17.1 RSSI curve when AGC is disabled

17.3 Carrier detect

A7129 provides a CD signal (Carrier Detect output from GIO1 or GIO2) to monitor that there is a carrier or not. If the carrier signal strength is greater than the value set by bit RTH[7:0] in ADC register, CD will go high, or it will stay low. In RX state, set ADC register bit CDM=1, set mode control register bit ADCM=1 to start the carrier signal measurement. The value is stored in bit ADC[7:0] and it will be updated in each measurement period till the end of detection action.

18. Battery Detect

A7129 has built-in battery detector to check supply voltage (REGI pin). After enable battery detect function, user can read VBD flag or output VBD to GIO1 or GIO2. The detect range is 2.0V ~ 2.7V in 8 levels.

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
08h PM	W	CST	POWRS	CELS	STS	LVR	--	RGC1	RGC0	SPSS	RGV1	RGV0	QDS	BVT2	BVT1	BVT0	BDS
Reset		-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BVT [2:0]: Battery Voltage Threshold select.
[000]: 2.0V. **[001]:** 2.1V. **[010]:** 2.2V. **[011]:** 2.3V. **[100]:** 2.4V. **[101]:** 2.5V. **[110]:** 2.6V. **[111]:** 2.7V.

BDS: Battery Detection selection.
[0]: Disable. **[1]:** Enable.

Below is the procedure of battery detect for low voltage detection (ex., below 2.1V):

1. Set A7129 in standby or PLL mode.
2. Set detection level by BVT [2:0] = [001] and enable BDS = 1.
3. After 5 us, BDS is auto clear.
4. MCU check VBD flag.
   If REGI pin > 2.1V,
   VBD = 1. Else, VBD = 0.

19 TX power setting

A7129 supports programmable TX power by setting TBG[3:0], TDC [1:0] and PAC [1:0] from TXII register (09h).

Address/Name	R/W	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
09h TX II	W	MCNTR	DPR2	DPR1	DPR0	BT1	BT0	TDL1	TDL0	TXDI	PAC1	PAC0	TDC1	TDC0	TBG2	TBG1	TBG0
	R	DID15	DID14	DID13	DID12	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4	DID3	DID2	DID1	DID0
Reset		0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

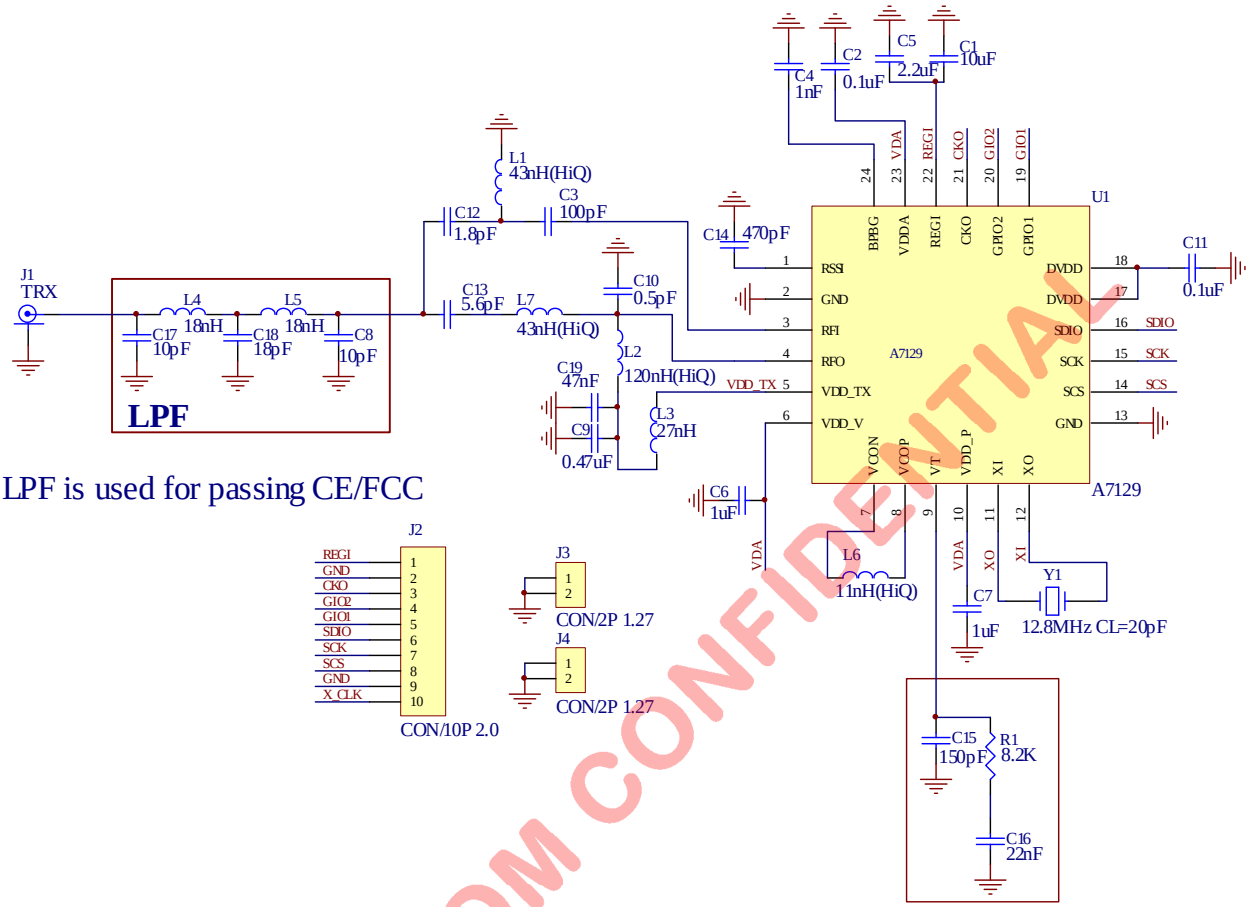
PAC[1:0]: PA current setting.

TDC[1:0]: TX Driver current setting.

TBG[2:0]: TX Buffer Gain setting.

20. Application Circuit

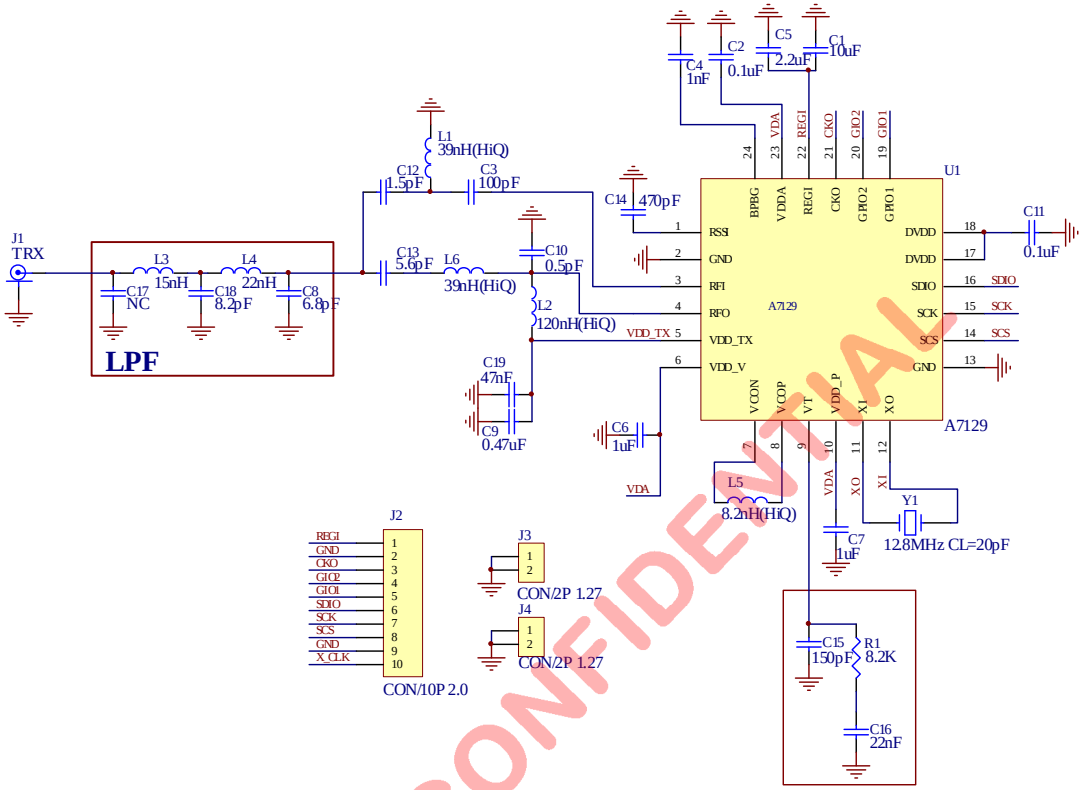
20.1 MD7129-A40 (434MHz Band)



LPF is used for passing CE/FCC

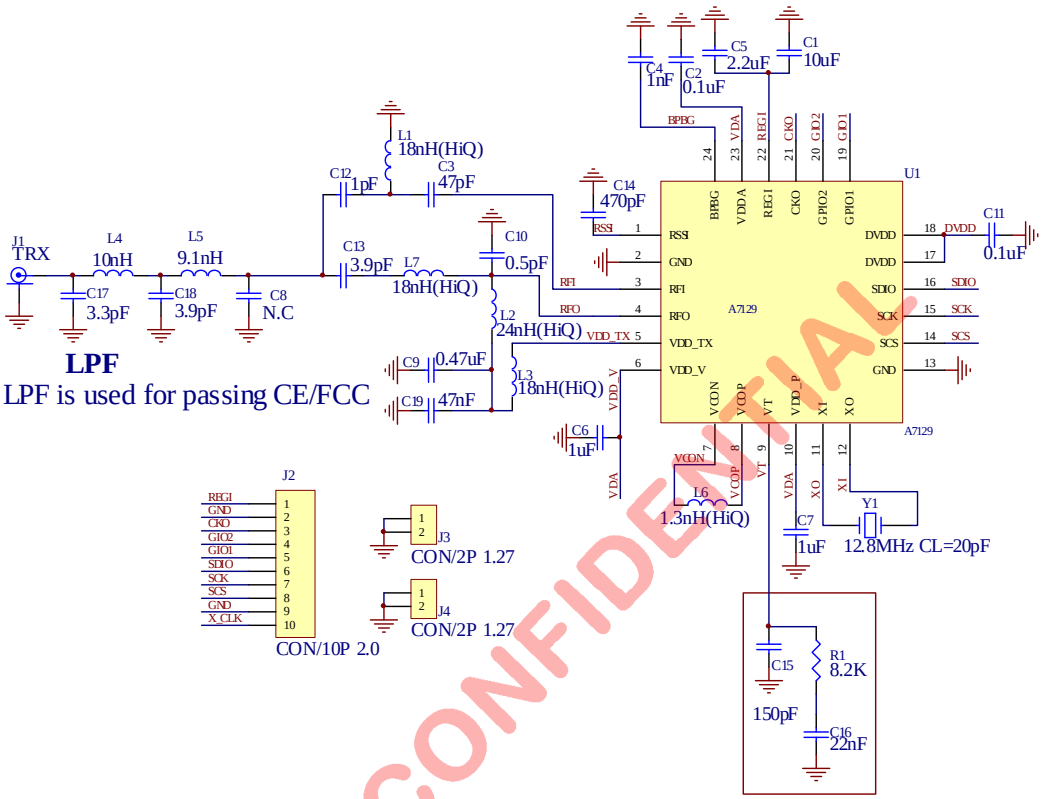
Where Xtal is 12.8MHz with 20 pF C-load.

20.2 MD7129-A50 (470MHz~510MHz Band)



Where Xtal is 12.8MHz with 20 pF C-load.

20.3 MD7129-A80 (868MHz Band)



Where Xtal is 12.8MHz with 20 pF C-load.

21. Abbreviations

ADC	Analog to Digital Converter
AFC	Automatic Frequency Compensation
AGC	Automatic Gain Control
BER	Bit Error Rate
BW	Bandwidth
CD	Carrier Detect
CRC	Cyclic Redundancy Check
FEC	Forward Error Correction
FIFO	First in First out
FSK	Frequency Shift Keying
ID	Identifier
IF	Intermediate Frequency
ISM	Industrial, Scientific and Medical
LO	Local Oscillator
MCU	Micro Controller Unit
PFD	Phase Frequency Detector for PLL
PLL	Phase Lock Loop
POR	Power on Reset
RX	Receiver
RXLO	Receiver Local Oscillator
RSSI	Received Signal Strength Indicator
SPI	Serial to Parallel Interface
SYCK	System Clock for digital circuit
TX	Transmitter
TXRF	Transmitter Radio Frequency
VCO	Voltage Controlled Oscillator
XOSC	Crystal Oscillator
XREF	Crystal Reference frequency
XTAL	Crystal

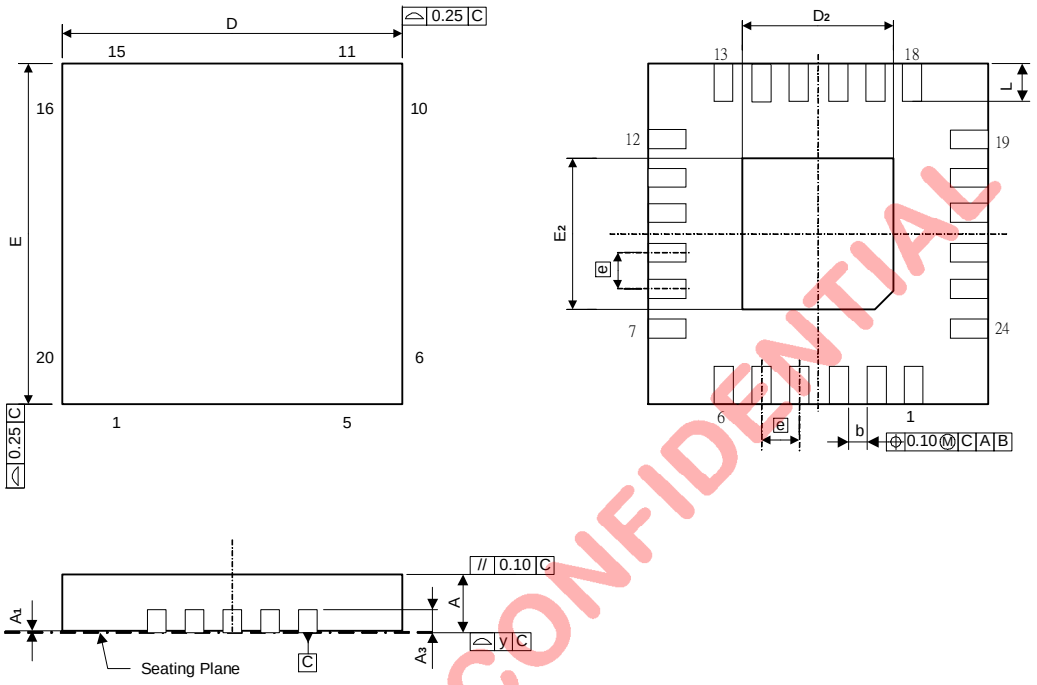
22. Ordering Information

Part No.	Package	Units Per Reel / Tray
A71X29AQFI/Q	QFN24L, Pb Free, Tape & Reel, -40℃～85℃	3K
A71X29AQFI	QFN24L, Pb Free, Tray, -40℃～85℃	490EA
A71X29AH	Die form, -40℃～85℃	250EA

23. Package Information

QFN 24L (4 X 4 X 0.8mm) Outline Dimensions unit: inches/mm

TOP VIEW **BOTTOM VIEW**

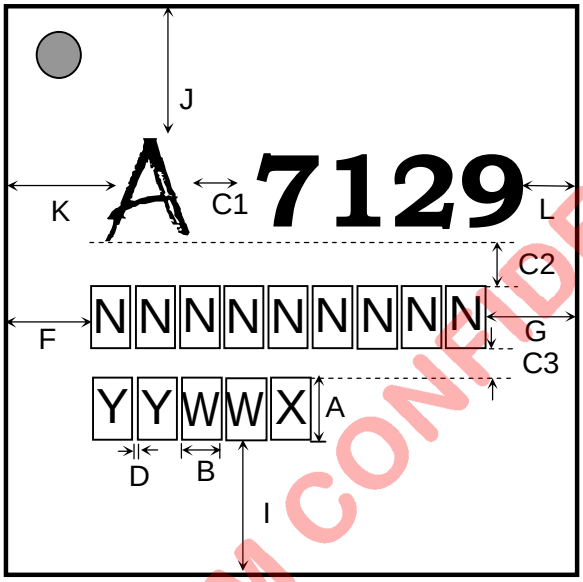


Symbol	Dimensions in inches			Dimensions in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.028	0.030	0.032	0.70	0.75	0.80
A_1	0.000	0.001	0.002	0.00	0.02	0.05
A_3		0.008 REF			0.203 REF	
b	0.007	0.010	0.012	0.18	0.25	0.30
D	0.154	0.158	0.161	3.90	4.00	4.10
D_2	0.075	-.	0.114	1.90	-	2.90
E	0.154	0.158	0.161	3.90	4.00	4.10
E_2	0.075	-	0.114	1.90	-	2.90
e		0.020 BSC			0.50 BSC	
L	0.012	0.016	0.020	0.30	0.40	0.50
y		0.003			0.08	

24. Top Marking Information

A71X29AQFI

- Part No. : **A71X29AQFI**
- Pin Count : **24**
- Package Type : **QFN**
- Dimension : **4*4 mm**
- Mark Method : **Laser Mark**
- Character Type : **Arial**



❖ **CHARACTER SIZE : (Unit in mm)**

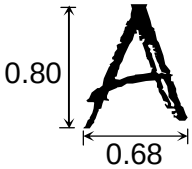
A : 0.55
B : 0.36
C1 : 0.25 C2 : 0.3 C3 : 0.2
D : 0.03

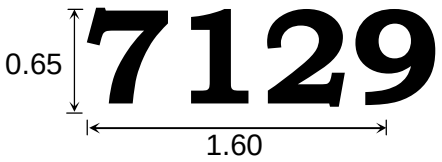
F=G
I=J
K=L

Y Y W W : DATECODE

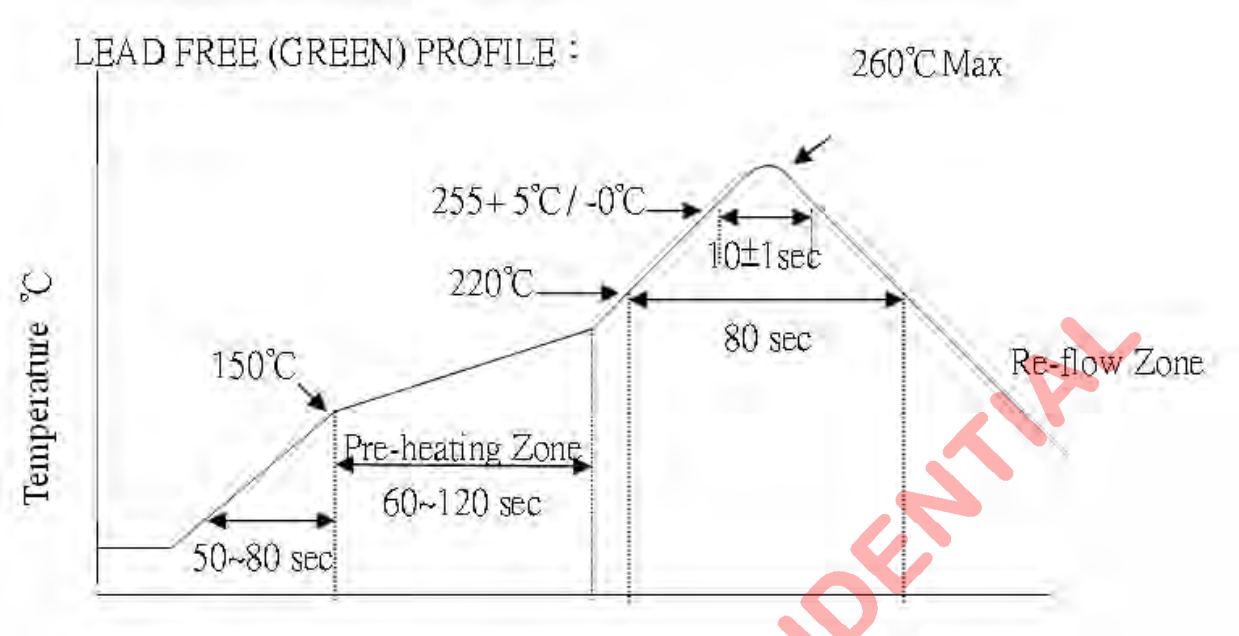
X : PKG HOUSE ID

N N N N N N N N N : LOT NO.
(max. 9 characters)



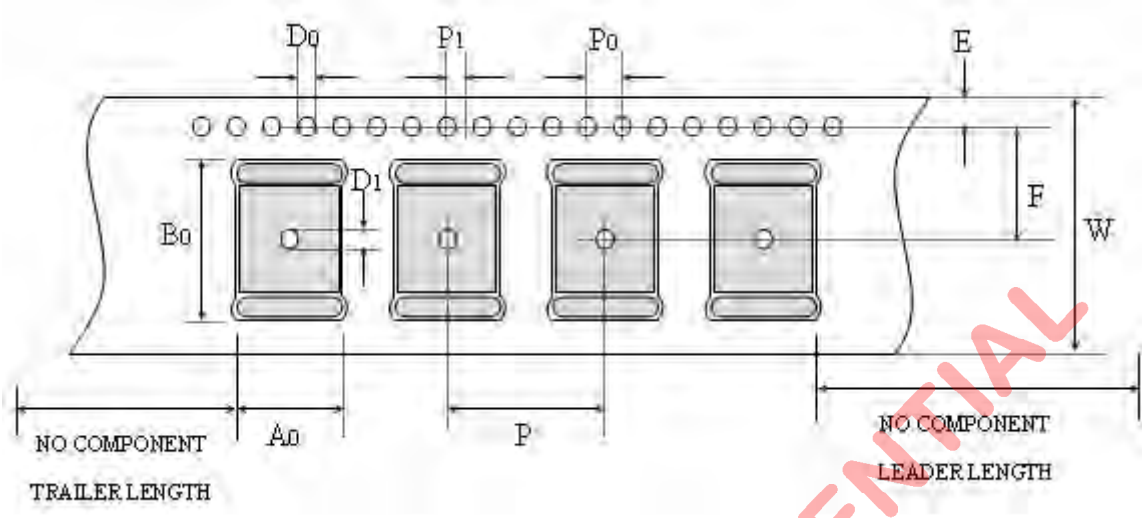


25. Reflow Profile



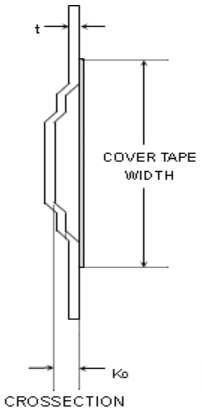
26. Tape Reel Information

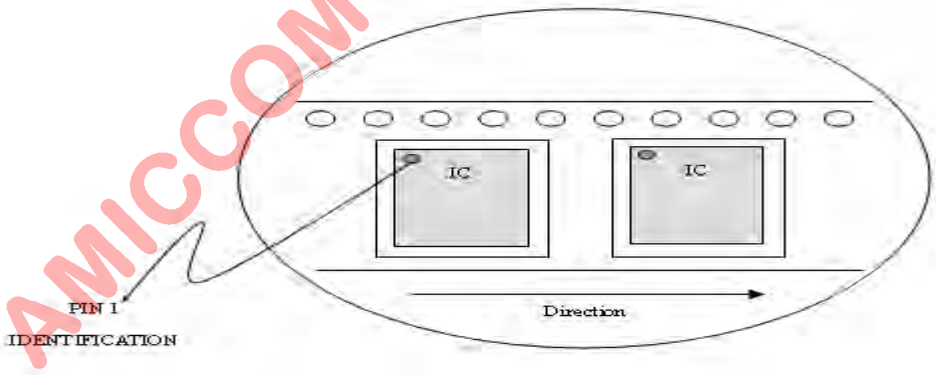
Cover / Carrier Tape Dimension



Unit: mm

TYPE	P	A0	B0	P0	P1	D0	D1	E	F	W
20 QFN 4*4	8	4.35	4.35	4.0	2.0	1.5	1.5	1.75	5.5	12
24 QFN 4*4	8	4.4	4.4	4.0	2.0	1.5	1.5	1.75	5.5	12
32 QFN 5*5	8	5.25	5.25	4.0	2.0	1.5	1.5	1.75	5.5	12
QFN3*3 / DFN-10	4	3.2	3.2	4.0	2.0	1.5	-	1.75	1.9	8
20 SSOP	12	8.2	7.5	4.0	2.0	1.5	1.5	1.75	7.5	16
24 SSOP	12	8.2	8.8	4.0	2.0	1.5	1.5	1.75	7.5	16



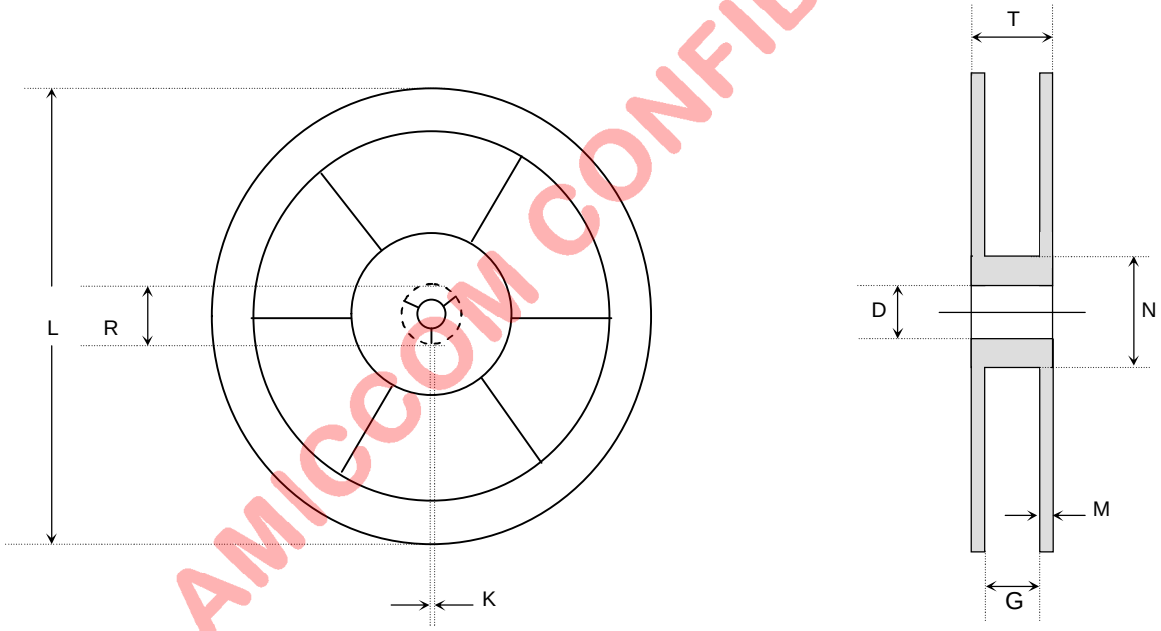


TYPE	K0	t	COVER TAPE WIDTH
20 QFN (4X4)	1.1	0.3	9.2
24 QFN (4X4)	1.4	0.3	9.2
32 QFN (5X5)	1.1	0.3	9.2
QFN3*3 / DFN-10	0.75	0.25	8
20 SSOP	2.5	0.3	13.3
24 SSOP	2.1	0.3	13.3

REEL DIMENSIONS

UNIT IN mm

TYPE	G	N	T	M	D	K	L	R
20 QFN(4X4) 24 QFN(4X4) 32 QFN(5X5) DFN-10	12.8+0.6/-0.4	100 REF	18.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
48 QFN(7X7)	16.8+0.6/-0.4	100 REF	22.2(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
28 SSOP (150mil)	20.4+0.6/-0.4	100 REF	25(MAX)	1.75±0.25	13.0+0.5/-0.2	2.0±0.5	330+0.00/-1.0	20.2
20 SSOP 24 SSOP	16.4+2.0/-0.0	100 REF	22.4(MAX)	1.75±0.25	13.0+0.2/-0.2	1.9±0.4	330+0.00/-1.0	20.2



27 Product Status

Data Sheet Identification	Product Status	Definition
Objective	Planned or Under Development	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	Engineering Samples and First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification	Noted Full Production	This data sheet contains the final specifications. AMICCOM reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Obsolete	Not In Production	This data sheet contains specifications on a product that has been discontinued by AMICCOM. The data sheet is printed for reference information only.

RF ICs AMICCOM

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